A no-verification Multi-Level-Cell (MLC) operation in Cross-Point OTS-PCM

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Abstract

We present the first MLC operation for OTS-PCM with comprehensive operation algorithm study. An ADM chip with fast write speed (<300ns) and robust operation (>10^9 cycles) are shown indicating the potential for high performance MLC OTS-PCM. A desirable 2-bits/cell operation up to 10^8 cycles without further read verification is achieved based on 100 cells data from 1Mbit crosspoint array. Systematic discussions of MLC operation under "1/2V" scheme is further presented, and threshold voltage (Vt) drift is evaluated accordingly.

I. Introduction

Phase Change Memory (PCM) is considered the most suitable candidate for SCM (storage class memory) applications. With the help of ovonic threshold switch (OTS) to serve as the access device, it has shown great success to achieve large density, low cost 3D crosspoint arrays using 1S1R (one selector plus one PCM) structure [1-2].

MLC (multi level cell) operation is a viable path to further reduce cost per bit [3]. Early studies have shown the feasibility of 2-bits/cell on a 512Mbit PCM chip with the help of iterative MLC programming and using transistors to control programming current [4], however, the chip density is still limited by transistor design and cannot meet the density requirement for SCM application [3].

In this work, we systematically study the MLC feasibility in the OTS-PCM crosspoint array that includes 3D stackable pillar PCM (here, doped $Ge_2Sb_2Te_5$) and TeAsGeSiSe-based OTS [1-2,5]. The requirements of MLC operation based on "1/2V" scheme and threshold voltage (Vt) drift are discussed and evaluated. Our "no-verify, no-iterative programming" results achieve 2-bits/cell operation for the crosspoint array, which provides a feasible path to further reduce cost per bit in the 3D OTS-PCM array.

II. Characteristics of 1Mbit OTS-PCM chip

Figure 1 shows the structure of 3D stackable OTS-PCM crosspoint array. Each cell has 1S1R structure that is accessed by selected word line (WL) and bit line (BL). In this study, we use a 1S1R1T ADM to characterize reliability of $Ge_2Sb_2Te_5$ based PCM and TeAsGeSiSe based OTS [2] **(Fig. 2)** and we further investigate MLC in OTS-PCM 1S1R crosspoint array.

Figure 3 shows the set speed characteristics from ADM (1k cells tested). 99% of the PCM cells could be fully set into crystalline state within 300ns, which is consistent with recent reported set feature from pillar type OTS-PCM cells [6]. The extraordinary dump mode endurance characteristics (no read verification) are presented in **Fig. 4**, where one can see ~1V memory window (Vtr-Vts, where Vtr/Vts is Vt of OTS-PCM when PCM is in reset state/set state) remains almost unchanged after 10^9 cycles that can fulfill SCM requirements.

III. Investigating MLC operation

To further enhance the chip density, the MLC operation for OTS-PCM was studied for the first time. The 10×10 macro array within 1Mbit 1S1R corsspoint array was utilized for device level characterization considering flexibility in the measurement setup. The remaining unselected cells in the 1Mbit array always stay in the unselected conditions to mimic real chip level crosspoint operation under "1/2V" scheme.

Figure 5 demonstrates the different read methodologies. DC read is typically performed by sweeping pulse amplitude using SMU that each pulse has the order around millisecond, and AC triangle pulse could detect Vt response less than microsecond. As shown in **Fig.6**, it is clearly observed that Vt is increased under faster AC pulse (i.e., shorter rise/fall time), which can be explained by filamentary switching of OTS [7].

Figure 7 evaluates polarity effect to write OTS-PCM. Both forward and reverse write pulse provide almost the same Vtr and Vts, which indicates the middle metal line can be shared by both top and bottom OTS-PCM layers (**Fig.1**), and the extra metal cost can be saved.

Two write methods to realize MLC OTS-PCM are depicted in **Fig.8**. The partial-SET pulse (control amorphous to crystalline transition time) and partial-RESET pulse (adjust amount of PCM for melt-quench, requires pre-set the cell first) were studied. Choosing suitable conditions based on OTS-PCM characteristics makes it possible to achieve 2-bits/cell for both partial-SET and partial-RESET methods. Here we apply open-loop programming (i.e., no read verify and no re-write) for the 100 cells of a 1Mbit crosspoint array under "1/2V" scheme (**Fig.9**). To further tighten Vt distribution, one could read-verify-rewrite (sacrifice latency).

Feasible Vts and Vtr combination is required in order to successfully implement "1/2V" scheme to write and read OTS-PCM array [8]. As such, for MLC operation, distinguishable levels need to be maintained within maximum possible memory window (MW, fully Vtr minus fully Vts) in order to write and read cell under "1/2V" scheme (**Fig.10**).

As shown in **Fig. 11**, observable Vt drift with increased time after programming poses challenges on the readable memory window. We further characterized drift using factor γ (defined as Vt change per time decade, as illustrated in **Fig. 12**). Both programming methods do not clearly show cell state dependence on the Vt drift. The drift is less from partial-SET method than the one from partial-RESET (γ~0.05, and ~0.07, **Fig. 13**). One possible explanation could be attributed to accelerated relaxation of local traps under partial-SET programming (illustrated in **Fig. 14**), and it still requires further study to fully understand the underlying mechanisms. To further mitigate the impact of Vt drift for the MLC operation in OTS-PCM, increasing memory window, tightening distribution of each cell state, certain refresh operations and device material/structure development would be necessary. **Figure 15** provides a guideline for OTS-PCM. Multiple SPECs including MLC levels, distribution, drift, and "1/2V" scheme are considered. Suitable MW and reduced Vt drift are key considerations to improve MLC performance.

Fig.16 shows endurance characteristics from a typical cell under MLC operation. The robustness to program the OTS-PCM cell is confirmed up to 10^8 cycles.

IV. Summary

Robust (>10^8 cycles) MLC operation is demonstrated within selected cells from 1Mbit OTS-PCM 1S1R crosspoint array, without read verification and iterative programming. Detailed discussions for MLC SPECs under "1/2V" scheme are presented, and Vt drift is evaluated in order to further improve MLC performance in OTS-PCM crosspoint array.

References

[1] H. Y. Cheng, et al., IEDM, p 28-31, 2017. [2] C.W. Yeh, et al., VLSI, pp. 205-206, 2018. [3] G. Burr, et al., IEEE Journal on Emerging and Selected Topics in Circuits and Systems. 6.2 (2016): 146-162. [4] W.C. Chien, et al, VLSI, pp. 100-101, 2015. [5] W.C.Chien, et al., TED, 65(11), pp. 5172-5179, 2018. [6] T.Kim, et al., IEDM, pp. 851-854, 2018. [7] F. Hatem, et al., IEDM, pp. 827-320, 2019. [8] W.C Chien, et al., VLSI, pp. 60-61, 2019.

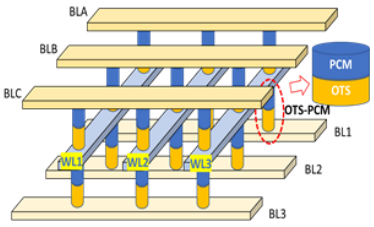


Fig. 1 3D stackable OTS-PCM crosspoint array structure.

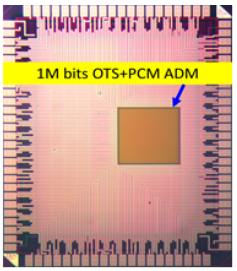


Fig. 2 Optical image of OTS+PCM+nFET ADM array.

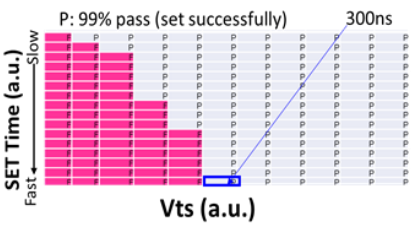


Fig. 3 Set speed: 99% of the cells are successfully set within 300ns.

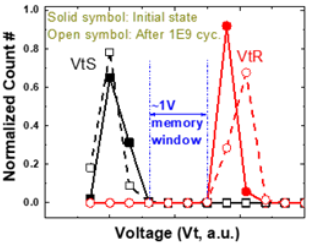


Fig. 4 Endurance is greater than 10^9 cycles.

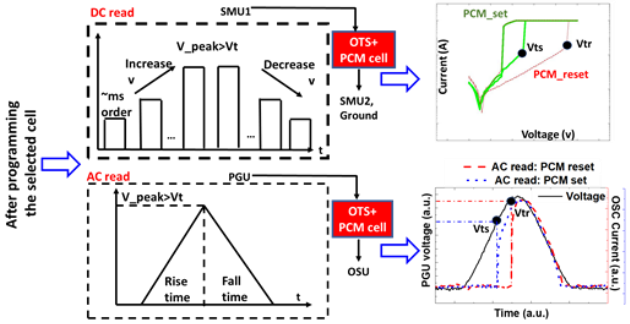


Fig. 5 DC and AC read methodology. AC read is capable to detect Vt response to the read pulse within less than microsecond.

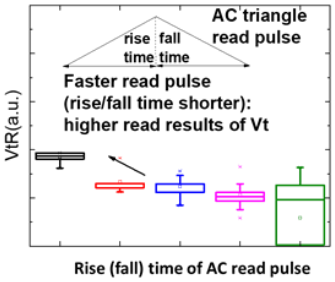


Fig. 6 Higher Vtr is detected under faster read pulse.

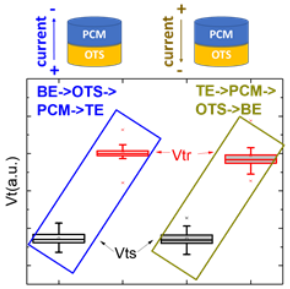


Fig. 7 Negligible polarity effect to write OTS-PCM (both Vtr, and Vts).

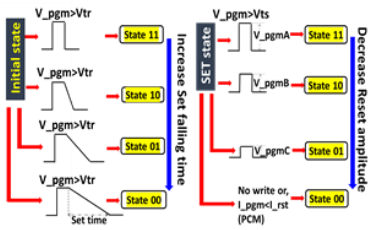
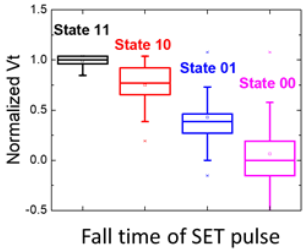


Fig. 8 Two write methods for MLC: partial-SET and partial-RESET.



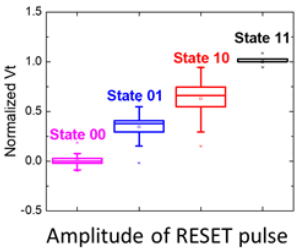


Fig. 9 MLC operation (here, 2-bits/cell) is achieved by both partial-SET and partial-RESET methods.

Fig. 10 Vtr is limited within a range in order to write and read under 1/2V scheme.

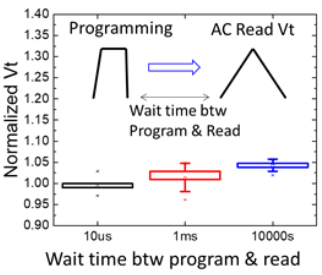


Fig. 11 Vt drifts with increased time between program and read.

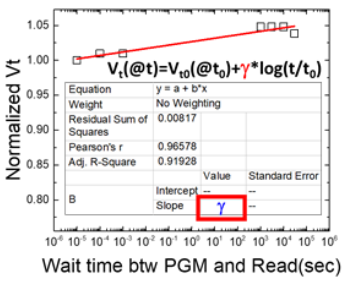
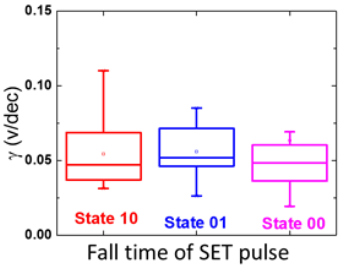


Fig. 12 Vt drift is characterized by the slope (γ).



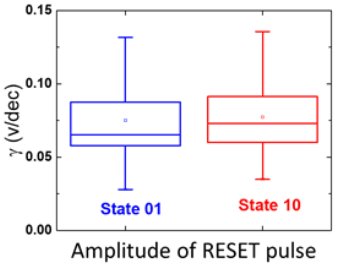


Fig. 13 Vt drift factor γ not clearly depends on different resistance level. Partial-SET method (left, ~0.05) show less drift than partial-RESET method (right, ~0.07).

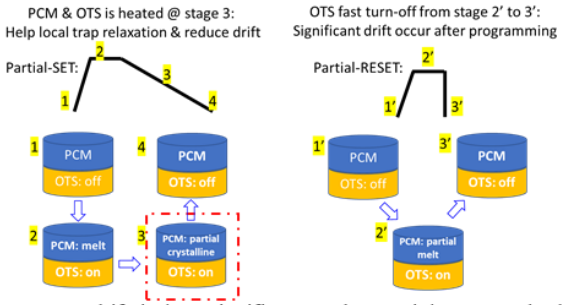


Fig. 14 Vt drift is less significant under partial-SET method: Accelerated trap anneal during partial-SET programming helps reduce Vt drift afterwards.

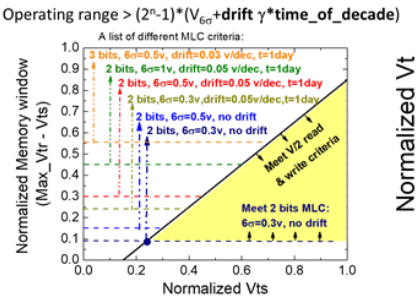


Fig. 15 Impact of Vt drift on the MLC SPECs.

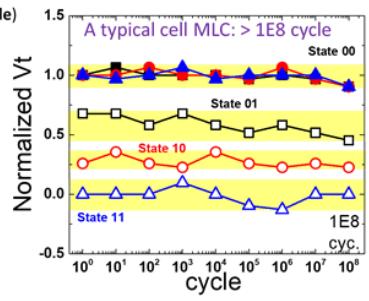


Fig. 16 Robust endurance of 2 bits/cell MLC: larger than 10^8 cycles.