# Reliability and Variability of 1S1R OxRAM-OTS for High Density Crossbar Integration

D. Alfaro Robayo[1,2], G. Sassine, J. Minguet Lopez, L. Grenouillet, A. Verdy, G. Navarro, M. Bernard, E. Esmanhotto, C. Carabasse, D. Deleruyelle[3], E. Vianello, N. Castellani, L. Ciampolini, B. Giraud, C. Cagli, G. Ghibaudo[2], E. Nowak, G. Molas

CEA, LETI, MINATEC Campus, GRENOBLE, France, diego.alfarorobayo@cea.fr, [2]IMEP LAHC CNRS France, [3]INL CNRS, INSA Lyon, France

*Abstract*— $HfO_2$ OxRAM was co-integrated with an optimized OTS back-end selector in 1S1R memory arrays showing outstanding performances. Up to 3 decades of current window margin and 5 decades of selectivity were achieved. More than $10^6$ programming, $10^8$ reading and $10^9$ read disturb cycles were demonstrated. Ultra low OTS leakage current is compatible with 100Mb-1Gb bank size. Semi-analytical model of OTS was developed to analyze stochastic switching behavior. Variability of voltage margin, selectivity and current margin were deeply investigated in a statistical way for the 1st time to identify the most critical features for high-density crossbar arrays.

## I. Introduction

Resistive Random-Access Memories (RRAM) are one of the most promising suitable technologies for crossbar architectures to be used in Storage Class Memory and In Memory Computing applications. In high-density crossbars, a back-end selector is required to suppress sneak path currents on unselected cells. Ovonic Threshold Switching (OTS) [1] selector is one of the most interesting solutions due to its high non-linearity, high endurance and high ON/OFF current ratio [2]. In previous works, successful co-integrations of OTS selectors (1S) and RRAM devices (1R) were achieved in 1S1R stacks, showing promising functionality [3-4]. In such architectures, current window margin (WM), reading voltage margin (VM) and selectivity are known to be the most critical features required for high-density integration. While promising features of co-integrated 1S1R systems were showed [5-6], no clear investigation of overall reliability and variability has been demonstrated. In this work, we propose a global study allowing to quantify the criticality of these parameters and to link them to both RRRAM and OTS characteristics. To this aim, oxide-based RRAM (OxRAM) is co-integrated with an OTS on top of a FEOL CMOS, showing excellent overall 1S1R performances. Results are analyzed by means of numerical models and Monte Carlo simulations. Then, device optimizations are proposed to provide reliable 1S1R structures for high-density crossbar arrays.

## II. Technological Details

OxRAM+OTS 1S1R structures are integrated on memory arrays on top of Metal 4 of a 130nm technology (**Fig.1.a-b)** with 300nm memory cell size. OxRAM devices are made of a TiN/10nm $HfO_2$ (ALD)/Ti stack. Magnetron sputtering is used to deposit the OTS based on a Se-rich Ge-Se alloy. Sb-doping allows to reduce the operating voltages while N-doping is used to stabilize the amorphous structure; leading to GSSN (Ge-Se-Sb-N) selector [7]. GSSN thickness is adjusted in order to favor low voltage operation (15 nm) or high insulating properties (25 nm). Selector device is sandwiched between two carbon electrodes aiming to avoid TiN diffusion allowing to enhance OTS endurance [8]. **Fig.1.c** and **Fig.1.d** present TEM and EDX device cross sections showing a clear separation of the layers composing the 1S1R device.

## III. Results and Discussion

### A. 1S1R working principle and switching characteristics

**Fig.2** presents an example of IV characteristics of 1S1R system for a 15nm GSSN thickness. There, the main electric parameters to be considered are highlighted as detailed in [4]. As it is the case for resistive memories, OTS devices require a forming process, $V_{forming}$. OTS and OxRAM are formed simultaneously. For the following operations, voltage and current, necessary to switch the selector device from the OFF state to the ON state are named threshold voltage and threshold current respectively ($V_{th}$, $I_{th}$). In this work, GSSN OTS presents a $V_{th\text{-}OTS}$ higher than the SET and RESET voltage ($V_{SET}$, $V_{RESET}$) of the OxRAM. Therefore, both OTS and OxRAM switch once the threshold voltage of the selector device is reached. The voltage drop over the resistive memory, which is bigger for the HRS, causes a shift over the $V_{th\text{-}1S1R}$, known as $\Delta V_{th}$. Thus, two $V_{th\text{-}1S1R}$ are observed as a function of the OxRAM state, $V_{th1}$ (OxRAM in HRS) and $V_{th2}$ (OxRAM in LRS). Hence, $V_{th1} > (V_{th2} \sim |V_{th\text{-}OTS}|)$. **Fig.3** shows the impact of the programming current (controled by the select transistor) on the ON state resistance measured on 1S, 1R and 1S1R structures. Interestingly, we show for the 1st time that after programming, OxRAM and OTS reach the same resistance level and follow the same universal law.

### B. OTS thickness adjustment for tuned 1S1R performances

In previous works, various GSSN stoichiometries were optimized to achieve highly reliable selectors [4, 7]. Thus, we fixed GSSN composition and adjusted the thickness for targeted specifications. **Fig.4** shows the impact over the forming voltage with 1V increase for 5nm of OTS. Evolution of the threshold voltages are presented in **Fig.5**. $V_{th2}$ and $V_{th1}$ present similar slopes as a function of the GSSN thicknesses (250mV every 5nm) confirming once again that such voltages are mainly dependent on the $V_{th\text{-}OTS}$. It was decided to focus our study on 15-25nm GSSN thicknesses, providing low voltage or high insulation solutions. **Fig.6** demonstrates that OTS leakage current ($I_{leak} \sim 1nA$) remains significantly lower

than the ON current of the 1S1R system. (100µA programming current).

### C. Device performances and reliability

As illustrated by the IV behavior of the 1S1R system, $\Delta V_{th}$ is the most adequate reading strategy to know the OxRAM state. $V_{read}$ must be chosen in such a way that $V_{th2}<V_{read}<V_{th1}$ to obtain two different current values inherent to the selector device but determined by the resistive memory state. In this strategy, three key features are identified: window margin (WM), selectivity and reading voltage margin (VM), (**Fig.7**); they are quantified and studied in a statistical point of view in order to properly design crossbar arrays.

#### 1) Current margin at $V_{read}$

Current margin is the ratio between the read current when the resistive memory is in the LRS ($I_{on}$) and HRS ($I_{off}$). It ranges between 2 and 3 decades (**Fig.8**), which is significantly higher than what is measured in 1R structures, thanks to the selector low $I_{off}$. **Fig.8** presents read disturb when the 1S1R cell is read at $V_{read}$. In this case, OxRAM cells are not switched; only successive read operations are performed. More than $10^8$ reading cycles were achieved with ~3 decades for the current ratio. **Fig.9** shows corresponding $I_{on}$ and $I_{off}$ distributions, confirming the high stability of the ON and OFF currents for both GSSN considered thicknesses.

#### 2) Selectivity

**Fig.10** represents $I_{off}$ and $I_{leak}$ distributions for 15nm and 25nm GSSN. Selectivity, defined as $I_{on}/I_{leak}$ ratio, is in the order of 5 and 6 decades respectively. These values allow quantifying the total leakage current in a crossbar array for $V_{read}/2$ and $V_{read}/3$ reading schemes. We thus estimate, for $V_{read}/2$ biasing scheme, respective maximum bank sizes of 100Mb and 1Gb insuring enough margin between the total array leakage and the read current (**Fig.11**). Overall, it appears that bank size is more limited by the technology node scaling and acceptable voltage drop along the array rather than by the device selectivity itself (**Fig.12**). Finally, **Fig.13** shows no read disturb on unselected cells of the array, which undergo $V_{read}/2$ for more than $10^9$ cycles.

#### 3) Voltage Margin

**Fig.14** shows 1S1R endurance with up to $5.10^6$ cycles. Significant margin up to 3 decades is measured. However, some punctual read failures are observed when the read OxRAM memory state is different from the programmed one. **Fig 15** shows a slight shift of reading margin after 1M cycles, while an acceptable VM is maintained for a reliable reading operation. In order to investigate these read failures, $V_{th}$ evolution is analyzed with transient measurements (**Fig.16**). In **Fig.17**, $V_{th1}$ and $V_{th2}$ median values (measured on a population of 30 devices), are presented showing cycle to cycle variability. Thus, $V_{read}$ should be accurately chosen in order to minimize erratic reading operations (**Fig.18**). **Fig.19** to **Fig.21** show $V_{th1}$ and $V_{th2}$ distributions. $V_{th1}$ is more dispersed than $V_{th2}$ probably due to combination of OTS and OxRAM variability. Same distributions (with shifted median value) were measured for 15nm and 25nm GSSN. Cycle to cycle and device to device distributions are found to be similar. $V_{th1}$ dispersion could be correlated to the intrinsic HRS dispersion of the OxRAM. It was calculated that a variation of 1 decade of $R_{HRS\text{-}OxRAM}$ (measured) leads to a shift of ~1V of OxRAM+OTS switching voltage due to more voltage drop in the OxRAM (**Fig.22**).

### D. Simulations and Discussion

#### 1) Semi-analytical statistical model

Semi-analytical simulations of 1S were deployed using a physical model based on field-induced nucleation theory (**Fig.23**) [9-10]. The model assumes that switching occurs upon the nucleation of successive metastable domains throughout the GSSN layer as depicted in eq.1 & 2 of **Fig. 23**. Monte-Carlo simulation were undertaken assuming standard deviations of 1nm and 0.1eV for the OTS thickness and zero-field nucleation barrier respectively evidencing a successful agreement with experimental data (**Fig.24a**). Finally, $V_{th1}$ switching voltage distribution of 1S1R was obtained by correlating OTS switching voltage with OxRAM $R_{HRS}$ dispersion, reproducing experimental data (**Fig.24.b**).

#### 2) Device optimization

**Fig.25** shows calculated $V_{th1}$ for various reported RRAM technologies assuming 15nm OTS. Higher $R_{HRS\text{-}OxRAM}$ median value increases $V_{th1}$ and therefore larger voltage margin, improving 1S1R reliability. In **Fig.26**, measured $V_{th1}$ is reported for various GSSN thicknesses, showing that reading window is insured in all cases. $R_{HRS\text{-}OxRAM}$ was calculated from measured $V_{th1}$ in each configuration and agrees with values measured on 1T1R OxRAM structures [11]. **Fig.27** illustrates the measured tradeoff between OTS leakage current and switching voltage (changing OTS thickness) and shows that increased GSSN thickness improves read margin. Finally, **Table.1** summarizes the overall excellent 1S1R performances in this work benchmarked with data reported in literature.

## IV. CONCLUSIONS

OxRAM-OTS reliability was investigated based on experiments on 1S1R arrays. Current margin (~$10^3$) and selectivity (~$10^5$) during more than $10^6$ programming cycles and $10^8$ reading cycles were demonstrated and are compatible with 100Mb-1Gb crossbar bank sizes. We experimentally and theoretically showed that voltage read margin variability is the most critical feature. This latter was correlated thanks to semi analytical model to intrinsic variability of both OTS switching phenomenon and OxRAM HRS resistance dispersion.

**Acknowledgments:** This work has been partially supported by the European 783176 WAKeMeUP project and the LABEX MINOS ANR-10-LABX-55-01.

**References:** [1] S.R. Ovshinsky, *Phys. Rev. Lett.*, vol. 21, pp. 1450-1453, 1968. [2] G. Navarro et al., *in Proc. 2017 VLSI*, T94-T95, 2017. [3] M. Alayan et al. *in Proc. 2017 IEEE IEDM*, pp. 2.3.1-2.3.4, 2017. [4] D. Alfaro Robayo et al. *in Proc. 2019 IEEE IMW*, pp. 1-4, 2019. [5] T. Kim et al. *in Proc. 2018 IEEE IEDM,* pp. 37.1.1-37.1.4, 2018. [6] S. Yasuda et al., *in Proc. 2017 VLSI*, T30-T31, 2017. [7] A. Verdy et al. *in Proc. 2018 IEEE IEDM,* pp. 37.4.1-37.4.4, 2019 [8] A. Verdy et al. *in Proc. 2018 IEEE IRPS,* pp. 6D.4-1-6D.4-6, 2018 [9] V.G. Karpov et al., PRB, 78, 052201, 2008. [10]V.G. Karpov et al., APL, 90, 123504, 2007 [11] G. Sassine et al. *in Proc. 2018 IEEE IMW* pp. 1-4, 2018 [12] Sung Hyun Jo et al. *in Proc. 2014 IEEE IEDM,* pp. 6.7.1-6.7.4, 2014

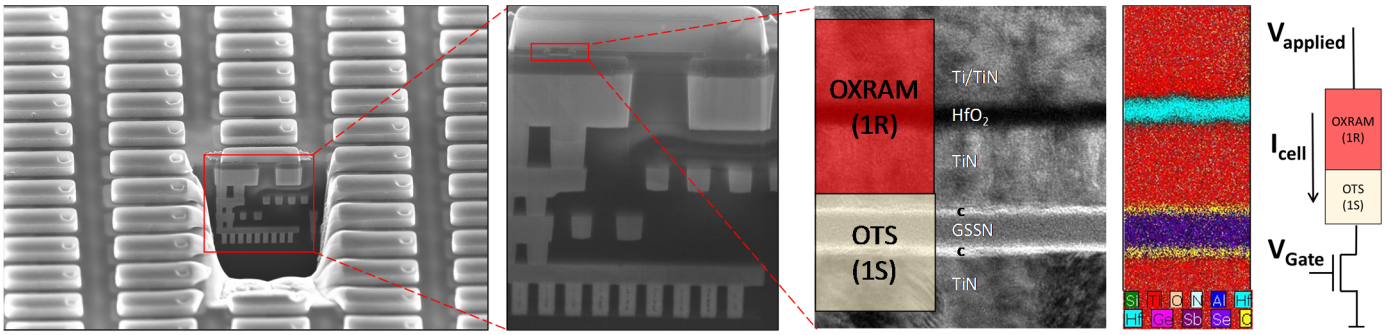



Fig. 1. (a-b) SEM images of the 1T1S1R system showing the 1S1R stack integrated in M4 on top of FEOL transistor. (c-d) TEM and EDX cross sections of the 1S1R stack with $HfO_2$/Ti OxRAM and GeSeSbN OTS.

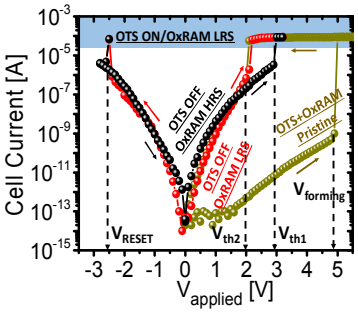



Fig. 2. Typical IV characteristics of the 1S1R stack (GSSN 15nm) for forming, RESET, and SET operations. Programming current is controled by a select transistor.

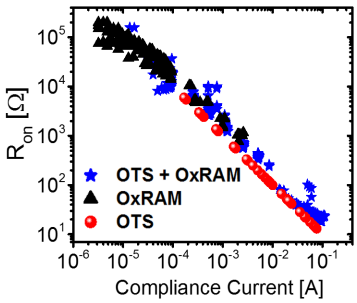



Fig. 3. Impact of the programming current (controled by the select transistor) on the ON state resistance for OTS, OxRAM and OxRAM+OTS structures.

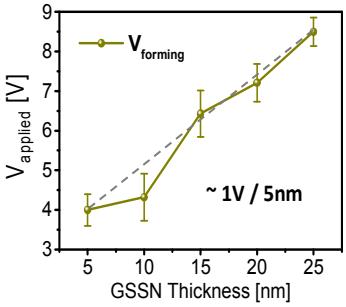



Fig. 4. Impact of GSSN thickness on 1S1R forming voltage (DC mode).

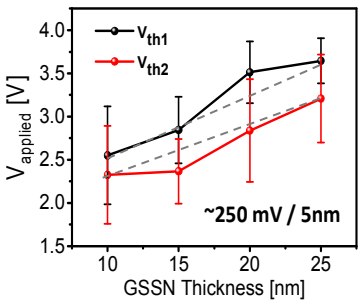



Fig. 5. Impact of GSSN thickness on 1S1R DC switching voltage when the OxRAM is in HRS ($V_{th1}$) and in LRS ($V_{th2}$).

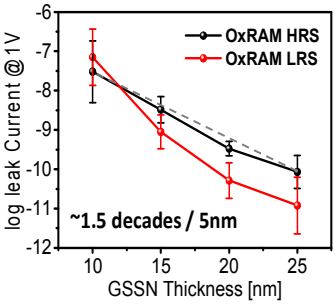



Fig. 6. Impact of GSSN thickness on 1S1R leakage current measured at 1V (DC mode) when the OxRAM is in LRS and in HRS.

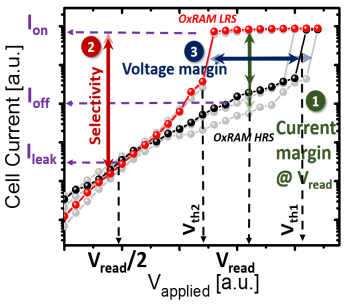



Fig. 7. Representation of the three key features investigated in this work: current margin at $V_{read}$ ($I_{on}/I_{off}$), selectivity ($I_{on}/I_{leak}$), and voltage margin ($\Delta V_{th}= V_{th1} - V_{th2}$)

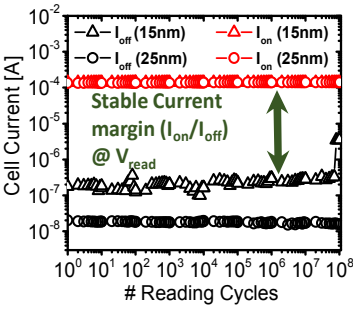



Fig. 8. Reading cycles of 1S1R (for 15nm and 25nm GSSN) without 1S switching when the 1R is in HRS and with 1S switching when the OxRAM is in LRS.

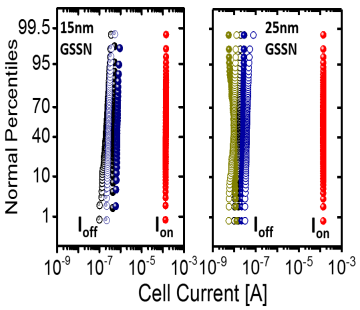



Fig. 9. Distribution of read current for ON and OFF states for various 1S1R devices, illustrating the window margin (from Fig.8). (left) 15nm GSSN, (right) 25nm GSSN.

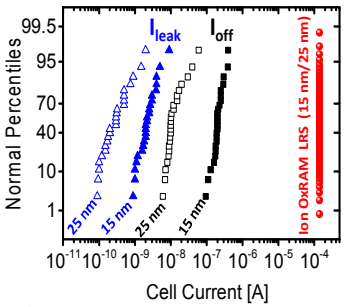



Fig. 10. $I_{on}$, $I_{leak}$ (V/2 read scheme) and $I_{off}$ distributions for 1S1R cells for 15nm and 25nm GSSN.

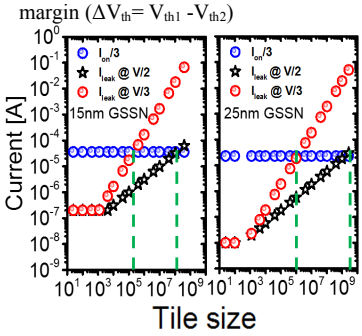



Fig. 11. Impact of the tile size (crossbar array) on the cumulated leakage current due to sneak paths on selected word and bitlines. Maximum tile size is reached when total leakage current reaches $I_{ON}/3$. 15nm and 25nm GSSN are represented.

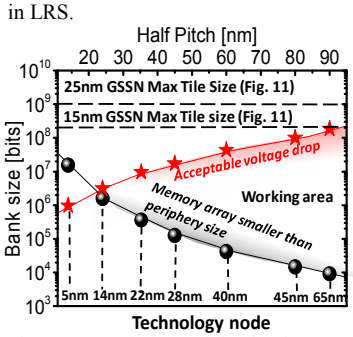



Fig. 12. Evolution of bank size as function of the technology half pitch. Working areas are defined depending on (1) voltage drop along the metal line, (2) memory/periphery area ratio, (3) total $I_{leak}$ vs read $I_{off}$.

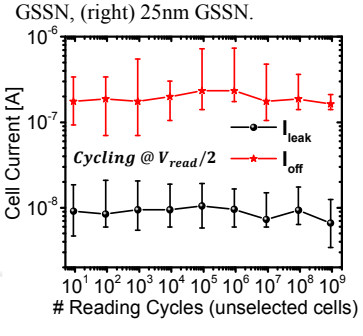



Fig 13. Evolution of $I_{off}$ and $I_{leak}$ for non selected cells: $V_{read}/2$ is applied for each reading cycle. Error bars correspond to min and max values on 6 1S1R devices (15nm GSSN).

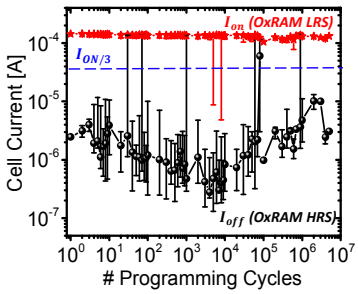



Fig. 14. Endurance characteristics of 30 1S1R structures (15nm GSSN). $t_{pulse}$=1µs. Current is read at 3.4V in transient mode.

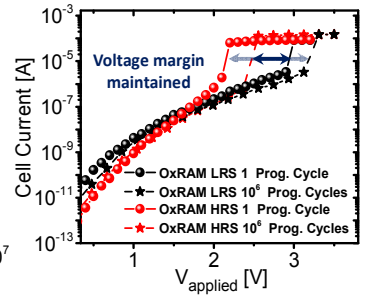



Fig. 15. IV DC characteristics of 1S1R (15nm GSSN). $\Delta V_{th}$= $V_{th1}$ -$V_{th2}$ window is maintained after $10^6$ cycles.

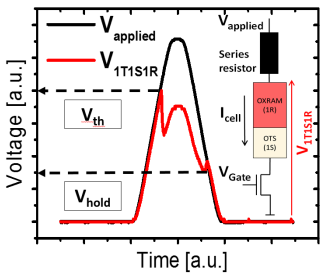



Fig. 16. Schematic of the pulse mode setup used to measure $V_{th1}$, $V_{th2}$ and $V_{hold}$ switching voltages. A series resistor allows to detect the switching events at $V_{th}$.

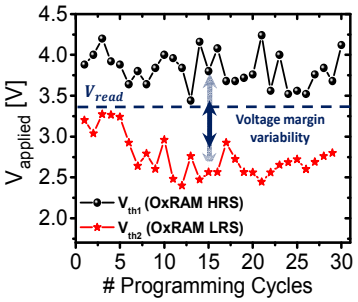



Fig. 17. $V_{th1}$ and $V_{th2}$ measured on SET RESET cycles on ~30 1S1R cells (25 nm GSSN).

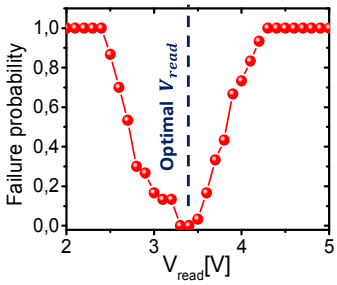



Fig. 18. Probability to read a 1S1R cell in the good state depending on the reading voltage. Adjusting $V_{read}$ optimizes read yield.

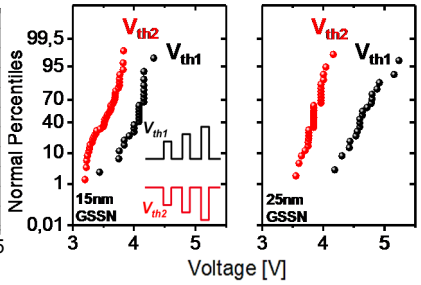



Fig. 19. $V_{th1}$ and $V_{th2}$ distributions of 1S1R cells before aging for 15nm and 25nm GSSN thickness. Staircase pulses are used to increase accuracy of $V_{th}$ extraction.

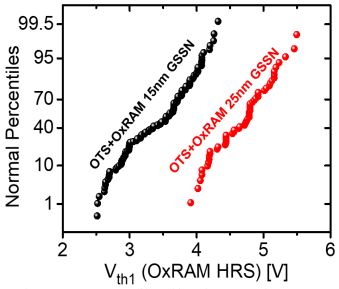



Fig. 20. $V_{th1}$ distributions of 1S1R cells for 15nm and 25nm GSSN thickness.

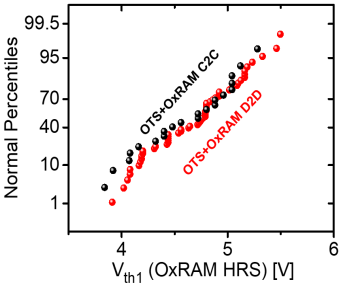



Fig. 21. $V_{th1}$ Device to device (D2D) vs Cycle to Cycle (C2C) distributions of 1S1R cells for 25nm GSSN thickness.

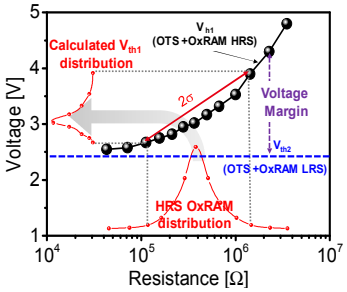
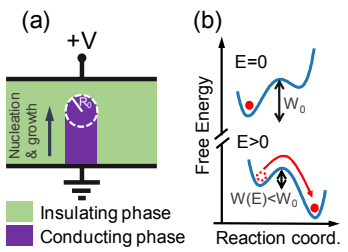



Fig. 22. Calculated $V_{th1}$ (15nm GSSN) versus OxRAM $R_{HRS}$. $V_{th1}$ distribution (left) is calculated for each measured $R_{HRS}$ value (down). HRS variability [11] leads to $V_{th1}$ dispersion, reducing the reading margin.




**Free energy:**

(1) $W(E) = \frac{W_0}{\left(1 + 4\pi\epsilon_0\epsilon_r \frac{R_0^3}{W_0} E^2\right)^2}$

**Nucleation time:**

(2) $\tau_n = \frac{1}{\nu} \exp\left(-\frac{W(E)}{k_b T}\right)$

E: Electric field [V/m]
$W_0$: zero-field nucleation barrier: 2.65 eV
$R_0$: domain radius: 3 0 nm
$\varepsilon_r$: relative permittivity: 10.0

Fig 23. Description of the semi-analytical model used to describe OTS switching based on field-induced nucleation theory. Equations describing free energy and nucleation time depending on material parameters.

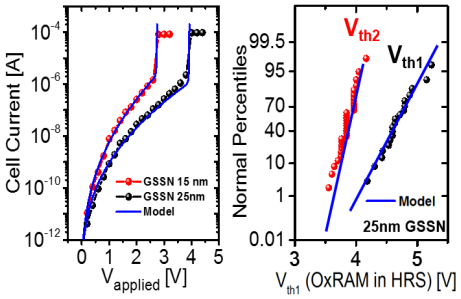



Fig 24. (a) Simulation (from Fig.23) of IV characteristics of 15nm and 25nm OTS. (b) Measured and simulated $V_{th2}$ (OxRAM in LRS) and $V_{th1}$ (OxRAM in HRS) switching voltages for 25nm OTS.

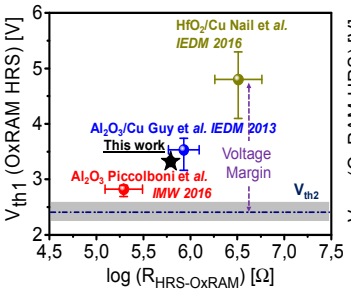



Fig. 25. Impact of OxRAM $R_{HRS}$ mean value and dispersion (from litterature) on $V_{th1}$ value and dispersion. $V_{th1}$ is calculated based on the voltage drop in the RRAM and OTS using a Poole-Frenkel conduction regime in the HRS.

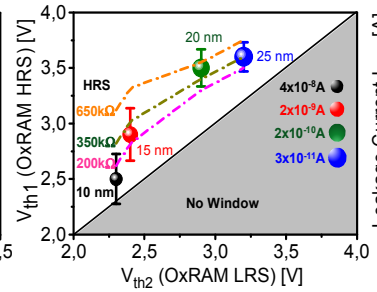



Fig. 26. Measured $V_{th1}$ and $V_{th2}$ for various GSSN thicknesses. The size of the symbols represents $I_{leak}$ value. Dashed lines: calculated $V_{th1}$ for various OxRAM $R_{HRS}$ allowing to estimate $R_{HRS}$ in all cases. Acceptable voltage margin $\Delta V_{th}$= $V_{th1}$ -$V_{th2}$ is achieved for sufficient $R_{HRS}$.

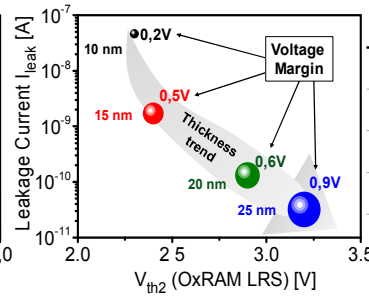



Fig. 27. Experimental $I_{leak}$ vs $V_{th2}$ for various GSSN thickness showing that $I_{leak}$ decreaseswith $V_{th2}$ increase. The size of the symbols represents the reading window (proportionally compared to other GSSN thicknesses), the thicker the GSSN, the wider the reading voltage margin.

| Device feature | This work | [12] | [6] | [3] | Impacted by |
|---|---|---|---|---|---|
| Selectivity $I_{on}/I_{leak}$ | $10^6$ | $10^6$ | - | 100 | OTS leakage |
| Endurance #cycles | $5.10^6$ | $10^5$ | $10^7$ | - | RRAM endurance |
| Read end. #cycles | $10^8$ | $10^8$ | $10^8$ | $10^6$ | OTS endurance |
| Current margin $I_{on}/I_{off}$ | $10^3$ | $10^3$ | >10 | 10 | $I_{prog}$ OTS $I_{off}$ |
| Read voltage margin $\Delta V_{th}$ | 1V | 1V | 1V | 1V | OTS and RRAM variablity |

Table 1. Summary table describing the physical origin of failure for the 3 main 1S1R realibility features addressed in this work.