

Resistive Switching Behavior of Titanium Oxynitride Fabricated Using a Thermal Nitridation Process

Chih-Chieh Hsu¹, Member, IEEE, and Wun-Ciang Jhang¹

Abstract—A titanium oxynitride (TiO_xN_y) resistive random-access memory (RRAM) with write-once-read-many-times (WORM) characteristics is proposed. The TiO_xN_y resistive switching (RS) layer with a thickness of 62 nm was fabricated using a thermal nitridation process of an evaporated Ti metal film. The residual Ti layer with a thickness of 8 nm is used as the bottom contact. The $\text{Al}/\text{TiO}_x\text{N}_y/\text{Ti}/\text{n}^+\text{-Si}$ RRAM shows a large memory window of 10^7 at a low read voltage of 0.2 V. Stable high-resistance state (HRS) and low-resistance state (LRS) are observed in the endurance test for 10^4 read cycles. High read-disturb immunity can be found for over 10^4 s. The energy band diagram, carrier conduction and the RS mechanisms of the RRAM are investigated.

Index Terms—Titanium oxynitride, nitridation, resistive memory, write-once-read-many-times (WORM).

I. INTRODUCTION

CHEMICAL vapor deposition (CVD) is a common method for fabrication of oxide and nitride materials. In complementary metal-oxide-semiconductor (CMOS) processes, CVD-grown SiO_2 and Si_3N_4 films can be used as gate insulators or surface passivation layers. In recent years, CVD is also considered as an alternative epitaxial growth of large graphene crystals [1]. However, thin films grown by thermal oxidation and nitridation are suitable for large-scale productions, and they have advantages of high quality, good adhesion and excellent uniformity [2].

Metal oxide materials are known to be promising for fabricating embedded resistive random-access memory (RRAM) cells, and they can be easily integrated with back-end-of-line process [3], [4]. A WO_x RRAM using a rapid thermal oxidation process was demonstrated in [3]. WO_x was obtained by annealing a W plug in oxygen ambient at 500 °C. The ratio of the resistance in the high resistance state (HRS) to that in the low resistance state (LRS) is 5. In [4], thermal

oxidation processes at 350 °C and 450 °C were employed to W to fabricate $\text{TiO}_x\text{N}_y/\text{WO}_x/\text{W}/\text{TiN}$ resistive memory cells. The resistive window is >10 . The resistive switching (RS) mechanism is explained with a model, which is based on the movement of oxygen ions in the WO_x RS layer.

Titanium and Ti-based compounds are known to be indispensable in device technologies such as photovoltaic devices [5], [6] and energy devices [7]. Ti, TiO_2 , and TiN are also widely used as electrodes, adhesion layers and diffusion barriers in device fabrication and semiconductor processes [8]–[10]. Among them, Titanium oxynitride (TiO_xN_y) has drawn much attention in device applications because of its good photocatalytic behavior and high insulation property [11]. It has been extensively employed in optoelectronic devices and CMOS technology [12]. However, application of TiO_xN_y in RRAM technology is seldom observed.

This work demonstrates the write-once-read-many-times (WORM) behavior of a TiO_xN_y RRAM. In addition, the TiO_xN_y RS layer was grown by thermally nitriding a Ti metal layer, rather than by a CVD process. The $\text{Al}/\text{TiO}_x\text{N}_y/\text{Ti}/\text{n}^+\text{-Si}$ device exhibits a large memory window, a low read voltage and high stability. The energy band diagram is depicted. The carrier conduction and RS mechanisms are investigated, and their correlation is also discussed.

II. EXPERIMENTS

Titanium oxynitride (TiO_xN_y), which was fabricated by thermally nitriding a Ti metal thin film, was used as the RS layer of the $\text{Al}/\text{TiO}_x\text{N}_y/\text{Ti}/\text{n}^+\text{-Si}$ WORM memory. First, the native oxide on a $\text{n}^+\text{-Si}$ substrate was stripped using a buffered oxide etch solution. Second, a Ti metal layer was deposited on the $\text{n}^+\text{-Si}$ substrate using a thermal evaporator. Then, the sample was treated in a furnace under flowing N_2 at 700 °C for 4 h. After that, Al was deposited using the thermal evaporator as the top electrode. The device was reproduced five times and measured with the same voltage sweep condition. The surface morphologies of the Ti films before and after the nitridation process were examined using a scanning electron microscope (SEM, JSM-6701F). The chemical composition of the TiO_xN_y layer was investigated by X-ray photoelectron spectroscopy (XPS, JAMP-9500). The $\text{Al}/\text{TiO}_x\text{N}_y/\text{Ti}/\text{n}^+\text{-Si}$ WORM memory is analyzed using a transmission electron microscope (TEM, JEOL-3010). A Keysight B1500A semiconductor device analyzer was used to measure the electrical characteristics.

III. RESULTS AND DISCUSSION

Fig. 1(a) shows the SEM image of the Ti metal layer before the nitridation process. The film is compact without cracks

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The authors are with the Graduate School of Engineering Science and Technology, National Yunlin University of Science and Technology, Douliu 64002, Taiwan, and also with the Graduate School of Electronic Engineering, National Yunlin University of Science and Technology, Douliu 64002, Taiwan (e-mail: cchsu@yuntech.edu.tw; M10713323@yuntech.edu.tw).

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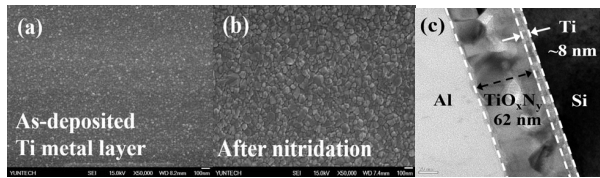


Fig. 1. SEM images of the Ti metal layer (a) before and (b) after nitridation process. (c) TEM cross-sectional image of the Al/TiO_xN_y/Ti/n⁺-Si memory.

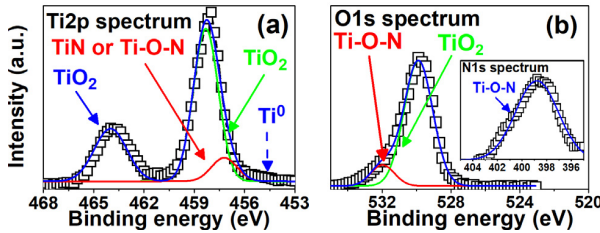


Fig. 2. XPS (a) Ti2p and (b) O1s spectra of the TiO_xN_y layer. The inset in (b) is the N1s spectrum.

or voids, and the surface is smooth. After the nitridation process, significant grain growth is observed, as shown in Fig. 1(b). Grains with sizes of ~20–40 nm can be found. The film is intact without noticeable exfoliation. Fig. 1(c) shows the TEM cross-sectional image of the Al/TiO_xN_y/Ti/n⁺-Si memory. A distinct TiO_xN_y layer between the Ti metal layer and the top Al electrode is observed. The thickness is 62 nm. Notably, large grains with sizes of ~20–40 nm are observed in the TiO_xN_y layer, which is consistent with the finding in the SEM image. After the nitridation process, most of the Ti film is transformed into TiO_xN_y. Only a thin Ti layer with a thickness of 8 nm remains.

Fig. 2(a) shows XPS Ti2p spectrum of the TiO_xN_y RS layer. Two distinct peaks at 464 eV and 458 eV are observed. The peak at the higher binding energy is assigned to the Ti⁴⁺ in TiO₂ [13]. The peak at the lower binding energy can be deconvoluted into two contributions. The Gaussian peak centered at 458.3 eV is also attributed to the Ti⁴⁺ in TiO₂, while the other peak at 457.2 eV is assigned to Ti³⁺ in TiO_xN_y or TiN [13]. The Ti XPS result indicates that the nitrogen is successfully incorporated into the film by the nitridation process, and residual oxygen in the annealing ambient also joins the reaction to yield TiO_x and TiO_xN_y. Notably, the binding energy for the XPS peak caused by Ti⁰ is 454.3 eV [14], where is indicated in Fig. 2(a). A clear peak is not found at this position, which verifies that the Ti in the TiO_xN_y layer is almost transformed to TiO_xN_y, TiN and TiO_x. To further confirm the chemical structure of the TiO_xN_y layer, XPS O1s and N1s spectra are examined and revealed in Fig. 2(b). A strong O1s peak, which is composed of two Gaussian peaks, is observed. The major peak centered at 529.9 eV corresponds to TiO₂, while the minor peak at 532 eV is related to TiO_xN_y [15]. The N1s spectrum shown in the inset of Fig. 2(b) reveals a peak located at 398.7 eV, which is also attributed to the Ti-O-N species [13]. The XPS results for Ti, O and N are mutually consistent, and they confirm that the distinct layer observed in the TEM image (Fig. 1(c)) is composed of TiO_xN_y.

Fig. 3(a) shows RS characteristics of the Al/TiO_xN_y/Ti/n⁺-Si WORM memory with voltage loops of 0 V → 4 V → 0 V → -4 V → 0 V. The voltage was applied to the Al top electrode while the n⁺-Si was grounded. A sudden current increase can be observed during the voltage sweep

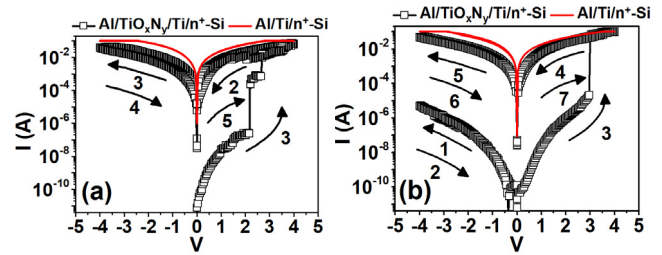


Fig. 3. Current-voltage characteristics of the TiO_xN_y memory with voltage loops of (a) 0 V → 4 V → 0 V → -4 V → 0 V and (b) 0 V → -4 V → 0 V → 4 V → 0 V.

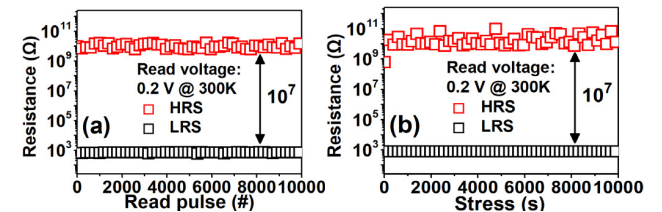


Fig. 4. (a) Read endurance and (b) read disturb test of the TiO_xN_y memory.

of 0 V → 4 V, corresponding to a RS from a HRS to a LRS. Afterward, the memory remains in the LRS in the following voltage sweeps. Notably, the LRS current does not achieve the compliance current. The I-V curves indicate that once the data is written into the memory, it cannot be erased, which corresponds to WORM behavior.

To confirm the effect of nitridation, the I-V curves of the as-deposited Ti layer are also measured and depicted in Fig. 3. Obviously, a high conduction current and nonswitching behavior are observed. Notably, the current in the high voltage region is limited by the compliance current. Fig. 3(b) shows RS characteristics of the Al/TiO_xN_y/Ti/n⁺-Si WORM memory with reverse voltage cycles. Difference in the currents is not observed during the initial voltage sweep of 0 V → -4 V → 0 V. When the voltage sweeps to the positive voltage region, an abrupt current increase is found, corresponding to the RS from the HRS to the LRS, and the resistance state is unchanged in the following voltage cycles. The measurement results presented in Fig. 3(a) and (b) indicate that the writing process of the Al/TiO_xN_y/Ti/n⁺-Si WORM memory can only occur in the positive voltage region and suggest that the RS behavior is induced by the drift of positive metal ions from the metal electrode [16]. The same RS behavior is observed in the reproduced TiO_xN_y memories. The I-V curves show nearly the same resistance window, and the set voltages are all ~3.5 V.

Fig. 4(a) shows read endurance characteristics of the Al/TiO_xN_y/Ti/n⁺-Si memory at a read voltage of 0.2 V. Stable HRS and LRS are observed for over 10⁴ read cycles. The memory window is 10⁷, which is significantly larger than the value of 10⁵ of an Au/TiO₂/Au memory [17]. A read-disturb test was further performed to examine the data retention capability, as shown in Fig. 4(b). A clear memory window of 10⁷ is also observed. Degradation in the HRS and the LRS is not detected for over 10⁴ s. The WORM property and the large memory window of the Al/TiO_xN_y/Ti/n⁺-Si device is verified. In literature, e-gun evaporation, thermal oxidation, and sol-gel processes are usually used to fabricate Ti-related RRAMs. The reported read voltages are 0.25–1 V and resistive windows are 5–10⁵ [3], [4], [17]–[19]. By comparison, the TiO_xN_y RRAM demonstrated in this paper shows a progress in the performance.

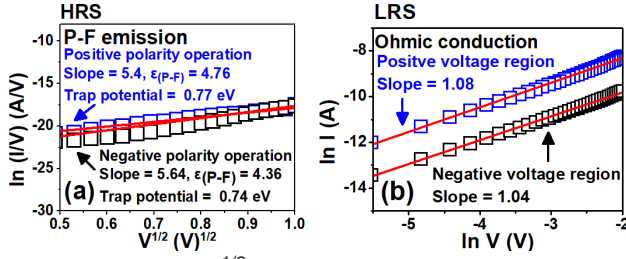


Fig. 5. (a) $\ln(I/V)$ vs. $V^{1/2}$ plot (P-F emission) and (b) $\ln I$ vs. V plot (Ohmic conduction) of the TiO_xN_y memory under positive and negative voltage operations.

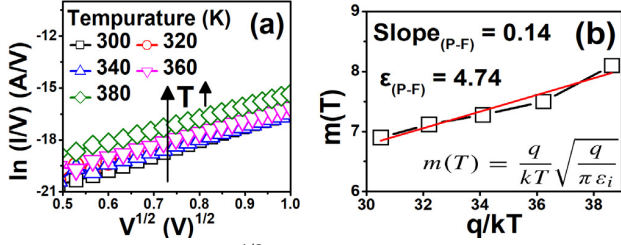


Fig. 6. (a) $\ln(I/V)$ vs. $V^{1/2}$ plot as a function of temperature and (b) dependence of $m(T)$ on the temperature for the TiO_xN_y memory.

As observed in the XPS and TEM analyses [Fig. 1 and Fig. 2], the TiO_xN_y film is not single-crystalline and is composed of different chemical structures. Therefore, crystal defects and oxygen vacancy defects in the TiO_xN_y film are expectable. Fig. 5(a) shows a $\ln(I/V)$ vs. $V^{1/2}$ plot of the TiO_xN_y memory in HRS. A clear linear relationship is observed both in positive and negative voltage operations, suggesting that P-F emission is a possible conduction mechanism for carrier transport [20]. We also investigated the $\ln(I/V)$ vs. $V^{1/2}$ relationship of the TiO_xN_y memory under unipolar operations. A linear relationship is also found (not shown). The dielectric constants extracted under different operation modes are 3.5–4.76. According to the P-F equation, where the μ is $1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [21] and the N_c is $\sim 2.5 \times 10^{19} \text{ m}^{-3}$ [22], the trap level ϕ_t can be further extracted from the intercepts of the fitting lines [20]. The ϕ_t are found to be 0.74–0.82 eV, which is highly in agreement with the value of 0.81 eV reported in the literature [23].

Temperature dependence analysis was further performed to confirm the conduction mechanism. As indicated in Fig. 6(a), $\ln(I/V)$ indeed increases with an increasing temperature. In addition, the $\ln(I/V)$ vs. $V^{1/2}$ curves measured at different temperatures all show a clear linear relationship. This observation is consistent with the prediction of the P-F equation [24]. By plotting $m(T)$ as a function of q/kT , where $m(T)$ is $[q/(e\pi)]^{0.5}/kT$ [25], the dielectric constant can be extracted from the slope of the linear fitting line. It is found to be 4.74 [Fig. 6(b)], which is consistent with the value of 3–10 proposed in the literature [11], and is also highly in agreement with the values of 3.5–4.76 extracted from the slopes of the $\ln(I/V)$ versus $V^{1/2}$ plots measured at room temperature. The above analyses verify that P-F mechanism is responsible for the carrier conduction of the TiO_xN_y memory in the HRS. When the TiO_xN_y memory switches to the LRS, a linear relationship with slopes of 1.04 and 1.08 ($I \propto V$) is observed in the $\ln I$ vs. $\ln V$ plot [Fig. 5(b)], which indicates that the current of the TiO_xN_y memory in the LRS is dominated by Ohmic conduction.

Fig. 7(a) shows the energy band diagram of the $\text{Al/TiO}_x\text{N}_y/\text{Ti}/n^+-\text{Si}$ device in the HRS. Carriers emitted from

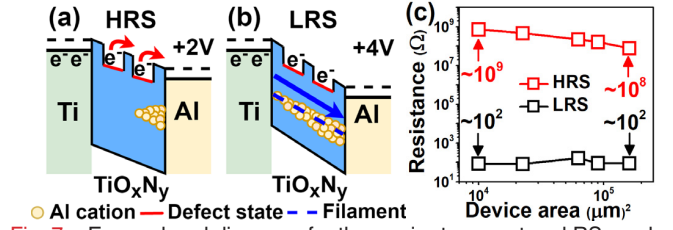


Fig. 7. Energy band diagrams for the carrier transport and RS mechanism when the TiO_xN_y memory is in the (a) HRS and (b) LRS. (c) Size dependencies of the HRS and LRS for the TiO_xN_y memory.

the traps induced by thermal excitation and P-F barrier lowering effect [26] are responsible for the conduction current. Reversible RS behavior, which is caused by the carrier trapping in the TiON and SiO_2 layers, of a $\text{W/TiN/TiON/SiO}_2/n^+-\text{Si}$ device was reported in [19]. A SiO_2/TiON bilayer and an inert W electrode are required for obtaining the reversible RS behavior. In this study, a single TiON layer and an active Al electrode were used to fabricate the RRAM. When a positive bias was applied to the Al electrode, Al cations can be easily generated. Then, they start to drift into the TiO_xN_y RS layer [16]. The injected Al cations are reduced to Al by the electrons coming from the anode. Once the conductive filaments between the cathode and the anode are formed, an abrupt current increase is observed, and the memory switches from the HRS to the LRS [Fig. 3(a)]. As depicted in Fig. 7(b), because electrons can easily be transported via the conductive path, Ohmic conduction is expectable, as is verified in Fig. 5(b). These established solid filaments are difficult to fully rupture in the following voltage sweeps [27]. Therefore, the RS is irreversible, and the write-once-read-many-times behavior is observed. WORM characteristics induced by Al filaments have also been reported in [28].

To further verify the proposed filamentary mechanism, size dependencies of the HRS and LRS are studied and shown in Fig. 7(c). A decrease in one order of magnitude in the R_{HRS} is observed as the device area increases from 10^4 to $\sim 10^5 \mu\text{m}^2$. When the TiO_xN_y memory is in the HRS, no conductive filaments are formed, and therefore the current flows uniformly across the TiO_xN_y layer. An increase in the current, corresponding to a decrease in the resistance, is expected as the device area increases. When the conductive filament is formed in the TiO_xN_y layer (LRS), the carriers will transport via this localized conductive path. Therefore, the device area has little impact on the LRS resistance [29]. The finding verifies that the filamentary mechanism is valid for explaining the switching behavior of the TiO_xN_y memory.

IV. CONCLUSION

The WORM characteristics of the $\text{Al/TiO}_x\text{N}_y/\text{Ti}/n^+-\text{Si}$ RRAM with a memory window of 10^7 is demonstrated. The distinct TiO_xN_y layer with polycrystalline grains is clearly observed in the TEM image. The TiO_xN_y layer is composed of Ti-O-N, Ti-O and Ti-N, as is verified by XPS analysis. The RS behavior of the RRAM is induced by the drift of the metal cations because the RS can only occur in the positive voltage region. The non-volatility and the high stability of the data storage are observed in the endurance and read-disturb tests. The carrier conduction mechanism in the HRS is dominated by Poole-Frenkel emission. When the RRAM switches to the LRS, carriers transport via the conductive metal filaments, and the Ohmic conduction is responsible for the device current.

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