Effect of Moisture Stress on the Resistance of HfO_2/TaO_x-Based 8-Layer 3D Vertical Resistive Random Access Memory

Rui Gao, Dengyun Lei, Zhiyuan He, Yiqiang Chen, Yun Huang, Yunfei En, Xiaoxin Xu, and Feng Zhang

***Abstract*— Non-filament 3D vertical random access memory (VRRAM) is a promising technology for emerging high-density memory applications, which can significantly improve system performance by simplifying memory hierarchy. Reliability issue is one of the most challenging concerns precluding the commercial application of RRAM. The bulk of RRAM reliability papers focus on the electric stress, while the effect of moisture stress from ambient environment has seldomly been studied. In this brief we examine the aging kinetics of moisture stress through statistical measurements on state-of-the-art 8-layer 3D VRRAMs. The results reveal that R_{HRS} and on/off window declines significantly while R_{LRS} remains unaltered in terms of the average value of multiple devices. Meanwhile, reset current Ireset increase obviously. Moreover, different layers exhibit the same aging kinetics. We speculate the observed degradation is due to the moisture stress introduces defects at HfO_2/TaO_x interface and brings down the barrier.**

***Index Terms*— Moisture stress, 3D vertical RRAM.**

I. Introduction

ASCRIBING to the growing disparity of speed between CPU and memory, memory latency is becoming an overwhelming bottleneck in system performance. High-performance and low-cost emerging non-volatile Memories (NVMs) is a promising way to boost the system performance through simplifying memory hierarchy and filling the performance and density gap between memory and storage [1]. 3D vertical RRAM is one of the most competitive candidates for emerging NVMs by virtue of simple structure, excellent compatibility with CMOS fabrication, and easy integration in the back end of line.

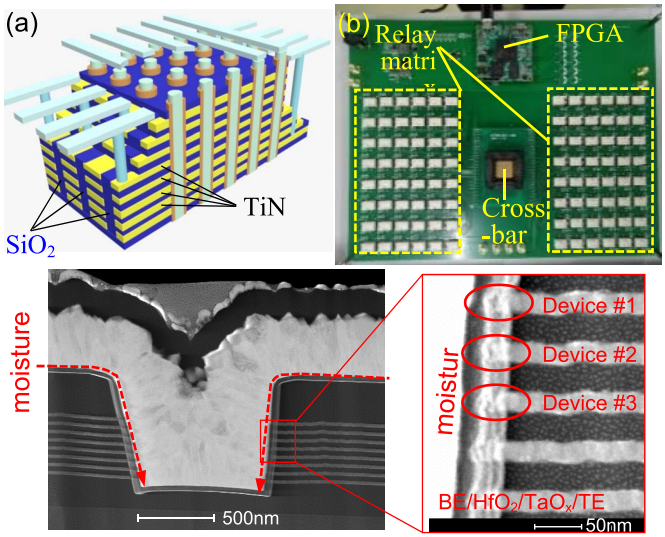

Fig. 1. (a) Schematic of the 3D VRRAM crossbar architecture, the top layer is 1st. (b) FPGA-controlled relay matrix to achieve test automation. (c) TEM image of our device structure with the moisture permeation path illustrated in the dashed arrows.

Owing to the above-mentioned advantages, RRAM has received enormous attention from both industrial and academic communities. Among the ever-increasing amount of RRAM reliability papers published in recent years, only very few reports on the moisture stress. This is not entirely surprising: many RRAM suffer from large variability in their resistance and switching characteristics [2], [3], which can easily obscure the time-dependent effects of ambient environment and make statistical measurements on multiple RRAM device a prerequisite. Moreover, among the limited number of moisture-related RRAM papers, only 2D planar devices are investigated, all of which are filamental RRAMs [4]–[7]. To the best of authors' knowledge, moisture effect on 3D vertical RRAM, has not been reported yet.

II. Device and Experiments

The architecture of the 8-layer 3D VRRAM crossbar used in this work was shown in Fig. 1a. Firstly SiO_2(200nm)

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was deposited on a Si substrate as the bottom layer, then 8 TiN(20 nm)/SiO_2(20 nm) layers were deposited by PVD and PECVD alternately form the plain electrodes and isolation, SiO_2(250nm) was deposited as the capping layer. A Trench is dry etched down to the bottom SiO_2 layer to split the plane electrode (Write Line: WL). After SiO_2 filling in the trench, 500 nm hole is etched down to the bottom SiO_2. HfO_2/TaO_x bilayer were deposited on the sidewall sequentially by ALD and sputtering, followed by depositing of Ti/TiN/W by the sputtering to fill the hole as the pillar electrode (Bit Line: BL). Each horizontal WL was opened by selective etching successively. The size of the memory cell was defined by the thickness of bottom electrode TiN and the perimeter of the hole [8].

We recently proposed an automated test scheme to measure the resistance statistics of RRAM crossbar array [9]. To implement repetitive tests for statistics, the crossbar was encapsulated using ceramic quad flat package with a copper cap and then embedded in a PCB board on which an FPGA-controlled relay matrix was adopted as a switching matrix enabling access to all devices without changing the cabling, as illustrated in Fig. 1b.

To explore the gradual degradation under moisture stress, "Measure-Stress-Measure" scheme was adopted in this brief. The resistance statistics of fresh devices was firstly measured through an FPGA-controlled automated testing scheme (Fig. 1b) as described in [9], then the crossbar encapsulation cap was unfolded and the non-hermetic devices were exposed to 85°C/85% relative humidity (RH) conditions (IPC/JEDEC J-STD-020D [10]) in a humidity chamber for an intermittent stress time of 0.17, 0.5, 1, 3, 13, 44, 100 hours ("hrs" for short in figures to save space), resulting in an accumulated stress time ("stress time" for short in the following context) of 0.17, 0.67, 1.67, 4.67, 17.67, 61.67 and 161.67 hours, respectively. After each stress period, the devices were taken out and measured to monitor the degraded resistance. All the measurements were carried out under room temperature with Keysight B1500. Dual IV sweep from -3V to 5V was performed to get the switching characteristics and Vread was selected to be 3V to calculate R_{HRS}, R_{LRS}.

III. Results and Discussion

The moisture-induced aging kinetics of two individual devices are shown in Fig. 2. The top panels show the IV on both fresh and stressed devices, for the readability only fresh and 1.67 and 61.67 hours stressed IV characteristics are plotted, as shown in. Fig. 2a&f. The entire aging kinetics R_{HRS}, R_{LRS} and on/off Window ("Window" for short) data obtained at Vread = 3V from the IV curves are shown in Fig. 2b–d&g–i. Fresh data is also plotted in each panel for comparison. Due to the stress time is in log scale, fresh data is plotted at 0.01s stress time (far smaller than the first stress time 0.17s) instead of zero in order to be displayed. Note the y-axis intervals in Fig. 2b–d&g–i are set to be exactly the same for the convenience of visual comparison. We see the aging kinetics exhibits large device-to-device variability, and manifests non-monotonous dynamics against stress time within a single

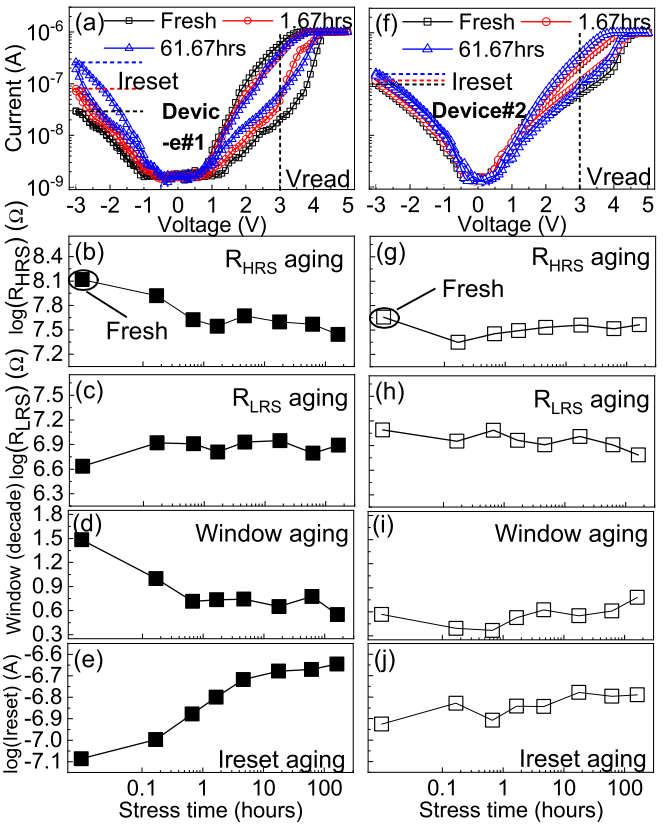

Fig. 2. Aging kinetics of 2 individual devices. Due to the large variation of IV characteristics (a&f), R_{HRS} (b&g), R_{LRS} (c&h), Window(d&i) and Ireset(e&j) aging on individual device exhibit very different behavior, making statistics measurement on multiple devices indispensable to investigate the moisture stress kinetics.

device, making multiple devices measurements requisite to examine the moisture stress kinetics. In the negative bias region, Ireset at −3V is also monitored to disclose the underlying mechanism of moisture-induce stress, which turns out to be increasing against stress time on both devices.

By adopting the test scheme in [9], we managed to obtain the statistics of aging kinetics of moisture stress on multiple devices, as illustrated in Fig. 3. It is observed although the aging kinetics on a single device seems to be stochastic, their average exhibits clear trends and reveals the effects of moisture. μ_R_{HRS} declines by 0.36 decade after 161.67 hours stress, while μ_R_{LRS} shows only a fluctuation within ±0.034 decades referring to the fresh value. As the difference between μ_R_{HRS} and μ_R_{LRS}, μ_Window manifest a 0.39 decade decrease compared to fresh state, which might cause failure in RRAM memory circuits. Control experiments under 85°C/0%RH are carried out to exclude the temperature impact, the negligible degradation indicates aging under 85°C/85%RH is mainly due to moisture. Moreover, Fig. 3 shows the degradation hardly recovers under 105°C 24 hours' baking, which makes the reliability concern more severe in humid environments.

Although the detailed switching mechanism of RRAM is still controversial, it is generally believed that non-filament HfO_2/TaO_x-based RRAM switching is accomplished by the

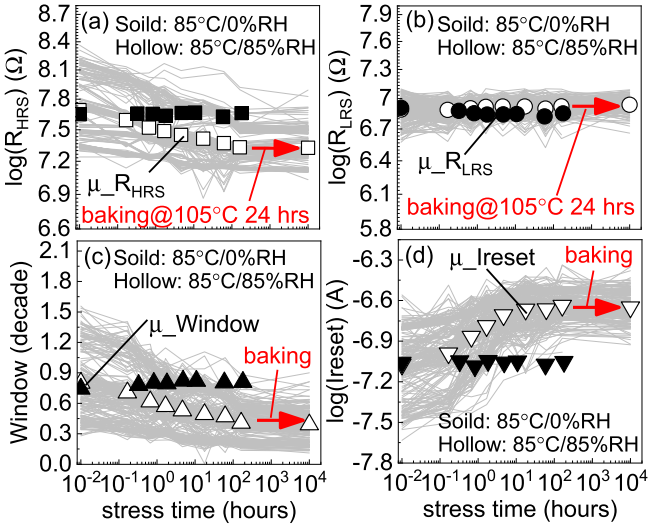

Fig. 3. Aging kinetics of (a) R_{HRS}, (b) R_{LRS}, (c) Window and (d) Ireset on multiple VRRAM devices under 85°C/85%RH moisture stress. Each grey line represents a single device and the hollow symbols in each panel stand for the mean value of the corresponding grey lines. The solid symbols in each panel gives the averaged values (individual result not shown) of each parameter subject to 85°C/0%RH stress as control experiments to exclude the impact from temperature. 24 hours baking is also implemented to further investigate the recoverability of moisture-induced degradation.

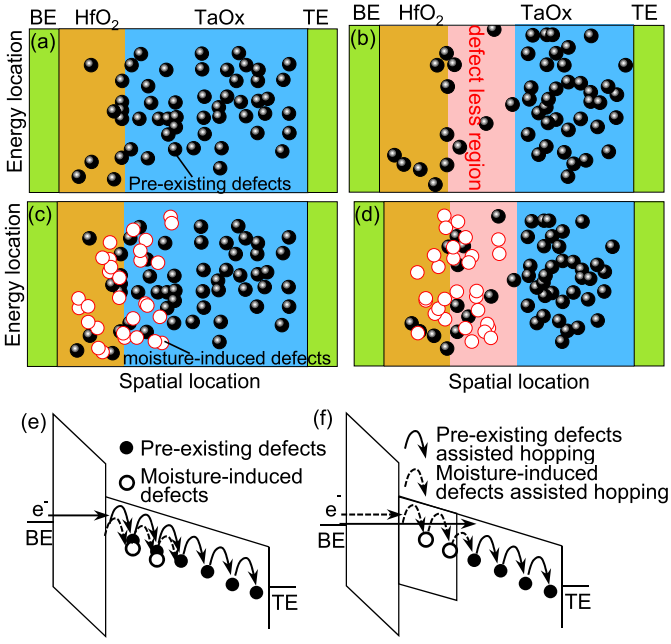

Fig. 4. Illustration of the Defects' energy and spatial location [11]. (a) LRS before stress, (b) HRS before stress, (c) LRS after stress, (d) HRS after stress, (e) Energy band of LRS, (f) Energy band of HRS.

modulation of the barrier at HfO_2/TaO_x interface [8], [11]. Gong *et al.* [11] reported that the barrier originates from the lack of defects. During the VRRAM set/reset operation, defects are gathered/expelled by the electric field at HfO_2/TaO_x interface, resulting in a periodically annihilated/formed "defect less region (DLR) [11]", eventually leading to the LRS/HRS.

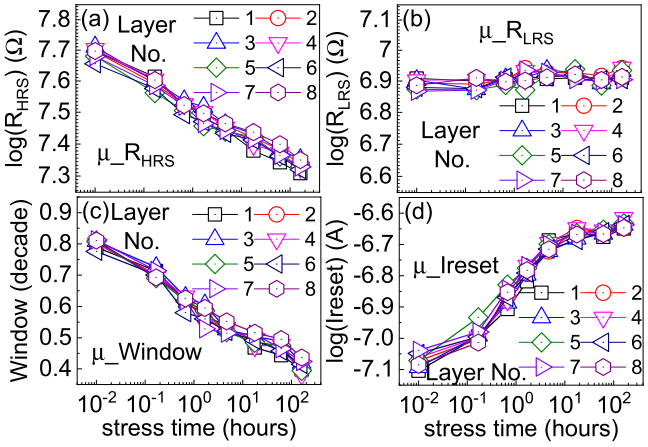

Fig. 5. Moisture stress degradation manifests little layer dependence in terms of (a) R_{HRS}, (b) R_{LRS}, (c) Window and (d) Ireset.

Lübben *et al.* [7] reported that moisture is able to provide additional charged species and enabling the formation of oxygen vacancies in HfO_2/TaO_x materials. Under LRS state, these additional moisture-related defects could enhance electron hopping by providing extra hopping routine in the vicinity of HfO_2/TaO_x interface, but in the majority of bulk TaO_x which is away from interface, the hopping routines are unaltered (Fig. 4d&e), thus current hardly increases, resulting in a constant R_{LRS} during moisture stress. However, under HRS state, current is dominate by the barrier caused by the DLR, which can be seriously affected by the moisture-induced extra defects, resulting in extra hopping routines (Fig. 4d&f) thus giving rise to a lower R_{HRS} and higher Ireset.

Layer-dependence of the moisture stress kinetics was also investigated. μ_R_{HRS}, μ_R_{LRS}, μ_Window and μ_Ireset at each layer were extracted and compared, as shown in Fig. 5. The well agreement of data from different layer devices indicates the layer dependence of moisture stress is trivial.

IV. Conclusion

We report the effect of moisture stress on the resistance of HfO_2/TaO_x-based 8-Layer 3D vertical RRAM in this brief. The results show μ_R_{HRS} and μ_Window manifest significant decrease while μ_R_{LRS} hardly alters. μ_Ireset exhibits an increase as stress time evolves. Barrier drop at HfO_2/TaO_x caused by the incorporation of moisture-induced defects is speculated to be the source of observed degradation. Little layer-dependence of aging kinetics is observed, indicating the moisture can penetrate through all 8 layers within relatively short time (<0.17 hours). In terms of fabrication process, thicker SiO_2 passivation layers are usually adopted to isolate the active region from ambient environments thus can potentially improve the VRRAM reliability against moisture.

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