An Access-Transistor-Free (0T/1R) Non-Volatile Resistance Random Access Memory (RRAM) Using a Novel Threshold Switching, Self-Rectifying Chalcogenide Device

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Abstract

A new concept for non-volatile memory is demonstrated. This new technique controls the threshold voltage of the chalcogenide storage device by varying the height and duration of the write pulse. Consequently, the chalcogenide device serves as both the access element and the memory element. Therefore, it does not need any access transistor in the memory array. The new memory achieves the requirement of non-volatility, fast writing/reading, random access, high scalability, compact cell size, and low cost.

Introduction

An ideal memory should possess high read/write speed, high density, low power, low cost, and nonvolatile characteristics. Conventional chalcogenide memory, (CRAM, *Chalcogenide RAM* or OUM, *Ovonic Unified Memory*) uses the resistance difference between the amorphous phase and the crystalline phase of a chalcogenide layer, and has received much attention (1,2). However, large current (0.2-1.0 mA), which cannot be supplied by a nominal size NMOSFET in the cell, is required to induce the phase change. Thus the cell size is large due to the need to accommodate a large active device (1,3). In this paper we introduce a new device and a new non-volatile memory cell using the unique threshold switching and memory characteristics of Ovonic (chalcogenide) materials. Fundamentally different from the phase change between crystalline phase and amorphous phase of the previous CRAM devices, the chalcogenide material in the device always contains amorphous phase. Therefore, it always provides self-rectification and thus requires no access transistor. In the following sections we will detail the characteristics of this 0T/1R, $4F^2$ new memory. For convenience we name this device TF-RRAM (Transistor Free Resistance Random Access Memory).

Device Structure and Cell Operation

Fig. 1 shows the structure of the TF-RRAM device. A TF-RRAM device needs only a top electrode, a chalcogenide layer, and a bottom electrode. In this study, the device is established by using typical 180nm CMOS processes. A single device consists of a TiW top electrode, a $Ge_2Sb_2Te_5$ chalcogenide layer, and a W bottom electrode. The I-V curves of the TF-RRAM device are shown in Fig. 2. The device always contains amorphous state, but can be programmed into two states with different threshold voltages

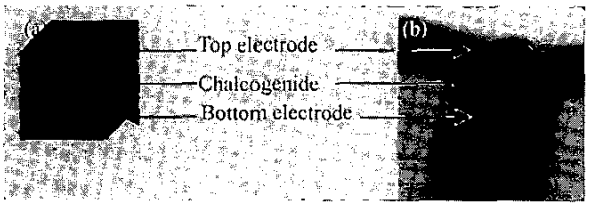

Fig. 1 The structure of a TF-RRAM device. (a) A cell contains top electrode, chalcogenide layer, and bottom electrode. (b) A cross-sectional TEM picture of the device studied in this work. The top electrode, chalcogenide, and bottom electrode are TiW, $Ge_2Sb_2Te_5$, and W, respectively

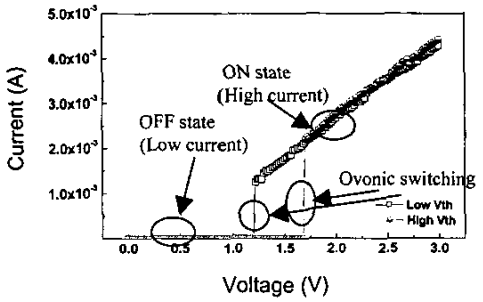

Fig. 2 The I-V curve of a TF-RRAM device. Ovonic switching, "OFF" state, and "ON" state of the device are shown. The open squares represent the I-V curve of a device with Vth=1.2 V and the circles show the I-V curve of a device with Vth=1.7 V.

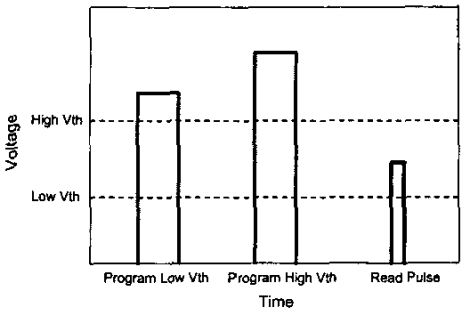

Fig. 3 The pulses for programming low Vth, high Vth, and for reading. Both programming pulses have higher voltages than the high Vth. The read pulse voltage is between the two Vths and the read pulse width is short.

(Vth). In each state the device shows a normal Ovonic switching behavior. Below Vth (OFF state), the current is low, but once the biasing voltage is greater than Vth (ON state), the current increases dramatically and the ON/OFF ratio is high. The threshold voltage can be accurately tuned by electrical pulses, as shown in Fig. 3. A pulse causes a

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reversible change of the Vth state. The higher the pulse, the higher the resulting Vth. Note that this Vth change is fundamentally different from the phase-change modes used in CRAM (OUM). The TF-RRAM device always contains the amorphous state and never exhibits the Ohmic behavior of the crystalline state. The detailed mechanism is not understood yet, but we suspect it is either a change in the microstructure (nanostructure in this case) of the amorphous phase, or an electronic change (4). To read, a narrow pulse with height between Vth-high and Vth-low is applied. Since the read pulse is narrow, it is not sufficient to change the state, but can detect the resistance difference between the two Vth states of the device. Furthermore, the TF-RRAM device also serves as a rectifying element because the sub-threshold current is low and the ON/OFF current ratio is high. A schematic architecture of the TF-RRAM memory array is shown in Fig. 4. Each word line (W/L) and bit line (B/L) is connected with a select transistor. However, in the array, only TF-RRAM devices are used without the need of any access transistor, thus achieving a $4F^2$ cell.

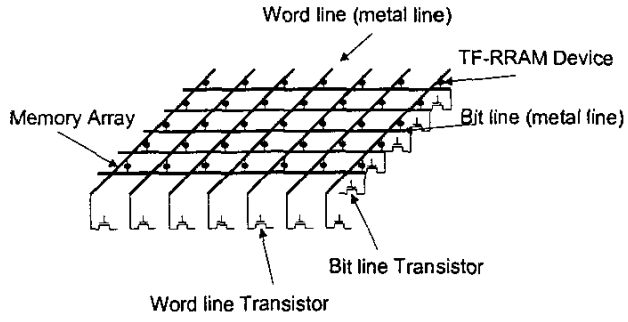

Fig. 4 A schematic of the architecture of TF-RRAM memory array. The word lines and the bit lines are selected by word line transistors and bit line transistors, respectively. The TF-RRAM device serves both as the memory element and as the access element.

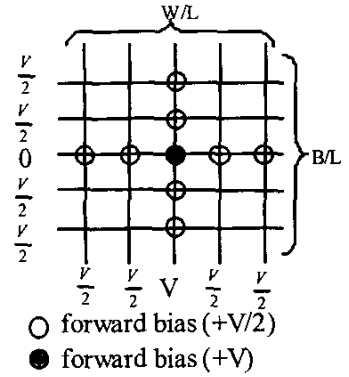

Fig. 5 Schematic plot of applied voltage and bias on the TF-RRAM cells of the 1/2 method. On the selected word line, full voltage (V) is applied. Half voltage (V/2) is applied on the other word lines. 0 voltage is applied on the selected bit line and half voltage is applied on the other bit lines. The solid circle cell is under forward bias of V, the hollow circle cells are under forward bias of V/2, and other cells are not under bias.

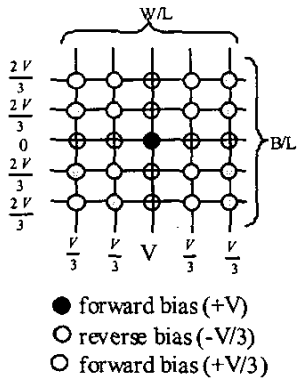

Fig. 6 Schematic plot of applied voltage and bias on the TF-RRAM cells of the 1/3 method. On the selected word line, full voltage (V) is applied. One-third voltage (V/3) is applied on the other word lines. 0 voltage is applied on the selected bit line and two-third voltage (2V/3) is applied on the other bit lines. The solid cell is under forward bias of V, the hollow cells are under forward bias of V/3, and other (shaded) cells are under bias of -V/3.

0T/1R Self-Rectifying Array Analysis

To increase the sensing margin of the memory device in the array, biasing voltages may be applied on word lines and bit lines. Figs. 5 and 6 show the applied biasing voltages on the cells of two selection methods, 1/2-method and 1/3-method. The currents on the selected and unselected B/L and W/L for these methods are listed in Table 1. Current analysis results for a 4 Kb block (64x64) are in Table 2. The single device data is extracted from a 0.4μm TF-RRAM device. The Vth-high, Vth-low, and V-read are 1.3V, 1.0V, and 1.15V, respectively. The array current during programming is a function of array architecture. Comparing the two methods above, the program current for 1/3-method is lower, and the read margin for 1/3-method is higher. Lower read current for 1/2-method is due to fewer leakage paths. The programming current using the 1/3-method is acceptable and the sensing margin is high. Generally, the 1/3-method is superior, but for special low-read-current applications, 1/2-method may be used for reading. Larger memory size can be manufactured by fracturing the arrays into 4 Kb to 16 Kb blocks without adding access transistors to the blocks.

TABLE 1

Analysis of the TF-RRAM array current stressed by the 1/2 method and the 1/3 method. Assuming there are m word lines and n bit lines. I(V), I(V/2), I(V/3), and I(-V/3) are the single cell current under bias of V, V/2, V/3, and -V/3, respectively.

Item	1/2 method	1/3 method
Selected W/L	I(V)+(n-1) I(v/2)	I(V)+(n-1) I(v/3)
Selected B/L	-[I(V)+(m-1) I(v/2)]	-[I(V)+(m-1) I(v/3)]
Unselected W/L	I(V/2)	-[(n-2) I(-V/3)]
Unselected B/L	-I(V/2)	(m-2) I(-V/3)
Total current	I(V)+ (m+n-2)I(v/2)	I(V)+(m-1)(n-1) I(V/3)

TABLE 2

Current requirements for a 4 Kb TF-RRAM array. The current is extracted from a 0.4 μm TF-RRAM device. Comparing the two methods, the program current for 1/3-method is lower, and the read margin for 1/3- method is higher. The read current for 1/2-method is lower due to fewer leakage paths.

Item	1/2 Method	1/3 Method
Max. total program current	129 mA	16 mA
Max.total read current	1.23 mA	2.63 mA
Max read current on selected B/L of a low Vth cell	1.14 mA	1.08 mA
Max read current on selected B/L of a high Vth cell	94.2 μA	28.1 μA
Read margin	12 times	38 times

Cell Characteristics

Fig. 7 shows the programming window for TF-RRAM. The shaded area indicates the region exhibiting Ovonic switching and clear threshold voltage. As illustrated in the figure, the cell can be programmed at <10ns. Fig. 8 shows Vth as a function of programming voltage. Low programming voltage (<4V) is sufficient and the Vth increases with the programming voltage. Fig. 9 shows the Vth as a function of programming cycles. Program/erase cycling result indicates that the device can be programmed to high or low Vth states more than 1000 times. Fig. 10 shows that reading of the TF-RRAM device is non-destructive. Vth is stable after 10^{10} times of reading at 8 ns. Fig. 11 shows room temperature data retention and the result indicates that the memory is non-volatile, with characteristics similar to that for the conventional CRAM.

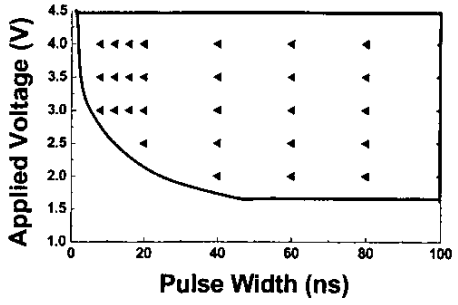

Fig. 7 The programming window of TF-RRAM devices. Shaded area is where the device functions.

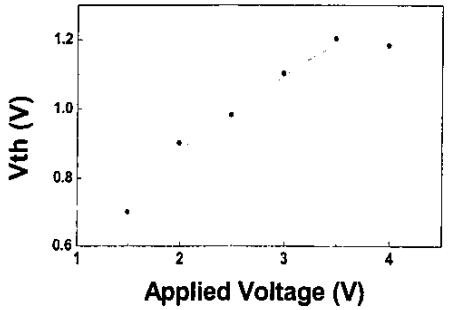

Fig. 8 Vth as a function of applied voltage, showing that the Vth is highly dependent on the applied voltage. The diameter of the W plug is 0.3 μm.

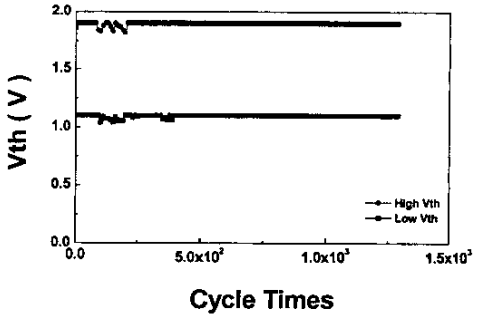

Fig. 9 Vth as a function of program/erase cycles. The initial high Vth and low Vth are 1.9 V and 1.1 V, respectively.

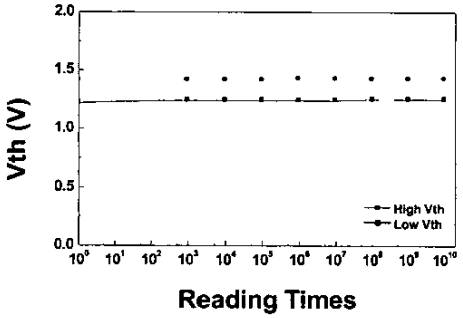

Fig. 10 Vth as a function of read cycles. After 10^{10} times of reading @ 1.3V/8 ns.

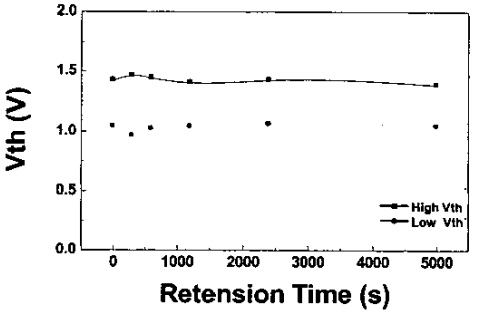

Fig. 11 Data retention test at room temperature.

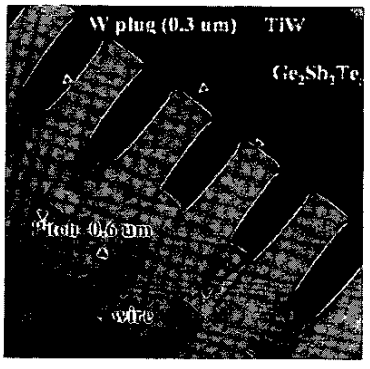

Fig. 12 Bright field TEM picture of the mini array. The diameter of W plugs is 0.3 μm and the pitch of the mini-array is 0.6 μm.

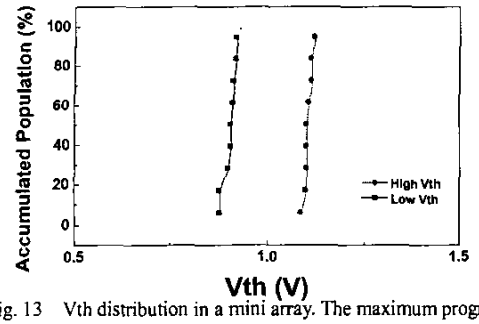

Fig. 13 Vth distribution in a mini array. The maximum program pulse width is 100 ns.

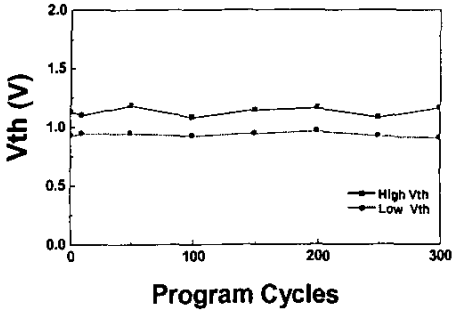

Fig. 14 Vth as a function of disturb program/erase cycles in neighboring cells. The distance between two cells is 0.3 μm.

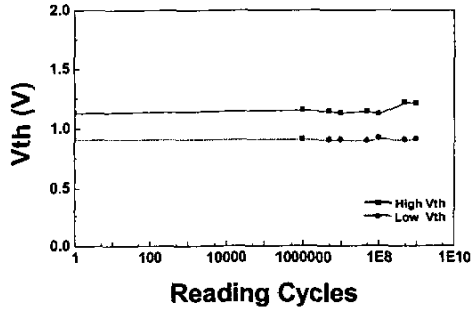

Fig. 15 Vth as a function of read cyling in the neighboring cells. The reading voltage is the average of the high Vth and low Vth. The reading pulse width is 8 ns. The distance between two cells is 0.3 μm.

Array Characteristics

A 33x13 mini-array of TF-RRAM devices is fabricated and tested; a cross-sectional TEM is shown in Fig. 12. The Vth distribution is shown in Fig. 13. The Vth-high and Vth-low are well separated. Vth as a function of programming cycle on the neighboring cell is shown in Fig. 14; the TF-RRAM device is not disturbed by programming of neighboring cells. Even the distance between two TF-RRAM devices is only 0.3 μm. Fig. 15 shows that the cell is also immune to read disturb; after 10^9 readings on the neighboring cells, the Vth-high and Vth-low remain well separated.

Comparison with Other Memory Devices

Table 3 shows a comparison of TF-RRAM memory with other memories. The TF-RRAM memory combines the characteristics of high read/write speed, low operation voltage, low cost, low power, high density, and non-volatility. Although this device is still in the research stage, however, it seems that it may become the ideal memory.

Conclusion

A novel memory device derived from the chalcogenide device is proposed and studied in this work. The device combines the functions of both memory and addressing. In the memory array, only chalcogenide devices are needed. From array analysis, a 4 Kb array can be programmed and read by the state of art of CMOS technology with reasonable current. Single device and mini array characteristics are tested from many aspects and the experimental results reveal that the device is very fast in read/write, low operation voltage, high reading endurance, and non-volatile.

References

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TABLE 3
Comparison of DRAM, SRAM, NOR FLASH, OUM (CRAM), and TF-RRAM memory.

	DRAM	SRAM (6T)	FLASH (NOR)	OUM (CRAM)	TF-RRAM
Transistors	1T	6T	1T	1T	0T
Cell size (F^2)	6-12	50-80	7-11	5-8	4
Volatile/Nonvolatile	Volatile	Volatile	Nonvolatile	Nonvolatile	Nonvolatile
Write/Erase/Read time	50ns/50ns/50ns	8ns/8ns/8ns	1μs/1-100ms(block)/ 60ns	10ns/50ns/20ns	<10ns/<10ns/<10ns
Programming energy	Medium	Medium	High	Low	Low
Direct Over-write	Yes	Yes	No	Yes	Yes
Bit/Byte Write/Erase	Yes	Yes	Block	Yes	Yes
Read	Destructive	Partial-destructive	Non-destructive	Non-destructive	Non-destructive
Read Margin	100-200mV	100-200mV	Delta Current	10x-100x R	>10x Current
Operation voltage	Low	Low	High	Low	Low
New material	Yes	No	No	Yes	Yes
Scalability limits	Capacitor	6T	Tunnel Oxide/HV	Transistor current drive	Not seen yet
CMOS logic Compatibility	Bad	Good	Medium	Good	Good
Cost per bit	Low	High	Medium	Low	Very low