

# An Artificial Neuron Based on a Threshold Switching Memristor

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**Abstract**—Artificial neurons and synapses are critical units for processing intricate information in neuromorphic systems. Memristors are frequently engineered as artificial synapses due to their simple structures, gradually changing conductance and high-density integration. However, few studies have designed memristors as artificial neurons. In this letter, we demonstrate an integration-and-fire artificial neuron based on a Ag/SiO<sub>2</sub>/Au threshold switching memristor. This neuron displays four critical features for action-potential-based computing: the all-or-nothing spiking of an action potential, threshold-driven spiking, a refractory period, and a strength-modulated frequency response. As a post-synaptic neuron, the designed neuron was demonstrated to be applicable to digit recognition. These results demonstrate that the developed artificial neuron can realize the basic functions of spiking neurons and has great potential for neuromorphic computing.

**Index Terms**—Integration-and-fire (IF), memristor, threshold switching, artificial neuron.

## I. INTRODUCTION

NEUROMORPHIC computing based on spiking neural networks has attracted significant interest due to its low energy consumption and high similarity to biological neural systems. To effectively implement artificial neural net-

works directly in hardware, two key elements must be developed: artificial electronic synapses and neurons. In particular, memristors present promising characteristics for developing artificial synapses to realize brain-inspired computing [1]–[3]. Recently, many bio-synaptic functions have been successfully emulated by various memristors, such as pair-pulse facilitation/depression (PPF/PPD) [4], long-term potentiation/depression (LTP/LTD) [5] and spike-time-dependent plasticity (STDP) [6]. However, most reported artificial neurons are primarily based on CMOS circuits, which require many active components to achieve neuron functions [7]–[9]. These artificial neurons have much lower power efficiency and integration density than memristor-based artificial synapses. Fortunately, several novel artificial neurons with simple devices based on, for example, Nb<sub>2</sub>O<sub>5</sub> [10], VO<sub>2</sub> [11], ferromagnetism [12] and phase change materials [13], have been reported recently. In these innovative neurons, the critical functions of neurons were tentatively demonstrated, opening up a new path to the design of artificial neurons. To develop advanced neuromorphic computing systems, further studies on artificial neurons made from emerging devices are needed.

In this letter, we report a new integration-and-fire (IF) artificial neuron based on a Ag/SiO<sub>2</sub>/Au threshold switching memristor (TSM). To implement the TSM neuron, the TSM device was first connected to a resistor, and then both components were paralleled by a capacitor. By utilizing the circuit structure, we achieved four critical neuron functions: the all-or-nothing spiking of an action potential, threshold-driven spiking, a refractory period and a strength-modulated frequency response. To understand these characteristics, we carefully considered the switching mechanism of the TSM device and the corresponding operating principles of the neuron circuit. Furthermore, through system simulations, we verified the feasibility of using the artificial neuron in a neural network for digit recognition.

## II. EXPERIMENTS

The fabrication processes of the Ag/SiO<sub>2</sub>/Au device are as follows. First, vertical lines of Au/Ti (40/10 nm) as bottom electrodes were deposited on the SiO<sub>2</sub>/Si substrate by e-beam evaporation after the first lithography process and released by the first lift-off process. Then, after the second lithography process, 30 nm SiO<sub>2</sub> was deposited by magnetron sputtering to form the functional layer followed by the second lift-off process. Finally, after the last lithography step, horizontal lines of Ag (40 nm) as top electrodes were deposited

Manuscript received November 20, 2017; revised December 5, 2017 and December 7, 2017; accepted December 8, 2017. Date of publication December 12, 2017; date of current version January 25, 2018. This work was supported in part by the National Natural Science Foundation of China under Grant 61521064, Grant 61732020, Grant 61422407, Grant 61474136, Grant 61334007, Grant 61574166, Grant 61404164, and Grant 61522408, in part by the National High Technology Research Development Program under Grant 2017YFB0405603 and Grant 2016YFA0201803, in part by the Beijing Training Project for the Leading Talents in S&T under Grant ljrc201508, and in part by the Opening Project of the Key Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences under Grant Y7YS063005 and Grant Y7YS033003. The review of this letter was arranged by Editor B. Govoreanu. (Xumeng Zhang and Wei Wang contributed equally to this work.) (Corresponding author: Qi Liu.)

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Digital Object Identifier 10.1109/LED.2017.2782752

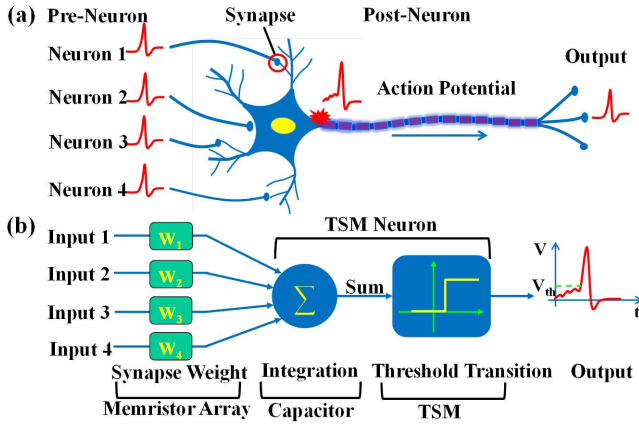


Fig. 1. (a) A biological neuron receives inputs from other neurons by interconnected synapses. (b) A representative TSM neuron for accumulating inputs generated by different pre-neurons.

on the  $\text{SiO}_2$  film by magnetron sputtering, and then the  $\text{Ag/SiO}_2/\text{Au}$  devices were released by the third lift-off process. The area of the devices is  $5 \mu\text{m} \times 5 \mu\text{m}$ . In the electrical measurement, a Tektronix AFG3102 pulse generator acted as the input source, and a Tektronix DPO3032 oscilloscope was used to measure the input/output voltages. The electrical characteristics of a single TSM device were tested by an Agilent B1500A.

### III. RESULTS AND DISCUSSION

The IF artificial neuron aims to replicate a crucial neuron function related to the accumulation of electric charge through the cellular membrane [14]. Fig. 1(a) shows a schematic illustration of a simple connected biological neuron network. A biological neuron receives input spikes from other neurons through connected synapses and triggers an output action potential when the membrane potential reaches a threshold value. Correspondingly, the equivalent of the TSM neuron network is shown in Fig. 1(b). The memristor crossbar cells act as artificial synapses to connect the pre- and post-neurons. The TSM neuron acts as a post-neuron to integrate the signals from inputs 1, 2, 3, and 4 via a capacitor. When the accumulated capacitor potential (membrane potential) approaches a certain value, the neuron fires and outputs a spiking pulse. Subsequently, the post-neuron is prevented from spiking again for a certain duration of time known as the refractory period [15]. After the refractory period, the neuron accumulates the inputs again and prepares the next spiking.

The circuit schematic of the TSM neuron with a connected synaptic resistor is shown in Fig. 2(a). The TSM device is in series with a resistor ( $R_o = 51 \text{ k}\Omega$ ), and the two components are in parallel with a capacitor ( $C = 100 \text{ nF}$ ). Finally, the neuron connects with a synapse resistor ( $R_s = 510 \text{ k}\Omega$ ). The input signal is a voltage pulse source applied to the left node (input). In addition, the change in the voltage on  $R_o$  is regarded as the output spike. During operation, the circuit can be divided into the charging loop (CL: 1-2-3-1) and the discharging loop (DL: 2-4-3-2), which are marked by red arrows in Fig. 2(a). Fig. 2(b) shows the I-V and R-V curves of the TSM device under a certain compliance current ( $100 \mu\text{A}$ ). If the applied voltage is above a threshold value ( $V_{th2}$ ), the device switches from the high resistance state (HRS)

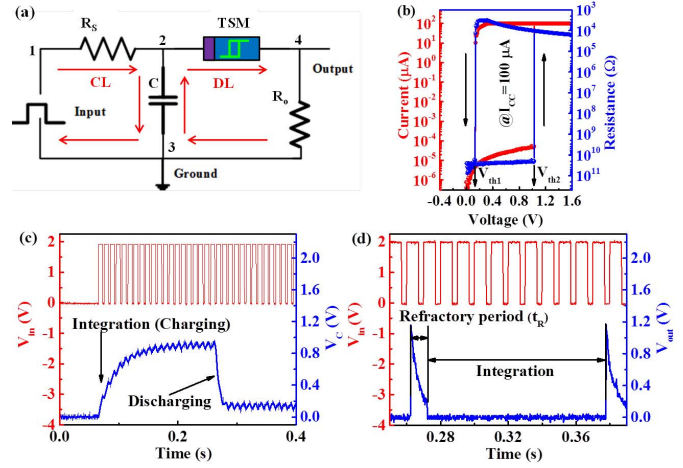


Fig. 2. (a) Schematic illustration of the proposed neuron circuit. (b) The I-V characteristics of the TSM device and the corresponding switching of the resistance. (c) The voltage variation across the capacitor. The voltage increases when the TSM is in the HRS and decreases when in the LRS. (d) The output neuron spike with the corresponding refractory period and integration moment.

to the low resistance state (LRS) by forming Ag filaments. When the applied voltage is lower than a certain value ( $V_{th1}$ ), the device reverts to the HRS due to the regrouping of Ag atoms [16]. When a series of voltage pulses (100 Hz frequency, 7 ms width) with 2 V amplitudes are fed into the left node, the capacitor will accumulate the charges and lift up the voltage potential of node “2”, as shown in Fig. 2(c). During charging, the TSM device remains in the HRS ( $R_H \sim 20 \text{ G}\Omega$ ). Therefore, the RC time constant ( $\tau_C = R_s C$ ) in the CL is much shorter than that ( $\tau_D = (R_H + R_o)C$ ) in the DL, implying that current leakage through the TSM is negligible and that the capacitor is charged (Fig. 2c). When the voltage between nodes “2” and “4” is beyond  $V_{th2}$ , the TSM device will switch from the HRS to the LRS. Once the device is in the LRS ( $R_L \sim 3 \text{ k}\Omega$ ), the RC time constant ( $\tau'_D = (R_L + R_o)C$ ) in the DL is much shorter than the total  $\tau_C$  in the CL. In this case, the capacitor will discharge and the neuron will fire an output voltage spike, as shown in Fig. 2(d). The voltage between nodes “2” and “4” will decrease due to the discharging of the capacitor. When the voltage decreases below  $V_{th1}$ , the TSM device will spontaneously revert to the HRS again to prepare the next fire action. The maximum firing events of the neuron is corresponding to the endurance of TSM device. Fortunately, this kind of devices has satisfied endurance characteristics ( $> 10^8$  switching cycles) [17], [18], which means that the maximum firing events can be more than  $10^8$  times.

Notably, the net charge integration in the capacitor is virtually zero during the neuron spiking time [11], because any input voltage pulse is directly drained by the DL when the device is turned on. This characteristic can emulate the refractory period of biological neurons [15]. Only when the refractory period is complete, can the TSM device revert to the HRS, and the capacitor recharges during the integration stage. The refractory period and integration stage of the neuron are shown in Fig. 2(d). The results show that the TSM neuron can successfully emulate the IF function with a refractory period, similar to biological neurons.

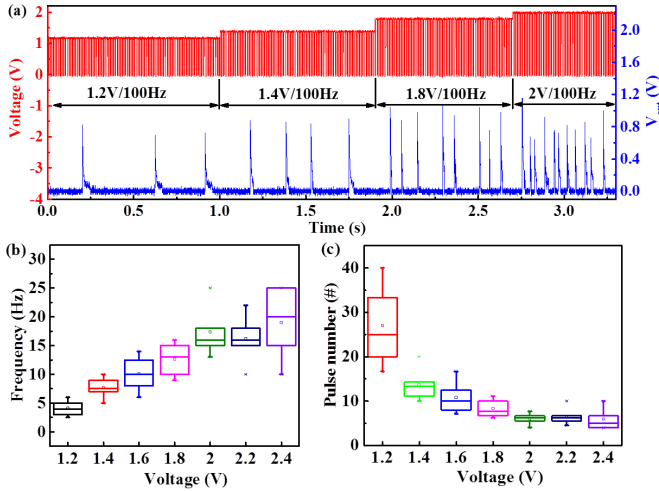


Fig. 3. (a) The TSM neuron spikes under different input intensities. (b) Statistical voltage/spike-frequency relationship of the neuron. (c) The statistical pulse number/amplitude relationship of the neuron.

In biological neurons, the spike frequency increases with increased stimulus strength [15]. To emulate this strength-modulated spike frequency characteristic, a series of pulses (100 Hz frequency, 7 ms width) with different amplitudes (1.2 V, 1.4 V, 1.8 V and 2 V) were applied to the artificial neuron, as shown in Fig. 3(a). The spike frequency clearly increases with increasing input pulse amplitude. Fig. 3(b) shows the statistical results of the spike frequency with seven different pulses. This characteristic results from the various integration rates of the capacitor under different pulse amplitudes. Under the lower amplitude pulse input, the capacitor needs more pulses to trigger the output spike, whereas at higher amplitudes, less pulses are needed. To more clearly demonstrate the integration process, the pulse number/amplitude relationship of the neuron extracted from Fig. 3(b) is shown in Fig. 3(c). These results show that the TSM neuron can successfully realize the strength-modulated spike frequency characteristics of biological neurons.

To verify the feasibility of the TSM neuron for application in a spiking neuron network, we present a digit recognition system based on a memristor synapse array and the TSM post-neurons. Fig. 4(a) shows the schematic of this system [19], [20]. The input images are  $5 \times 6$  pixels [21]. The black and white squares indicate logic “1” and “0”, which are mapped to an input voltage pulse (1 V, 10 ms) and 0 V, respectively. The off-line training process was implemented on MATLAB, and then the weight values of the synapses were input into the memristor array. When an image of a digit, for example, “6”, was applied to the 30 input nodes, the 10 post-neurons integrate the current, but only neuron “6” fires because the other neurons are inhibited by the winner-take-all rule. The schematic of the lateral inhibition circuit of neuron “1” is shown in Fig. 4(b). Nine n-type MOS transistors serve as on-off switches to connect two terminals of the capacitor, and then gates are connected to the output end of the other neurons separately. When neuron “6” first fires, the output spike is applied to the connected gates of the other nine neurons, and the corresponding transistors are turned on. Once the transistor is open, the capacitor connected to it will be

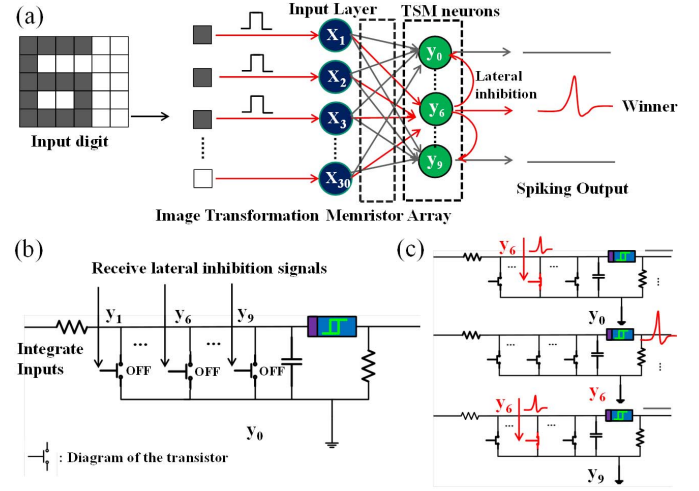


Fig. 4. (a) Schematic illustration of the input digits and the two layer spiking neuron network with lateral inhibition. (b) The lateral inhibition circuit of neuron “1” with 9 inhibitory inputs. (c) States of the transistors and neurons when neuron “6” fires.

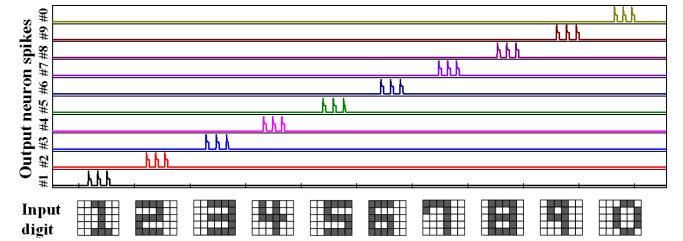


Fig. 5. The output results of 10 TSM neurons when the corresponding digits are input.

short-circuited and will discharge, and an output spike will not be produced, as shown in Fig. 4(c). The open transistor is labeled in red, whereas the closed one is labeled in black. It is worth to note that the lateral inhibition circuit is only a simple example, further optimization should be studied to promote the large scale application of the TSM neuron in the output layer. When images of digits are applied to the input nodes, the simulation results confirm that only the target neuron fires whereas the others remain at zero, as shown in Fig. 5. These results demonstrate that our TSM neuron can be successfully used for system-level applications and has great potential for neuromorphic computing.

#### IV. CONCLUSION

In conclusion, a TSM neuron was shown to emulate biological neuron functions. The TSM neuron successfully achieved four key behaviors of bio-neurons: the all-or-nothing spiking of an action potential, threshold-driven spiking, a refractory period, and a strength-modulated frequency response. Furthermore, a digit recognition system composed of TSM neurons was successfully simulated. These results show that the TSM neuron has a great potential to be used in brain-inspired computing systems. To broaden the application of the TSM neuron for multilayer neural network, the performance of the neuron unit and peripheral circuits (i.e. fan-out circuit, lateral inhibition circuit and so on) are needed to be further optimized in the follow-up study. We believe that after the subsequent optimization operation, a high efficient neuromorphic system based on the TSM neuron will be constructed.



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