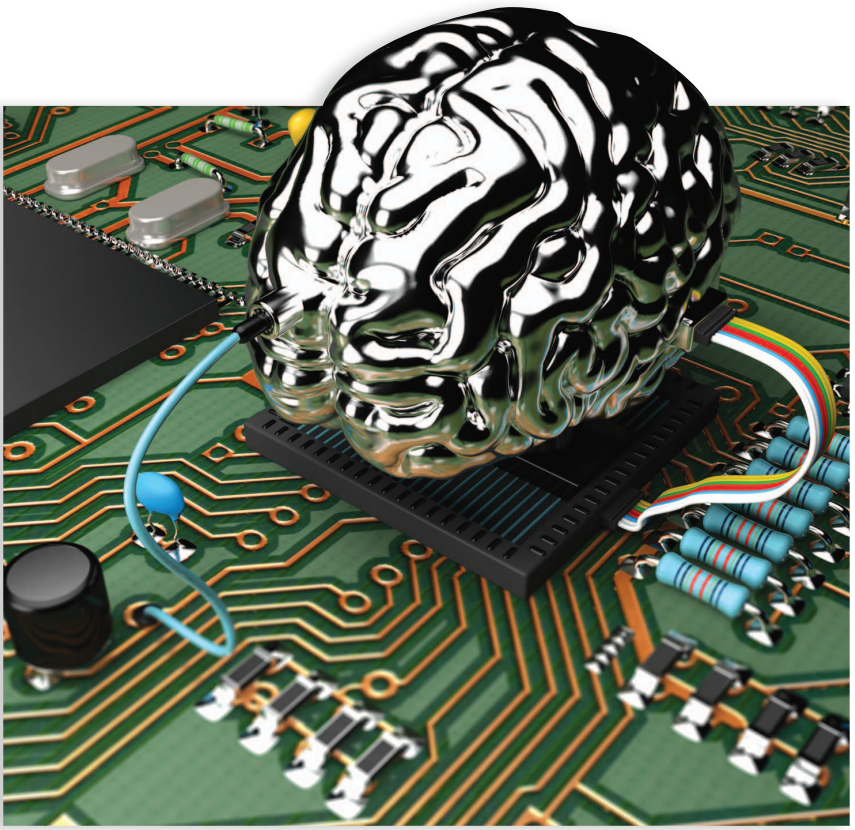
# Resistive Memory-Based Analog Synapses

## The pursuit for linear and symmetric weight update.

THIS ARTICLE REVIEWS THE recent developments in a type of random access memory (RAM) called *resistive RAM* (*RRAM*) for the analog synapse, which is an important building block for neuromorphic computing systems. To achieve high learning accuracy in an artificial neural network based on the back-propagation learning rule, a linear and symmetric weight update behavior of the analog synapse is critical. The physical mechanisms in the RRAM (interfacing switching versus filamentary switching) are discussed, and the pros and cons of each mechanism to emulate the analog synaptic weights are compared. Then, various strategies from a materials and device engineering perspective are surveyed to achieve linearly and symmetric conductance changes under identical pulses. Finally, future research directions are outlined.

### A NANOELECTRONIC SYNAPSE FOR AN ARTIFICIAL NEURAL NETWORK

Artificial intelligence that is sufficiently powerful will allow machines to think and act like human beings. In recent years, deep learning with deep neural networks have unprecedently improved the accuracy in large-scale image/speech recognition and classification tasks, with some results even surpassing human-level accuracy [1]. State-of-the-art deep-learning models with millions of parameters, if directly implemented on-chip, pose significant challenges in terms of computation, memory, and communication. This is especially true for embedded and mobile applications, such as autonomous driving, machine translation, and smart wearable devices, where severe constraints exist in performance, power, and area. Several application-specific integrated circuit (ASIC) solutions in silicon complementary metal–oxide–semiconductor



©ISTOCKPHOTO.COM/ZINCO79

JIYONG WOO AND SHIMENG YU

*Digital Object Identifier 10.1109/MNANO.2018.2844902*
*Date of publication: 16 July 2018*



1932-4510/18©2018IEEE

(CMOS) technology (e.g., Eyeriss [2] and Envision [3]) have been previously proposed to parallelize the computations on-chip; however, limitations still exist on memory footprint, in-memory computing, on-/off-chip communication, and online learning capabilities. In particular, the silicon CMOS ASIC designs show that memory is the biggest bottleneck for energy-efficient computing in terms of storing millions of parameters and loading/communicating them to the place where computing actually occurs. Although static RAM (SRAM) technology has been following the CMOS scaling trend well, the SRAM density (100–200 $F^2$ per cell, F is the technology node) and the on-chip SRAM capacity (typically a few MB) are insufficient for the extremely large number of parameters in deep-learning algorithms.

In this regard, nanoelectronic devices, such as emerging nonvolatile memories including ferroelectric RAM, phase change RAM, and RRAM have been proposed to replace the conventional SRAM as the compact synaptic element [4]. In particular, the excellent scalability (<10 nm), analog-like multilevel capability, and relatively low power programming (sub-pJ) [5] makes RRAM attractive for building an ultrahigh-density memory array with a small cell size of 4 $F^2$ employing a cross-point array architecture. The neuromorphic system consisting of three-dimensionally stackable cross-point RRAM arrays [6] is thus expected to have as many synapses as needed in the deep neural networks, ultimately eliminating the off-chip memory access.

> The selection of suitable oxide materials facilitates the movement of oxygen ions through the entire area.

In addition, the cross-point RRAM array, where word and bit lines are perpendicular to each other, is beneficial for in-memory computation that accelerates the vector-matrix multiplications in a massively parallel fashion [7]. Unlike the memory applications that select a certain word line and bit line to read a specific RRAM cell, the read voltage, as an input vector, is applied to each word line in parallel. The synaptic weights stored in RRAM in the form of conductance are then multiplied by the read voltages at each cross-point, and a summation of the weights as a read-out current along the bit line is integrated at the end of the bit line by Kirchhoff's law. During the training of the deep neural network, when the actual output differs from the expected value, the weights are incrementally adjusted to minimize the difference at the given input based on the back-propagation algorithm [8]. Therefore, the conductance analog tuning capability is critical to enable the online learning for the nanoelectronic synaptic device.

In a recent system-level analysis [9], [10], it was found that the weight update behavior, i.e., how the conductance of the device is changed with respect to the programming pulses, is strongly related to the learning accuracy of the neural networks. Specifically, the conductance state should be linearly and symmetrically increased (potentiation) and decreased (depression), which means that the degree of change in conductance per pulse must always be constant. Figure 1 shows the ideal characteristics of the synaptic devices (from the system-level simulation [11] for recognizing the Modified National Institute of Standards and Technology data), including the high precision (>6 b) in the weight, or equivalently >64 levels in the conductance, and sufficiently on/off ratio (>10). Preferably, identical pulse trains (e.g., 1 V/10 ns) are applied to

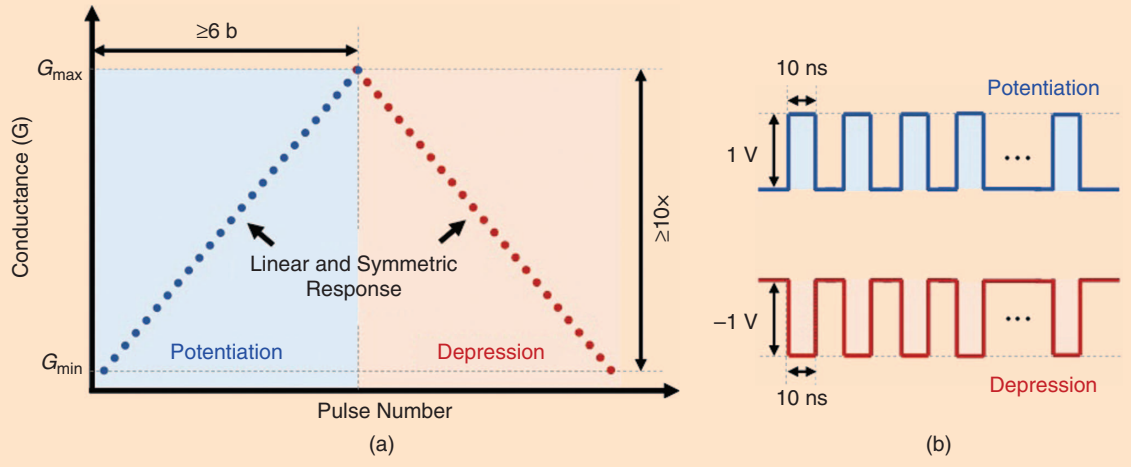



**FIGURE 1** (a) A schematic illustration of ideal characteristics of the synaptic devices. The conductance should be linearly and symmetrically updated by the identical pulse trains for (b) potentiation and depression.

tune the conductance. Therefore, via a thorough literature survey, the aim of this article is to review the strategies from the perspectives of materials and device engineering to achieve and improve the linearity and symmetry of synaptic behaviors in RRAM devices.

## AN ANALOG SYNAPSE WITH AN INTERFACIAL RRAM

These desirable analog synaptic characteristics have mainly been emulated in interfacial RRAM, where the working principle of the resistance switching mechanism is based on the shift of the oxygen ions/vacancies distribution at either the electrode/oxide or oxide/oxide interface, resulting in the formation of a Schottky barrier [12] or tunneling barrier [13]. Particularly, the selection of suitable oxide materials facilitates the movement of oxygen ions through the entire area, allowing the thickness of the barrier to be adjusted, as shown in Figure 2(a).

When a reactive Al electrode material having a low work function was contacted with a $PrCaMnO_3$ (PCMO) serving as an ionic conductor, an insulating $AlO_x$ layer was formed by absorbing oxygen ions from the PCMO based on the chemical reaction [14], which was confirmed by an in situ transmission electron microscopy analysis [15]. The reversibly modulated $AlO_x$ thickness by the field-driven oxygen ions depending on the bias polarity not only enables analogously changed resistance states in the PCMO device during both potentiation and depression, but it also allows for excellent cycle-to-cycle and cell-to-cell uniformities of the multiple states [16].

Figure 2(b) shows the quasi-dc current-voltage (I-V) characteristics of the PCMO devices. However, the PCMO RRAM showed state instability where

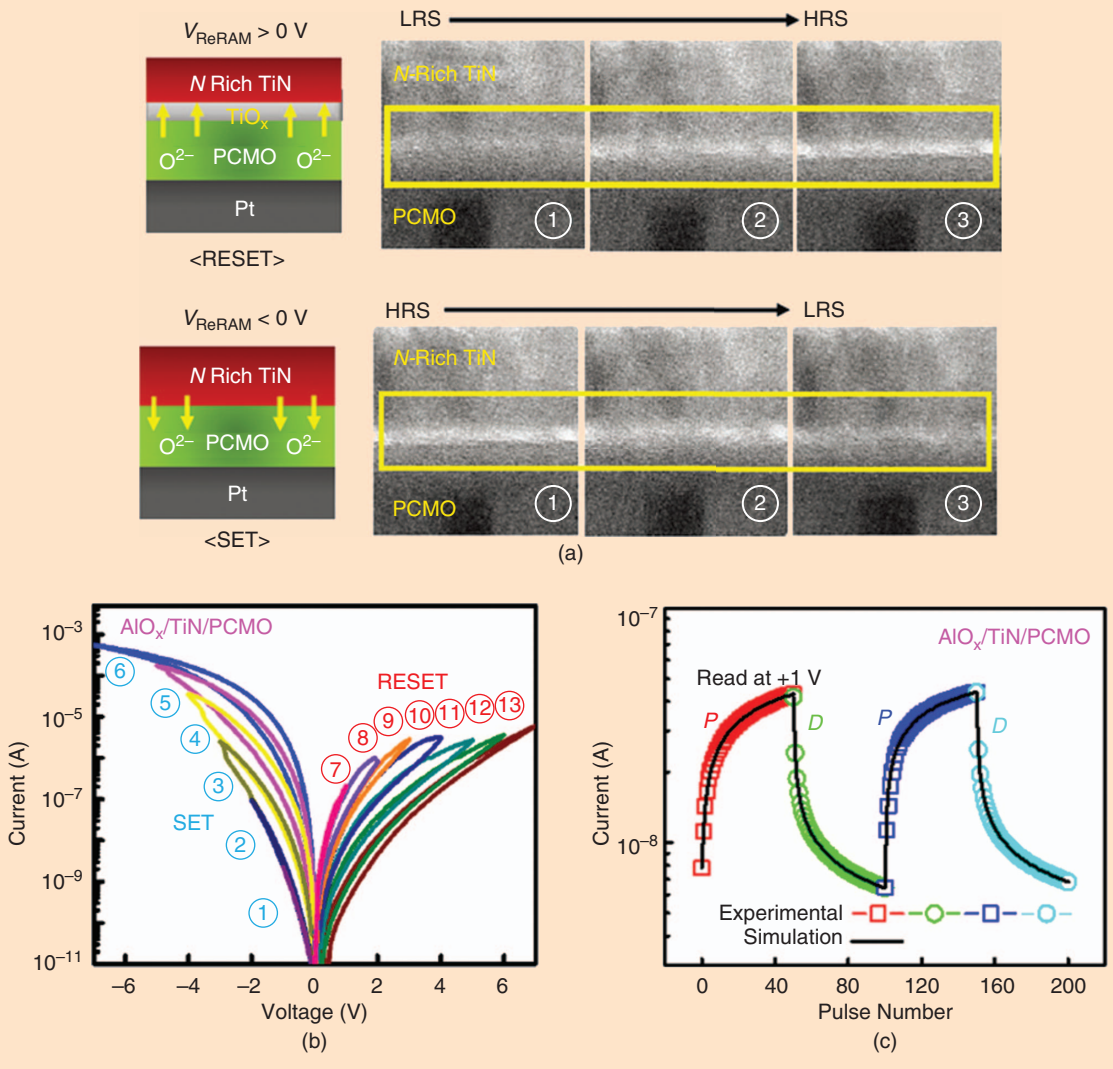



**FIGURE 2** (a) When oxygen ions were driven from the PCMO to the TiN electrode under a positive bias, the interfacial layer based on the oxidation process became thicker (HRS). On the other hand, the thinned layer caused by the reduction process under a negative bias led to the achievement of LRS. Reversely, modulation of the interfacial layer allowed the resistance to be changed analogously in both polarities. (b) Quasi-dc I-V characteristics. (c) The weight update under identical pulses showing nonlinear and asymmetric potentiation and depression. Adapted from [15] and [17].

the multiple states were degraded to a high-resistance state (HRS) over time. It is explained that the oxidation process is thermodynamically favored by the low activation energy from the Al to the $AlO_x$ as a result of the low Gibbs free energy of $AlO_x$ formation [14]. Therefore, the multiple low-resistance states (LRSs) tended to return to the HRS spontaneously, and the LRS was also easily decreased by the single pulse for the depression, leading to unstable retention characteristic and a nonlinear weight update response in the depression.

To mitigate this problem, metal electrodes with moderate reactivity such as TiN [17] and Mo [18] were introduced to balance the activation energies of the oxidation and reduction processes, resulting in slightly improved linearity of the depression. The $WO_x$ [19] and $TaO_x$/$TiO_2$ [20] RRAM systems with a Schottky barrier at the electrode/oxide interface, which plays a similar role as the $AlO_x$, also exhibited the analog synaptic characteristics because the oxygen vacancies acting as dopants driven toward the electrode modified the height and width of the Schottky barrier.

Meanwhile, the movement of these ions may only be involved in adjusting the relative distribution of the insulating state inside the oxide layer [13]. As an example, the $TiO_x$/$TiO_2$ RRAM [21] could be divided into two different resistive regions from a stoichiometric point of view. The oxygen vacancies supplied from the defective $TiO_x$ layer to the $TiO_2$ under bias narrowed the $TiO_2$ region as a tunneling barrier, allowed the smoothly changed resistance, and vice versa. This concentration gradient layer can also be designed by incorporating Ag into the silicon layer during the fabrication process [22]. When two Ag and Si targets were sputtered simultaneously (called the *combinatorial process*), most of the Ag particles were evenly distributed on the top of the silicon matrix, resulting in two Ag-rich (high-conductivity) and Ag-poor (low-conductivity) silicon regions. By adjusting the range of the Ag-poor region, the resistance under bias conditions could thus be progressively and linearly changed.

In the early stages, these material and device systems that utilize the interfacial barriers seemed attractive for achieving analog switching characteristics under an identical pulse. However, the nonlinear response of the barrier change by oxygen ions/vacancies makes it difficult to realize a constant increment (or decrement) ratio during the potentiation (or depression), causing a nonlinear and asymmetric weight update [see the representative weight update behavior in PCMO in Figure 2(c)]. In addition to the synaptic behavioral perspective, driving the oxygen ions/vacancies through the entire area, which is very sensitive to activation energies for the kinetic motions (diffusion and drift) and chemical reactions, usually requires a sufficiently long pulsewidth (PW) of ms-scale to ensure the multiple states and their retention properties. These interfacial RRAM-based synapses can thus be a disadvantage for fast and reliable operation of the neuromorphic systems.

A finely increased compliance current allowed more oxygen vacancies to be migrated to thicken the filament.

## ANALOG SYNAPSE WITH FILAMENTARY RRAM-I: RAMPING PULSE CONDITIONS WITH NONIDENTICAL PULSES

Therefore, there have been attempts to use filamentary RRAM, which was considered to be more suitable for the memory applications than the neuromorphic applications due to the difficulty in achieving the analog behavior. The major working principle of the RRAM has been generally described by the formation and rupture of a filament [5], [12] in the dielectrics. When oxygen vacancies or metal ions such as $Ag^+$ or $Cu^+$ are provided from the oxide or electrode in various ways, these charged species are then driven by a vertical electric field under bias to form the nanoscale conductive filament, which means a set transition from HRS to LRS. On the other hand, the species start away from the filament under the reset bias of an opposite polarity, and a tunneling gap between the filament and electrode is formed, resulting in the HRS.

These two resistance states could be further extended to multiple states by ramping the measurement conditions related with the geometry of the filament in the various oxide, silicon, and chalcogenide material systems such as $HfO_x$ [23]–[27], $TaO_x$ [28], [29], $AlO_x$ [30], $FeO_x$ [31], $TiO_x$ [32], $Al_2O_3$/$TiO_x$ [33], $SiN_x$ [34], Cu/$SiO_2$ [35], Cu/Si [36], and Ag/$GeS_2$ [37]. A finely increased compliance current allowed more oxygen vacancies to be migrated to thicken the filament, and a lower LRS was thus successively obtained. Whereas, as the HRS was controlled by the distance of the gap, a higher HRS was shown by a steadily enlarged gap by increasing the magnitude of the reset voltage.

For practical synaptic operation, when the identical set pulses were sequentially applied to most filamentary RRAM devices, the HRS was abruptly switched to the LRS by the first pulse, and no further change of the LRS was observed in the subsequent pulses, resulting in only a binary state. While the LRS was gradually decreased by the number of the identical reset pulses during the depression, its linearity was also well-tuned by the amplitude or width of the pulse, as shown in Figure 3(a) [26]. This highly abrupt response of the resistance caused by the two states in the potentiation is an obstacle to obtaining reasonable accuracy for pattern recognition [38]. As can be expected, multiple weights are achieved by continuously ramping up the pulse conditions [Figure 3(b)], but the generation of the nonidentical pulses causes an additional burden to design the peripheral circuitries as well as the latency and power consumption. For this reason, a primary concern of the filamentary RRAM is

During the reset process, the dissolution of oxygen vacancies from the filament through the $AlO_x$ layer was constrained.

how to elaborately manage the dynamic growth/dissolution of the filament for the linear potentiation characteristic.

## ANALOG SYNAPSE WITH FILAMENTARY RRAM-II: OPTIMIZED PROGRAMMING SCHEMES WITH IDENTICAL PULSES

The identical pulse scheme required for synaptic operation means that a particular sequence of either a single or a pair of pulses must be applied repeatedly, no matter how the pulse pattern is constructed. Several studies have intentionally introduced a weak reset pulse after the set pulse to $HfO_2$ [26] and $TaO_2/TiO_x$ [39] RRAM devices during potentiation, as shown in Figure 4(a). The small reset pulse partially disconnected the filament formed by the first set pulse, resulting in an intermediate resistance state (IRS) close to the HRS after the first identical pulse pair.

During the set pulse in the next pulse pair, the stronger filament was formed because of the higher electric field between the residual filament and electrode. The same amount of out-diffused oxygen vacancies driven from the thicker filament by the reset in the next pulse pair led to a less dissolved filament, which showed a higher IRS compared with the previous cycle. Thus, the IRS in the range of HRS and LRS continued to be adjusted linearly as a function of the number of pulse pairs.

In addition to adding the reset pulse, another set pulse prior to the typical set pulse was used for the $Ta_2O_5/TaO_x$ RRAM [40], as shown in Figure 4(b). The introduction of the pulse of a long duration was sufficient to induce heat to the device, which promoted the diffusion process of oxygen vacancies. The thermally activated oxygen vacancies expanded the size of the filament, and the saturated current was slightly increased.

Meanwhile, a study was reported that solves a similar saturation problem from a power perspective [41]. As the conductance of the $Mo/TiO_x$ RRAM was decreased, the amount of change was reduced because the effective power (calculated from $P = V^2 \times G$) produced by the identical voltage pulse became smaller. The identical current pulse that can continuously increase the effective power ($P = I^2/G$) instead of the voltage pulse was thus utilized for the depression, while the voltage pulse was used for potentiation. With the help of the hybrid scheme (an identical voltage pulse train for the set and an identical current pulse train for the reset), the linearity in the weight update was improved. This study applied this scheme to the interfacial RRAM, but using identical current pulse or device engineering to control the power would also be helpful to the filamentary RRAM.

## ANALOG SYNAPSE WITH FILAMENTARY RRAM-III: STACK AND STRUCTURAL ENGINEERING

Physical descriptions of the filamentary RRAM have recently shown how filament evolutions are linked with the synaptic characteristics, as shown in Figure 5 [42], [43]. The results revealed that the inherent drawback of the filamentary RRAM is mainly related to strong and single filament formation, making it difficult to further evolve the filament by

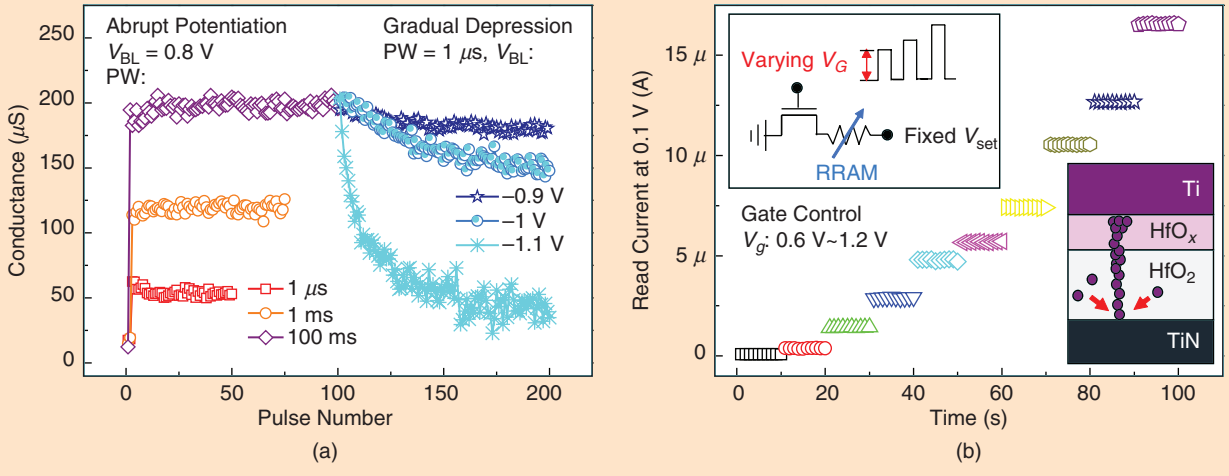



**FIGURE 3** (a) Binary and multiple states were shown in the filamentary $HfO_x$ RRAM by the identical set and reset pulses during potentiation and depression, respectively. (b) The nonidentical pulses that continuously increase the compliance current enabled multiple states in the potentiation. Adapted from [26] and [27].

subsequent pulses. Therefore, as a methodology to prevent the filament evolution in an unwanted direction, additional $AlO_x$ [27] or $TaO_x$ [44] served as a barrier, or a thermal-enhanced layer was introduced to the filamentary $HfO_2$ RRAM devices.

As observed in the $HfO_2$ RRAM, the $HfO_2/AlO_x$ bilayer system also exhibited a sudden current increase in the forming process, which means that the filament was formed throughout the bilayer. On the other hand, during the reset process, the dissolution of oxygen vacancies from the filament through the $AlO_x$ layer was constrained because of slower oxygen vacancy mobility than that of the $HfO_2$ layer [45], resulting in an incompletely disconnected filament without the gap. Therefore, the laterally modulated width of the filament by moving oxygen

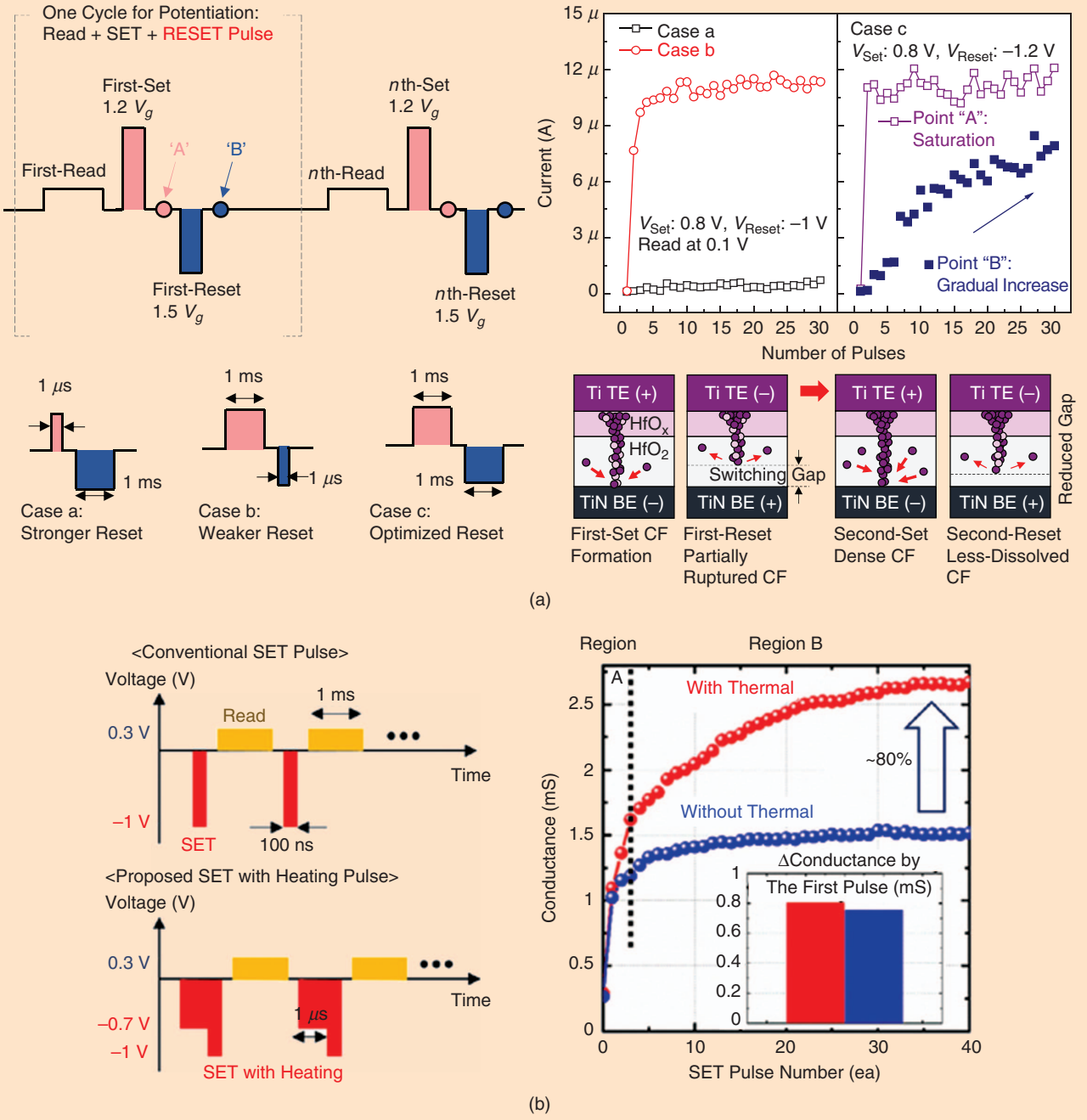



**FIGURE 4** Optimized programming schemes using the identical pulse-pair for potentiation. (a) The reset pulse that is sequentially addressed following the set pulse for $HfO_x$ RRAM. Adapted from [26]. (b) Additional pulse of low amplitude and long duration for heating prior to the typical set pulse for $TaO_x$ RRAM. Adapted from [40].

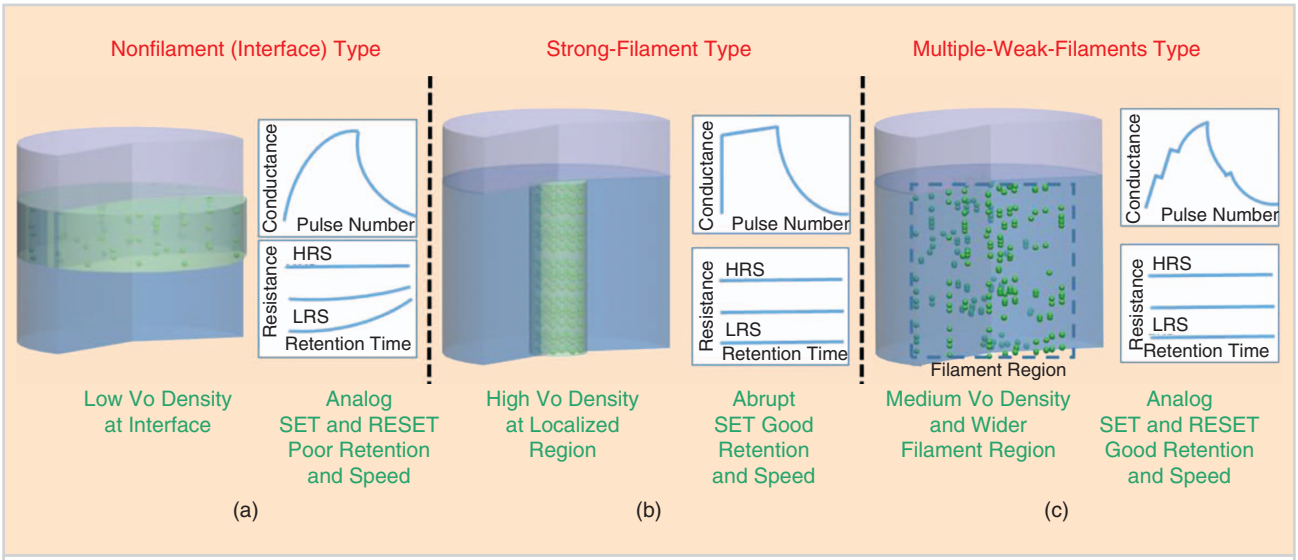



**FIGURE 5** Schematic diagrams of how the distributions of oxygen vacancies strongly relevant to filament properties are linked with synaptic characteristics. (a) Interfacial RRAM showed the analog synaptic behaviors based on the modulation of the interface barrier driven by the motion of oxygen vacancies/ions through the entire area, which adversely was a drawback in terms of retention and operation speed. (b) Single-filament formation led to an abrupt current jump in potentiation, resulting in a binary state. (c) Multiple-weak-filaments that could be formed by widely distributed oxygen vacancies were suitable for achieving stable analog states. Adapted from [43].

vacancies through the $HfO_2$ was preferred instead of the abrupt filament formation during the set process. As a result, a continuous and linear increment in the conductance was repetitively achieved with respect to the identical pulse, as shown in Figure 6(a).

Filament formation is generally related with not only the field effect, but also with the thermal effect [5], [12]. When the $HfO_2$ RRAM was measured at high temperature (150 °C), a noticeable transition from the filamentary-to-analog-switching behaviors was observed, as shown in Figure 6(b) [43], [44]. To realize this thermal effect at room temperature, the oxygen-deficient $TaO_x$ material with a low thermal conductivity was selected and introduced to confine the heat generated during device operation in the $TaO_x/HfO_2$ RRAM, resulting in linearly strengthened potentiation [Figure 6(c)]. This result is explained by noting that the oxygen vacancies generated in the set process are widely spread by the heat. It thus leads to the formation of multiple weak filaments rather than a single filament.

In addition, when elements such as Al [43] and Mn [46] are doped in consideration of the relation with the $HfO_2$ matrix, the formation energy of the oxygen vacancy can be lowered, which implies that oxygen vacancies are easily generated near the dopant sites. Consequently, widely distributed dopants in the $HfAl_yO_x$ RRAM facilitated the construction of multiple weak filaments that enable the linear potentiation [43]. The structural engineering techniques also minimized the stochastic formation of the filament driven by the field and allowed for uniform and thermally stable distribution of multiple resistance states [47].

## SUMMARY AND OUTLOOK

RRAM-based analog synapses are attractive for implementing the artificial neural networks on-chip. Recent system-level analyses performed through simulations revealed that updating the linear and symmetric weight update plays a crucial role in achieving high online learning accuracy of the neuromorphic systems for pattern recognition. In this article, we surveyed strategies for approaching linear and symmetric conductance change as a function of identical pulses. The analog-synaptic devices were classified into interfacial and filamentary types based on the switching mechanisms. In the early stage of research, the interfacial RRAM devices were promising to emulate the analogously tuned resistances in both polarities because the barrier was reversely modulated by the back and forth motion of oxygen ions/vacancies toward the interface. However, because the extent of the barrier change strongly depended on bias polarity, the nonlinear and asymmetric weight update behaviors occurred, which are major factors to the degradation of the learning accuracy. Since pulses of a sufficiently long duration (~ms) are required to migrate the ions/vacancies to modify the barrier, slow speed and state instability dilemma also exist.

Therefore, the filamentary RRAM, which seemed to have only binary states in potentiation due to strong and single filament formation, has been attractively reconsidered for analog synapses. It is particularly important to make an environment in which the filament can be enlarged in the lateral direction or multiple weak filaments can be formed. The introduction of an optimized programming pulse or additional layers/dopant allowed the conductance to be updated linearly and rapidly driven by the identical pulses of ~100 ns or µs without the need for ramping pulse conditions that increase the complexity of the external circuitry.

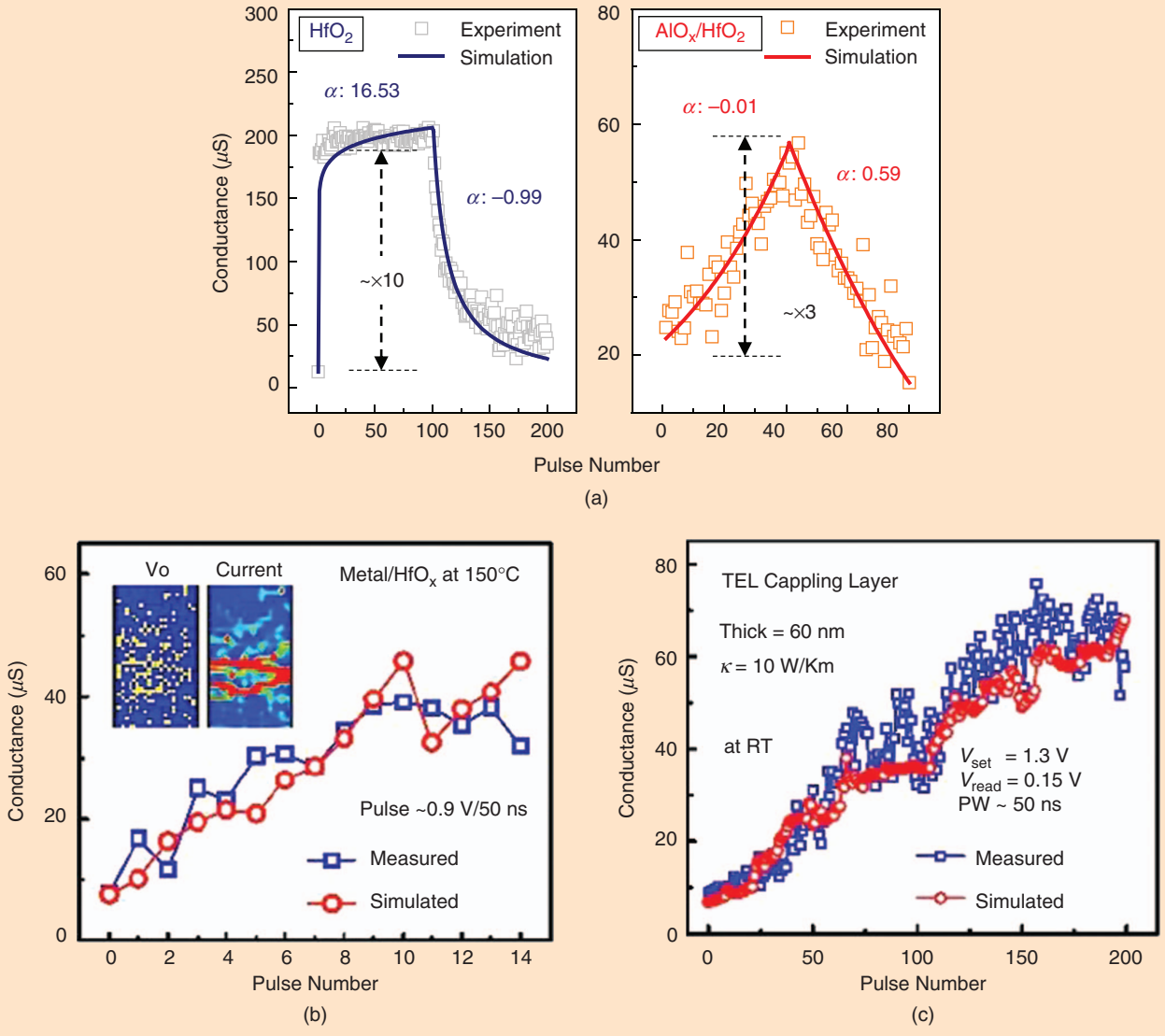



**FIGURE 6** Asymmetric weight update behavior caused by the nonlinear potentiation of filamentary $HfO_x$ RRAM. (a) Introducing $AlO_x$ layer or (b) measuring the RRAM device at high temperature enabled the linear response in the conductance with respect to the identical pulse. (c) Particularly, the thermally assisted linear potentiation characteristic at room temperature was demonstrated by inserting the thermal enhanced layer ($TaO_x$). Adapted from [27] and [43].

As the direction for future research, increasing the programming speed to sub-10 ns while maintaining the properties such as a linear and symmetric weight update, sufficient on/off ratio and number of levels, as well as the stability of each conductance state are necessary. The yield and variability at the array-level needs to be further controlled, although the neural networks could be somewhat resilient to some of the yield and variability limitations [9]–[12]. We hope that this article will provide fundamental insights for advanced development of analog RRAM-based synapses to be used for neuromorphic applications.

## ACKNOWLEDGMENTS

This work is supported in part by the National Science Foundation (NSF) Computing and Communication Foundations 1552687, NSF/Semiconductor Research Corporation (SRC) Energy Efficient Computing: from Devices to Architecture (E2CDA), and Applications and Systems Driven Center for Energy-Efficient Integrated NanoTechnologies (one of the six SRC/Defense Advanced Research Projects Agency Joint University Microelectronics Program Centers).

## ABOUT THE AUTHORS

***Jiyong Woo*** (jiyong.woo@asu.edu) is with the School of Electrical, Computer, and Energy Engineering at Arizona State University, Tempe.

***Shimeng Yu*** (shimeng.yu@ece.gatech.edu) is with the School of Electrical and Computer Engineering at the Georgia Institute of Technology, Atlanta.

## REFERENCES


[1] Y. LeCun, Y. Bengio, and G. Hinton, "Deep learning," *Nature*, vol. 521, no. 7553, pp. 436–444, May 2015.

[2] Y.-H. Chen, T. Krishna, J. Emer, and V. Sze, "Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2016, pp. 262–263.

[3] B. Moons, R. Uytterhoeven, W. Dehaene, and M. Verhelst, "ENVISION: A 0.26-to-10TOPS/W subword-parallel dynamic-voltage-accuracy-frequency-scalable convolutional neural network processor in 28 nm FDSOI," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2017, pp. 246–247.

[4] D. Kuzum, S. Yu, and H.-S. P. Wong, "Synaptic electronics: Materials, devices and applications," *Nanotechnology*, vol. 24, no. 38, pp. 382,001–382,023, Sept. 2013.

[5] H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, "Metal-oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, June 2012.

[6] G. C. Adam, B. D. Hoskins, M. Prezioso, F. Merrikh-Bayat, B. Chakrabarti, and D. B. Strukov, "3-D memristor crossbars for analog and neuromorphic computing applications," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 312–318, Jan. 2017.

[7] S. Yu, "Neuro-inspired computing with emerging nonvolatile memory," *Proc. IEEE*, vol. 106, no. 2, pp. 260–285, Feb. 2018.

[8] D. Rumelhart, G. Hinton, and R. Williams, "Learning representations by back-propagating errors," *Nature*, vol. 323, pp. 533–536, Oct. 1986.

[9] G. Burr, R. Shelby, C. Nolfo, J. Jang, R. Shenoy, P. Narayanan, K. Virwani, E. Giacometti, B. Kurdi, and H. Hwang, "Experimental demonstration and tolerancing of a large-scale neural network (165,000 synapses), using phase-change memory as the synaptic weight element," in *Proc. IEEE Int. Electron Devices Meet.*, 2014, pp. 29.5.1–29.5.4.

[10] S. Yu, P.-Y. Chen, Y. Cao, L. Xia, Y. Wang, and H. Wu, "Scaling-up resistive synaptic arrays for neuro-inspired architecture: Challenges and prospect," in *Proc. IEEE Int. Electron Devices Meet.*, 2015, pp. 17.3.1–17.3.4.

[11] P.-Y. Chen, X. Peng, and S. Yu, "NeuroSim+: An integrated device-to-algorithm framework for benchmarking synaptic devices and array architectures," in *Proc. IEEE Int. Electron Devices Meet.*, 2017, pp. 6.1.1–6.1.4.

[12] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories—Nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, no. 25–26, pp. 2632–2663, July 2009.

[13] D. Strukov, G. Snider, D. Stewart, and R. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, May 2008.

[14] D. Seong, J. Park, N. Lee, M. Hasan, S. Jung, H. Choi, J. Lee, M. Jo, W. Lee, S. Park, S. Kim, Y. Jang, Y. Lee, M. Sung, D. Kil, Y. Hwang, S. Chung, S. Hong, J. Roh, and H. Hwang, "Effect of oxygen migration and interface engineering on resistance switching behavior of reactive metal/polycrystalline $Pr_{0.7}Ca_{0.3}MnO_3$ device for nonvolatile memory applications," in *Proc. IEEE Int. Electron Devices Meet.*, 2009, pp. 5.4.1–5.4.4.

[15] D. Lee, J. Park, K. Moon, J. Jang, S. Park, M. Chu, J. Kim, J. Noh, M. Jeon, B. Lee, B. Lee, B.-G. Lee, and H. Hwang, "Oxide-based nanoscale analog synapse device for neural signal recognition system," in *Proc. IEEE Int. Electron Devices Meet.*, 2015, pp. 4.7.1–4.7.4.

[16] S. Park, H. Kim, M. Choo, J. Noh, A. Sheri, S. Jung, K. Seo, J. Park, S. Kim, W. Lee, J. Shin, D. Lee, G. Choi, J. Woo, E. Cha, J. Jang, C. Park, M. Jeon, B. Lee, B. H. Lee, and H. Hwang "RRAM-based synapse for neuromorphic system with pattern recognition function," in *Proc. IEEE Int. Electron Devices Meet.*, 2012, pp. 10.2.1–10.2.4.

[17] S. Park, A. Sheri, J. Kim, J. Noh, J. Jang, M. Jeon, B. Lee, B. Lee, B. Lee, and H. Hwang, "Neuromorphic speech systems using advanced ReRAM-based synapse," in *Proc. IEEE Int. Electron Devices Meet.*, 2013, pp. 25.6.1–25.6.4.

[18] K. Moon, E. Cha, J. Park, S. Gi, M. Chu, K. Baek, B. Lee, S. Oh, and H. Hwang, "High density neuromorphic system with $Mo/Pr_{0.7}Ca_{0.3}MnO_3$ synapse and $NbO_2$ IMT oscillator neuron," in *Proc. IEEE Int. Electron Devices Meet.*, 2015, pp. 17.6.1–17.6.4.

[19] T. Chang, S. Jo, K. Kim, P. Sheridan, S. Gaba, and W. Lu, "Synaptic behaviors and modeling of a metal oxide memristive device," *Appl. Phys. A*, vol. 102, pp. 857–863, Feb. 2011.

[20] Y. Wang, Y. Lin, I. Wang, T. Lin, and T.-H. Hou, "Characterization and modeling of nonfilamentary $Ta/TaO_x/TiO_2/Ti$ analog synaptic device," *Sci. Rep.*, vol. 5, no. 10150, pp. 1–9, May 2015.

[21] K. Seo, I. Kim, S. Jung, M. Jo, S. Park, J. Shin, K. Biju, J. Kong, K. Lee, B. Lee, and H. Hwang, "Analog memory and spike-timing-dependent plasticity characteristics of a nanoscale titanium oxide bilayer resistive switching device," *Nanotechnology*, vol. 22, no. 254023, pp. 254,023–254,038, June 2011.

[22] S. Jo, T. Chang, I. Ebong, B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett.*, vol. 10, no. 4, pp. 1297–1301, Apr. 2010.

[23] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang, and H.-S. P. Wong, "A low energy oxide-based electronic synaptic device for neuromorphic visual systems with tolerance to device variation," *Adv. Mater.*, vol. 25, pp. 1774–1779, Jan. 2013.

[24] B. Gao, Y. Bi, H.-Y. Chenm, R. Liu, P. Huang, B. Chen, L. Liu, X. Liu, S. Yu, H.-S. P. Wong, and J. Kang, "Ultra-low-energy three-dimensional oxide-based electronic synapses for implementation of robust high-accuracy neuromorphic computation systems," *ACS Nano*, vol. 8, no. 7, pp. 6998–7004, June 2014.

[25] L. Zhao, H. Chen, S. Wu, Z. Jiang, S. Yu, T.-H. Hou, H.-S. P. Wong, and Y. Nishi, "Multi-level control of conductive nano-filament evolution in $HfO_2$ ReRAM by pulse-train operations," *Nanoscale*, vol. 6, pp. 5698–5702, Mar. 2014.

[26] J. Woo, K. Moon, J. Song, M. Kwak, J. Park, and H. Hwang, "Optimized programming scheme enabling linear potentiation in filamentary $HfO_2$ RRAM synapse for neuromorphic systems," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 5064–5067, Dec. 2016.

[27] J. Woo, K. Moon, J. Song, S. Lee, M. Kwak, J. Park, and H. Hwang, "Improved synaptic behavior under identical pulses using $AlO_x/HfO_2$ bilayer RRAM array for neuromorphic systems," *IEEE Electron Device Lett.*, vol. 37, no. 8, pp. 994–997, Aug. 2016.

[28] R. Jacobs-Gedrim, S. Agarwal, K. Knisely, J. Stevens, M. Heukelom, D. Hughart, J. Niroula, C. James, M. Marinella, "Impact of linearity and write noise of analog resistive memory devices in a neural algorithm accelerator," in *Proc. IEEE Int. Conf. Rebooting Computing*, 2017, pp. 1–10.

[29] S. Kim, S. Choi, J. Lee, and W. Lu, "Tuning resistive switching characteristics of tantalum oxide memristors through Si doping," *ACS Nano*, vol. 8, no. 10, pp. 10,262–11,069, Sept. 2014.

[30] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H.-S. P. Wong, "An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2729–2737, Aug. 2011.

[31] C. Wang, W. He, Y. Tong, and R. Zhao, "Investigation and manipulation of different analog behaviors of memristor as electronic synapse for neuromorphic applications," *Sci. Rep.*, vol. 6, no. 22970, pp. 1–9, Mar. 2016.

[32] F. Alibart, L. Gao, B. Hoskins, and D. Strukov, "High-precision tuning of state for memristive devices by adaptable variation-tolerant algorithm," *Nanotechnology*, vol. 23, no. 075201, pp. 075,201–075,208, Feb. 2012.

[33] M. Prezioso, I. Kataeva, F. Merrikh-Bayat, B. Hoskins, G. Adam, T. Sota, K. Likharev, and D. Strukov, "Modeling and implementation of firing-rate neuromorphic-network classifiers with bilayer $Pt/Al_2O_3/TiO_{2-x}/Pt$ memristors," in *Proc. IEEE Int. Electron Devices Meet.*, 2015, pp. 17.4.1–17.4.4.

[34] S. Kim, H. Kim, S. Hwang, M. Kim, Y. Chang, and B. Park, "Analog synaptic behavior of a silicon nitride memristor," *ACS Appl. Materials Interfaces*, vol. 9, pp. 40,420–40,427, Oct. 2017.

[35] W. Chen, R. Fang, M. Balaban, W. Yu, Y. Gonzalez-Velo, H. Barnaby, and M. Kozicki, "A CMOS-compatible electronic synapse device based on $Cu/SiO_2/W$ programmable metallization cells," *Nanotechnology*, vol. 27, no. 255202, pp. 255,202–255,211, May 2016.

[36] X. Zhang, S. Liu, X. Zhao, F. Wu, Q. Wu, W. Wang, R. Cao, Y. Fang, H. Lv, S. Long, Q. Liu, and M. Liu, "Emulating short-term and long-term plasticity of bio-synapse based on Cu/a-Si/Pt memristor," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1208–1211, Sept. 2017.

[37] M. Suri, O. Bichler, D. Querlioz, G. Palma, E. Vianello, D. Vuillaume, C. Gamrat, and B. Salvo, "CBRAM devices as binary synapses for low-power stochastic neuromorphic systems: Auditory (Cochlea) and visual (Retina) cognitive processing applications," in *Proc. IEEE Int. Electron Devices Meet.*, 2012, pp. 10.3.1–10.3.4.

[38] J. Jang, S. Park, G. Burr, H. Hwang, and Y. Jeong, "Optimization of conductance change in $Pr_{1-x}Ca_xMnO_3$-based synaptic devices for neuromorphic systems," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 457–459, May 2015.

[39] I.-T. Wang, C.-C. Chang, L.-W. Chiu, T. Chou, and T.-H. Hou, "3D $Ta/TaO_x/TiO_2/Ti$ synaptic array and linearity tuning of weight update for hardware neural network applications," *Nanotechnology*, vol. 27, no. 365204, pp. 365,204–365,212, Aug. 2016.

[40] Y. Jeong, S. Kim, and W. Lu, "Utilizing multiple state variables to improve the dynamic range of analog switching in a memristor," *Appl. Phys. Lett.*, vol. 107, no. 173105, pp. 1–5, Oct. 2015.

[41] J. Park, M. Kwak, K. Moon, J. Woo, D. Lee, and H. Hwang, "$TiO_x$-based RRAM synapse with 64-levels of conductance and symmetric conductance change by adopting a hybrid pulse scheme for neuromorphic computing," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1593–1562, Dec. 2016.

[42] J. Woo, A. Padovani, K. Moon, M. Kwak, L. Larcher, and H. Hwang, "Linking conductive filament properties and evolution to synaptic behavior of RRAM devices for neuromorphic applications," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1220–1223, Sept. 2017.

[43] B. Gao, H. Wu, W. Wu, X. Wang, P. Yao, Y. Xi, W. Zhang, N. Deng, P. Huang, X. Liu, J. Kang, H. Chen, S. Yu, and H. Qian, "Modeling disorder effect of the oxygen vacancy distribution in filamentary analog RRAM for neuromorphic computing," in *Proc. IEEE Int. Electron Devices Meet.,* 2017, pp. 4.4.1–4.4.4.

[44] W. Wu, H. Wu, B. Gao, N. Deng, S. Yu, and H. Qian, "Improving analog switching in $HfO_x$-based resistive memory with a thermal enhanced layer," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1019–1022, Aug. 2017.

[45] L. Goux, A. Fantini, R. Degraeve, N. Raghavan, R. Nigon, S. Strangio, G. Kar, D. J. Wouters, Y. Y. Chen, M. Komura, F. De Stefano, V. V. Afanas'ev, and M. Jurczak, "Understanding of the intrinsic characteristics and memory trade-offs of sub-$\mu$A filamentary RRAM operation," in *Proc. Symp. VLSI Technology*, 2013, pp. T162–T163.

[46] S. Mandal, A. El-Amin, K. Alexander, B. Rajendran, and R. Jha, "Novel synaptic memory device for neuromorphic computing," *Sci. Rep.*, vol. 4, no. 5333, p. 1–10, June 2014.

[47] M. Zhao, H. Wu, B. Gao, Q. Zhang, W. Wu, S. Wang, Y. Xi, D. Wu, N. Deng, S. Yu, H. Chen, and H. Qian, "Investigation of statistical retention of filamentary analog RRAM for neuromorphic computing," in *Proc. IEEE Int. Electron Devices Meet.*, 2017, pp. 39.4.1–30.4.4.