Ovonic threshold switching selectors for three-dimensional stackable phase-change memory

Min Zhu, Kun Ren, and Zhitang Song

High-current switching performance of ovonic threshold switching (OTS) selectors have successfully enabled the commercialization of high-density three-dimensional (3D) stackable phase-change memory in Intel's 3D Xpoint technology. This bridges the huge performance gap between dynamic random access memory (DRAM) and Flash. Similar to phase-change memory, OTS uses chalcogenide-based materials, but whereas phase-change memory reversibly switches between a high-resistance amorphous phase and a low-resistance crystalline phase, OTS freezes in the amorphous phase. In this article, we review recent developments in OTS materials and their performance in devices, especially current density and selectivity. Advantages and challenges of OTS devices in the integration with the phase-change memory are discussed. We introduce the evolution of theoretical models for explaining the OTS behavior, including thermal runaway, field-induced nucleation, and generation/recombination of charge carriers.

Introduction

Computers have not only profoundly transformed our lives, they also provide solutions to some of society's most pressing challenges, from analyzing big data to understanding human language. To meet these and future requirements, faster computing ability and larger data storage are needed.[1,2] However, the huge performance gap between volatile static random-access memory/dynamic random-access memory (SRAM/DRAM) and nonvolatile Flash memory in the storage architecture of current computers (**Figure 1**a) has become a critical bottleneck for further development.[3,4] Since 2008, storage class memory, a term describing emerging memory technologies that may eventually replace Flash and perhaps even DRAM, has been proposed by IBM to bridge this gap.[4–7]

Phase-change memory, based on the physical structural change between a high-resistance amorphous phase and a low-resistance crystalline phase of chalcogenides, is the most promising candidate in storage class memory.[8–10] Indeed, the 3D Xpoint, a commercial phase-change memory released by Intel in 2015 (Figure 1b), has demonstrated device performance between DRAM and Flash memory, including operation speed, device lifetime, and storage density.[11,12]

To achieve the highest $4F^2$ (F = feature size) density as Flash memory, the crossbar array seems to be the most attractive device architecture, which has also been used in the 3D Xpoint (Figure 1c).[11,12] This device architecture is commonly operated using a "Half-V" select scheme, in which the read voltage is applied to the targeted phase-change memory cell, while other lines in the array remain biased at half the voltage. However, the neighboring cells in the same row or column as the selected cell (half-selected cells) become half-biased and can enable unwanted current pathways known as "sneak currents."[13] This decreases the read sense margin (the difference in total resistance between the 1 and 0 states), increases power consumption, and limits the array size. A nonlinear switch such as a selector device is connected to each phase-change memory cell in order to suppress sneak currents from the half-selected cells, as shown in Figure 1c. That is, ultralow current (off-current, I_{off}) flows through the selectors when only half the read voltage is applied. When the full read voltage is applied, the "on" threshold voltage, V_{th}, of the selector is exceeded, and the selectors sustain a high current (on-current, I_{on}), sufficient to drive the targeted (selected) phase-change memory cell.

Until now, several selector candidates have been proposed, including a Si-based diode/metal oxide semiconductor

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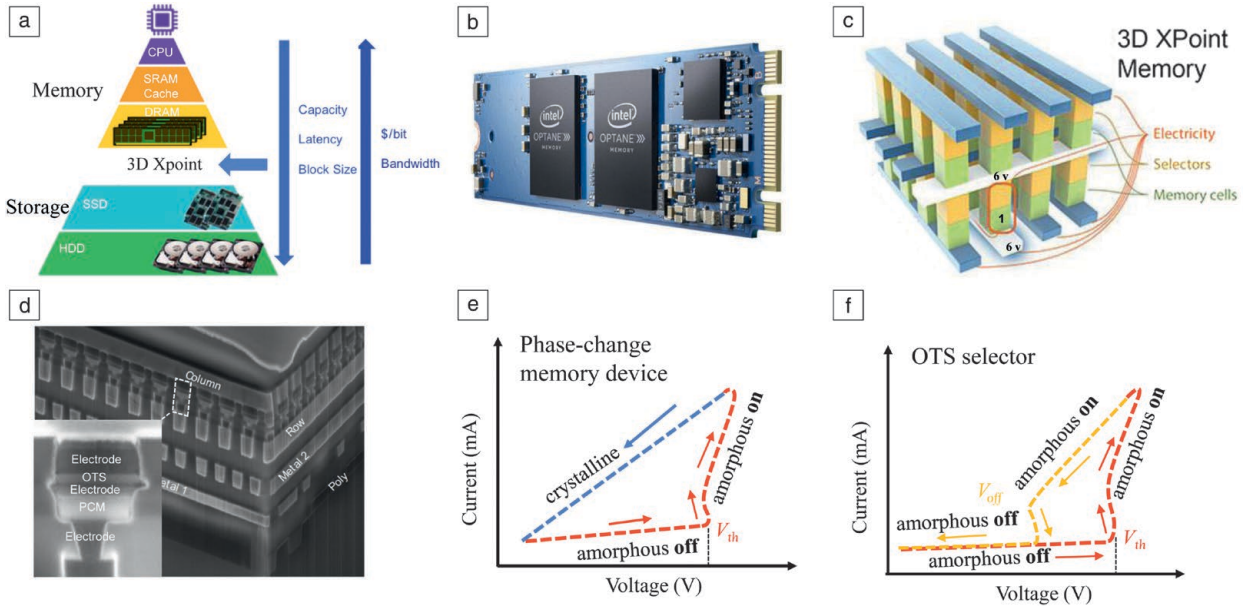

Figure 1. (a) Performance gap in the storage architecture of a current computer. (b) Photo of 3D Xpoint memory released by Intel in 2015. (c) 1S1R stackable crossbar structure of 3D Xpoint memory, showing a selected memory cell in the high-resistance state (1). (d) Ovonic threshold switch (OTS) + phase-change memory (PCM) in a 3D stackable crosspoint array reported by Intel in 2009. The inset highlights one integrated memory cell consisting of one OTS and one PCM cell. (e) Voltage–current curve of a PCM device, showing ovonic memory switching behavior. (f) Voltage–current curve of an OTS device, distinct from that of PCM. Note: S, selector; M, phase-change memory; CPU, central processing unit; SRAM, static random–access memory; DRAM, dynamic random–access memory.

field-effect transistor (MOSFET),[14,15] an ovonic threshold switch (OTS),[16] Mott-insulator transition (MIT),[17] conductive bridge threshold switch (CBTS),[18] and field-assisted-superliner-threshold (FAST) selector.[19] However, to integrate the selector with the phase-change memory, there are several requirements. Most importantly, the selector should be capable of providing >10 MA/cm^2 to melt-quench the chalcogenide in the phase-change memory. Nonlinearity or selectivity, defined as I_{on}/I_{off}, should be >10^4 to achieve a dense (>1 Mb) phase-change memory array. The selector needs to be accessed for >10^6 cycles since the device lifetime of phase-change memory is >10^6 cycles. The selector also needs to be switched within 100 ns, comparable to that of the phase-change memory cell. The selector needs to be fabricated by a process compatible with phase-change memory. High-temperature film deposition should be avoided, which would cause phase segregation of the chalcogenides. The nonlinear behavior of the selector should be able to withstand 450°C for 30 min in the back-end-of-the-line process, in which the metal wire and insulating layer are deposited. Most selector candidates thus far fail to meet one or more of these requirements. Among them, the OTS, providing high I_{on} and being compatible with phase-change memory, has been successfully used in 3D stackable crossbar phase-change memory, as reported by Intel in 2009 (Figure 1d), as well as in the 3D Xpoint.[16]

Interestingly, OTS selectors employ chalcogenide materials, which are also the basis of phase-change memory. By employing chalcogenides with different stoichiometries, these devices exhibit distinctly different electronic behaviors, as respectively illustrated in Figure 1e–f for an OTS selector and a phase-change memory device. Both cells show negative-differential-resistance behavior as V_{th} is reached, and then mA-scale high current flows. When gradually removing the voltage, the phase-change memory cell becomes highly conductive (with 10^2–10^4 ohm resistance) and shows ohmic property, whereas the OTS cell returns to its initial high resistance state at a certain voltage (V_{hold}, $0 < V_{hold} < V_{th}$). The dramatic resistance drop of the phase-change memory is attributed to the crystallization of the amorphous chalcogenide film, usually GeTe, Sb_2Te_3, or GeTe-Sb_2Te_3 pseudobinary alloys (Figure 1e).[20,21] The current–voltage electrical behavior of phase-change memory is known as ovonic memory switching (OMS). In contrast, the OTS cell freezes in the amorphous phase, and these devices are commonly based on GeSe chalcogenides (Figure 1f).

To date, two interpretations have been proposed to explain this difference. The first one is that OTS materials always have a high crystallization temperature and ultralow crystallization speed, so that they remain intact against thermal fluctuations.[13] This explanation is supported by the performance change of the Ge-Te binary alloy from OMS (GeTe alloy[22]) to OTS ($GeTe_6$ alloy[23]) with increasing Te concentration. Another explanation is based on the bonding mechanism, namely, phase-change memory materials possess a unique bonding mechanism, metavalent bonding, whereas OTS utilizes conventional covalent bonding (see the article by Pries et al. in this issue).[24,25]

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In this article, we first discuss the evolution of OTS materials, especially those discovered after 2009. We summarize their device performance. Finally, we revisit the potential switching mechanisms of the OTS.

Emerging OTS materials

The OTS phenomenon was first observed in the As-Te-I system in 1964 by Noverthover and Pearson.[26] Two years later, Ovshinsky also described the behavior and possible device structures, using it in his patent.[27] In 1968, he reported the OTS behavior of $Te_{48}As_{30}Si_{12}Ge_{10}$ chalcogenide and noticed that the removal of As resulted in OMS behavior.[28] Subsequently, several researchers continued to investigate OTS. The idea of integration with phase-change memory as the selector was proposed in 1970.[29] Interest in the OTS selector was rekindled by the breakthrough achievement of a 3D stackable crossbar phase-change memory array with OTS elements in 2009;[16] the OTS materials used have not yet been made public. Since then, numerous OTS materials have been proposed,[11,12,23,30–52] as summarized in **Figure 2**.

The first material family developed was a Te-based alloy, represented by Ge-Te,[23,31] doped with elements such as, Si, and N,[31–34] as shown in Figure 2. These materials were characterized by short switching times. For example, $GeTe_6$[23] and Ge-As-Te-Si-N[33] OTS showed <5 ns switching speed. Moreover, B-Te[35] and C-Te[36] OTS were reported to switch within 2 ns. A second material family was a Se-based alloy, in which the addition of Ge seems to be essential.[12,37–43] As shown in Figure 2, Ge-Se OTS has received increasing attention owing to low I_{off} and good thermal stability. Usually, N, As, Si, and Sb were incorporated to strengthen these advantages.[38–43] A composition doped with As and Si is believed to be the OTS material used in 3D Xpoint.[11,12] In some cases, both Te and Se were involved in the OTS, such as for the Ge-Se-Te-As-Si alloy.[44] From Figure 2, we can see that the composition of the OTS material has become increasingly complicated over the years, with five or more elements used. This presents a major challenge to achieve a precise stoichiometry across a silicon wafer for applications. Even if this issue can be solved satisfactorily, electromigration of different atoms toward a positive or negative electrode under regularly applied strong electric fields will limit the device lifetime by altering the stoichiometry.

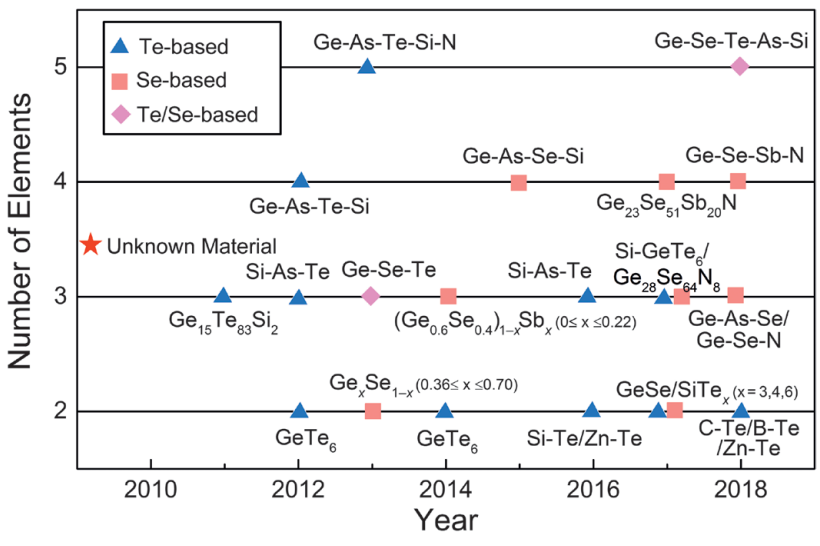

Figure 2. The evolution of emerging ovonic threshold switching (OTS) materials since 2009.[11,12,23,30–52] The red star highlights the breakthrough achievement of a 3D stackable crossbar phase-change memory array with OTS elements by Intel in 2009; the OTS material used is still unknown.

OTS performance

Using various materials, OTS cells exhibit varying performance. Here, we summarize device performances of emerging OTS devices, as shown in **Table I**. As previously discussed, higher on-current density (J_{on}) and selectivity are favorable for 3D integration with a phase-change memory cell. Typically, Te-based OTSs show a high J_{on} of >1 MA/cm^2. For instance, J_{on} of 11 MA/cm^2 has been obtained for a Ge-As-Te-Si-N OTS.[32,33] Nevertheless, these devices showed low selectivity of <10^4, which was insufficient for achieving a dense (>1Mb) phase-change memory array.[45,46] Noticeably, OTSs employing a Te binary alloy (such as Si-Te,[47] C-Te,[36] and B-Te[35]) have demonstrated J_{on} of >10 MA/cm^2 and selectivity of >10^5. Among these devices, the B-Te OTS possesses the highest J_{on} of 55 MA/cm^2 in the literature.[35] In addition, high endurance up to 10^8 cycles and thermal stability up to 450°C was reported.

Se-based OTSs, as shown in Table I, typically present MA/cm^2-scale J_{on}, although a J_{on} >20 MA/cm^2 was also reported for undoped and N-doped Ge-Se OTSs.[39,43] Remarkably, they show long device lifetimes of >6 × 10^{11} cycles for As-doped Ge-Se OTS.[44] Moreover, the ultrahigh amorphous resistance, Se-based OTS is also characterized by low I_{off} of ~0.1 nA for $Ge_{58}Se_{42}$ and As-doped Ge-Se OTSs.[41,44] For OTS with the same material, varying J_{on} and selectivities were reported, which may be due to different cell structures, electrode sizes, and fabrication processes.[48–52]

Figure 3 shows the scalability of J_{on} for a Ge-As-Te-Si-N-based OTS, as reported by Lee et al.[32] Bez reported that for a 500 × 500 nm^2 cell, a J_{on} of 0.039 MA/cm^2 was obtained, 10 times smaller than that required to operate the phase-change memory cell.[53] Fortunately, the J_{on} of the OTS exponentially increases as the device size shrinks. Although similar scaling behavior of current density was found for operating a phase-change memory cell, it increased much slower than that observed for OTS. As the device shrinks to 20 × 20 nm^2, the J_{on} of the OTS is expected to reach 22 MA/cm^2,[32] sufficient for programming the PCM cell.

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Table I. Summary of ovonic threshold switching device performances using different materials.[23,32–52]

Material	Device Size	On/Off Ratio	J_{on} (MA/cm^2)	I_{off} (A)	V_{th} (V)	V_h (V)	Speed (ns)	Endurance
Ge-Se[39]	50 nm	10^3	23	10^{-7}	~1.4	~0.5	**~2**	10^8
Ge-Se-N[43]	50 nm	10^5	23	2×10^{-9}	~4	~1	—	10^8
Ge-Se-As[44]	350 nm	10^5	7.9	1.3×10^{-10}	~3.5	~1.2	~10	**6×10^{11}**
Ge-Se-Sb-N[52]	—	10^4	1.4	10^{-9}	2.2	0.76	—	10^6
$Ge_{58}Se_{42}$[41]	300 nm	10^5	1.5	**10^{-10}**	3.5	1.7	~50	10^9
$GeTe_6$[23]	60 nm	~10^5	~1.8	—	~1.6	~ 0.7	~	600
Si-Te[47]	100 nm	**10^6**	10	~8×10^{-10}	~1.2	—	**~2**	5×10^5
Zn-Te[51]	200 nm	10^5	13	~6×10^{-6}	**~0.6**	~0.4	—	—
C-Te[36]	30 nm	10^5	11	5×10^{-9}	**~0.6**	**~0.3**	**~2**	10^8
B-Te[35]	30 nm	10^5	**~55**	~10^{-9}	~0.75	**~0.3**	**~2**	10^8
Ge-As-Te-Si-N[32,33]	30 nm	10^3	11	~10^{-6}	~1.8	~1.5	—	10^8
Ge-As-Se-Te-Si[45]	350 nm	10^4	0.44	1.9×10^{-9}	~2.2	~1.5	~50	10^{10}

*Bold items highlight the best performances among these devices.

Potential switching mechanism

Although more and more OTS materials are being proposed, the inherent mechanism remains unclear. In the past half of a century, many models have been proposed to explain this phenomenon. Among them, the representative ones are thermal runaway, field-induced nucleation, and pure electronic models, as shown in **Figure 4**.

The thermal runaway model, illustrated in Figure 4a, was first described by Kroll et al. in the 1970s.[54,55] With increasing applied voltage, the current passing through the OTS cell increases. As a result, the induced Joule effect increases the temperature of the chalcogenide film, which further triggers more carriers. When the temperature rises sufficiently, a positive feedback switches on and the conductivity exponentially increases. Once the voltage reaches V_{th}, the voltage subsequently decreases in order to maintain a high current density, resulting in the threshold switching. However, this model was greatly challenged by disagreement with the experimental conductivity-temperature relationship and the absence of negative-resistance behavior in simulations.[56]

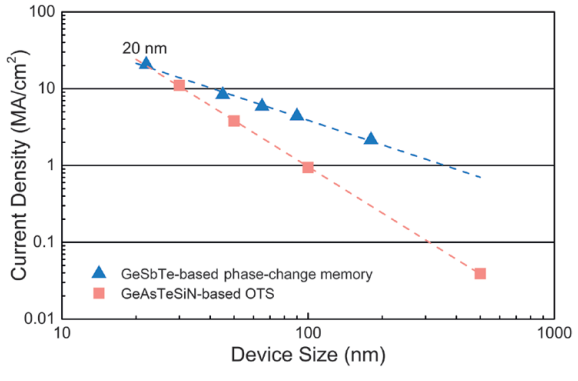

Figure 3. Scalability of current densities with device size provided by GeAsTeSiN-based ovonic threshold switching (OTS)[32] and current densities required for operating GeSbTe-based phase-change memory.[53]

Karpov et al. proposed[57,58] the field-induced nucleation model in 2007, based on the classical nucleation theory, as illustrated in Figure 4b. According to classical nucleation theory,[59] the crystal growth process only take place after the nuclei exceed a critical size (R_0). Under an applied strong electrical field, subcritical nuclei form heterogeneously at the chalcogenide/electrode interface, reducing the device conductivity.[57] Nevertheless, these unstable subcritical nuclei will disappear when the electrical field is removed. This results in the transient nature of the OTS and the relaxation from a low-resistance to high-resistance state (Figure 1f). In contrast, if the electrical field is maintained, these subcritical nuclei develop into stable supercritical ones, even after the field is removed. As the crystalline filament is formed by the growth of these supercritical nuclei, the cell freezes in the highly conductive crystalline state, inducing the OMS behavior seen in Figure 1e.[60] The field-induced nucleation model predicts the experimentally observed V_{th}–temperature relationship and switching delay time. Yet, the poor conductivity of crystalline OTS material when compared to the amorphous state, observed in GeSe, raises questions about this mechanism.[61]

The electronic model can be tracked back to Kaplan and Adler's work published in 1971;[56] they noticed that a pure thermal model could not achieve negative differential resistance observed in OTS. In 1980, Adler et al. described the threshold switching effect as an interaction of charge-carrier generation and recombination mechanisms.[62] In this model, lone-pair-induced traps above the valence band mobility play a critical role in the conductivity. More specifically, under an applied low electrical field, the field-induced carriers are captured by these traps, which leads to low conductivity. Under a strong field, the

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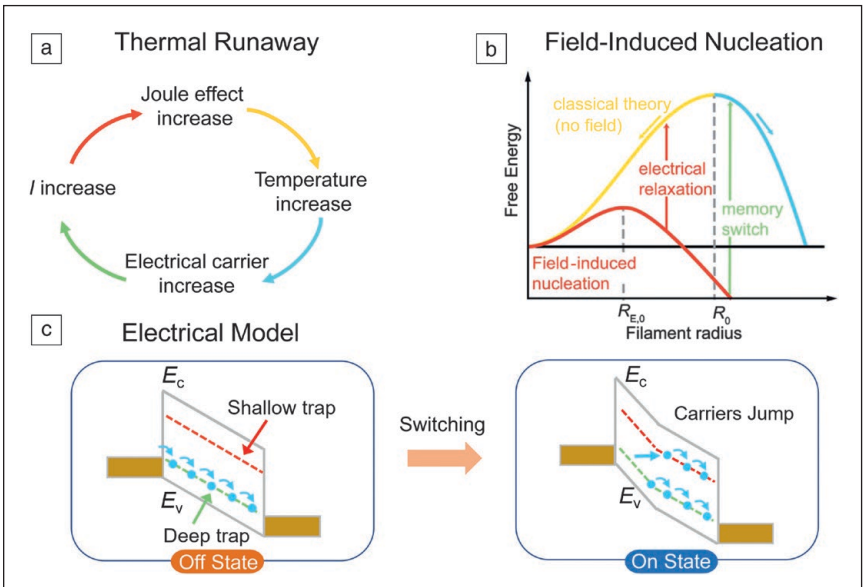

Figure 4. Three representative models to explain the ovonic threshold switching (OTS) phenomena: (a) thermal runaway,[54,55] (b) field-induced nucleation,[57,58] and (c) pure electrical phenomenon (yellow bars represent metal electrode).[66] Note: $R_{E,0}$, critical size of nuclei induced by electric field; R_0, critical size of nuclei induced by thermal energy; E_v, valence band; E_c, conduction band.

generation mechanism dominates, and threshold switching occurs, as all of the traps are filled so that the carriers can move freely. A current filament formed by these carriers leads to an amorphous on-state. As long as any filament remains, only a voltage above V_{hold} is required to resuscitate the on-state. Upon further decreasing the voltage, the recombination mechanism dominates again and the filament disappears, resulting in the transition to the amorphous off-state.[63] Pirovano et al.[64] and Redaelli et al.[65] reformulated Adler's model after 2000, incorporating impact ionization from the charge carriers.

Ielmini et al., in their work, differed from Adler's model and considered how traps play a positive effect on the conductivity[66] (Figure 4c). Under a stronger field, carriers can jump from deep trap states into shallow trap states through thermal emission or tunneling processes. The energy of the excited carriers can be shared among neighboring ones, which causes a nonequilibrium distribution of carriers and nonuniform electric-field distribution. When sufficient carriers are excited into shallow trap states, the threshold switching behavior appears.[60] Ielmini's model successfully accounts for the complete current–voltage relationship, which has been widely accepted. Clima et al. recently proved using first-principles simulations that an electric field can promote carrier repopulation, thereby increasing the conductivity of the OTS.[67]

Conclusions

This article reviewed the evolution of emerging OTS materials after the successful integration of phase-change memory and OTS cells, and discussed their device performance. Continuous Te-based OTS materials have been reported, characterized by nanosecond-scale rapid switching speeds and >10 MA/cm^2 large on current density. Another class of material is Ge-Se-based alloys, often doped with N, Sb, and As. They have gained much attention in recent years owing to good thermal stability, low leakage current and good endurances. As they can provide the high current densities required for programming conventional phase-change memory cells, current OTS cells have the capability of driving phase-change memory cells as the cell size shrinks to 20 nm.

Finally, we revisited the underlying physical mechanisms for the OTS phenomenon, including thermal runaway, field-induced nucleation as well as generation/recombination of charge carriers. It is generally accepted that the threshold switching is a purely electronic process, which seems to be well explained using Ielmini's model. Even so, a clear and full understanding of the threshold switching behavior is still needed to enable the design of better OTS for high-density 3D stackable phase-change memory application.

Acknowledgments

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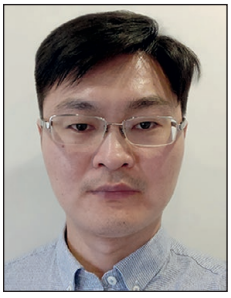

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