INVITED PAPER

Metal–Oxide RRAM

The authors discuss metal–insulator–metal structures that can be adopted to integrate 3-D nonvolatile memory chips and neuromorphic computing.

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ABSTRACT | In this paper, recent progress of binary metal-oxide resistive switching random access memory (RRAM) is reviewed. The physical mechanism, material properties, and electrical characteristics of a variety of binary metal-oxide RRAM are discussed, with a focus on the use of RRAM for nonvolatile memory application. A review of recent development of large-scale RRAM arrays is given. Issues such as uniformity, endurance, retention, multibit operation, and scaling trends are discussed.

KEYWORDS | Emerging memory; metal oxide; multibit memory; nonvolatile memory; OxRAM; ReRAM; resistance change memory; resistive switching memory; resistive switching random access memory (RRAM); solid-state memory

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I. INTRODUCTION

The observation that oxides that are nominally insulators can undergo an abrupt switching event to transition into a conductive state has been known for over 40 years. The first reports of such resistive switching phenomena date back to the 1960s [1]–[4]. The device structure is simply an oxide material sandwiched between two metal electrodes, called the metal–insulator–metal (MIM) structure. The early observations of resistance switching were not robust enough for memory applications and those reports remain in the domain of scientific studies. The recent revival of interest in resistive switching began in the late 1990s, first with complex metal oxides such as the pervoskite oxides of $SrTiO_3$ [5], $SrZrO_3$ [6] and later the binary metal oxides such as NiO [7] and TiO_2 [8]. Various acronyms such as OxRAM, ReRAM, and RRAM, have been used in the literature for these devices that exhibit resistive switching between a high-resistance state (HRS) and a low-resistance state (LRS). Research activity began to intensify after 2004 when Samsung presented a paper [9] at the International Electron Devices Meeting (IEDM) that demonstrated NiO memory cells integrated with conventional 0.18-μm complementary metal–oxide–semiconductor (CMOS) in a one-transistor–one-resistor (1T1R) device structure. The paper included a more complete set of memory-technology-oriented data such as data retention, endurance, and programming characteristics that suggested that a memory technology based on resistive switching may be feasible.

The expectation for RRAM is that it will be a memory technology that can be integrated with conventional CMOS in a simple way, using a material set compatible with the conventional CMOS fabrication environment and process temperatures that allow it to be fabricated on the metal layers or within the contact vias to the source and drain of a metal–oxide–semiconductor field-effect transistor (MOSFET) of a CMOS chip. Because the fabrication temperature is back-end-of-the-line (BEOL) compatible, it is often additionally envisioned that the RRAM can be stacked in 3-D in a cross-point architecture with an effective memory cell area of

$4\,F^2/n$, where n is the number of 3-D-stacked memory layers [10]. On the system level, it is envisioned that a revolution in memory hierarchy and system architecture will be realized by this low-cost, BEOL-compatible, nonvolatile memory with tens of nanosecond bit-alterable READ/WRITE speed, over 10^6 endurance cycles, and potentially low power/energy consumption.

While the concept of a MIM memory cell is simple, to give a comprehensive review of the topic is virtually impossible. This is because there are numerous materials that exhibit resistive switching. The switching behavior is not only dependent on the oxide materials but also dependent on the choice of metal electrodes and their interfacial properties. Recent reviews by Waser *et al.* [11]–[13], Sawa [14], and Akinaga *et al.* [15] provide excellent broad overviews and a useful taxonomy of the proposed switching and conduction mechanisms of the various types of RRAM and will not be repeated here. And we will not discuss the conductive-bridge RAM (CBRAM) [16], which relies on the fast-diffusing Ag or Cu ions into the oxide (or chalcogenide) to form a conductive bridge. In this paper, we focus on the simple binary metal–oxide RRAM and review its proposed resistance switching mechanisms (Section II), materials properties and device characteristics (Section III), memory cell, selection device and memory array design considerations (Section IV), and key performance metrics and their device scaling trends (Section V). Even when we limit this review to binary metal oxides, there are still too many materials to cover. We selected some of the more promising or interesting materials (HfO_x, AlO_x, NiO_x, TiO_x, and TaO_x) and review them in more detail. Note that the oxides here are often nonstoichiometric, thus we use subscript "x" for the oxygen composition in this review paper. Section VI concludes this paper with a future outlook for RRAM and its emerging applications for reconfigurable logic and neuromorphic computing.

II. RESISTIVE SWITCHING MECHANISM

We first introduce some basic concepts and terminologies about metal–oxide RRAM. The switching event from HRS to LRS is called the "set" process. Conversely, the switching event from LRS to HRS is called the "reset" process. Usually for the fresh samples in its initial resistance state, a voltage larger than the set voltage is needed to trigger on the resistive switching behaviors for the subsequent cycles. This is called the "electroforming" or "forming" process. The switching modes of metal–oxide RRAM can be broadly classified into two switching modes: unipolar and bipolar. Fig. 1 shows a sketch of the I–V characteristics for the two switching modes. Unipolar switching means the switching direction depends on the amplitude of the applied voltage but not on the polarity of the applied voltage. Thus, set/reset can occur at the same polarity. If the unipolar switching can symmetrically occurs at both positive and negative voltages, it is also referred as a nonpolar switching mode. Bipolar switching means the switching direction depends on the polarity of the applied voltage. Thus, set can only occur at one polarity and reset can only occur at the reverse polarity. For either switching modes, to avoid a permanent dielectric breakdown in the set process, it is recommended to enforce a set compliance, which is usually provided by the semiconductor parameter analyzer, or more practically, by a memory cell selection transistor/diode or a series resistor. To read the data from the cell, a small READ voltage is applied that does not affect the state of the memory cell to detect whether the cell is in HRS or LRS.

There have been many efforts in the literature to fit the I–V characteristics of current conduction in the HRS and the LRS. Most reports show a linear or ohmic relationship in the LRS. But, the conduction characteristics in HRS are quite diverse: Poole–Frenkel emission ($\log(I/V) \sim V^{1/2}$) [17], [18], Schottky emission ($\log(I) \sim V^{1/2}$) [19], [20], the space charge limited current (SCLC) characteristic (the ohmic region $I \sim V$, and the Child's square law region $I \sim V^2$) [21], [22] were observed in various metal–oxide RRAMs.

A simple I–V fitting with the aforementioned established model may not be sufficient to describe the conduction in metal–oxide RRAM. In general, Fig. 2 shows all the possibilities for an electron pass from cathode to

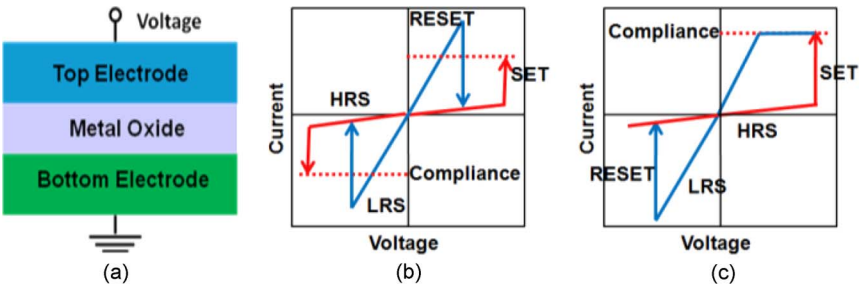


Fig. 1. *(a) Schematic of MIM structure for metal–oxide RRAM, and schematic of metal–oxide memory's I–V curves, showing two modes of operation: (b) unipolar and (c) bipolar.*

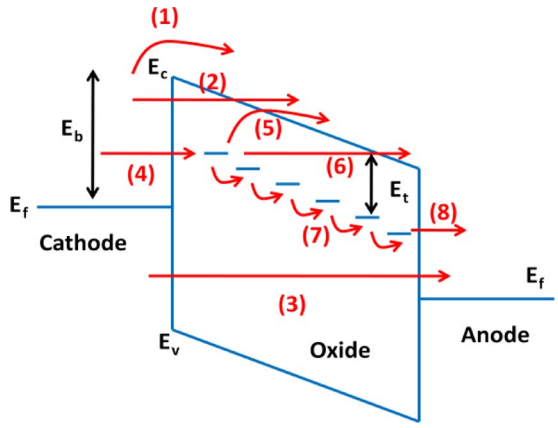


Fig. 2. *Schematic of the possible electron conduction paths through a MIM stack. (1) Schottky emission: thermally activated electrons injected over the barrier into the conduction band. (2) Fowler–Nordheim (F–N) tunneling: electrons tunnel from the cathode into the conduction band; usually occurs at high field. (3) Direct tunneling: electron tunnel from cathode to anode directly; usually occurs when the oxide is thin enough. If the oxide has substantial number of traps (e.g., oxygen vacancies), trap-assisted tunneling contributes to additional conduction, including the following steps: (4) tunneling from cathode to traps; (5) emission from trap to conduction band, which is essentially the Poole–Frenkel emission; (6) F–N-like tunneling from trap to conduction band; (7) trap to trap hopping or tunneling, maybe in the form of Mott hopping when the electrons are in the localized states or maybe in the form of metallic conduction when the electrons are in the extended states depending on the overlap of the electron wave function; and (8) tunneling from traps to anode. Adapted from [23].*

anode [23] (note that most of the RRAM oxides are n-type conducting). Whether any one particular process dominates is determined by its transition rate; electrons would seek the least resistive paths among all the possibilities. Therefore, various metal–oxide RRAMs may have different dominant conduction mechanism depending on the dielectric properties (bandgap or trap energy level, etc.), the fabrication process conditions (annealing temperature, annealing ambient, etc.), and the properties of the interface between the oxides and the electrodes (interfacial barrier height). For HfO_x memory, Yu *et al.* verified that at low bias regime the HRS conduction is dominated by trap-assisted tunneling using various characterization techniques such as varying temperature [23], [24], low-frequency noise [25], and alternate current (AC) conductance measurement [26]. The I–V relationship at the low bias regime is mainly determined by the electron conduction process for a given configuration of the conductive filaments (CFs), while at the high bias regime, the motion of atoms (such as oxygen ions/vacancies) would change the configuration of the CFs and trigger a change of the current. The details of the physical mechanism for a resistance switching phenomenon in metal–oxide memory are still an active research area. Here we aim to give a broad overview for simple binary metal–oxide RRAM.

A. Forming/Set

The forming/set process for the fresh samples is interpreted to be a dielectric soft breakdown [27]. Statistical time-dependent dielectric breakdown (TDDB) measurements show the exponential dependence of forming time on applied voltage, confirming that forming process is not a spontaneous process at some critical voltage, but an upsurge process resulting from stress-induced defects [28]. Under the high electric field (> 10 MV/cm), the oxygen atoms are knocked out of the lattice, and drift toward the anode. Simultaneously, defects in the bulk oxide are generated. The localized deficiency of oxygen leads to the formation of CFs with either oxygen vacancies [29] or metal precipitates [30]. The localized CFs paths were observed in various metal–oxide RRAMs by conductive atomic force microscopy (C-AFM) confirming the filamentary conduction mechanism [31]–[34]. Usually the as-deposited RRAM oxide thin films are amorphous or polycrystalline, and the CFs are preferentially generated along the grain boundaries as revealed by C-AFM [35]. Recently, Kwon *et al.* [36] directly observed the nanoscale (< 10 nm in diameter) CFs with oxygen-deficient phase in TiO_x memory by imaging the cross-section image of the MIM structure by high-resolution transmission electron microscopy (HR-TEM).

In fresh samples, usually the amount of intrinsic defect is few, thus a high forming voltage is needed to initiate the switching. After the forming, a sufficient amount of defects is present. In the subsequent switching cycles, only a portion of the defects, the ones near one electrode, can be recovered during the reset process. This is why the set voltage is smaller than the forming voltage, and the resistance in HRS is much smaller than the resistance in the initial fresh samples. Often, the remaining defect-rich region is referred to as the "virtual electrode."

Obviously, it is not desirable to have a large forming voltage in practical applications. Thus, significant efforts have been made to achieve the so-called "forming-free" devices. It is found that the forming voltage is linearly dependent on the thickness of the oxide film [37]–[39]. So a thinner oxide film is effective for reducing the forming voltage. Lee *et al.* [37] showed that HfO_x memory is free from the forming process as the thickness of the film is reduced to 3 nm. Forming is also a strong function of film deposition conditions [40]. It was found that controlling the annealing ambient during deposition is also helpful in reducing the forming voltage [41]–[43], possibly due to the introduction of defects to make the films oxygen deficient.

B. Unipolar/Bipolar Reset

Although the forming/set mechanism appears to have a consensus as discussed above, the reset mechanism for different switching modes is a controversial topic. It seems that the thermal dissolution model [44] can explain parts of the unipolar switching characteristics, while the ionic migration model [45] can explain parts of the bipolar switching characteristics. However, a full physical

Table 1 The Switching Modes for Various Metal–Oxide RRAM Devices With Different Electrode Combination

Unipolar	Bipolar
Pt/NiO/Pt [7]	Pt/NiO/$SrRuO_3$ [54]
Pt/TiO_2/Pt [8]	Pt/TiO_2/TiN [55]
Pt/ZnO/Pt [18]	TiN/ZnO/Pt [56]
Pt/ZrO_2/Pt [57]	Ti/ZrO_2/Pt [57]
Pt/HfO_2/Pt [58]	TiN/HfO_2/Pt [59]
Pt/Al_2O_3/Ru [60]	Ti/Al_2O_3/Pt [61]

description of the two switching modes that can explain all the experimental observations is still incomplete for these models.

Experimental observations by various materials characterization techniques reveal that the oxygen migration is present in the switching process and plays an important role in both bipolar devices [46]–[49] and unipolar devices [50]. Electrothermal calculations suggest that the local temperature around the CFs would rise by several hundred Kelvin due to the large current flow [51]–[53], which may enhance the oxygen migration. In addition, it is found that the electrode materials have a significant effect on the switching modes of the metal–oxide memory. Table 1 summarizes the switching modes for various metal–oxide memories with different electrode combinations [7], [8], [18], [54]–[61]. Even with the same oxide material but with different electrode materials, the switching modes can be different. Therefore, it is inferred that the switching mode is not an intrinsic property of the oxide itself but a property of both the oxide material and electrode/oxide interfaces. In most cases, the unipolar mode is obtained with a noble metal such as Pt or Ru as both top and bottom electrodes. With one of the electrodes replaced by oxidizable materials such as Ti or TiN, the bipolar mode is obtained. Zhou *et al.* [62] performed TEM and Auger electron spectroscopy (AES) analyses on the depth profile of the CuO_x memory, and found the interfacial TaON layer may be responsible for the bipolar TaN/Cu_xO/Cu structure, while no interfacial oxide layer is found for the unipolar Pt/Cu_xO/Cu structure.

Based on the above observations, Yu *et al.* [63] proposed a unified reset mechanism for both unipolar/bipolar modes. Fig. 3 is a schematic illustration of switching processes. During the forming process, soft dielectric breakdown occurs and oxygen ions drift to the anode interface by the high electric field, where they are discharged as neutral nonlattice oxygen if the anode materials are noble metals or react with the oxidizable anode materials to form an interfacial oxide layer. Thus, the electrode/oxide interface behaves like an "oxygen reservoir" [64]. For a memory cell in the LRS, the current flows through the CFs in the bulk oxide. During the reset process, oxygen ions migrate back to the bulk either to recombine with the oxygen vacancies or to oxidize the metal precipitates and return the memory cell to the HRS. For devices that switch in the unipolar mode, Joule heating from the current thermally activates the diffusion of oxygen ions. Oxygen ions diffuse from the interface or the region around the CFs [65] due to the concentration gradient, thus usually the unipolar switching mode requires a relatively higher reset current to raise the

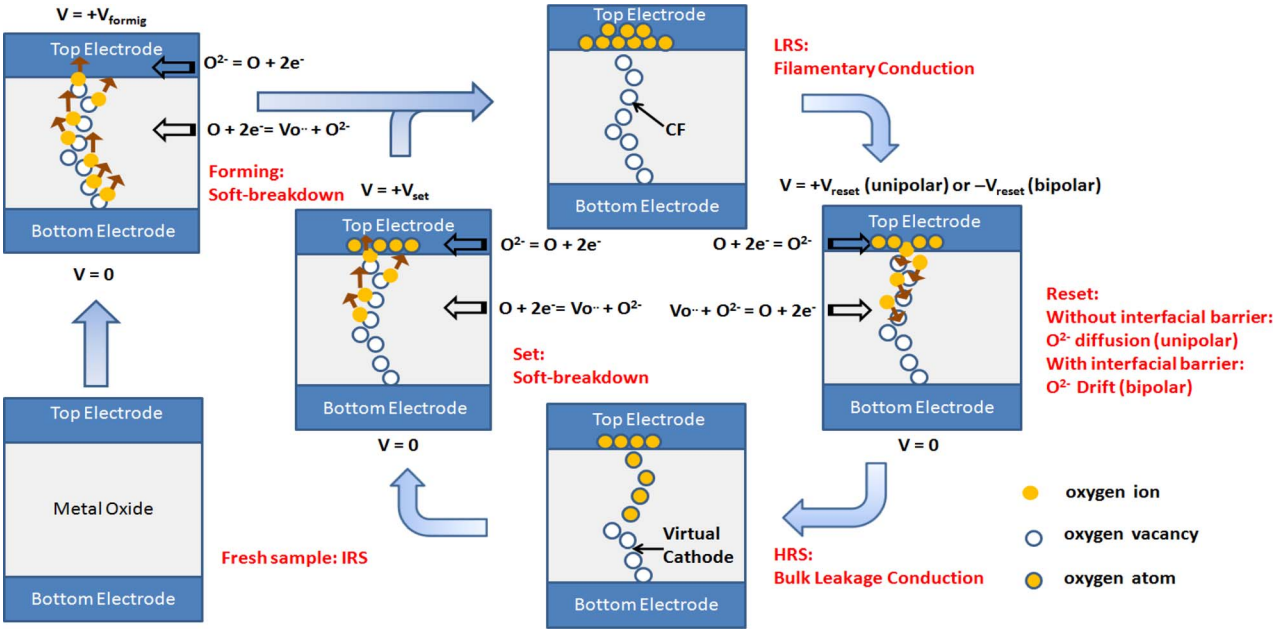
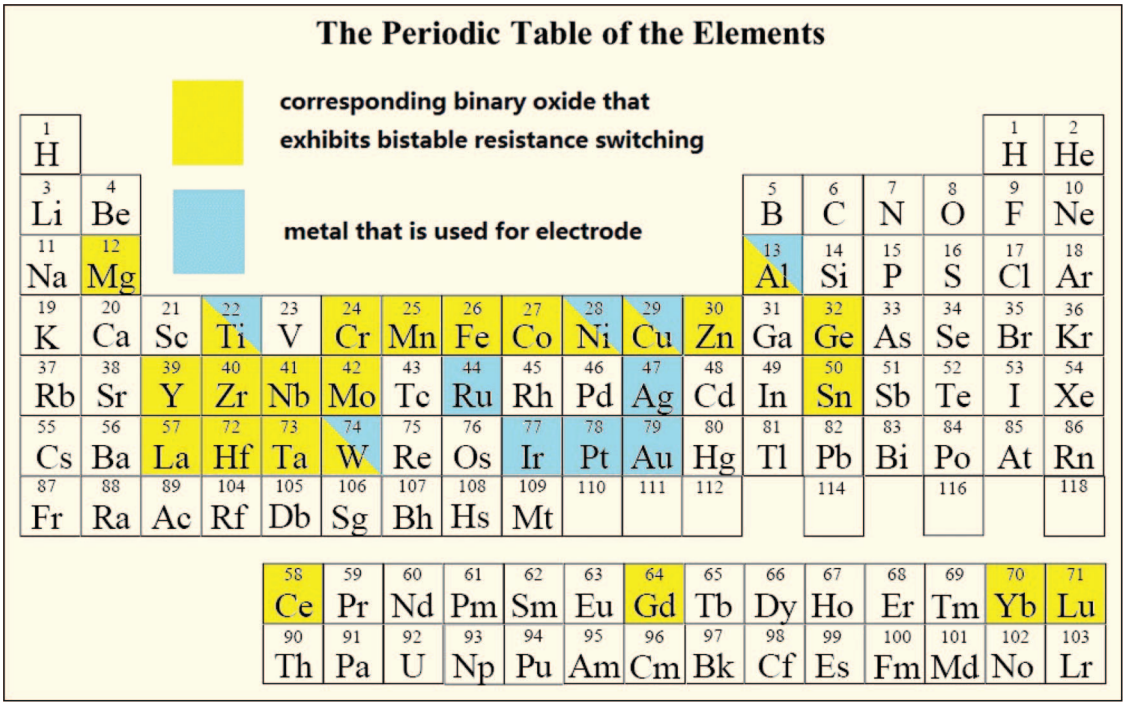


Fig. 3. *Schematic illustration of the switching process in the simple binary metal–oxide RRAM. Adapted from [68].*

Table 2 Summary of the Materials That Have Been Used for Binary Metal–Oxide RRAM. Metals of the Corresponding Binary Oxides Used for the Resistive Switching Layer Are Colored in Yellow. Metals Used for the Electrodes Are Colored in Blue. Adapted From [68]



local temperature around CFs. For devices that switch in the bipolar mode, the interfacial oxide layer may present a significant diffusion barrier, and pure thermal diffusion is not sufficient, thus oxygen ions migration needs to be aided by the reverse electric field. The physical picture presented here combines the previous thermal model [44] and ionic migration model [45]. This picture can at best be viewed as a phenomenological description of the above experimental observations for the binary metal–oxide RRAM. Details of the physics of switching remain an area of active research. Alternative theories have been proposed, such as those by Strukov *et al.* [66] and Yang *et al.* [67].

III. MATERIAL AND DEVICE PROPERTIES

Plenty of binary metal oxides have been found to exhibit resistive switching behavior. Most of them are transition metal oxides, and some are lanthanide series metal oxides. The materials for the resistive switching oxide layer and the electrodes are summarized in Table 2. Note that some conductive nitrides, e.g., TiN and TaN, are also used as electrode materials. Among various oxides, CuO_x [69], [70] and WO_x [71], are most compatible with the conventional CMOS process because a simple additional oxidation step of the Cu or W via/plug is needed. Due to the limited space, we will not discuss them. Here we choose HfO_x, AlO_x, NiO_x, TiO_x, and TaO_x, because they have drawn most attention and have been extensively studied in the past several years. The properties of the devices based on these oxides are discussed in the following sections. The deposition methods of these binary metal oxides usually include the oxidation of a corresponding metal, reactive sputtering, pulse laser deposition (PLD), and atomic layer deposition (ALD). Among these methods, ALD is recently widely used due to the ability to precisely control the thickness and uniformity of the thin film.

A. Hafium Oxide (HfO_x)

HfO_x-based materials have been employed as a high-k dielectric for the gate insulator for high-performance CMOS MOSFETs [72]. Interestingly, defect-rich HfO_x is also a superior RRAM material. In the early stage of HfO_x memory exploration, the TiN/HfO_x/Pt structure [73] is usually employed to achieve the bipolar switching characteristics. In this structure, TiN acts as an oxygen reservoir. To make the fabrication process to be CMOS compatible (avoiding the uses of Pt since Pt is hard to etch), TiN/metal capping layer/HfO_x/Pt structure is used. The metal capping layer is inserted to deplete the O atoms from the HfO_x thin film and act as an oxygen reservoir. Lee *et al.* [37] adjusted the dielectric strength of HfO_x with a Ti capping layer by postdeposition annealing. In Fig. 4(a), a schematic diagram of a typical RRAM cell consisting of HfO_x film with a transistor as a current limiter (the 1T1R configuration) is illustrated. Fig. 4(b) shows the HR-TEM image of the stacked layers consisting of TiN/Ti/HfO_x/TiN. The typical I–V curve for the resistive switching of the device, including 1R and 1T1R configuration, is demonstrated in Fig. 5(a). The resultant bipolar HfO_x RRAM with

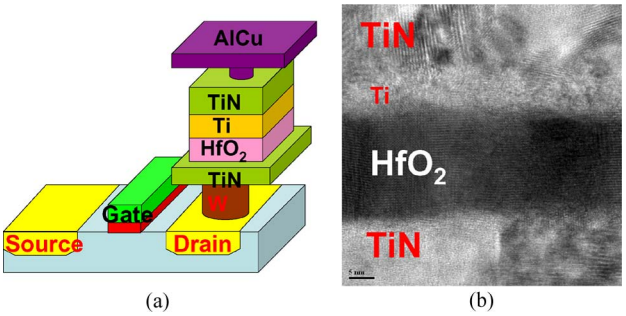


Fig. 4. *(a) A typical 1T1R structure of RRAM with HfO_x; (b) HR-TEM image of the TiN/Ti/HfO_x/TiN stacked layer; the thickness of the HfO_2 is 20 nm.*

high-speed operation (< 10 ns) has large ON/OFF ratio (> 100), reliable switching endurance [> 10^6 cycles; Fig. 5(b)], long high-temperature lifetime, multibit storage, and high device yield (~100%). The same group also used AlCu and Ta as the capping layer for the HfO_x memory. These devices also show stable bipolar resistance switching but they have a small ON/OFF ratio (~4) [22]; the oxygen capture ability of the capping metal layer may be responsible for these results. With an ultrathin HfO_x (3 nm), the Ti/HfO_x stack after a postmetal anneal exhibits forming-free characteristics [37]. Recently, Govoreanu *et al.* [74] reported excellent performances for a 10-nm × 10-nm TiN/Hf/HfO_x/TiN RRAM stack with Hf as the capping layer. So far, HfO_x is one of the most mature RRAM materials explored.

B. Aluminum Oxide (AlO_x)

The first observation of negative resistance phenomenon of anodic AlO_x can be traced back several years ago to the report by Hickmott [1]. AlO_x memory behaves in a way similar to HfO_x memory in many characteristics. In addition, AlO_x is of interest because of the lower reset current, possibly due to a large band gap (~8.9 eV). Most RRAM devices reported in the early literatures show typical switching current in the order of mA or hundreds of μA. Wu *et al.* [75] first demonstrated low reset current down to ~1 μA in Al/AlO_x/Pt stack. Recently, Kim *et al.* [76] doped the AlO_x with nitrogen and achieved even lower reset current (< 100 nA). The low power/energy consumption of AlO_x memory is attractive. Furthermore, the low reset current leads to LRS resistance above MΩ. The higher LRS resistance can potentially enable ultralarge-scale memory arrays without selection devices because the sneak leakage currents are significantly reduced due to the high LRS resistance [77].

AlO_x can also be stacked with other RRAM materials to improve the uniformity of the device characteristics. Chen *et al.* [78] used an AlO_x buffer layer underneath the HfO_x resistive layer to enhance the READ disturb immunity. Yu *et al.* [79] utilized a bilayer HfO_x/AlO_x cell structure and obtained better switching uniformity than the pure HfO_x layer cells.

C. Nickel Oxide (NiO)

NiO is one of the earliest materials investigated for the RRAM application. It has been reported that various metals, such as Pt, Au, W, Ru, and Ni, can be used as the electrodes in the NiO memory. When using these metals as electrodes, NiO usually shows unipolar switching behavior. The reported reset voltages range from 0.5 to 2 V and reported set voltages range from 1 to 3 V after the forming process. Programming endurance has been demonstrated up to 10^6 cycles and retention time is larger than eight months [9] [Fig. 6(a) and (b)]. Previously, the reset current of NiO memory has been usually large (> mA), but recently reset current smaller than 10 μA has been reported [80] [Fig. 6(c)].

Due to the unipolar switching property, NiO allows for use of diode [Fig. 6(d)], instead of transistor, for selecting a memory cell in the memory array during WRITE and READ operations as the one-diode–one-resistor configuration (1D1R) [81]. However, because of the unipolar switching

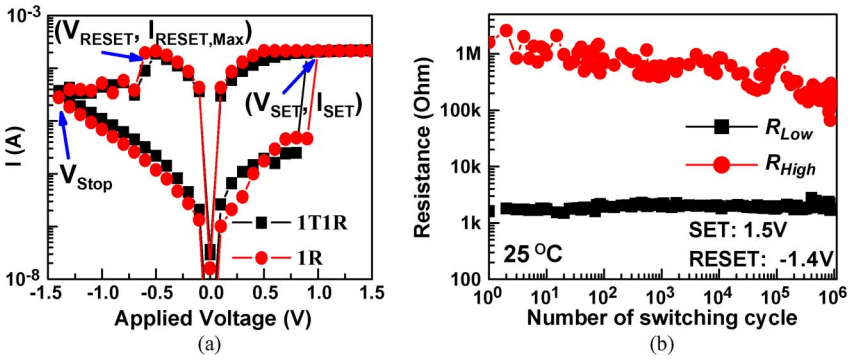


Fig. 5. *(a) Bipolar resistance switching characteristic of TiN/TiO_x/HfO_x/TiN device in 1R and 1T1R configuration. (b) Switch endurance of 10^6 cycles by 500-μs pulse. Reprinted from [37].*

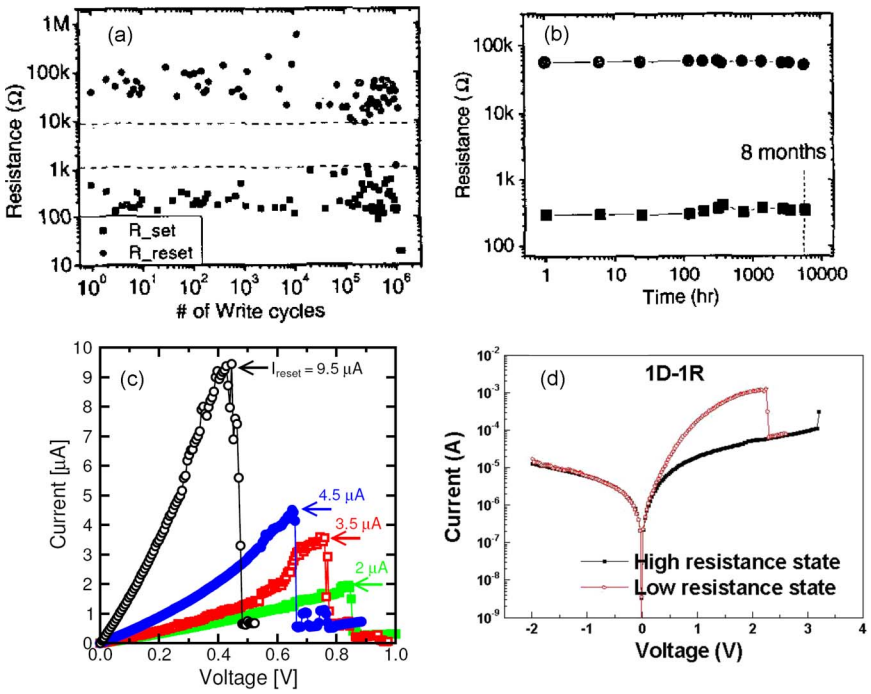


Fig. 6. *(a) Programming endurance data measured from a NiO memory demonstrating 10^6 cycles; adapted from [9]. (b) Retention of the two states (ON/OFF) measured from NiO for eight months; adapted from [9]. (c) Reset current as low as 2 μA with NiO; adapted from [80]. (d) I–V characteristics of a NiO memory cell in series with a diode; adapted from [81]. The leakage from the unselected memory cells can be suppressed by the reverse bias on the 1D1R stack.*

property for which the set and reset are the same voltage polarity, it is crucial to have narrow distributions of set and reset parameters. Poor switching uniformity is one of the well-known issues with NiO RRAM, which has to be overcome to achieve low failure rate and possible multilevel capability. Recent studies showed that the uniformity of NiO can be improved by using novel nanoscale CFs confined structures [82].

D. Titanium Oxide (TiO_x)

TiO_x is also one of the earliest materials investigated for the RRAM application. Although extensive studies have been carried out for TiO_x RRAM, most of these studies focused on investigating the switching mechanism and thus there is limited endurance and retention data in the literature. As noted before, Kwon *et al.* [36] directly observed the nanoscale CFs in TiO_x memory by HR-TEM, and identified the CFs composition to be the oxygen-deficient Magnéli phase, e.g., Ti_4O_7.

$Pt/TiO_2/Pt$ cell shows the typical unipolar switching behavior [8], [34], [83], [84]. In principle, bipolar reset can coexist in symmetric unipolar switching devices. However, the reset current for the unipolar reset is larger than that for the bipolar reset in $Pt/TiO_x/Pt$ cells [85], [86]. $Pt/TiO_x/TiN$ cell showed bipolar switching behavior as expected. Yet, the unipolar reset is still observable at the Pt/TiO_x interface [87]. Recently, the substoichiometric TiO_{2-x} layer has been deliberately stacked with the stoichiometric TiO_2 layer to form a bilayer structure. Yang *et al.* [67] fabricated 50-nm × 50-nm $Pt/TiO_2/TiO_{2-x}/Pt$ devices, which showed bipolar switching with set occurring under the negative bias on the top electrode. Strukov *et al.* [66] proposed that the switching mechanism of this device is due to the migration of the positive charged oxygen vacancies that push forward/backward the oxygen rich/poor region interface front. However, Do *et al.* [88] fabricated a similar $Pt/TiO_2/TiO_{2-x}/Pt$ cell structure, and found the bipolar switching direction is opposite with set occurring under a positive bias on the top electrode. At this point, there is no consensus on the switching mechanism for such oxygen-rich/oxygen-poor bilayer structure.

E. Tantalum Oxide (TaO_x)

TaO_x recently has drawn much attention due to good endurance. X-ray photoelectron spectroscopy (XPS) [89] and electron energy-loss spectroscopy (EELS) [90] reveal that TaO_x usually consists of two phases and oxygen migration exists between the two phases during the switching: one is closer to TaO_2 phase (more conducting), and the other is closer to Ta_2O_5 phase (more insulating). And TaO_2/Ta_2O_5 bilayer stack can be intentionally designed as RRAM stack [91]. Wei *et al.* [89] reported a pulse switching endurance ($> 10^9$ cycles) in TaO_x memory. Yang *et al.*

[92] reported a pulse switching endurance ($> 10^{10}$ cycles) in TaO_x memory. Lee *et al.* [91] reported a pulse switching endurance ($> 10^{12}$ cycles) in TaO_x memory. Such a long endurance capability enables RRAM devices to be used in embedded memory applications and potentially can make a change of the memory hierarchy.

IV. RRAM MEMORY ARRAYS

A. Cell Design

A filamentary RRAM device exhibits a characteristic of abrupt current increase during the forming/set process, when CFs are formed/reformed in the oxide matrix. Therefore, a current limiter, which can optimally clamp the forming/set current, is necessary for the filamentary switching device to prevent the degradation of HRS and even the failure of the memory device [37], [93], [94]. Due to the benefits of fast response time and very large resistance at the saturation region, a transistor is a better current limiter than an external electrical measurement instrument [37], [93]. Special consideration must be taken in the design of memory cell of 1T1R structure to avoid having a large parasitic capacitance between the transistor and the RRAM. The parasitic capacitance causes overshoot current during the forming/set process which in turn increases the reset current [37], [93]. Specifically, during the forming/set process, the RRAM resistance changes instantly while the voltage drop across the RRAM cannot drop instantly due to the presence of parasitic capacitance. Therefore, during the overshoot period that the voltage across the RRAM gradually decreases, excessive oxygen vacancies form and the CFs tend to grow laterally and increase in diameter or multiple CFs can be generated. Fig. 7 shows that the 1T1R configuration can effectively limit the current overshoot. While this observation was investigated primarily for explaining the correlation between the reset current and the compliance current for directly probed RRAM, we note that the analogous situation of parasitic capacitance is present in a large memory array. The bit line capacitance plays the role of the parasitic capacitance in a large memory array with long bit lines. This is a direct result of the large resistance ratio and the high HRS resistance of RRAM.

Since the maximum reset current for the memory device is almost the same as the compliance current in the forming/set process, one can evaluate the degree of overshoot current in the memory cell by comparing the difference between the maximum reset current and nominal compliance current used in forming/set process: the greater is the current difference between the maximum reset current and the nominal compliance current, the larger is the overshoot current through the memory cell during the forming/set process [37], [43], [93], [94]. Gu *et al.* [94] reported that the device structure also plays a role in determining the overshoot current. The memory

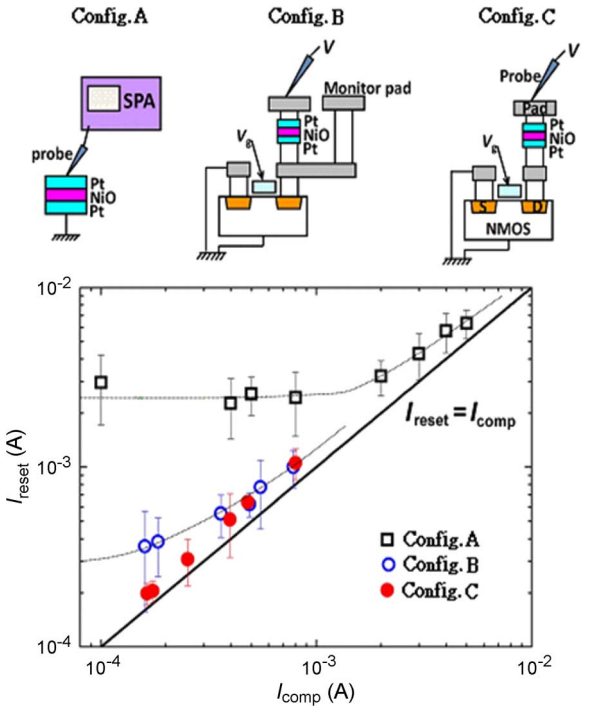


Fig. 7. *I_{reset} versus I_{comp} in various measurement configurations. Configuration A: 1R with semiconductor parameter analyzer. Configuration B: 1T1R with monitor pad. Configuration C: 1T1R. Adapted from [93].*

device with a concave structure, which has a large parasitic capacitance due to the supporting oxide, shows larger overshoot current than the ones with a pillar structure. The contact RRAM, which minimizes the parasitic capacitance from the interconnect between the transistor and the RRAM by fabricating the RRAM directly on the MOSFET's source/drain contact, can provide good current clamp in sub-100-μA region [95].

B. Process Technology

Although the preferred material for RRAM technology has not been determined yet, the fabrication process of the memory cell should be carefully controlled to prevent the aforementioned oxide layers from suffering process damage, such as plasma damages from the etching step and the deposition process. Avoiding the forming process, which needs voltage larger than the set process and increases testing time of the memory chip, is of great importance in the study of filamentary switching devices, as mentioned earlier. However, the methods for fabricating a forming-free device such as reducing oxide thickness may increase the initial defect density and also severely decrease the resistivity of the oxide layer and may decrease the resistance of HRS. Therefore, there is a compromise between the forming voltage and memory window. On the other hand, the metallic residue on the sidewall of the memory

cell, which leads to unwanted leakage path, should be avoided during the etching process [96].

Since the breakdown voltage of dielectrics depends on the number of defects rather than the defect density in the dielectric layer, the breakdown voltage increases with the decreasing device size and a linear correlation was found between the breakdown voltage and the device size in log–log scale [97], [98]. Because the forming process leads to oxide breakdown in the RRAM device, this linear correlation was also found between the forming voltage and the device size and can be used to monitor the fabrication process of the memory cell across a range of cell sizes. In the work of Gu *et al.* [95], as the device is scaled down to the nanoscale region, the sidewall reaction between the encapsulating low-temperature oxide and the Ti layer in the Ti/HfO_x memory becomes important and results in deviation of the forming voltage from the predicted value. An alternative low-temperature nitride encapsulating layer was proposed to suppress this sidewall reaction.

C. Memory Array

To effectively clamp the forming/set current, NOR-type memory array with 1T1R unit cell is preferred for a filamentary RRAM device. The NOR-type RRAM memory roughly includes the following components: memory array, word line decoder, bit line decoder, sense amplifier, output buffer, READ driver, and WRITE driver. Sato *et al.* [99] demonstrated that NiO unipolar RRAM with NOR-type memory array can have a unit cell as small as 6 F^2 in a 0.18-μm technology. They proposed a voltage-clamp transistor connected to 1T1R unit cell to stabilize the reset pulse operation without undesirable set. However, memory array of this device cannot be shrunk accordingly in the technology node beyond 90 nm. This is because the transistor in the column or source-selective gate should maintain the same size adopted in 0.18-μm technology node to sustain the set and reset voltages, which is around 2 V and cannot be reduced further. A unique circuit configuration, where each pair of source lines connects to each source-line selective gate, was proposed by the same group to allow the design of 6 F^2 unit cells in the 90-nm technology node [100]. NOR-type memory array with 1T1R unit cell is also adopted in bipolar RRAM [69], [89], [101], [102]. For example, Sheu *et al.* [102] demonstrated 4-Mb macrocircuit of HfO_x RRAM with < 10-ns WRITE/READ time using 0.18-μm technology. However, considering the shrinkage of memory array size, the bipolar RRAM, where both bit line and source line need to deliver the voltage signal, is less competitive than unipolar RRAM one. In order to reduce the bit cost of bipolar RRAM, vertical bipolar junction transistor (BJT) has been proposed to replace the planar MOSFET as the selection device [103].

To be implemented in the 3-D stacking memory in a cross-point architecture, usually a memory cell selection device is needed at each crosspoint. For this purpose, a 1D1R configuration is needed. The traditional single-crystalline silicon p/n diode is not compatible with the BEOL low-temperature processing. For the unipolar RRAM, several oxide-based diodes with large ON/OFF ratio have been demonstrated, such as NiO_x/TiO_x [10] and $CuO_x/InZnO_x$ [81]. With GaInZnO peripheral thin-film transistor and $CuO_x/InZnO_x$ diode, Lee *et al.* realized all oxide 3-D RRAM [104]. Tallarida *et al.* [105] showed a Schottky diode (Ag/ZnO/TiAu) using ZnO. For the bipolar RRAM, a bidirectional diode, which provides large ON/OFF current for both voltage polarities, is necessary. Huang *et al.* [106] showed a 1D1R stack (Ni/TiO_x/Ni/HfO_x/Pt) using HfO_x as memory cell and Ni/TiO_x/Ni as bidirectional diode with current density 10^5 A/cm^2. Recently, Kawahara *et al.* [107] showed a 1D1R stack (Ir/Ta_2O_5/TaO_2/TaN/SiN_x/TaN) using TaO_x as memory cell and TaN/SiN_x/TaN as bidirectional diode with current density 10^5 A/cm^2, and based on this structure, they demonstrated a 8-Mb macrocircuit with < 25-ns WRITE/READ time using 0.18-μm technology. However, the current densities of these oxide diodes currently are not large enough to program RRAM at sub-30-nm dimensions. For example, assuming a 20-nm × 20-nm RRAM with a 5-μA reset current, it requires a cell selection device that can deliver current density at 1.25 MA/cm^2. The oxide diodes demonstrated so far can provide large enough current to program the RRAM only because the device areas were large. Besides diodes, a device that shows a threshold switching can also serve as the selector. For example, Lee *et al.* [108] proposed using VO_2 as a selection device, utilizing its metal–insulator–transition (MIT) property. However, the threshold voltage of MIT in VO_2 strongly depends on the temperature, which rapidly drops to zero when temperature rises to around 67 °C [109], [110]. Therefore, the thermal instability is a major barrier for VO_2 for practical applications. Kau *et al.* [111] used ovonic threshold switch (OTS) and achieved 10^6 ON/OFF ratio. Gopalakrishnan *et al.* demonstrated mixed ionic electronic conduction (MIEC)-material-based bidirectional diode with 10^7 ON/OFF ratio and 15 MA/cm^2 ON current [112]. Table 3 summarizes the memory cell selection device published in the literature. It should be pointed out that there needs to be a balance between the conductivity of the nonlinear element such as the diode and the conductivity of the RRAM itself. A highly resistive nonlinear element as compared to the RRAM LRS resistance will reduce the resistance window of HRS and LRS since most of the applied voltage will be dropped across the nonlinear element. On the other hand, a nonlinear element that is too conductive as compared to the RRAM LRS resistance will not be an effective current limiter.

For cross-point memory array without the selection device, a large nonlinearity in the *I–V* characteristics of the RRAM itself is needed to mitigate the leakage current of the array [77]. For example, the CMO_x, where both LRS and HRS are characteristic of a nonlinear *I–V* curve with very large current ratio between WRITE and READ operations, can

Table 3 Memory Cell Selection Device Published in the Literature. Adapted From [113] and Updated With Recent Experimental Results

Selector type	Material	Voltage range*	On-current	On/off ratio#	Reference
PN junction diode	polySi	+/- 2V	8 MA/cm^2	8 x 10^4	Y. Sasago et al. Symp. VLSI Tech. 2009
PN junction diode	Epitaxial Si	+/- 1.8V	28 MA/cm^2	10^8	J.H. Oh et al. IEDM 2006
PN junction diode	p-CuO_x/n-$InZnO_x$	+/- 2V	3x10^4 A/cm^2	3x10^4	M.J. Lee et al. IEDM 2007
PN junction diode	p-NiO/n-TiO_2	+/- 3V	20A/cm^2	1x10^4	I.G. Baek et al. IEDM 2005
PN jucntion diode	n-Ge nanowire / p-Si	+/- 4V	10^5-10^6 A/cm^2	50	S. Kim et al. Trans. Elec. Dev. 2008
Schottky diode	Ag/ZnO/TiAu	+/- 2V	10^4 A/cm^2	10^8	G. Tallarida et al. IMW 2009
Schottky diode	Ni/TiO_x/Ni	+/- 4V bidirectional	10^5 A/cm^2	50 @ half Vdd	Huang et al. IEDM 2011
Schottky diode	TaN/SiN_x/TaN	+/- 2V bidirectional	10^5 A/cm^2	150 @ half Vdd	Kawahara et al. ISSCC 2012
Metal-insulator-transition (MIT)	Pt/VO_2/Pt	0.4V / 0.6V	400A/cm^2	10^3	M.-J. Lee et al. Adv. Mater. 2007
Ovonic threshold switch (OTS)	chalcogenide alloy (undisclosed)	N/A	N/A	10^6	D. Kau et al. IEDM 2009
Mixed Ionic Electronic Conduction (MIEC)	Cu-containing MIEC	~1.6V	15 MA/cm^2	10^7	K. Gopalakrishnan et al. Symp. VLSI Tech. 2010

be implemented in cross-point array without diode as the selection device [114], [115]. A 64-Mb CMO_x chip with 0.5-F^2 effective bit size has been realized in 0.13-μm technology node by using four-layer cross-point array. A general analysis of the maximum allowable memory array size for memory cells with highly nonlinear I–V curves, as noted above, is given by Liang *et al.* [77].

V. KEY DEVICE PERFORMANCE METRICS

A. Uniformity

Poor uniformity of device characteristics is a major barrier to large-scale manufacturing of RRAM. Significant parameter fluctuations exist in terms of variations of the switching voltages as well as the resistances in HRS and LRS. The variations of the resistance switching include temporal fluctuations (cycle to cycle) and spatial fluctuations (device to device). The origin of the variations may be attributed to the stochastic nature of the oxygen vacancies/ions processes, as discussed in [116]. The LRS resistance variation comes from the variation of the number or the size of CFs, thus the reduction of possible filament paths effectively confines the active switching area and thereby may reduce the LRS variation. The HRS resistance variation comes from the variation of the ruptured CFs length, thus any small variation of the tunneling gap distance may be magnified to be an exponential dependence of the tunneling current on the tunneling distance. Therefore, the HRS variation is a more severe problem. It is found that the tail bits of the HRS variation correspond to a CF configuration with oxygen vacancies left over inside the tunneling gap region [116]. Essentially, the variation is an intrinsic property of metal–oxide RRAM associated with the stochastic atomic motion.

Many efforts have been expended to improve the uniformity, and various materials engineering methods have been explored. The first type of the methods is engineering the electrode/oxide interface by embedding appropriate buffer layers. Kim *et al.* [117] proposed to use IrO_2 as the top electrode for the NiO memory. Yu *et al.* [118] proposed to stack a thin Al buffer layer between TiN electrode and HfO_x bulk oxide for the HfO_x memory. The improvement of the set voltage distribution and resistance distribution is shown in Fig. 8. The second type of the methods is confining the CFs paths using the local electric field enhancement effect by inserting the seeds in the bulk oxide.

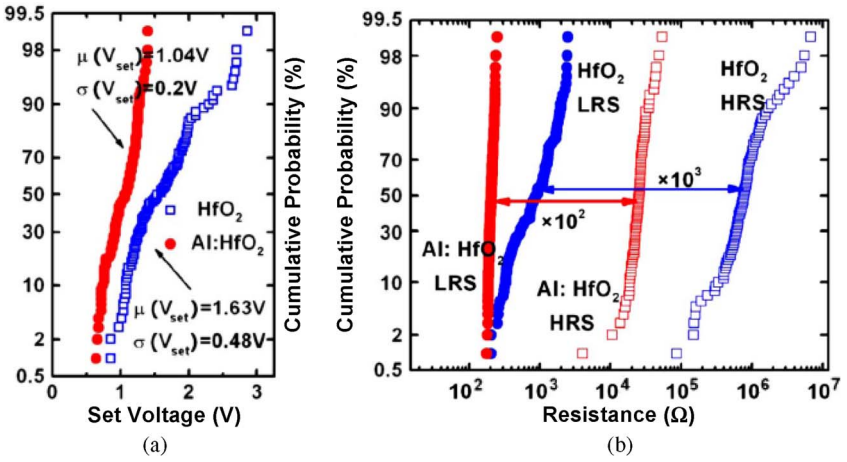


Fig. 8. ***Uniformity improvement of Al buffered HfO_x memory over pure HfO_x memory: (a) the statistical distribution of set voltages (V_{set}) obtained by 100 direct current (DC) sweep cycles; (b) the statistical distribution of resistances in HRS and LRS for 100 pulse sweep cycles. Adapted from [118].***

Chang *et al.* [119] proposed to embed Pt nanocrystals into the TiO_x memory. Liu *et al.* [120] proposed to implant Ti atoms into ZrO_x memory. The third type is to directly confine the region for the CFs paths by redesigning the cell structure or reducing the cell area. Lee *et al.* [82] placed the NiO layer on the sidewall between the top electrode and the bottom electrode in a cross-point architecture. The electric field is enhanced at the bottom corner of the top electrode and device uniformity is thus improved. Lee *et al.* [121] scaled down the cell size of ZrO_x/HfO_x bilayer memory devices to 50 nm. Compared with the large-size devices, these devices showed a remarkable improvement of the uniformity not only in cycle-to-cycle testing but also in device-to-device measurements across the wafer. Chang *et al.* [122] fabricated vertically aligned ZnO nanorod memory devices with the purpose of forming straight and extensible CFs along the direction of each single nanorod.

Besides the materials engineering approaches above, novel programming methods are also helpful in reducing parameter fluctuations. Two effective verification techniques are carried out to tighten the distributions of HRS and LRS in [78]. By ramping up the reset voltage (V_{RESET}), the HRS can be increased to acceptable resistance levels. However, to constrain the LRS values to certain range, a higher set voltage (V_{SET}) must be applied to the device after reset, since in this way a stronger filament might be formed. The above HRS verification method is also demonstrated in [123] for CuO_x memory. Using multiple pulses rather than a single pulse [124] or using a ramped series of pulses [123] can also improve the cycle-to-cycle uniformity.

B. Endurance

Generally, the WRITE endurance cycles of RRAM depend on a variety of factors: material, processing, device structure, operation scheme. During the cycling, in general, the HRS resistance tends to decrease, and usually the final failure state of RRAM cells is stuck with LRS and unable to reset back to HRS. This can be caused by too many defects such as oxygen vacancies accumulated during the cycling in a number of ways: 1) too many oxygen vacancies generated at or near the electrode–oxide interface; 2) too many oxygen vacancies in or near the filament; 3) too many oxygen vacancies in the oxide matrix. It is also noticed that during the cycling, sometimes there is a worn phase of LRS where LRS tends to increase, which may be caused by a formation of interfacial oxide layer between the electrode and the oxide [125], [126]. The oxygen vacancy accumulation is best mitigated by a verified reset operation as in [78], which effectively puts oxygen back into the RRAM switching region, in a well-monitored fashion. However, care must be taken not to overuse the verified reset operation, because over-reset CFs become difficult to set, if they are shunted by filaments or areas surrounding them which contain more oxygen vacancies [125]. This nonuniformity of the oxygen vacancy distribution is aggravated by the electric field nonuniformity arising from the roughness of the bottom electrode. To address this problem, Lee *et al.* [125] use chemical mechanical polishing (CMP) to flatten the memory bottom electrode and demonstrated HfO_x memory with endurance cycles over 10^{10} using 40-ns WRITE/ERASE pulses while maintaining a resistance ratio of around 20, which greatly improves the endurance property compared to their earlier work without CMP [37].

C. Retention

A data retention time longer than ten years is expected for nonvolatile memory. This retention must be maintained at thermal stress up to 85 °C (operating temperature) and small electrical stress such as a constant stream

of READ pulses. However, the combination of the requirements on memory WRITE speed (∼10 ns) and retention time (∼10^8 s) sets a voltage-time dilemma, discussed in [12], which suggests that a physical mechanism that has a large nonlinearity of the order of 10^{16} is required. Clearly, a thorough understanding of the physical mechanism of resistive switching is required to make reliable retention projections. The voltage-time dilemma may be resolved by the hyperbolic–sinusoidal ("sinh") dependence of oxygen vacancies/ions drift velocity on the electric field [63]. It was also experimentally observed that the switching time for both set and reset transitions (in the range from ∼ns to ∼ms) decreases exponentially when the programming voltage amplitudes are linearly increased [127], [128].

One common extrapolation method in the literature is to take the devices to a high temperature, and monitor the device's resistance by applying READ pulses at certain time intervals, e.g., every 1 s, and extrapolate the resistance evolution line to the ten-year point. However, this method, while easy to implement in an industrial test setting, has its limitation, because although the RRAM can maintain the resistance window over 10^4 or 10^5 s (the time interval that is convenient for testing), it cannot be guaranteed that the resistance window is still adequate after 10^6 or 10^7 s because it is often observed that the resistance window would collapse abruptly rather than gradually [129]. Also in this method, the READ voltage stress is applied to the cell during the retention test. To minimize the effect of the READ voltage stress, another often used method is to bake the device at elevated temperatures for an extended period and then read out the resistances at specific times (after cool-down), e.g., 24 h, 100 h, and so on. An alternative method is the temperature-accelerated method by varying the temperature to record the time-to-failure and draw the Arrhenius plot to extract the activation energy, and then extrapolate down to the operating temperature. In this method, one has to wait until the failure occurs, thus it is more time consuming and expensive. The activation energy extracted for TaO_x memory is 1.2 eV [20], and for HfO_x memory, it is 1.9 eV [129]. It should be mentioned that realistic statistics on retention property can only be collected on large memory arrays and the tail bits of the failure time distribution become the limiting factor for the whole array [130].

D. Multibit Operation

Among all memory characteristics, the so-called multibit operation or multilevel cell (MLC), which exploits the layout area of a memory device to realize more than one bit of digital data per cell, is a desirable capability for high-density memory application. RRAM modulates the resistance states to realize the MLC operation. As shown in Fig. 9, the LRS resistance can be changed by the set current compliance possibly due to the modulation of the diameter or number of CFs, while the HRS resistance can be controlled by the reset stop voltage possibly due to the modulation of the ruptured CF length [37]. In addition, for LRS, the current is clamped by the measurement instrument for the 1R device or by the gate voltage of the transistor for the 1T1R device. Therefore, minimizing the overshoot is crucial for achieving multilevel states in LRS. For a memory array, the current clamping must be provided by on-chip circuits. Most RRAM material systems, such as CuO_x [131], TiO_x [55], HfO_x [37], WO_x [132], and TaO_x [133], were reported to be capable of MLC operation. The largest number of resistance levels reported so far are five levels without verification for the HfO_x memory [37] and eight levels with verification for the WO_x memory [132]. Recently, Yu *et al.* [127] proposed and verified two equivalent pulse programming schemes to achieve the multilevel resistance values owing to the exponential voltage–time relationship: one is to exponentially increase the programming pulse width; the other is to linearly increase the programming pulse amplitude. Although both schemes were effective for achieving the target resistance, the transient current response measurements suggest the second scheme consumes considerably less energy for the programming.

For MLC operation, first, enough resistance window between any two states and the uniformity of each

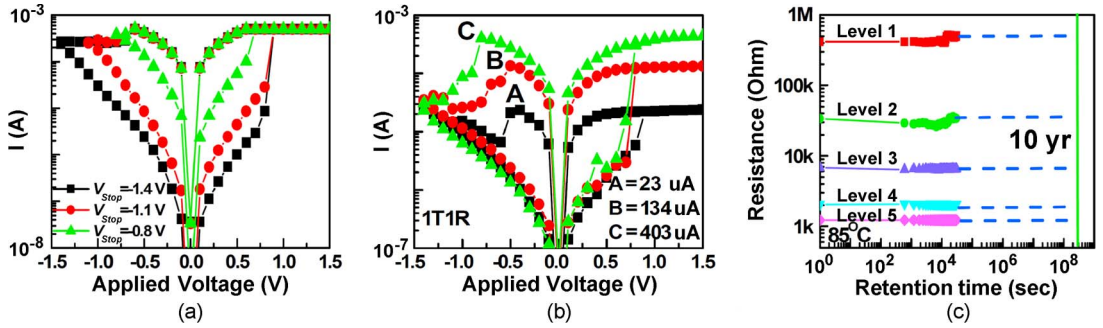


Fig. 9. *Multilevel characteristic for a TiN/TiO_x/HfO_x/TiN RRAM: (a) multilevel R_{High} is obtained by controlling V_{Stop} and (b) multilevel R_{Low} is obtained by controlling I_{Set}. (c) The retention of multilevel resistance values extrapolated to ten years at 85 °C. Adapted from [37].*

resistance state are required. Second, the cycling endurance for each state is also an important criterion. This was investigated for the WO_x memory in [132] and [134]. Without verification, only four levels were obtained and the endurance did not exceed 100 cycles [134]. However, when verification is employed, the eight-level resistance states were possible and the endurance of each state was more than 8000 cycles [132]. Third, the thermal stability of the stored data in each state is also important for the MLC operation. For HfO_x memory [37], [133], a four-level cell remains stable for 3×10^4 s above 85 °C. Last, the READ disturbance test of each resistance state must be considered. Good immunity of READ disturbance for four resistance states in HfO_x memory was demonstrated for total READ stress of 2×10^4 s (20 ms READ for 10^6 cycles) in [70].

As described earlier, verification can help improve the uniformity of the two basic resistance states (HRS and LRS) within an array. This can also be applied in the case of MLC [102]. Fig. 10 shows the effect of successively ramping up the compliance current (determined by word line voltage for 1T1R configuration) to the desired level. As the compliance current is ramped up, the resistance is decreased further. In the event that an excessively low resistance occurs, a reset operation is performed and the compliance current ramp is reattempted to achieve the target resistance.

E. Scaling Trends

The potential scalability to the nanometer regime is one of the key motivations that push the development of metal–oxide RRAM technology. Lee *et al.* [50] triggered the localized switching events successfully in NiO memory by manipulating the C-AFM, thus showing that the size of CF can be lower than 10 nm. Therefore, in principle, metal–oxide memory can potentially scale to sub-10 nm dimensions. In recent years, more and more metal–oxide memory devices with sub-100-nm feature size have been fabricated either by optical lithography [43], [95], nanoimprint lithography [67], [135], or e-beam lithography [82]. Chen *et al.* [78] scaled down the HfO_x memory device size to 30 nm, and demonstrated a 1-kb array with good yield. Recently, Govoreanu *et al.* [74] aggressively scaled down the HfO_x memory device size to 10 nm × 10 nm, while retained the good performances. Besides the conventional top-down fabrication approach, the self-assembly grown metal–oxide nanowires were able to exhibit the resistive switching behavior [136]–[138], further illustrating the scalability of RRAM to the nanometer regime.

The scaling trends of the RRAM device parameters are examined next. Fig. 11 plots the general scaling trend of HRS and LRS from various metal–oxide memories. The resistance of HRS increases as the inverse of the cell area, roughly following the Ohm's law. The conduction current in the LRS is mainly filamentary conduction current, as discussed before. So the resistance of LRS has only a slight

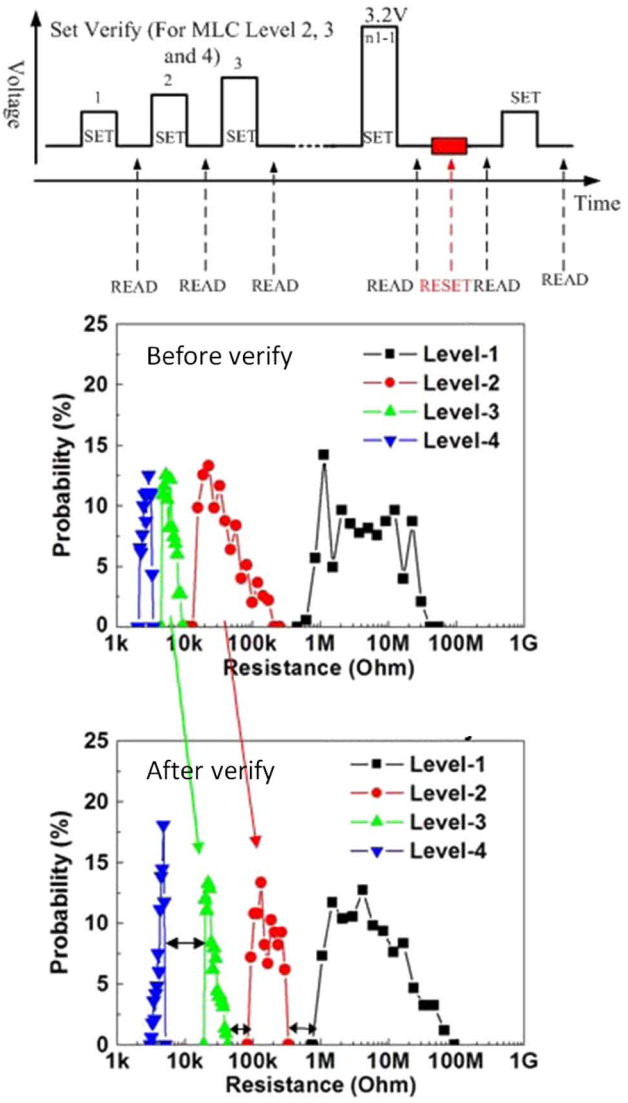


Fig. 10. ***MLC verification for HfO_x RRAM array. The verify scheme consists of ramping up the gate voltage (compliance current), but applying a reset and repeating reramping in order to avoid excessively low resistance. The desired outcome after verification is shown at the bottom. Adapted from [102].***

dependency on the cell area. This trend of increasing HRS/LRS resistance ratio as cell area decreases is a benefit of device scaling.

The peak current during the reset process (defined as the reset current) is another parameter of concern because the peak power consumption is mostly determined by the reset current. Most reports in the literature show a typical reset current for a single memory cell on the order of mA or hundreds of μA. Fig. 12 plots the general scaling trend of reset current and corresponding reset current density for unipolar NiO memory [9] and bipolar HfO_x memory [37]. It is seen that the reset current reduces only slightly when the devices are scaled down, thus leading to a

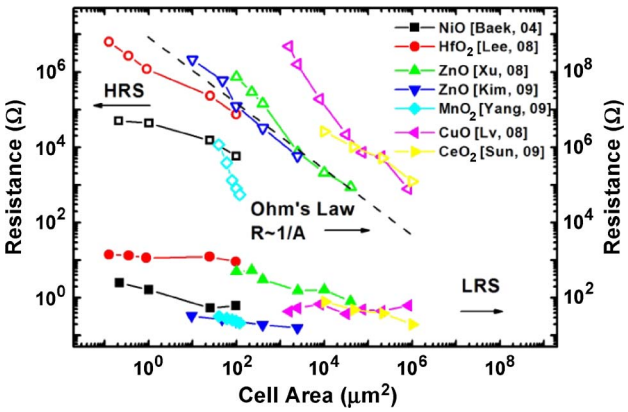


Fig. 11. *HRS and LRS resistance versus cell area of metal–oxide RRAM devices. Data were from [9], [37], [139], [140], [47], [141], and [142].*

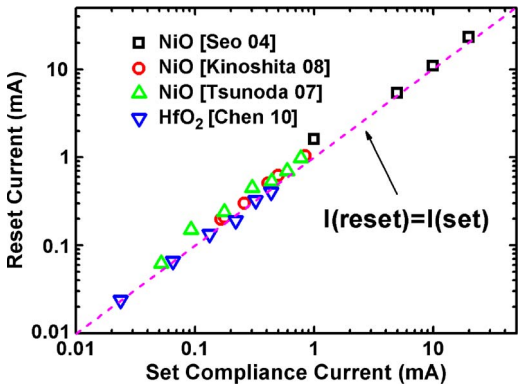


Fig. 13. *The reset current versus set compliance current. Data are collected from [7], [93], [146], and [147].*

remarkable increase of the current density required for reset. This apparently presents a significant challenge for the memory cell selection devices, which need to provide such a large current density for ultrascaled cells, e.g., $\sim 10^7$ A/cm^2 even for a relatively large 100-nm $\times$ 100-nm cell.

However, this apparent problem can be alleviated by using a smaller set compliance current during the set process, because the reset current is almost linear with the set compliance current, as shown in Fig. 13. A possible reason for the linear correlation of set and reset current is that a smaller set compliance current leads to weaker CFs and those weaker CFs require a smaller reset current to rupture them. To ensure this linear relationship well into the μA regime, the parasitic capacitance should be minimized [93]. Sub-100-μA reset current has been successfully demonstrated in 1T1R cell structures by adjusting the selection transistor's gate voltage to deliver a small set compliance current [37], [69], [99], [145]. However, as a consequence of the smaller set compliance, the LRS resistance becomes higher. For a certain HRS resistance, the requirement for a sufficient resistance window limits the smallest set compliance that can be used. Fortunately, the HRS resistance rises up with the decrease of cell area, as mentioned before. This means that for the scaled-down memory cell, a higher LRS resistance can be tolerated, and a smaller set compliance can be utilized to achieve a lower reset current. In brief, the reset current does not depend on the cell area but depends on the set compliance current; and in smaller area cells, smaller set compliance can be used, therefore the reset current can scale down with device size. Capitalizing on this concept, Ahn *et al.* [143] used 5-μA set compliance in a 100-nm $\times$ 100-nm NiO memory cell, and obtained a 50-μA reset current (reset current density: 5×10^5 A/cm^2) with sufficient HRS/LRS ratio ($\sim 10^4$), and Wu *et al.* [144] used 5-μA set compliance in a 500-nm $\times$ 10-nm (using several carbon nanotubes as one of the electrodes) HfO_x memory cell, and obtained sub-5-μA reset current (reset current density: 10^5 A/cm^2) with reasonable HRS/LRS ratio ($\sim$10). However, such forward current density ($\sim 10^5$ A/cm^2) is still quite challenging for today's low-temperature grown diodes to be implemented in the 1D1R cross-point memory architecture.

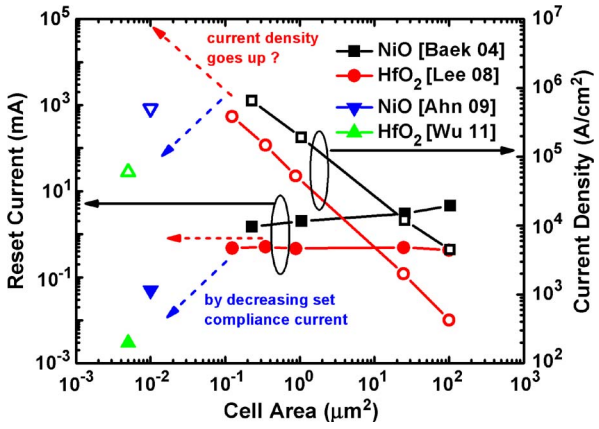


Fig. 12. *The peak value of reset current and corresponding current density versus cell area. Data are collected from [9], [37], [143], and [144]. Note that for the HfO_2 [37] data, the set compliance current was fixed at 500 μA, while for the NiO [9] data, the set compliance current changed from 200 to 20 μA as the cell area is scaled down. The HfO_2 data from [144] used a set compliance current of 5 μA. The NiO data from [143] also used a set compliance current of 5 μA.*

VI. FUTURE OUTLOOK

The development of metal–oxide RRAM has progressed rapidly in the last five years. In particular, binary metal oxides that use materials that are familiar to the semiconductor industry have seen intense research and development in both industry and academia. The vision for RRAM is a nonvolatile solid-state memory that is fast,

Table 4 A Representative List of Binary Metal–Oxide RRAM device characteristics. Data Are Collected From [9], [69], [146], [89], [37], [78], [71], [121], [76], [155], and [74]

	NiO IEDM 2004	Cu_xO IEDM 2005	Ti:NiO IEDM 2007	TaO_x IEDM 2008	Ti/HfO_x IEDM 2008	Ti/HfO_x IEDM 2009 &2010	WO_x IEDM 2010	ZrO_x/HfO_x IEDM 2010	$N:AlO_x$ VLSI 2011	TaO_x/Ta_2O_5 VLSI 2011	Hf/HfO_x IEDM 2011
switching type	unipolar	bipolar	unipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar
structure	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1R	1T-1R	1R	1T-1R
cell area (μm^2)	~0.2	~0.03	~0.49	~0.25	~0.1	0.0009 (30nm)	0.0036 (60nm)	0.0025 (50nm)	~1	~9000	0.0001 (10nm)
speed	~5µs	~50ns	~5ns	~10ns	~5ns	~0.3ns	~50ns	~40ns	N/A	~10ns	~10ns
peak voltage	<3V	<3V	<3V	<2V	<1.5V	<2.5V	<3V	<2V	<2V	<2.5V	<1.5V
peak current	~2mA	~45µA	~100µA	~170µA	~25µA	~200µA	~1mA	~50µA	~50nA	~30µA	~50 µA
HRS/LRS ratio	>10	>10	>90	>10	>100	>100	>10	>10	>100	>100	>10
endurance	10^6	600	100	10^9	10^6	10^{10}	10^6	10^6	10^5	10^{12}	$5x10^7$
retention	300h@ 150°C	30h@ 90°C	1000h@ 150°C	3000h@ 150°C	10h@ 200°C	28h@ 150°C	2000h@ 150°C	28h@ 125°C	28h@ 125°C	3h@ 200°C	30h@ 250°C

high-density, and compatible with integration with conventional Si CMOS technology. The early RRAM had large device areas, large programming currents (mA), long programming times (μs), low endurance ($< 10^3$ cycles), and requires a 1T1R structure which was limited in device density. Today, many of these deficiencies have been overcome. Table 4 summarizes some of the recent advances of RRAM reported in the literature. Device sizes down to 10 nm $\times$ 10 nm have been published, programming currents are now in the order of μA range, programming and READ speed are on the order of ns, endurance cycles are up to 10^{12}, retention time is up to 3000 h at 150 °C, and the forming process can be eliminated. Chip-scale memory arrays with megabit size were demonstrated. Demonstrations of multibit operation have been made, and rudimentary demonstration of integrated 1D1R-type devices for 3-D integration looks promising even though they do not meet all the requirements at this point. Meanwhile, further understanding of the underlying physics of RRAM has been obtained through modeling works from the atomistic level to the device level. For example, Park *et al.* [148] employed *ab initio* modeling techniques to study the oxygen vacancy's effect on the energy band diagram and electron density of states, and revealed that the ordering of oxygen vacancies into a filament would lead to substantial increase of the conductivity. Yu *et al.* [116] developed a Monte Carlo numerical simulator to quantify the electron conduction and the stochastic generation, recombination, and migration process of oxygen vacancies/ions during the switching. Simulations using this model empirically reproduced the experimentally observed abrupt set process, gradual reset process, current fluctuations, and switching parameter variations, and provided insights into the origin of the tail bits of the resistance distribution.

Since the device density is mostly determined by the memory cell selection device and not the memory cell itself, any expectations of device scalability and implementation of the cross-point architecture in a 3-D fashion necessarily need to ensure there is a scalable memory cell selection device that can provide the ON/OFF characteristics and device density commensurate with the RRAM programming requirement and 4-F^2 expectations. The challenge for a 3-D integrated RRAM is very much analogous to those faced by phase change memory (PCM) and is already discussed in [113] and not repeated here. Currently, the best RRAM device has a bipolar switching mode. This makes the search for a suitable cell selection device even more difficult (as compared to, say, PCM) as the selection device has to conduct current in both directions and the conventional reverse-bias blocking effect cannot be used. The major remaining challenge is device uniformity. Device variation is a major barrier for using the RRAM in large memory arrays as well as MLC operation. There is still substantial cycle-to-cycle variation as well as device-to-device variation of the device characteristics. To make progress in this area, it is necessary to have a more complete understanding of the conduction and resistive switching mechanism. In the end, the solution may come from a combination of materials engineering, device structure optimization, as well as innovations in addressing/readout circuitry.

While RRAM has the potential to be a standalone, high-capacity nonvolatile memory technology, it may be even more suitable for embedded applications. This is

because it offers the low programming voltage that FLASH does not offer and the nonvolatility that DRAM does not offer and yet has a speed that is comparable to DRAM. For embedded applications, the endurance cycles must be substantially improved. Novel applications that use RRAM as reconfigurable logic were also proposed. CMOS-nano hybrid reconfigurable field-programmable gate array (FPGA) architecture was designed [149] and 3-D FPGA based on RRAM was reported [150]. Another emerging application is using RRAM as artificial synapse element for hardware neuromorphic computing. Owing to RRAM's multilevel capability and low power/energy consumption, it can behave like an analog memory emulating the function of plastic synapses in a neural network. Recently, TiO_x- [151], WO_x- [152], and HfO_x-based [153] synapses have been demonstrated for spike timing-dependent plasticity [154] in the device level. Although the early vision for RRAM is to strive for a 4-F^2 cross-point architecture, with MLC and multiple 3-D integrated memory array layers, it is not entirely clear that these goals continue to make sense generally, given the many diverse potential applications of RRAM. For example, for embedded applications, improving other attributes of RRAM appears to be more important as far as research goals are concerned. And the ability to put an RRAM at the contact vias of the MOSFET without extensive process steps is an attractive device feature, especially for applications where only a low bit-count (memory capacity) embedded, multiple-time programmable, nonvolatile memory is required. As suggested in [113] and references therein, there is an enormous opportunity to completely rethink the design of the memory subsystem to gain orders of magnitude improvements in speed and/or power consumption. A revolution in the memory subsystem will bring about a fundamental change in how one can extract performance out of technology improvements. ■

REFERENCES

[1] T. W. Hickmott, "Low-frequency negative resistance in thin anodic oxide films," *J. Appl. Phys.*, vol. 33, 2669, 1962.

[2] J. F. Gibbons and W. E. Beadle, "Switching properties of thin NIO films," *Solid-State Electron.*, vol. 7, no. 11, pp. 785–790, 1964.

[3] G. Dearnale, A. M. Stoneham, and D. V. Morgan, "Electrical phenomena in amorphous oxide films," *Rep. Progr. Phys.*, vol. 33, 1129, 1970.

[4] J. G. Simmons, "Conduction in thin dielectric films," *J. Phys. D, Appl. Phys.*, vol. 4, 613, 1971.

[5] Y. Watanabe, J. G. Bednorz, A. Bietsch, Ch. Gerber, D. Widmer, A. Beck, and S. J. Wind, "Current-driven insulator-conductor transition and nonvolatile memory in chromium-doped SrTiO3 single crystals," *Appl. Phys. Lett.*, vol. 78, pp. 3738–3740, Jun. 4, 2001.

[6] A. Beck, J. G. Bednorz, C. Gerber, C. Rossel, and D. Widmer, "Reproducible switching effect in thin oxide films for memory applications," *Appl. Phys. Lett.*, vol. 77, pp. 139–141, 2000.

[7] S. Seo, M. J. Lee, D. H. Seo, E. J. Jeoung, D. S. Suh, Y. S. Joung, I. K. Yoo, I. R. Hwang, S. H. Kim, I. S. Byun, J. S. Kim, J. S. Choi, and B. H. Park, "Reproducible resistance switching in polycrystalline NiO films," *Appl. Phys. Lett.*, vol. 85, pp. 5655–5657, Dec. 2004.

[8] C. Rohde, B. J. Choi, D. S. Jeong, S. Choi, J. S. Zhao, and C. S. Hwang, "Identification of a determining parameter for resistive switching of TiO2 thin films," *Appl. Phys. Lett.*, vol. 86, 262907, Jun. 2005.

[9] I. G. Baek, M. S. Lee, S. Seo, M. J. Lee, D. H. Seo, D.-S. Suh, J. C. Park, S. O. Park, H. S. Kim, I. K. Yoo, U.-In. Chung, and J. T. Moon, "Highly scalable nonvolatile resistive memory using simple binary oxide driven by asymmetric unipolar voltage pulses," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2004, pp. 587–590.

[10] I. G. Baek, D. C. Kim, M. J. Lee, H.-J. Kim, E. K. Yim, M. S. Lee, J. E. Lee, S. E. Ahn, S. Seo, J. H. Lee, J. C. Park, Y. K. Cha, S. O. Park, H. S. Kim, I. K. Yoo, U.-In. Chung, J. T. Moon, and B. I. Ryu, "Multi-layer cross-point binary oxide resistive memory (OxRRAM) for post-NAND storage application," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2005, pp. 750–753.

[11] R. Waser, "Resistive non-volatile memory devices (Invited Paper)," *Microelectron. Eng.*, vol. 86, pp. 1925–1928, 2009.

[12] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories—Nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, pp. 2632–2663, 2009.

[13] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature Mater.*, vol. 6, pp. 833–840, 2007.

[14] A. Sawa, "Resistive switching in transition metal oxides," *Mater. Today*, vol. 11, pp. 28–36, 2008.

[15] H. Akinaga and H. Shima, "Resistive random access memory (ReRAM) based on metal oxides," *Proc. IEEE*, vol. 98, no. 12, pp. 2237–2251, Dec. 2010.

[16] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, "Electrochemical metallization memories—Fundamentals, applications, prospects," *Nanotechnology*, vol. 22, no. 25, 254003, 2011.

[17] Y. M. Kim and J. S. Lee, "Reproducible resistance switching characteristics of hafnium oxide-based nonvolatile memory devices," *J. Appl. Phys.*, vol. 104, pp. 114115-01–114115-06, Dec. 2008.

[18] W. Y. Chang, Y. C. Lai, T. B. Wu, S. F. Wang, F. Chen, and M. J. Tsai, "Unipolar resistive switching characteristics of ZnO thin films for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 92, 022110, Jan. 2008.

[19] C. Y. Lin, S. Y. Wang, D. Y. Lee, and T. Y. Tseng, "Electrical properties and fatigue behaviors of ZrO2 resistive switching thin films," *J. Electrochem. Soc.*, vol. 155, pp. H615–H619, 2008.

[20] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, T. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, and M. Oshima, "Highly reliable TaOx ReRAM and direct evidence of redox reaction mechanism," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2008, pp. 293–296.

[21] Q. Liu, W. H. Guan, S. B. Long, R. Jia, M. Liu, and J. N. Chen, "Resistive switching memory effect of ZrO2 films with Zr+ implanted," *Appl. Phys. Lett.*, vol. 92, 012117, Jan. 2008.

[22] H. Y. Lee, P.-S. Chen, T.-Y. Wu, Y. S. Chen, F. Chen, C.-C. Wang, P.-J. Tzeng, C. H. Lin, M.-J. Tsai, and C. Lien, "HfO_x bipolar resistive memory with robust endurance using AlCu as buffer electrode," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 703–705, Jul. 2009.

[23] S. Yu, X. Guan, and H. S. P. Wong, "Conduction mechanism of TiN/HfO(x)/Pt resistive switching memory: A trap-assisted-tunneling model," *Appl. Phys. Lett.*, vol. 99, 063507, Aug. 8, 2011.

[24] G. Bersuker, D. C. Gilmer, D. Veksler, P. Kirsch, L. Vandelli, A. Padovani, L. Larcher, K. McKenna, A. Shluger, V. Iglesias, M. Porti, and M. Nafria, "Metal oxide resistive memory switching mechanism based on conductive filament properties," *J. Appl. Phys.*, vol. 110, 124518, Dec. 15, 2011.

[25] S. Yu, R. Jeyasingh, Y. Wu, and H.-S. P. Wong, "Characterization of low-frequency noise in the resistive switching of transition metal oxide HfO2," *Phys. Rev. B*, vol. 85, 045324, 2012.

[26] S. Yu, R. Jeyasingh, Y. Wu, and H.-S. P. Wong, "AC conductance measurement and analysis of the conduction processes in HfOx based resistive switching memory," *Appl. Phys. Lett.*, vol. 99, 232105, Dec. 2011.

[27] N. Xu, L. F. Liu, X. Sun, X. Y. Liu, D. D. Han, Y. Wang, R. Q. Han, J. F. Kang, and B. Yu, "Characteristics and mechanism of conduction/set process in TiN/ZnO/Pt resistance switching random-access memories," *Appl. Phys. Lett.*, vol. 92, 232112, Jun. 2008.

[28] G. H. Buh, I. Hwang, and B. H. Park, "Time-dependent electroforming in NiO resistive switching devices," *Appl. Phys. Lett.*, vol. 95, 142101, Oct. 2009.

[29] M. Janousch, G. I. Meijer, U. Staub, B. Delley, S. F. Karg, and B. P. Andreasson, "Role of oxygen vacancies in Cr-doped SrTiO3 for resistance-change memory," *Adv. Mater.*, vol. 19, 2232–2235, Sep. 2007.

[30] G. S. Park, X. S. Li, D. C. Kim, R. J. Jung, M. J. Lee, and S. Seo, "Observation of

electric-field induced Ni filament channels in polycrystalline NiOx film," *Appl. Phys. Lett.*, vol. 91, 222103, Nov. 2007.

[31] J. Y. Son and Y. H. Shin, "Direct observation of conducting filaments on resistive switching of NiO thin films," *Appl. Phys. Lett.*, vol. 92, 222106, Jun. 2, 2008.

[32] K. Szot, W. Speier, G. Bihlmayer, and R. Waser, "Switching the electrical resistance of individual dislocations in single-crystalline SrTiO3," *Nature Mater.*, vol. 5, pp. 312–320, Apr. 2006.

[33] D. Lee, D. J. Seong, I. Jo, F. Xiang, R. Dong, S. Oh, and H. Hwang, "Resistance switching of copper doped MoOx films for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 90, 122104, Mar. 2007.

[34] B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, "Resistive switching mechanism of TiO2 thin films grown by atomic-layer deposition," *J. Appl. Phys.*, vol. 98, 033715, Aug. 2005.

[35] G. Bersuker, D. C. Gilmer, D. Veksler, J. Yum, H. Park, S. Lian, L. Vandelli, A. Padovani, L. Larcher, K. McKenna, A. Shluger, V. Iglesias, M. Porti, M. Nafria, W. Taylor, P. D. Kirsch, and R. Jammy, "Metal oxide RRAM switching mechanism based on conductive filament microscopic properties," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2010, pp. 456–459.

[36] D. H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X. S. Li, G. S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, "Atomic structure of conducting nanofilaments in TiO2 resistive switching memory," *Nature Nanotechnol.*, vol. 5, pp. 148–153, Feb. 2010.

[37] H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien, and M.-J. Tsai, "Low power and high speed bipolar switching with a thin reactive Ti buffer layer in robust HfO2 based RRAM," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2008, pp. 297–300.

[38] I. H. Inoue, S. Yasuda, H. Akinaga, and H. Takagi, "Nonpolar resistance switching of metal/binary-transition-metal oxides/metal sandwiches: Homogeneous/inhomogeneous transition of current distribution," *Phys. Rev. B*, vol. 77, 035105, Jan. 2008.

[39] C. Walczyk, C. Wenger, R. Sohal, M. Lukosius, A. Fox, J. Dabrowski, D. Wolansky, B. Tillack, H. J. Mussig, and T. Schroeder, "Pulse-induced low-power resistive switching in HfO2 metal-insulator-metal diodes for nonvolatile memory applications," *J. Appl. Phys.*, vol. 105, 114103, Jun. 2009.

[40] W. Wang, S. Fujita, and S. S. Wong, "Elimination of forming process for TiOx nonvolatile memory devices," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 763–765, Jul. 2009.

[41] W. Y. Chang, Y. T. Ho, T. C. Hsu, F. Chen, M. J. Tsai, and T. B. Wu, "Influence of crystalline constituent on resistive switching properties of TiO2 memory films," *Electrochem. Solid State Lett.*, vol. 12, pp. H135–H137, 2009.

[42] X. Cao, X. M. Li, X. D. Gao, W. D. Yu, X. J. Liu, Y. W. Zhang, L. D. Chen, and X. H. Cheng, "Forming-free colossal resistive switching effect in rare-earth-oxide Gd2O3 films for memristor applications," *J. Appl. Phys.*, vol. 106, 073723, Oct. 2009.

[43] L. Goux, J. G. Lisoni, X. P. Wang, M. Jurczak, and D. J. Wouters, "Optimized Ni oxidation in 80-nm contact holes for integration of forming-free and low-power Ni/NiO/Ni memory cells," *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2363–2368, Oct. 2009.

[44] U. Russo, D. Ielmini, C. Cagli, A. L. Lacaita, S. Spiga, C. Wiemer, M. Perego, and M. Fanciulli, "Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM," in *Proc. IEEE Int. Electron Devices Meeting*, 2007, pp. 775–778.

[45] B. Gao, S. Yu, N. Xu, L. F. Liu, B. Sun, X. Y. Liu, R. Q. Han, J. F. Kang, B. Yu, and Y. Y. Wang, "Oxide-based RRAM switching mechanism: A new ion-transport-recombination model," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2008, pp. 563–566.

[46] C. Yoshida, K. Kinoshita, T. Yamasaki, and Y. Sugiyama, "Direct observation of oxygen movement during resistance switching in NiO/Pt film," *Appl. Phys. Lett.*, vol. 93, 042106, Jul. 2008.

[47] M. K. Yang, J. W. Park, T. K. Ko, and J. K. Lee, "Bipolar resistive switching behavior in Ti/MnO2/Pt structure for nonvolatile memory devices," *Appl. Phys. Lett.*, vol. 95, 042105, Jul. 2009.

[48] H. Y. Jeong, J. Y. Lee, and S. Y. Choi, "Direct observation of microscopic change induced by oxygen vacancy drift in amorphous TiO2 thin films," *Appl. Phys. Lett.*, vol. 97, 042109, Jul. 2010.

[49] J. R. Jameson, Y. Fukuzumi, Z. Wang, P. Griffin, K. Tsunoda, G. I. Meijer, and Y. Nishi, "Field-programmable rectification in rutile TiO2 crystals," *Appl. Phys. Lett.*, vol. 91, pp. 112101–112101-3, 2007.

[50] M. J. Lee, S. Han, S. H. Jeon, B. H. Park, B. S. Kang, S. E. Ahn, K. H. Kim, C. B. Lee, C. J. Kim, I. K. Yoo, D. H. Seo, X. S. Li, J. B. Park, J. H. Lee, and Y. Park, "Electrical manipulation of nanofilaments in transition-metal oxides for resistance-based memory," *Nano Lett.*, vol. 9, pp. 1476–1481, Apr. 2009.

[51] Y. Sato, K. Kinoshita, M. Aoki, and Y. Sugiyama, "Consideration of switching mechanism of binary metal oxide resistive junctions using a thermal reaction model," *Appl. Phys. Lett.*, vol. 90, 033503, Jan. 2007.

[52] D. S. Jeong, B. J. Choi, and C. S. Hwang, "Study of the negative resistance phenomenon in transition metal oxide films from a statistical mechanics point of view," *J. Appl. Phys.*, vol. 100, 113724, Dec. 2006.

[53] U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, "Self-accelerated thermal dissolution model for reset programming in unipolar Resistive-Switching Memory (RRAM) devices," *IEEE Trans. Electron Devices*, vol. 56, no. 2, pp. 193–200, Feb. 2009.

[54] J. S. Choi, J. S. Kim, I. R. Hwang, S. H. Hong, S. H. Jeon, S. O. Kang, B. H. Park, D. C. Kim, M. J. Lee, and S. Seo, "Different resistance switching behaviors of NiO thin films deposited on Pt and SrRuO3 electrodes," *Appl. Phys. Lett.*, vol. 95, 022109, Jul. 2009.

[55] C. Yoshida, K. Tsunoda, H. Noshiro, and Y. Sugiyama, "High speed resistive switching in Pt/TiO2/TiN film for nonvolatile memory application," *Appl. Phys. Lett.*, vol. 91, 223510, Nov. 2007.

[56] N. Xu, L. F. Liu, X. Sun, C. Chen, Y. Wang, D. D. Han, X. Y. Liu, R. Q. Han, J. F. Kang, and B. Yu, "Bipolar switching behavior in TiN/ZnO/Pt resistive nonvolatile memory with fast switching and long retention," *Semicond. Sci. Technol.*, vol. 23, 075019, Jul. 2008.

[57] C. Y. Lin, C.-Y. Wu, C.-Y. Wu, T.-C. Lee, F.-L. Yang, C. Hu, and T.-Y. Tseng, "Effect of top electrode material on resistive switching properties of ZrO_2 film memory devices," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 366–368, May 2007.

[58] Y. M. Kim and J. S. Lee, "Reproducible resistance switching characteristics of hafnium oxide-based nonvolatile memory devices," *J. Appl. Phys.*, vol. 104, 114115, Dec. 2008.

[59] L. Goux, Y. Y. Chen, L. Pantisano, X. P. Wang, G. Groeseneken, M. Jurczak, and D. J. Wouters, "On the gradual unipolar and bipolar resistive switching of TiN\HfO2\Pt memory systems," *Electrochem. Solid State Lett.*, vol. 13, pp. G54–G56, 2010.

[60] K. M. Kim, B. J. Choi, B. W. Koo, S. Choi, D. S. Jeong, and C. S. Hwang, "Resistive switching in Pt/Al2O3/TiO2/Ru stacked structures," *Electrochem. Solid State Lett.*, vol. 9G343–G346, 2006.

[61] C. Y. Lin, C. Y. Wu, C. Hu, and T. Y. Tseng, "Bistable resistive switching in Al2O3 memory thin films," *J. Electrochem. Soc.*, vol. 154, pp. G189–G192, 2007.

[62] P. Zhou, M. Yin, H .J. Wan, H. B. Lu, T. A. Tang, and Y. Y. Lin, "Role of TaON interface for CuxO resistive switching memory based on a combined model," *Appl. Phys. Lett.*, vol. 94, 053510, Feb. 2009.

[63] S. Yu and H.-S. P. Wong, "A phenomenological model for the reset mechanism of metal oxide RRAM," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1455–1457, 2010.

[64] M. Fujimoto, H. Koyama, M. Konagai, Y. Hosoi, K. Ishihara, S. Ohnishi, and N. Awaya, "TiO2 anatase nanolayer on TiN thin film exhibiting high-speed bipolar resistive switching," *Appl. Phys. Lett.*, vol. 89, 223509, Nov. 2006.

[65] H. D. Lee, B. Magyari-Kope, and Y. Nishi, "Model of metallic filament formation and rupture in NiO for unipolar switching," *Phys. Rev. B*, vol. 81, 193202, May 2010.

[66] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, May 2008.

[67] J. J. Yang, M. D. Pickett, X. M. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nature Nanotechnol.*, vol. 3, pp. 429–433, Jul. 2008.

[68] S. Yu, B. Lee, and H.-S. P. Wong, "Metal oxide resistive switching memory," in *Functional Metal Oxide Nanostructures*. New York: Springer-Verlag, 2011.

[69] A. Chen, S. Haddad, Y.-C. Wu, T.-N. Fang, Z. Lan, S. Avanzino, S. Pangrle, M. Buynoski, M. Rathor, W. Cai, N. Tripsas, C. Bill, M. VanBuskirk, and M. Taguchi, "Non-volatile resistive switching for advanced memory applications," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2005, pp. 746–749.

[70] M. Wang, W. J. Luo, Y. L. Wang, L. M. Yang, W. Zhu, P. Zhou, J. H. Yang, X. G. Gong, Y. Y. Lin, R. Huang, S. Song, Q. T. Zhou, H. M. Wu, J. G. Wu, and M. H. Chi, "A novel Cu_xSi_yO resistive memory in logic technology with excellent data retention

and resistance distribution for embedded applications," in *Tech. Dig. Symp. Very Large Scale Integr. (VLSI)*, 2010, pp. 89–90.

[71] W. C. Chien, Y. R. Chen, Y. C. Chen, A. T. H. Chuang, F. M. Lee, Y. Y. Lin, E. K. Lai, Y. H. Shih, K. Y. Hsieh, and C.-Y. Lu, "A forming-free WOx resistive memory using a novel self-aligned field enhancement feature with excellent reliability and scalability," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2010, pp. 440–443.

[72] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-kappa gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, pp. 5243–5275, May 2001.

[73] L. Goux, P. Czarnecki, Y. Y. Chen, L. Pantisano, X. P. Wang, R. Degraeve, B. Govoreanu, M. Jurczak, D. J. Wouters, and L. Altimime, "Evidences of oxygen-mediated resistive-switching mechanism in TiN\HfO(2)\Pt cells," *Appl. Phys. Lett.*, vol. 97, Dec. 13, 2010.

[74] B. Govoreanu, G. S. Kar, Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, O. Richard, T. Vandeweyer, K Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D. J. Wouters, J. A. Kittl, and M. Jurczak, "10 $\times$ 10 nm^2 Hf/HfOx crossbar resistive RAM with excellent performance, reliability and low-energy operation," in *Tech. Dig. Int. Electron Device Meeting*, Washington, DC, 2011, pp. 729–732.

[75] Y. Wu, B. Lee, and H. P. Wong, "Al(2)O(3)-based RRAM using atomic layer deposition (ALD) with 1-mu A RESET current," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1449–1451, Dec. 2010.

[76] W. Kim, S. I. Park, Z. Zhang, Y.-L. Young, D. Sekar, H. P. Wong, and S. S. Wong, "Forming-free nitrogen-doped AlO X RRAM with sub-μA programming current," in *Proc. IEEE Symp. Very Large Scale Integr. (VLSI)*, 2011, pp. 22–23.

[77] J. Liang and H.-S. P. Wong, "Cross-point memory array without cell selectors—Device characteristics and data storage pattern dependencies," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2531–2538, Oct. 2010.

[78] Y. S. Chen, H. Y. Lee, P. S. Chen, P. Y. Gu, C. W. Chen, W. P. Lin, W. H. Liu, Y. Y. Hsu, S. S. Sheu, P. C. Chiang, W. S. Chen, F. T. Chen, C. H. Lien, and M.-J. Tsai, "Highly scalable hafnium oxide memory with improvements of resistive distribution and read disturb immunity," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2009, pp. 95–98.

[79] S. Yu, Y. Wu, C. Yang, J. Provine, and H.-S. P. Wong, "Characterization of switching parameters and multilevel capability in HfOx/AlOx Bi-layer RRAM devices," in *Proc. Int. Symp. Very Large Scale Integr. (VLSI) Technol. Syst. Appl.*, 2011, pp. 106–107.

[80] F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L. Goux, and D. J. Wouters, "Sub-10μA reset in NiO-based resistive switching memory (RRAM) cells," in *Proc. IEEE Int. Memory Workshop*, 2010, DOI: 10.1109/IMW.2010.5488317.

[81] M. J. Lee, Y. Park, B.-S. Kang, S.-E. Ahn, C. Lee, K. Kim, W. Xianyu, G. Stefanovich, J.-H. Lee, S.-J. Chung, Y.-H. Kim, C.-S. Lee, J.-B. Park, and I.-K. Yoo, "2-stack 1D-1R cross-point structure with oxide diodes as switch elements for high density resistance RAM applications," in *Tech. IEEE Int. Electron Devices Meeting*, 2007, pp. 771–774.

[82] B. Lee and H. S. P. Wong, "NiO resistance change memory with a novel structure for 3D integration and improved confinement of conduction path," in *Proc. Symp. Very Large Scale Integr. (VLSI) Technol.*, 2009, pp. 28–29.

[83] S. C. Chae, J. S. Lee, W. S. Choi, S. B. Lee, S. H. Chang, H. Shin, B. Kahng, and T. W. Noh, "Multilevel unipolar resistance switching in TiO2 thin films," *Appl. Phys. Lett.*, vol. 95, 093508, Aug. 2009.

[84] C. P. Hsiung, J. Y. Gan, S. H. Tseng, N. H. Tai, P. J. Tzeng, C. H. Lin, F. Chen, and M. J. Tsai, "Resistance switching characteristics of TiO2 thin films prepared with reactive sputtering," *Electrochem. Solid State Lett.*, vol. 12, pp. G31–G33, 2009.

[85] D. S. Jeong, H. Schroeder, and R. Waser, "Coexistence of bipolar and unipolar resistive switching behaviors in a Pt/TiO2/Pt stack," *Electrochem. Solid State Lett.*, vol. 10, pp. G51–G53, 2007.

[86] W. Wang, S. Fujita, and S. S. Wong, "RESET mechanism of TiOx resistance-change memory device," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 733–735, Jul. 2009.

[87] M. Fujimoto, H. Koyama, Y. Hosoi, K. Ishihara, and S. Kobayashi, "High-speed resistive switching of TiO2/TiN nano-crystalline thin film," *Jpn. J. Appl. Phys. 2—Lett, Exp. Lett.*, vol. 45, pp. L310–L312, Mar. 2006.

[88] Y. H. Do, J. S. Kwak, Y. C. Bae, K. Jung, H. Im, and J. P. Hong, "Hysteretic bipolar resistive switching characteristics in TiO2/TiO2-x multilayer homojunctions," *Appl. Phys. Lett.*, vol. 95, 093507, Aug. 2009.

[89] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, T. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, and M. Oshima, "Highly reliable TaO_x ReRAM and direct evidence of redox reaction mechanism," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2008, pp. 293–296.

[90] Z. Wei, T. Takagi, Y. Kanzawa, Y. Katoh, T. Ninomiya, K. Kawai, S. Muraoka, S. Mitani, K. Katayama, S. Fujii, R. Miyanaga, Y. Kawashima, T. Mikawa, K. Shimakawa, and K. Aono, "Demonstration of high-density ReRAM ensuring 10-year retention at 85 °C based on a newly developed reliability model," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, Washington, DC, 2011, pp. 721–724.

[91] M. J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U. I. Chung, I. K. Yoo, and K. Kim, "A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta(2)O(5-x)/TaO(2-x) bilayer structures," *Nature Mater.*, vol. 10, pp. 625–630, Aug. 2011.

[92] J. J. Yang, M. X. Zhang, J. P. Strachan, F. Miao, M. D. Pickett, R. D. Kelley, G. Medeiros-Ribeiro, and R. S. Williams, "High switching endurance in TaO(x) memristive devices," *Appl. Phys. Lett.*, vol. 97, 232102, Dec. 2010.

[93] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, and Y. Sugiyama, "Reduction in the reset current in a resistive random access memory consisting of NiOx brought about by reducing a parasitic capacitance," *Appl. Phys. Lett.*, vol. 93, 033506, Jul. 2008.

[94] P.-Y. Gu, Y.-S. Chen, H.-Y. Lee, P.-S. Chen, W.-H. Liu, W.-S. Chen, Y.-Y. Hsu, F. Chen, and M.-J. Tsai, "Scalability with silicon nitride encapsulation layer for Ti/HfOx pillar RRAM," in *Proc. Int. Symp. Very Large Scale Integr. (VLSI) Technol. Syst. Appl.*, 2010, pp. 146–147.

[95] Y. H. Tseng, C.-E. Huang, C.-H. Kuo, Y.-D. Chih, and C. J. Lin, "High density and ultra small cell size of contact ReRAM (CR-RAM) in 90 nm CMOS logic technology and circuits," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2009, pp. 99–102.

[96] V. Jousseaume, J. Buckley, Y. Bernard, P. Gonon, C. Vallee, M. Mougenot, H. Feldis, S. Minoret, G. Chamiot-Maitral, A. Persico, A. Zenasni, M. Gely, J. P. Barnes, E. Martinez, H. Grampeix, C. Guedj, J. F. Nodin, and B. De Salvo, "Back-end-of-line integration approaches for resistive memories," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2009, pp. 41–43.

[97] Y. S. Chen, H. Y. Lee, P. S. Chen, P. Y. Gu, C. W. Chen, W. P. Lin, W. H. Liu, Y. Y. Hsu, S. S. Sheu, P. C. Chiang, W. S. Chen, F. T. Chen, C. H. Lien, and M.-J. Tsai, "Highly scalable hafnium oxide memory with improvements of resistive distribution and read disturb immunity," in *Proc. IEEE Int. Electron Devices Meeting*, 2009, pp. 105–108.

[98] C. Sire, S. Blonkowski, M. J. Gordon, and T. Baron, "Statistics of electrical breakdown field in HfO2 and SiO2 films from millimeter to nanometer length scales," *Appl. Phys. Lett.*, vol. 91, 242905, 2007.

[99] Y. Sato, K. Tsunoda, K. Kinoshita, H. Noshiro, M. Aoki, and Y. Sugiyama, "Sub-1100-mu A reset current of nickel oxide resistive memory through control of filamentary conductance by current limit of MOSFET," *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1185–1191, May 2008.

[100] Y. Sato, K. Tsunoda, M. Aoki, and Y. Sugiyama, "Novel circuitry configuration with paired-cell erase operation for high-density 90-nm embedded resistive random access memory," *Jpn. J. Appl. Phys.*, vol. 48, 04C075, 2009.

[101] S. S. Sheu, P.-C. Chiang, W.-P. Lin, H.-Y. Lee, P. S. Chen, Y.-S. Chen, T.-Y. Wu, F. T. Chen, K.-L. Su, M.-J. Kao, K.-H. Cheng, and M.-J. Tsai, "A 5 ns fast write multi-level non-volatile 1 K bits RRAM memory with advance write scheme," in *Proc. Symp. Very Large Scale Integr. (VLSI) Circuits*, 2009, pp. 82–83.

[102] S.-S. Sheu, M.-F. Chang, K.-F. Lin, C.-W. Wu, Y.-S. Chen, P.-F. Chiu, C.-C. Kuo, Y.-S. Yang, P.-C. Chiang, W.-P. Lin, C.-H. Lin, H.-Y. Lee, P.-Y. Gu, S.-M. Wang, F. T. Chen, K.-L. Su, C.-H. Lien, K.-H. Cheng, H.-T. Wu, T.-K. Ku, M.-J. Kao, and M.-J. Tsai, "A 4 Mb embedded SLC resistive-RAM macro with 7.2 ns read-write random access time and 160 ns MLC-access capability," in *Proc. Int. Solid-State Circuits Conf.*, 2011, pp. 200–202.

[103] C.-H. Wang, Y.-H. Tsai, K.-C. Lin, M.-F. Chang, Y.-C. King, C. J. Lin, S.-S. Sheu, Y.-S. Chen, H.-Y. Lee, F. T. Chen, and M.-J. Tsai, "Three-dimensional 4F(2) ReRAM with vertical BJT driver by CMOS logic compatible process," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2466–2472, Aug. 2011.

[104] M. J. Lee, C. B. Lee, S. Kim, H. Yin, J. Park, S. E. Ahn, B. S. Kang, K. H. Kim, G. Stefanovich, I. Song, S. W. Kim, J. H. Lee, S. J. Chung, Y. H. Kim, C. S. Lee, J. B. Park,

I. G. Baek, C. J. Kim, and Y. Park, "Stack friendly all-oxide 3D RRAM using GaInZnO peripheral TFT realized over glass substrates," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2008, pp. 85–88.

[105] G. Tallarida, N. Huby, B. Kutrzeba-Kotowska, S. Spiga, M. Arcari, G. Csaba, P. Lugli, A. Redaelli, and R. Bez, "Low temperature rectifying junctions for crossbar non-volatile memory devices," in *Proc. IEEE Int. Memory Workshop*, 2009, DOI: 10.1109/IMW.2009.5090598.

[106] J.-J. Huang, Y.-M. Tseng, W.-C. Luo, C.-W. Hsu, and T.-H. Hou, "One selector-one resistor (1S1R) crossbar array for high-density flexible memory applications," in *Tech. Dig. Int. Electron Devices Meeting*, Washington, DC, 2011, pp. 733–736.

[107] A. Kawahara, R. Azuma, Y. Ikeda, K. Kawai, Y. Katoh, K. Tanabe, T. Nakamura, Y. Sumimoto, N. Yamada, N. Nakai, S. Sakamoto, Y. Hayakawa, K. Tsuji, S. Yoneda, A. Himeno, K.-I. Origasa, K. Shimakawa, T. Takagi, T. Mikawa, and K. Aono, "An 8 Mb multi-layered cross-point ReRAM macro with 443 MB/s write throughput," in *Proc. Int. Solid-State Circuits Conf.*, San Francisco, CA, 2012, pp. 432–434.

[108] M. J. Lee, Y. Park, D. S. Suh, E. H. Lee, S. Seo, D. C. Kim, R. Jung, B. S. Kang, S. E. Ahn, C. B. Lee, D. H. Seo, Y. K. Cha, I. K. Yoo, J. S. Kim, and B. H. Park, "Two series oxide resistors applicable to high speed and high density nonvolatile memory," *Adv. Mater.*, vol. 19, p. 3919, Nov. 2007.

[109] C. R. Cho, S. I. Cho, S. Vadim, R. Jung, and I. Yoo, "Current-induced metal-insulator transition in VOx thin film prepared by rapid-thermal-annealing," *Thin Solid Films*, vol. 495, pp. 375–379, Jan. 2006.

[110] C. Ko and S. Ramanathan, "Observation of electric field-assisted phase transition in thin film vanadium oxide in a metal-oxide-semiconductor device geometry," *Appl. Phys. Lett.*, vol. 93, 252101, Dec. 2008.

[111] D. C. Kau, S. Tang, I. V. Karpov, R. Dodge, B. Klehn, J. A. Kalb, J. Strand, A. Diaz, N. Leung, J. Wu, S. Lee, T. Langtry, K.-W. Chang, C. Papagianni, J. Lee, J. Hirst, S. Erra, E. Flores, N. Righos, H. Castro, and G. Spadini, "A stackable cross point phase change memory," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2009, pp. 617–620.

[112] K. Gopalakrishnan, R. S. Shenoy, C. T. Rettner, K. Virwani, D. S. Bethune, R. M. Shelby, G. W. Burr, A. Kellock, R. S. King, K. Nguyen, A. N. Bowers, M. Jurich, B. Jackson, A. M. Friz, T. Topuria, P. M. Rice, and B. N. Kurdi, "Highly-scalable novel access device based on Mixed Ionic Electronic conduction (MIEC) materials for high density phase change memory (PCM) arrays," in *Proc. Symp. Very Large Scale Integr. (VLSI) Technol.*, 2010, pp. 205–206.

[113] H.-S. P. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, "Phase change memory," *Proc. IEEE*, vol. 98, no. 12, pp. 2201–2227, Dec. 2011.

[114] R. Meyer, L. Schloss, J. Brewer, R. Lambertson, W. Kinney, J. Sanchez, and D. Rinerson, "Oxide dual-layer memory element for scalable non-volatile cross-point memory technology," in *Proc. 9th Annu. Non-Volatile Memory Technol. Symp.*, 2008, DOI: 10.1109/NVMT.2008.4731194.

[115] C. J. Chevallier, C. H. Siau, S. F. Lim, S. R. Namala, M. Matsuoka, B. L. Bateman, and D. Rinerson, "A 0.13 μm 64 Mb multi-layered conductive metal-oxide memory," in *Tech. Dig. IEEE Int. Solid-State Circuits Conf.*, 2010, pp. 260–261.

[116] S. Yu, X. Guan, and H.-S. P. Wong, "On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization," in *Tech. Dig. Int. Electron Devices Meeting*, Washington, DC, 2011, pp. 413–416.

[117] D. C. Kim, M. J. Lee, S. E. Ahn, S. Seo, J. C. Park, I. K. Yoo, I. G. Baek, H. J. Kim, E. K. Yim, J. E. Lee, S. O. Park, H. S. Kim, U. I. Chung, J. T. Moon, and B. I. Ryu, "Improvement of resistive memory switching in NiO using IrO2," *Appl. Phys. Lett.*, vol. 88, 232106, Jun. 2006.

[118] S. Yu, B. Gao, H. Dai, B. Sun, L. Liu, X. Liu, R. Han, J. Kang, and B. Yu, "Improved uniformity of resistive switching behaviors in HfO(2) thin films with embedded Al layers," *Electrochem. Solid State Lett.*, vol. 13, pp. H36–H38, 2010.

[119] W. Y. Chang, K. J. Cheng, J. M. Tsai, H. J. Chen, F. Chen, M. J. Tsai, and T. B. Wu, "Improvement of resistive switching characteristics in TiO2 thin films with embedded Pt nanocrystals," *Appl. Phys. Lett.*, vol. 95, 042104, Jul. 2009.

[120] Q. Liu, S. Long, W. Wang, Q. Zuo, S. Zhang, J. Chen, and M. Liu, "Improvement of resistive switching properties in ZrO_2-based ReRAM with implanted Ti Ions," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1335–1337, Dec. 2009.

[121] J. Lee, J. Shin, D. Lee, W. Lee, S. Jung, M. Jo, J. Park, K. P. Biju, S. Kim, S. Park, and H. Hwang, "Diode-less nano-scale ZrOx/HfOx RRAM device with excellent switching uniformity and reliability for high-density cross-point memory applications," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2010, pp. 452–455.

[122] W. Y. Chang, C. A. Lin, J. H. He, and T. B. Wu, "Resistive switching behaviors of ZnO nanorod layers," *Appl. Phys. Lett.*, vol. 96, 242109, Jun. 2010.

[123] M. Yin, P. Zhou, H. B. Lv, J. Xu, Y. L. Song, X. F. Fu, T. A. Tang, B. A. Chen, and Y. Y. Lin, "Improvement of resistive switching in CuxO using new RESET mode," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 681–683, Jul. 2008.

[124] I. K. Yoo, B. S. Kang, Y. D. Park, M. J. Lee, and Y. Park, "Interpretation of nanoscale conducting paths and their control in nickel oxide (NiO) thin films," *Appl. Phys. Lett.*, vol. 92, 202112, May 2008.

[125] H. Y. Lee, Y. S. Chen, P. S. Chen, P. Y. Gu, Y. Y. Hsu, S. M. Wang, W. H. Liu, C. H. Tsai, S. S. Sheu, P. C. Chiang, W. P. Lin, C. H. Lin, W. S. Chen, F. T. Chen, C. H. Lien, and M. Tsai, "Evidence and solution of over-RESET problem for HfOx based resistive memory with sub-ns switching speed and high endurance," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2010, pp. 460–463.

[126] B. Chen, Y. Lu, B. Gao, Y. H. Fu, F. F. Zhang, P. Huang, Y. S. Chen, L. F. Liu, X. Y. Liu, J. F. Kang, Y. Y. Wang, Z. Fang, H. Y. Yu, X. Li, X. P. Wang, N. Singh, G. Q. Lo, and D. L. Kwong, "Physical mechanisms of endurance degradation in TMO-RRAM," in *Tech. Dig. Int. Electron Devices Meeting*, Washington, DC, 2011, pp. 283–286.

[127] S. Yu, Y. Wu, and H. S. P. Wong, "Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory," *Appl. Phys. Lett.*, vol. 98, 103514, Mar. 7, 2011.

[128] F. T. Chen, H. Lee, Y. Chen, Y. Hsu, L. Zhang, P. Chen, W. Chen, P. Gu, W. Liu, S. Wang, C. Tsai, S. Sheu, M. Tsai, and R. Huang, "Resistance switching for RRAM applications," *Science China, Inf. Sci.*, vol. 54, pp. 1073–1086, May 2011.

[129] B. Gao, J. F. Kang, H. W. Zhang, B. Sun, B. Chen, L. F. Liu, X. Y. Liu, R. Q. Han, Y. Y. Wang, B. Yu, Z. Fang, H. Y. Yu, and D.-L. Kwong, "Oxide-based RRAM: Physical based retention projection," in *Proc. Eur. Solid-State Device Res. Conf.*, 2010, pp. 392–395.

[130] S. Yu, Y. Y. Chen, X. Guan, H.-S. P. Wong, and J. A. Kittl, "A Monte Carlo study of the low resistance state retention of HfOx based resistive switching memory," *Appl. Phys. Lett.*, vol. 100, 043507, 2012.

[131] S.-Y. Wang, C.-W. Huang, D.-Y. Lee, T.-Y. Tseng, and T.-C. Chang, "Multilevel resistive switching in Ti/Cu(x)O/Pt memory devices," *J. Appl. Phys.*, vol. 108, 114110, Dec. 1, 2010.

[132] W. C. Chien, Y. C. Chen, E. K. Lai, Y. Y. Lin, K. P. Chang, Y. D. Yao, P. Lin, S. F. Horng, J. Gong, S. C. Tsai, C. H. Lee, S. H. Hsieh, C. F. Chen, Y. H. Shih, K. Y. Hsieh, R. Liu, and C. Y. Lu, "High-speed multilevel resistive RAM using RTO WOX," in *Proc. Int. Conf. Solid State Devices Mater.*, 2009, pp. 1206–1207.

[133] M. Terai, Y. Sakotsubo, S. Kotsuji, and H. Hada, "Resistance controllability of Ta_2O_5/TiO_2 stack ReRAM for low-voltage and multilevel operation," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 204–206, Mar. 2010.

[134] W. C. Chien, K. P. Chang, Y. C. Chen, E. K. Lai, H. Mähne, Y. D. Yao, P. Lin, J. Gong, S. H. Hsieh, K. Y. Hsieh, R. Liu, and C.-Y. Lu, "Multilevel switching characteristics for WOX resistive RAM (RRAM)," in *Proc. Int. Conf. Solid State Devices Mater.*, 2008, pp. 1170–1171.

[135] D. K. Yun, K. D. Kim, S. Kim, J. H. Lee, H. H. Park, J. H. Jeong, Y. K. Choi, and D. G. Choi, "Mass fabrication of resistive random access crossbar arrays by step and flash imprint lithography," *Nanotechnology*, vol. 20, 445305, Nov. 2009.

[136] S. I. Kim, J. H. Lee, Y. W. Chang, S. S. Hwang, and K. H. Yoo, "Reversible resistive switching behaviors in NiO nanowires," *Appl. Phys. Lett.*, vol. 93, 033503, Jul. 2008.

[137] K. Oka, T. Yanagida, K. Nagashima, H. Tanaka, and T. Kawai, "Nonvolatile bipolar resistive memory switching in single crystalline NiO heterostructured nanowires," *J. Amer. Chem. Soc.*, vol. 131, p. 3434, Mar. 2009.

[138] K. Nagashima, T. Yanagida, K. Oka, M. Taniguchi, T. Kawai, J. S. Kim, and B. H. Park, "Resistive switching multistate nonvolatile memory effects in a single cobalt oxide nanowire," *Nano Lett.*, vol. 10, pp. 1359–1363, Apr. 2010.

[139] N. Xu, B. Gao, L. F. Liu, S. Bing, X. Y. Liu, R. Q. Han, J. F. Kang, and B. Yu, "A unified physical model of switching behavior in oxide-based RRAM," in *Proc. Symp. Very Large Scale Integr. (VLSI) Technol.*, Jun. 17, 2008, pp. 100–101.

[140] S. Kim, H. Moon, D. Gupta, S. Yoo, and Y.-K. Choi, "Resistive, switching characteristics of sol-gel zinc oxide films for flexible memory applications," *IEEE*

Trans. Electron Devices, vol. 56, no. 4, pp. 696–699, Apr. 2009.

[141] H. B. Lv, M. Yin, X. F. Fu, Y. L. Song, L. Tang, P. Zhou, C. H. Zhao, T. A. Tang, B. A. Chen, and Y. Y. Lin, "Resistive memory switching of Cu_xO films for a nonvolatile memory application," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 309–311, Apr. 2008.

[142] X. Sun, B. Sun, L. Liu, N. Xu, X. Liu, R. Han, J. Kang, G. Xiong, and T. P. Ma, "Resistive switching in CeOx films for nonvolatile memory application," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 334–336, Apr. 2009.

[143] S. E. Ahn, M. J. Lee, Y. Park, B. S. Kang, C. B. Lee, K. H. Kim, S. Seo, D. S. Suh, D. C. Kim, J. Hur, W. Xianyu, G. Stefanovich, H. A. Yin, I. K. Yoo, A. H. Lee, J. B. Park, I. G. Baek, and B. H. Park, "Write current reduction in transition metal oxide based resistance-change memory," *Adv. Mater.*, vol. 20, p. 924, Mar. 2008.

[144] Y. Wu, Internal data within the authors of Stanford, 2011, unpublished.

[145] A. Chen, S. Haddad, Y. C. Wu, T. N. Fang, S. Kaza, and Z. Lan, "Erasing characteristics of Cu2O metal-insulator-metal resistive switching memory," *Appl. Phys. Lett.*, vol. 92, 013503, Jan. 2008.

[146] K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Iizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, and Y. Sugiyama, "Low power and high speed switching of Ti-doped NiO ReRAM under the unipolar voltage source of less than 3 V," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2007, pp. 767–770.

[147] Y.-S. Chen, *Industrial Technology Research Institute (ITRI)*, 2010, Internal data within the authors of ITRI, unpublished.

[148] S.-G. Park, B. Magyari-Koäpe, and Y. Nishi, "Impact of oxygen vacancy ordering on the formation of a conductive filament in TiO(2) for resistive switching memory," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 197–199, Feb. 2011.

[149] S. Tanachutiwat, M. Liu, and W. Wang, "FPGA based on integration of CMOS and RRAM," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 11, pp. 2023–2032, Nov. 2011.

[150] Y. Y. Liauw, Z. Zhang, W. Kim, A. El Gamal, and S. S. Wong, "Nonvolatile 3D-FPGA with monolithically stacked RRAM-based configuration memory," in *Proc. Int. Solid-State Circuits Conf.*, San Francisco, CA, 2012, pp. 406–408.

[151] K. Seo, I. Kim, S. Jung, M. Jo, S. Park, J. Park, J. Shin, K. P. Biju, J. Kong, K. Lee, B. Lee, and H. Hwang, "Analog memory and spike-timing-dependent plasticity characteristics of a nanoscale titanium oxide bilayer resistive switching device," *Nanotechnology*, vol. 22, 254023, Jun. 24, 2011.

[152] T. Chang, S. H. Jo, and W. Lu, "Short-term memory to long-term memory transition in a nanoscale memristor," *Acs Nano*, vol. 5, pp. 7669–7676, Sep. 2011.

[153] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H. P. Wong, "An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2729–2737, Aug. 2011.

[154] G. S. Snider, "Spike-timing-dependent learning in memristive nanodevices," in *Proc. IEEE Int. Symp. Nanoscale Architectures*, 2008, pp. 85–92.

[155] Y.-B. Kim, S. R. Lee, D. Lee, C. B. Lee, M. Chang, J. H. Hur, M.-J. Lee, G.-S. Park, C. J. Kim, U.-I. Chang, I.-K. Yoo, and K. Kim, "Bi-layered RRAM with unlimited endurance and extremely uniform switching," in *Proc. IEEE Symp. Very Large Scale Integr. (VLSI) Technol.*, 2011, pp. 52–53.

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