Introduction

The aim of the beam steering network project is to design elements that

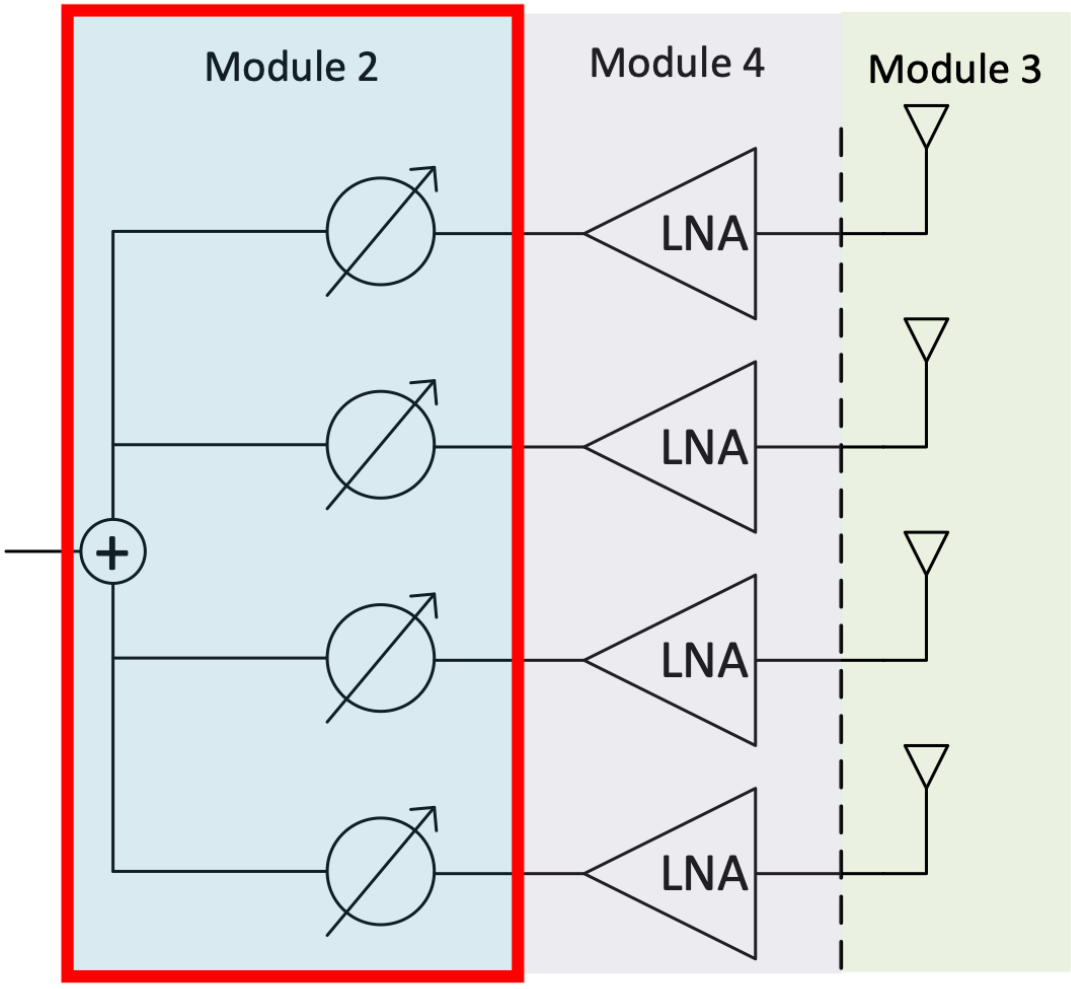


Figure1 : Beam steering network

when working together will enable us to do beam steering. The network involves 3 parts as shown in Fig 1. Module 2 involves designing the power combiner with analog phase shifters. Module 3 involves designing antenna to receive the signals. Module 4 involves designing low noise amplifier (LNA) to amplify the received signals.

In this report, the design aspects of Module 4 are discussed and also the related simulated data for Module 4 is mentioned.

Specification of Module 4

The specification as mentioned for this project are highlighted in Table 1.

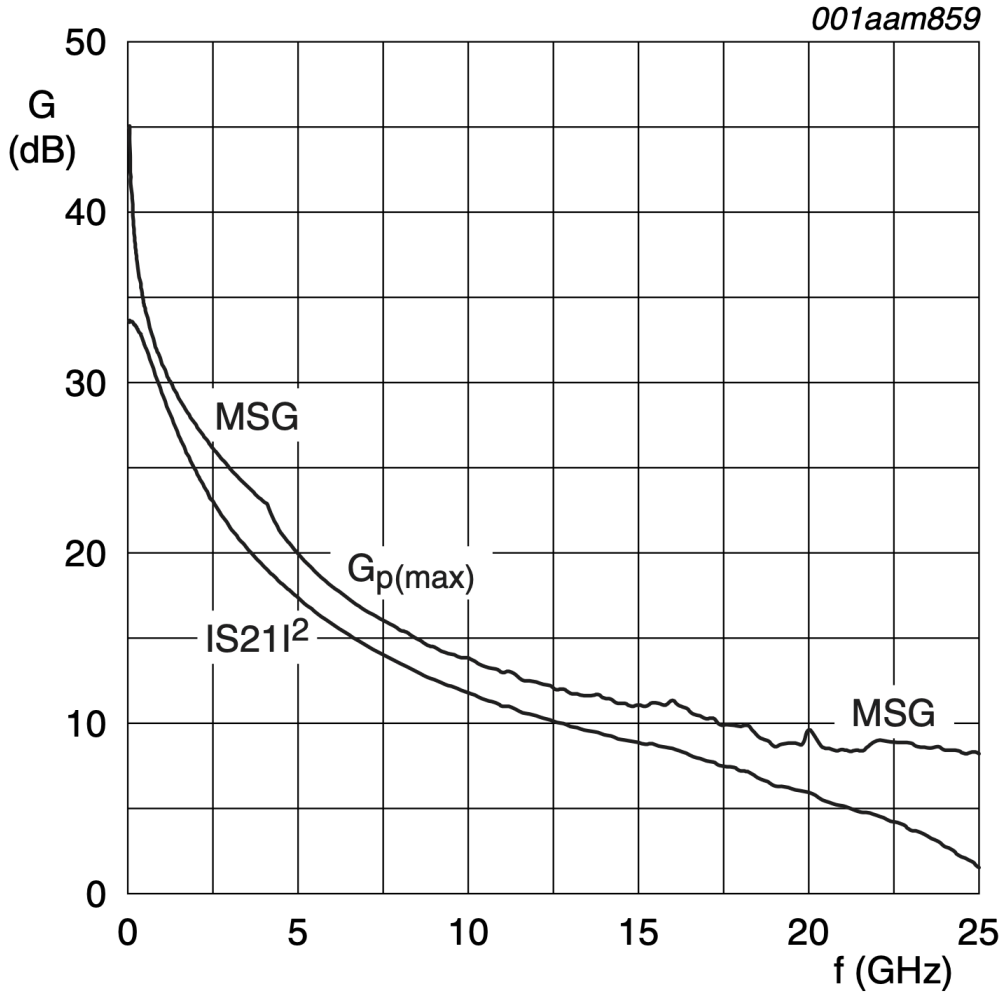
ID	Parameter	Specs
1	Operating bandwith	5.725 - 5.875 GHz
2	Port Match	S_{11} < -10dB @ Zo = 50Ohm S_{22} < -10dB @ Zo = 50Ohm
3	Transducer Power gain	S_{21} > 15dB @ Zo = 50Ohm
4	Noise Figure	NF < 2dB
5	Stability	Unconditional
6	Transistor	BFU730F

Table 1 : Specifications

Design of amplifier

The first and foremost point in designing LNA is to choose the right transistor. The transistor that has to be used is advised to be BFU730F.

The next point is to choose the right bias conditions for this transistor to provide the required gain, noise figure etc. Looking at the data sheet we can observe that the transistor has max operating gain of around 18dB at 5.8GHz with a bias conditions of Ic = 17mA, Vce = 2V



V_{CE} = 2 V; I_C = 17 mA; T_{amb} = 25 °C.

Figure 2: Transistor gain at the mentioned bias condition

Similarly, we can see that the transistor has a min Noise figure of around 0.8dB at this bias condition.

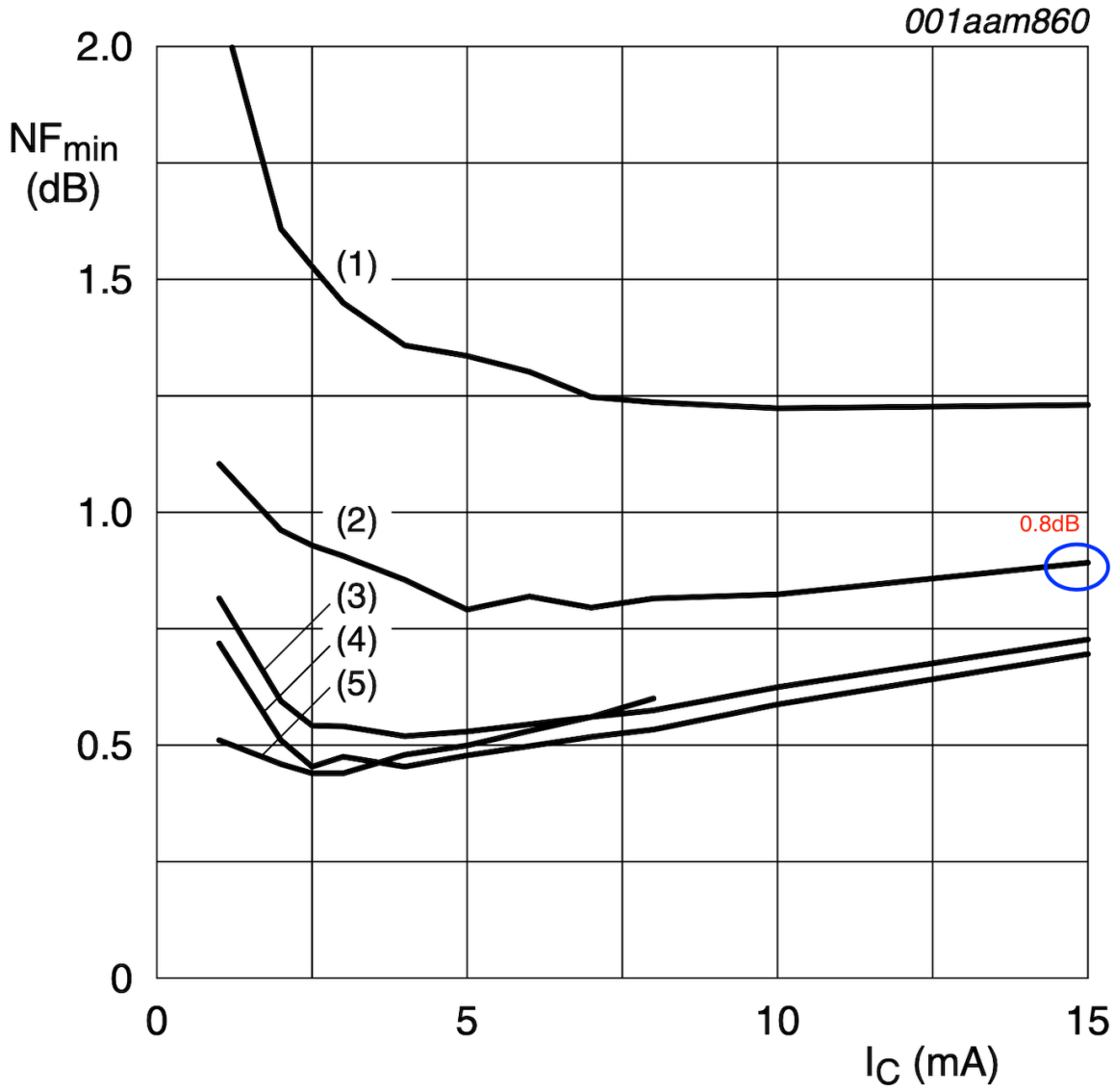


Figure 3: Min noise figure of the transistor v/s collector current

Keeping these in mind, the transistor bias was chosen to be Vce = 2V, Ic = 15mA, Ib = 50uA. The base current Ib can be seen from data sheet Fig.2.

The S-parameters of this transistor at the above bias condition is chosen. The corresponding schematic is depicted in Figure 4. The various parameters like S21, Noise figure, Stability factors, Stability circles are as well plotted in Figure 5.

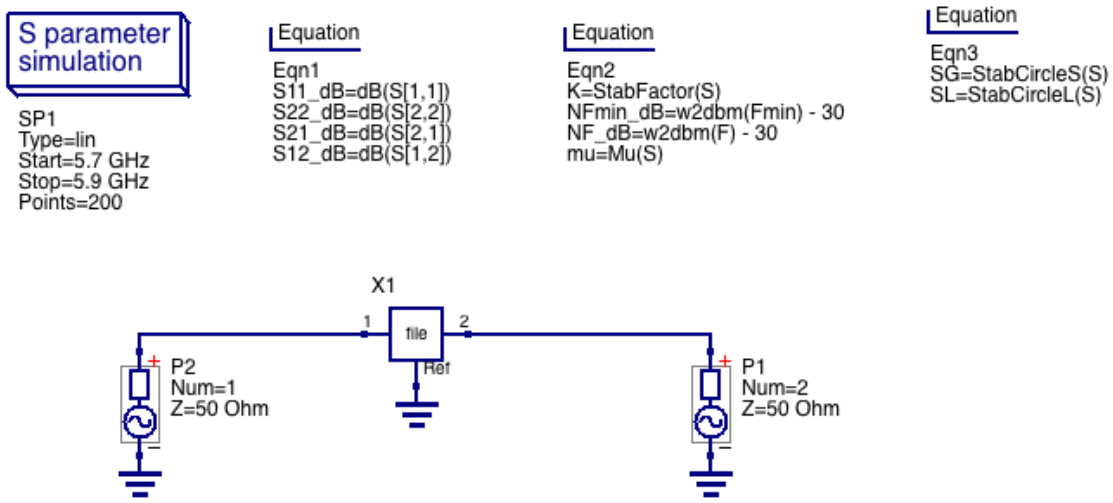


Figure 4: Schematic for s parameter simulation of transistor alone

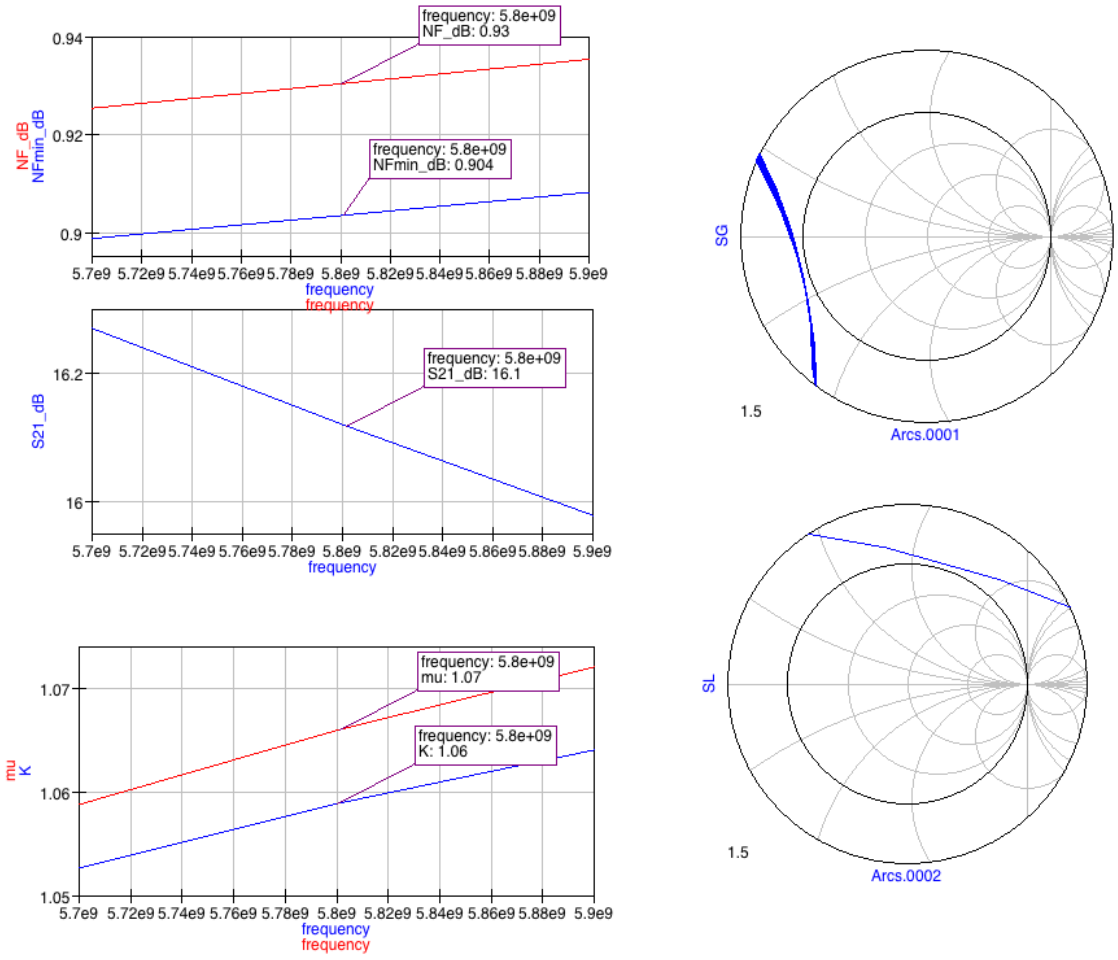


Figure 5: Different parameters of the transistor at Vce = 2V, Ic=15mA

As it can be seen from Figure 5, the transistor has S21 = 16dB. With right matching circuits, this can be further improved by 2-3dB which meets our requirements. Additionally, we can also see that the stability factor is > 1 for our frequency range of interest. This is also plotted on smith chart as stability circles where in we can see that these circles lie outside smith chart. In that sense, this is unconditionally stable for any source and load impedance. Further, the min noise figure is 0.904 dB which is well within our requirements

In the following, the analysis of the LNA is carried out at the center frequency of band which is 5.8GHz. Initially the bias network is designed to obtain Vce = 2V, Ic = 15mA, Ib=50uA. The schematic for the same is shown in Figure 6

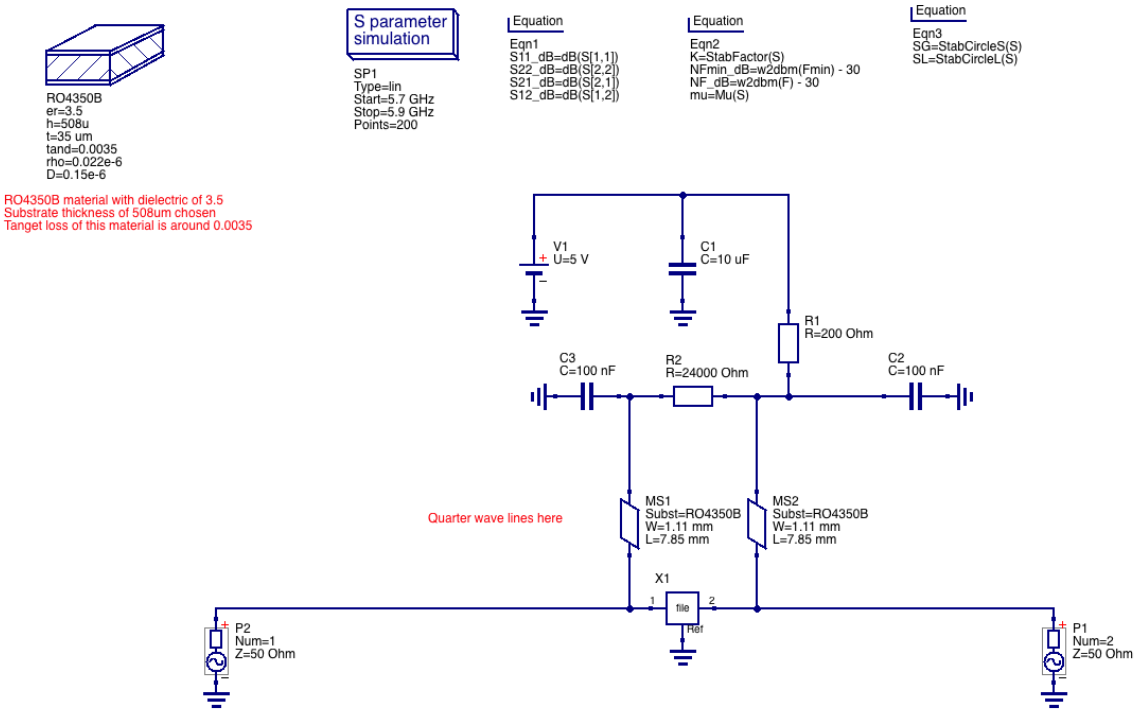


Figure 6: Bias network

The quarter wave transmission lines are used to isolate bias network from input and output. The quarter wave transmission MS1/MS2 has C3/C2 connected at one end. These capacitors C3/C2 are low impedance at

5.8GHz. So the quarter wave transmission lines can be viewed as shorted transmission lines. Looking at the other end of shorted quarter wave transmission line, we know its open circuit. This is the exact behaviour we want. This is again verified to make sure that the S-parameters are not disturbed.

Now in order to proceed with input matching, the noise circles, constant gain circles are analysed. The schematic is updated as Figure 7 to allow us to plot the various circles.

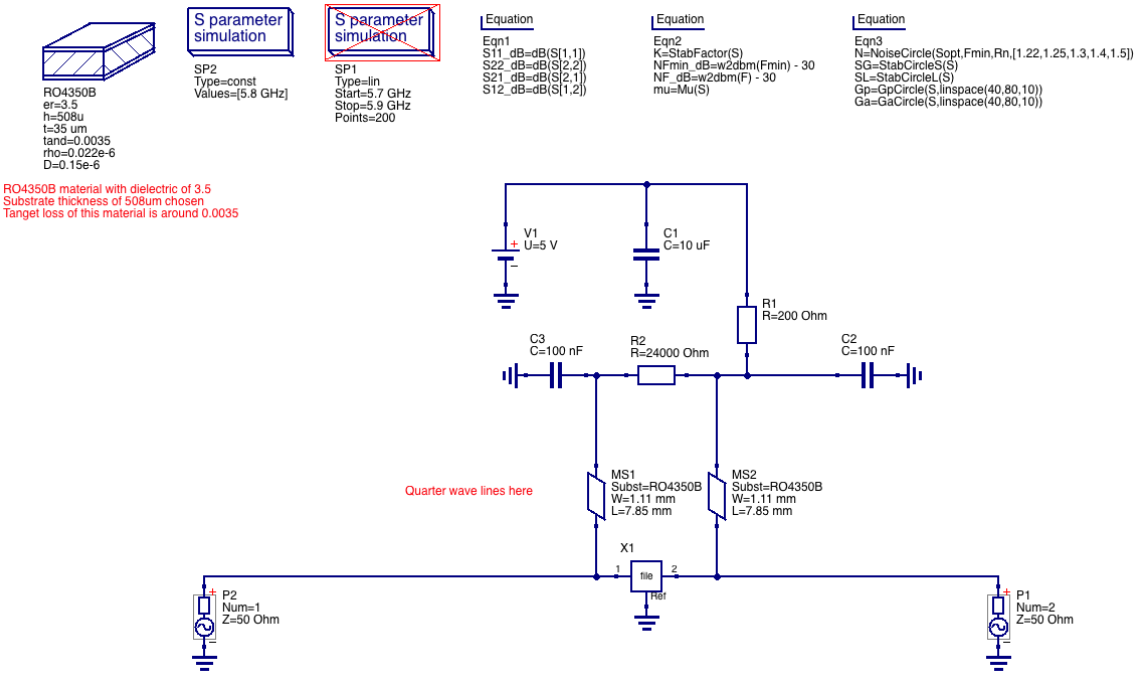


Figure 7: Schematic to draw various circles

Here we are drawing constant noise circles corresponding to 1.22,1.25,1.3,1.4,1.5 (0.86dB,0.97dB, 1.14dB, 1.46dB, 1.76dB) and constant gain circles corresponding to gain from 16dB to 19dB. The respective plots are shown in Figure 8

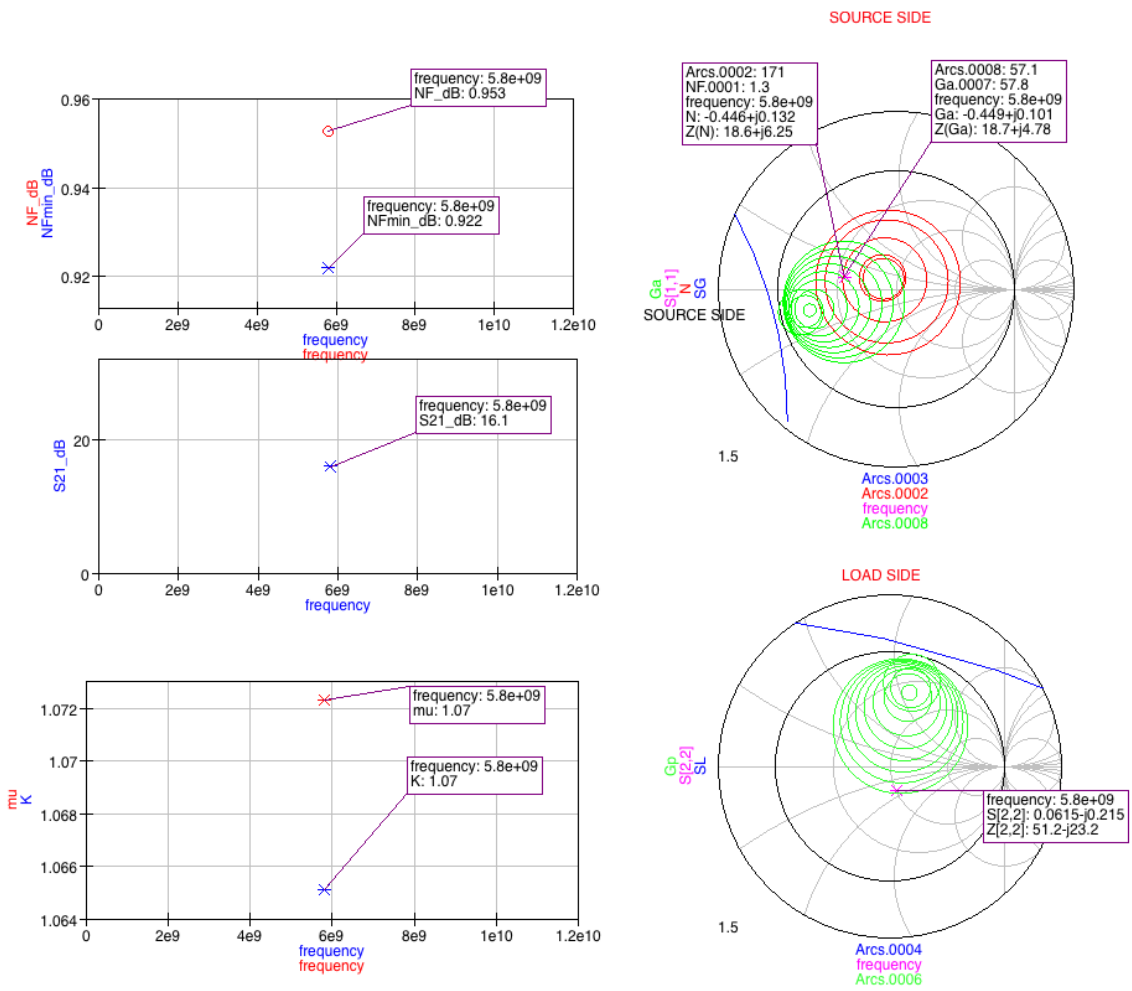


Figure 8: Constant Noise circles and gain circles

As we can see from Figure 8, for the source side, the constant noise circle for NF = 1.3 (1.14dB) and constant gain circle of 57.8(17.6dB) are marked with markers. These are close to the S11 point. So a conjugate match of S11 point will yield optimum noise, gain and matching.

The input matching circuit along with the transistor is shown in Figure 9. The resulting noise circles, gain circles, S11 and S21 are also shown in Figure 10. Also the input ac-coupling capacitor C5 is shown. This capacitor is chosen high enough that at 5.8GHz it presents as low impedance as possible.

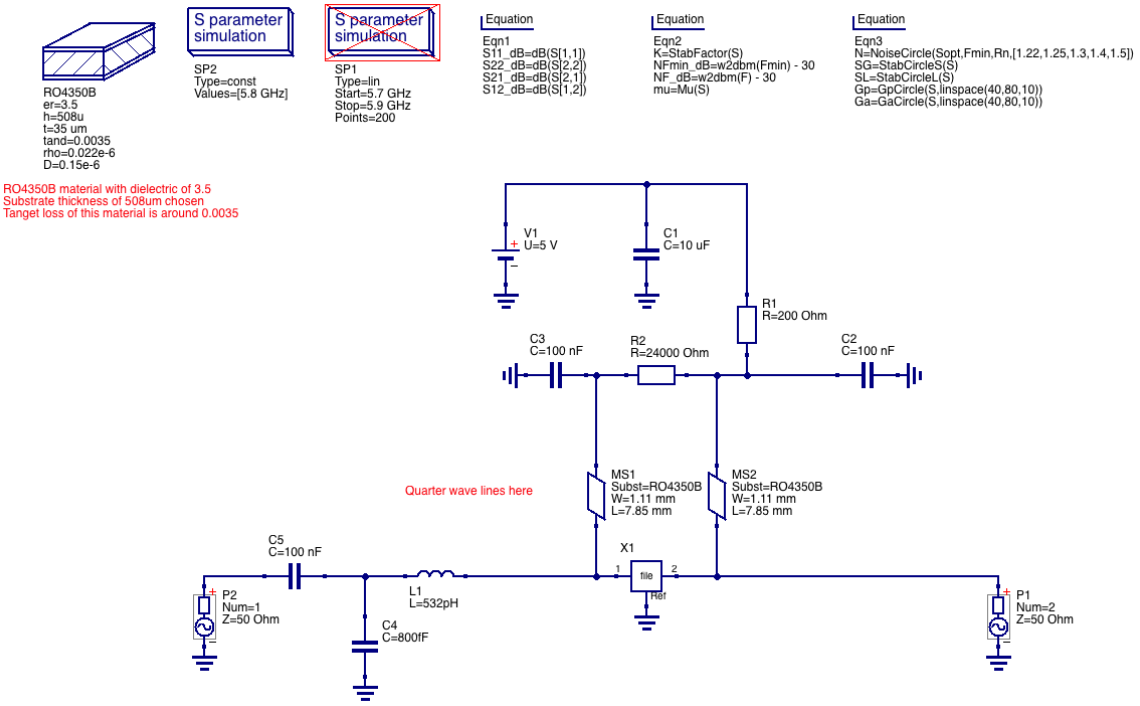


Figure 8: Input matching circuit

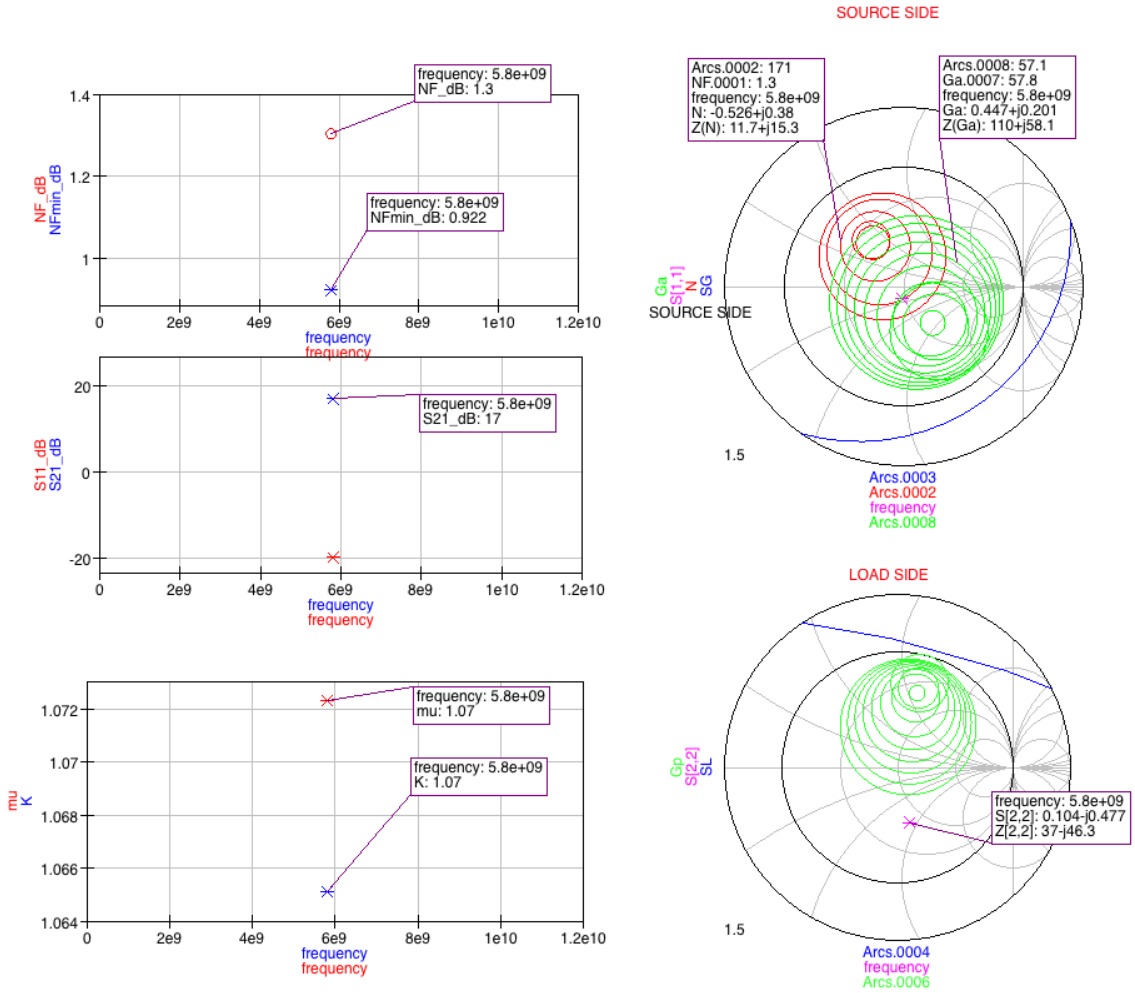


Figure 9: Resulting plots after input match. S11 < -10dB

The output matching is achieved by simply doing a power matching. That is a conjugate matching of S22. Right click on the marker of S22 and select power matching. This will give a power matching circuit.

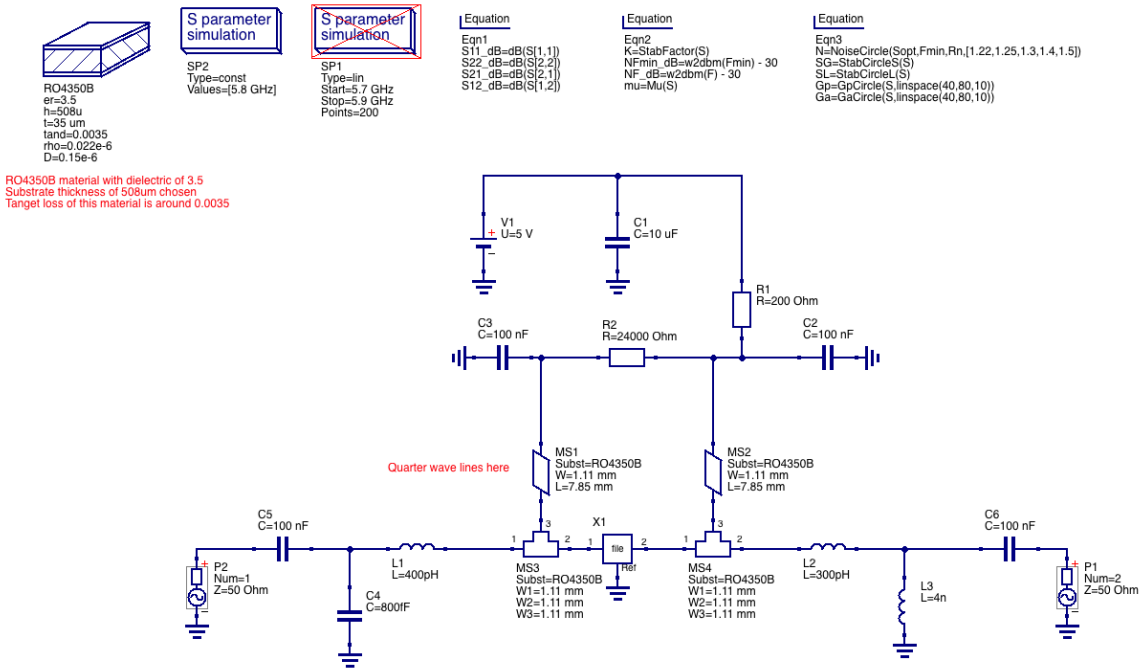


Figure 10: Output matching network

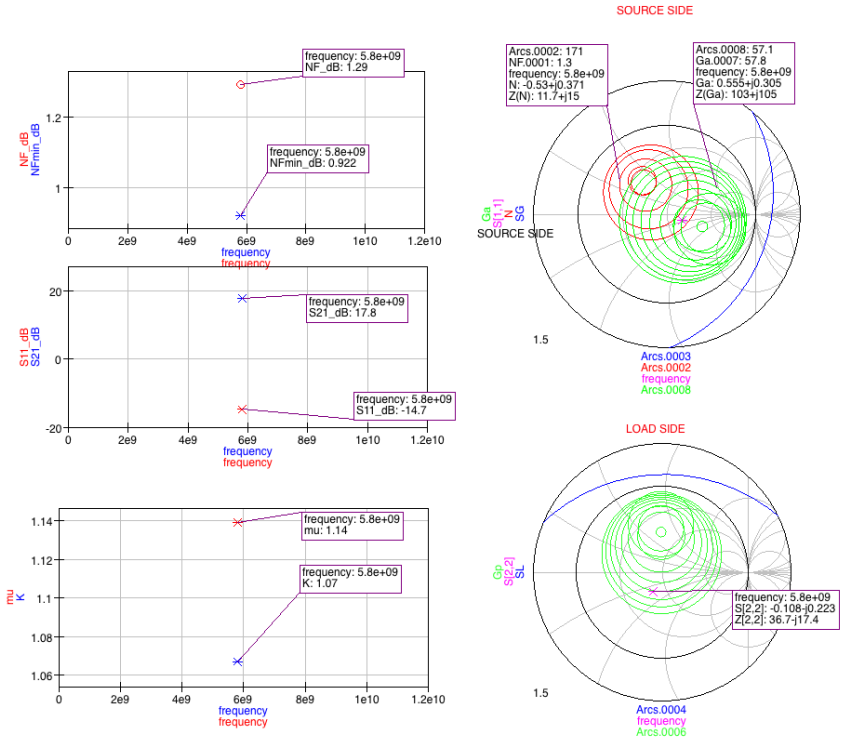


Figure 11: Plots after output matching and optimising input match

Finally, the sweep over the entire frequency band is made and the corresponding schematic and plots are depicted in Figure 12 & Figure 13.

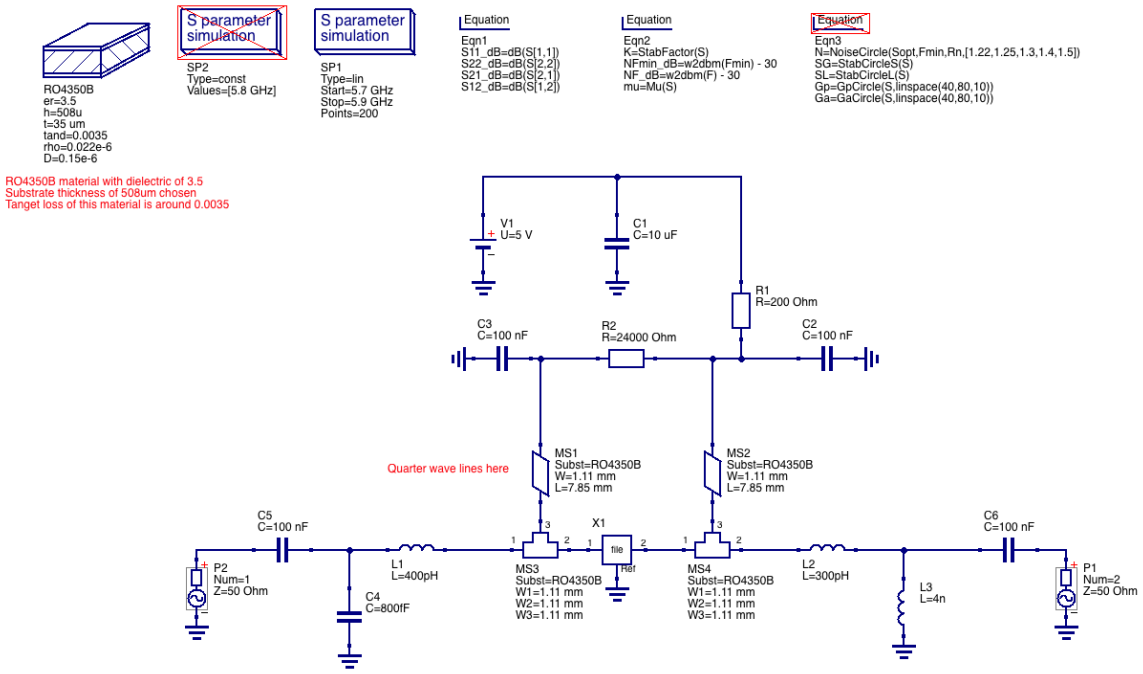


Figure 12: Sweep over the frequency range

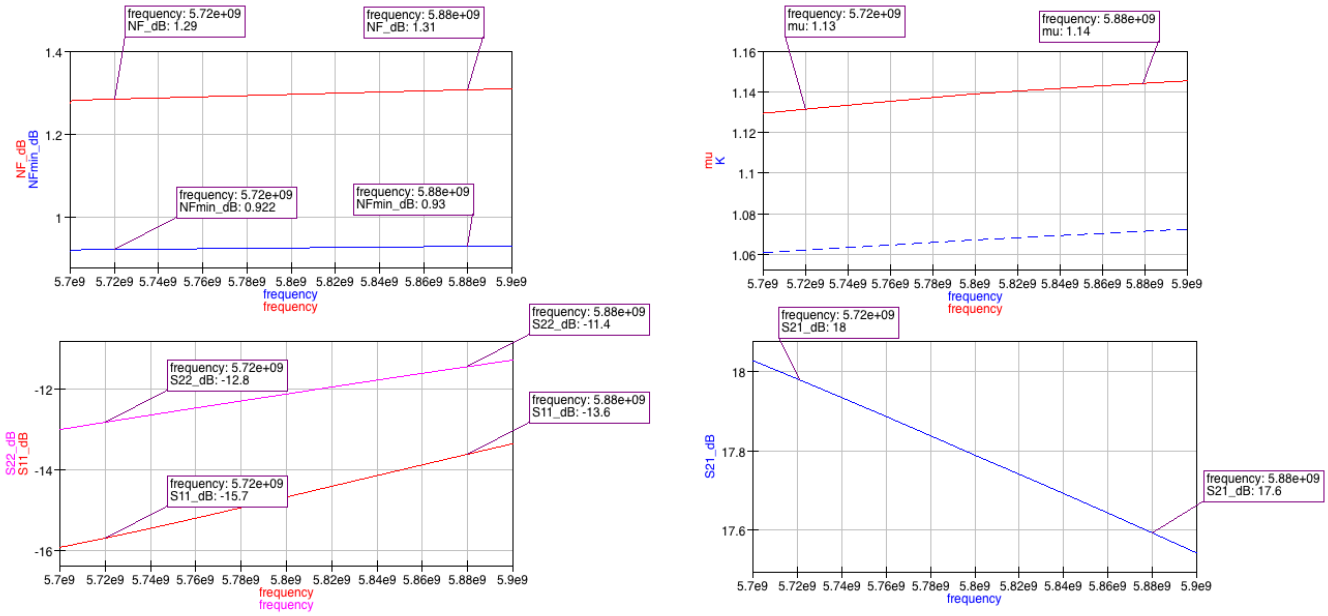


Figure 13: Noise figure, S11, S22, S21 and stability factor of the final LNA