CHAPTER 5

SIMULATION RESULTS

5.1 5 Level Cascaded H-Bridge multilevel inverter

The following are the results for the 5 Level casade H-Bridge multilevel inverter

To get the 5 level output waveform in CHB Topology the switches S_1, S_2, S_6 are turned on to get $+V_{dc}$. S_1, S_2, S_5, S_6 are turned on to get $+2V_{dc}$. S_4, S_7, S_8 are turned on to get $-V_{dc}$. S_3, S_4, S_7, S_8, are turned on to get $-2V_{dc}$. And to get smoth waveforms at the output LC filter is designed, and having a load of impedance Z = 90 Ω.

Table 5.1 Design parameters of 5 Level CHB

Parameter	Value
Input voltage	115V
Output voltage	230V
Output current	2.55A
Load resistor	90Ω
Filter inductor	35mH
Filter capacitor	5.5µF
Operating frequency of inverter	2500Hz
Output frequency	50Hz
Modulation index (m_a)	0.85

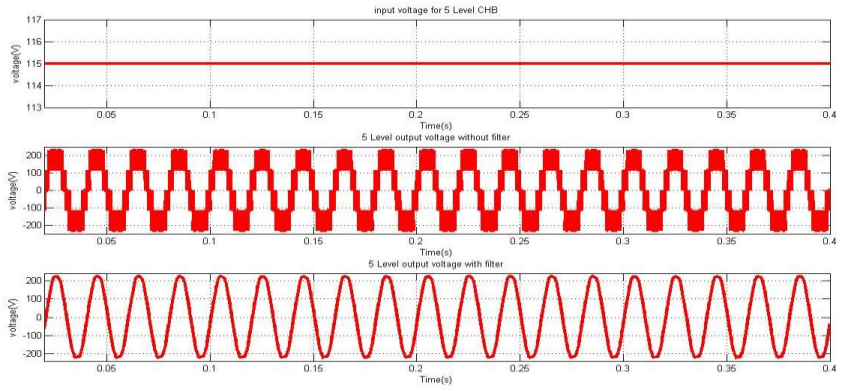

Fig.5.1 CHB 5 Level output voltage waveforms

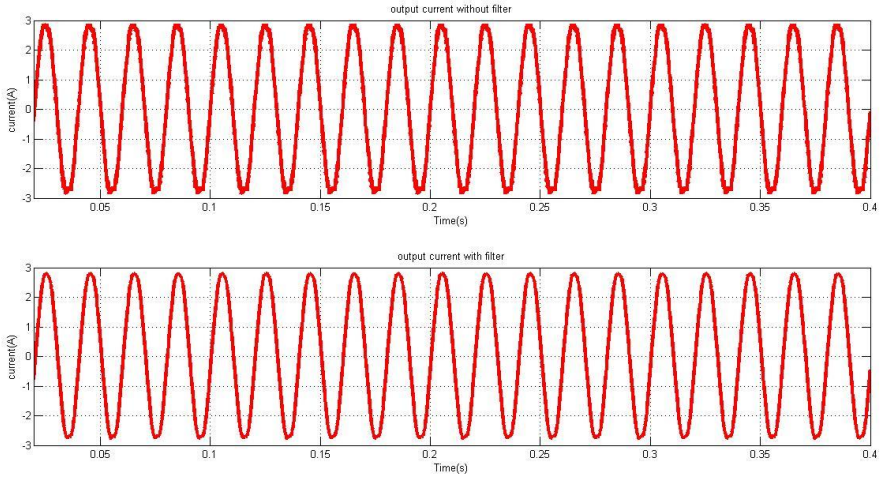

Fig.5.2 CHB 5 Level output current waveforms

The stepped 5 Level output voltage across the load is shown in fig 5.1(b), after passing that stepped waveform through LC filter the smooth 5 Level output waveform is obtained as shown in fig 5.1(c), the output current waveform for the 5 Level CHB without filter is shown in fig 5.2(a) and with filter is shown in fig.5.2(b). The input voltage given to the 5 Level CHB is 115V is as shown in fig.5.1(a).

The total harmonic distortion obtained for 5 Level CHB stepped output is 28.79% as shown in fig 5.3 and reduced to 2.99% as shown in fig.5.4 using LC filter

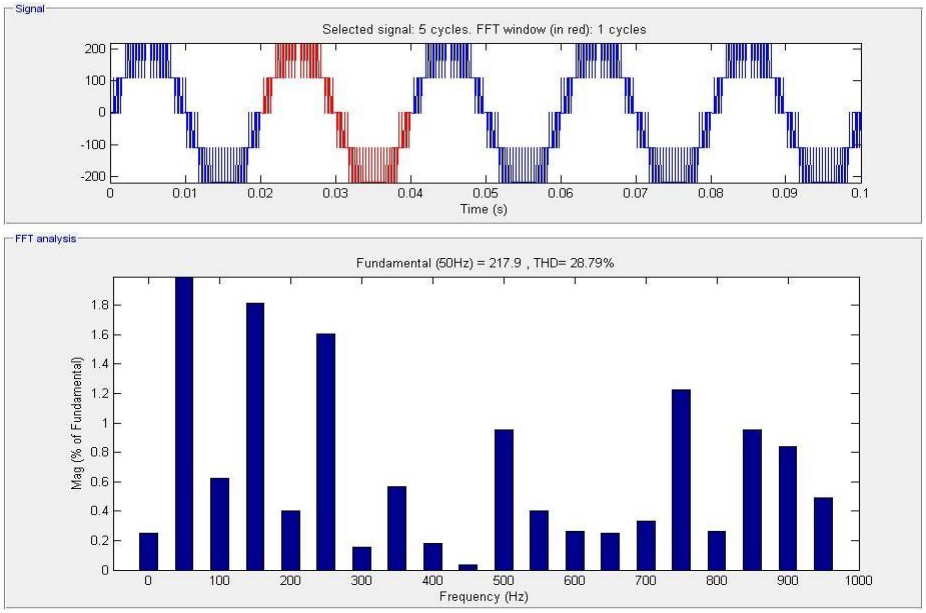

Fig.5.3 THD for CHB 5 Level output without filter

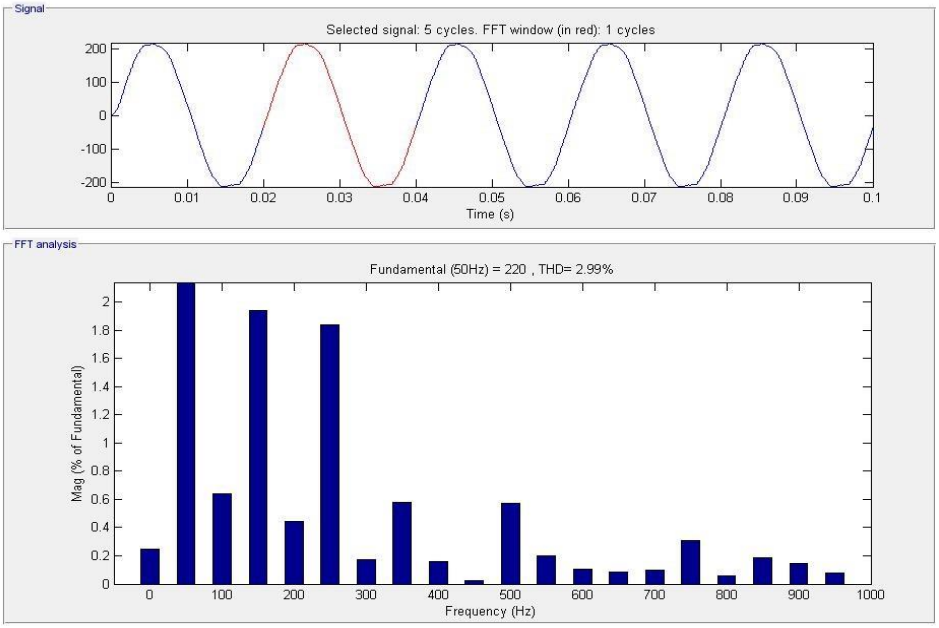

Fig.5.4 THD for CHB 5 Level output with filter

The gating pulse given the switches to get 5 Level positive cycle is shown in the fig.5.5

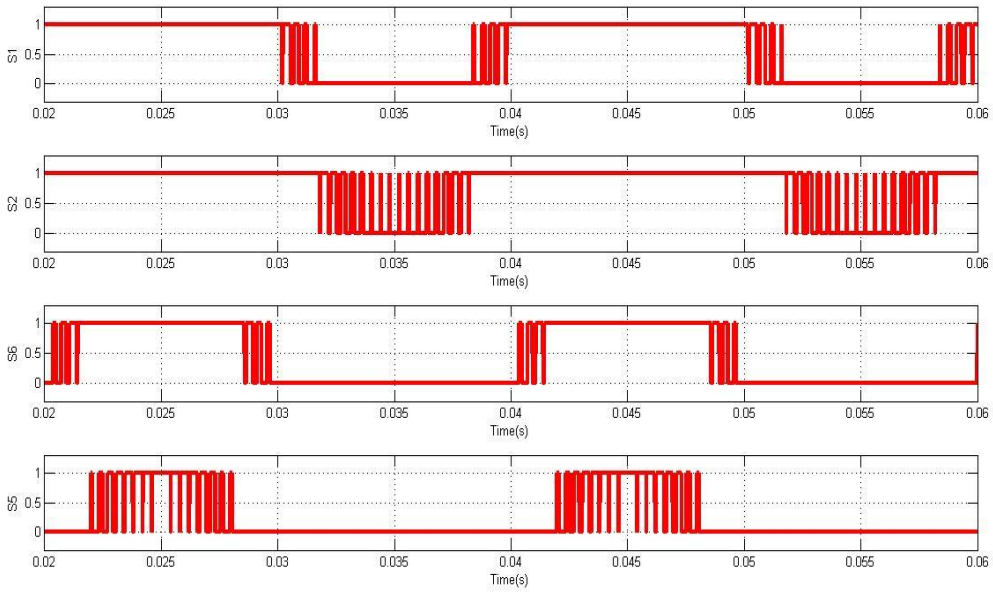

Fig 5.5 Gating pulses for positive half cycle of 5 Level CHB

The gating pulses given to the switches to get 5 Level negative cycle is shown in fig 5.6

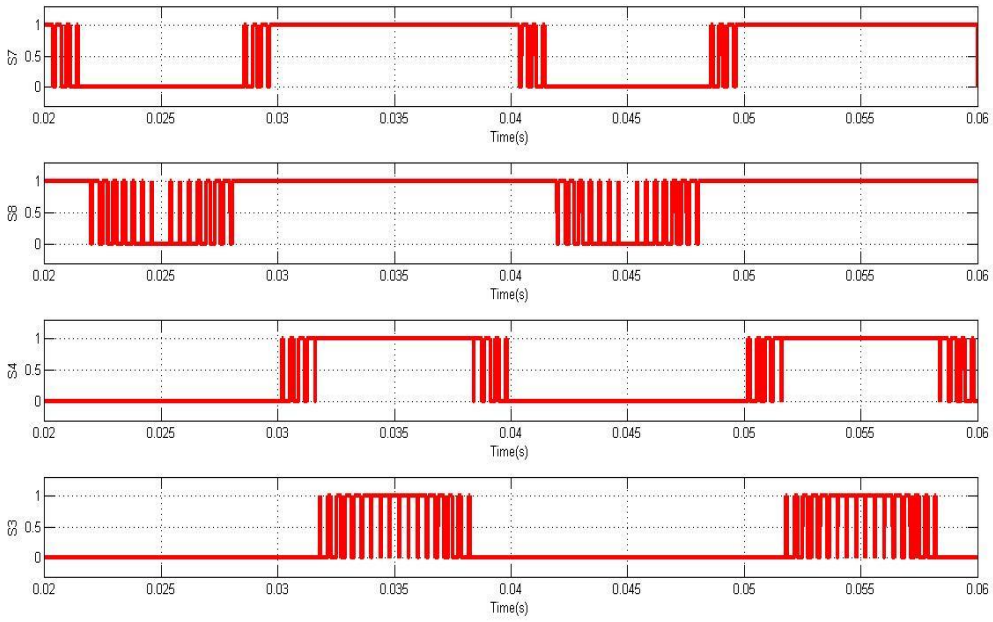

Fig. 5.6 Gating pulse for negative half cycle of 5 Level CHB

5.2 9 Level Cascaded H-Bridge multilevel inverter

The following are the results of the 9 Level Cascade multilevel inverter topology

To get 9 Level output the switches of CHB are turned on and off accordingly. To get $+V_{dc}$ the switches S_1, S_2, S_6, S_{10}, S_{14} are turned on.

Table 5.2 Design parameters of 9 Level CHB

Parameter	Value
Input voltage	57.5V
Output voltage	230V
Output current	2.55A
Load resistor	90Ω
Filter inductor	20mH
Filter capacitor	3.5μF
Operating frequency of inverter	2500Hz
Output frequency	50Hz
Modulation index (m_a)	0.85

To get $2V_{dc}$ the switches S_1, S_2, S_6, S_{10}, S_{13}, S_{14} are turned on To get $3V_{dc}$ the switches S_1, S_2, S_6, S_9, S_{10}, S_{13}, S_{14} are turned on. To get $4V_{dc}$ the swithes S_1, S_2, S_5, S_6, S_9, S_{10}, S_{13}, S_{14} are turned on.

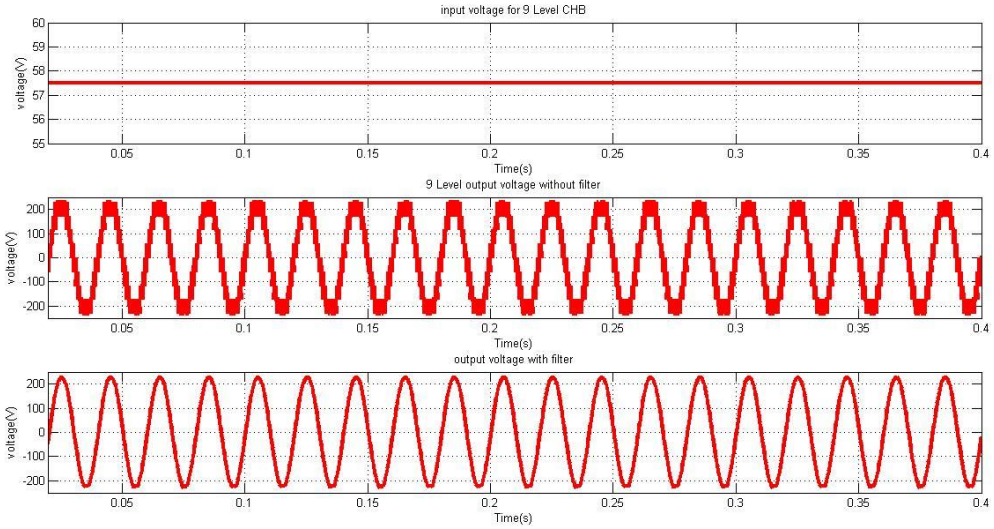

Fig.5.7 CHB 9 Level output voltage waveforms

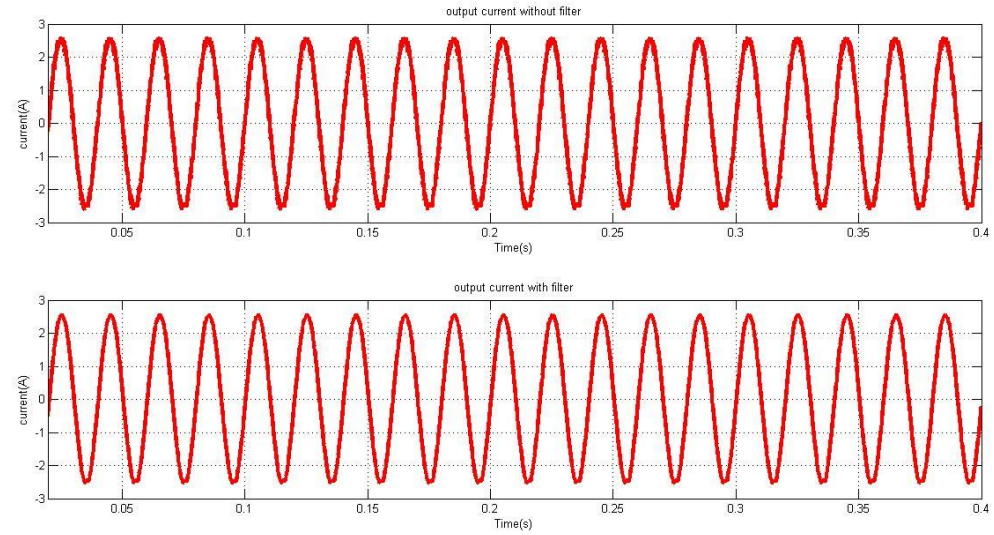

Fig.5.8 CHB 9 Level output current waveforms

To get $-V_{dc}$ the switches S_4, S_8, S_{12}, S_{15}, S_{16} are turned on. To get $-2V_{dc}$ the switches S_3, S_4, S_8, S_{12}, S_{15}, S_{16} are turned on. To get $-3V_{dc}$ the switches S_3, S_4, S_7, S_8, S_{12}, S_{15}, S_{16} are turned on. To get $-4V_{dc}$ the switches S_3, S_4, S_7, S_8, S_{11}, S_{12}, S_{15}, S_{16} are turned on. The load impedance of the CHB 9 Level multilevel inverter is Z = 90Ω. The filter design is same as the design of CHB 5 Level multilevel inverter.the 9 level CHB output waveforms are shown in fig.5.7 and fig.5.8.

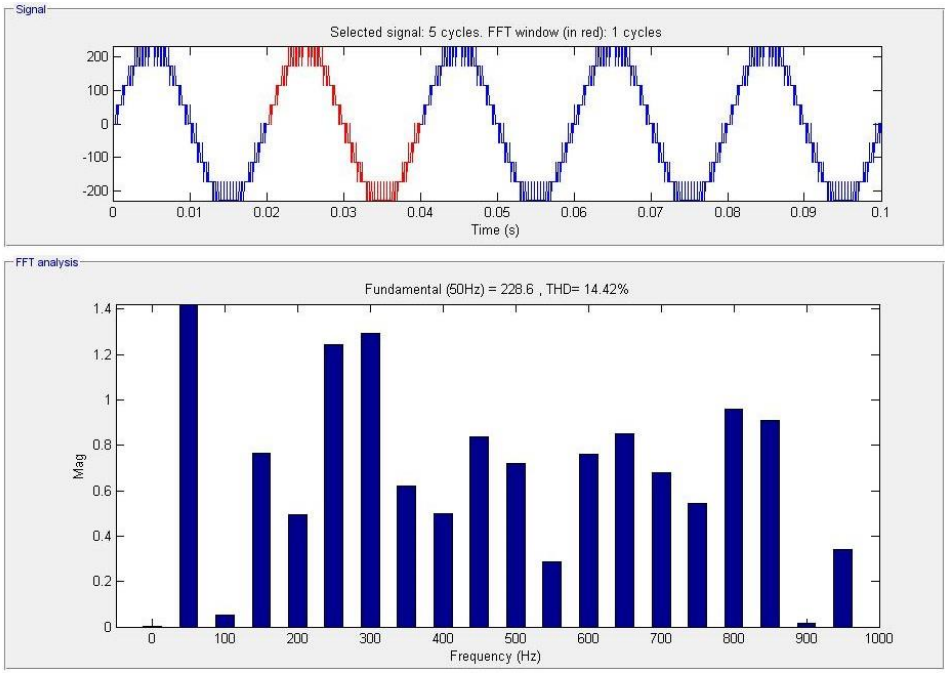

Fig.5.9 THD for CHB 9 Level output without filter

the 9 Level stepped output voltage is shown in fig 5.7(b), after passing that stepped output through filter the smooth sinusoidal waveform is obtained as shown in fig.5.7(c), the load current of CHB (level inverter is shown in fig.5.8) The total harmonic distortion for the CHB 9 Level inverter without filter is shown in fig.5.9 and with filter is shown in fig.5.10

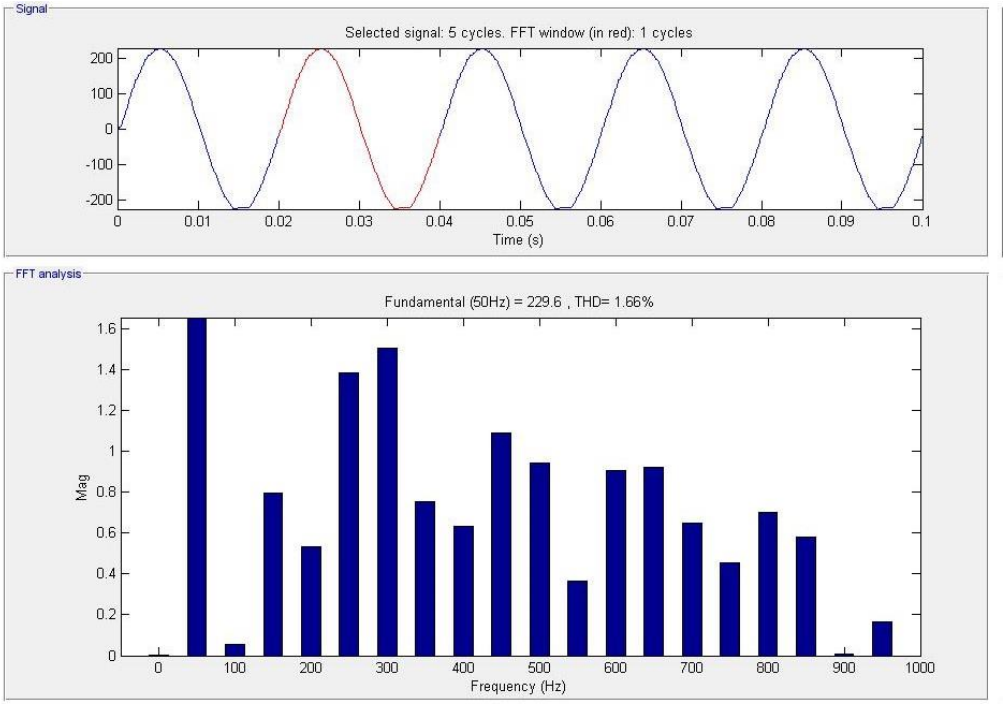

Fig.5.10 THD for CHB 9 Level output with filter

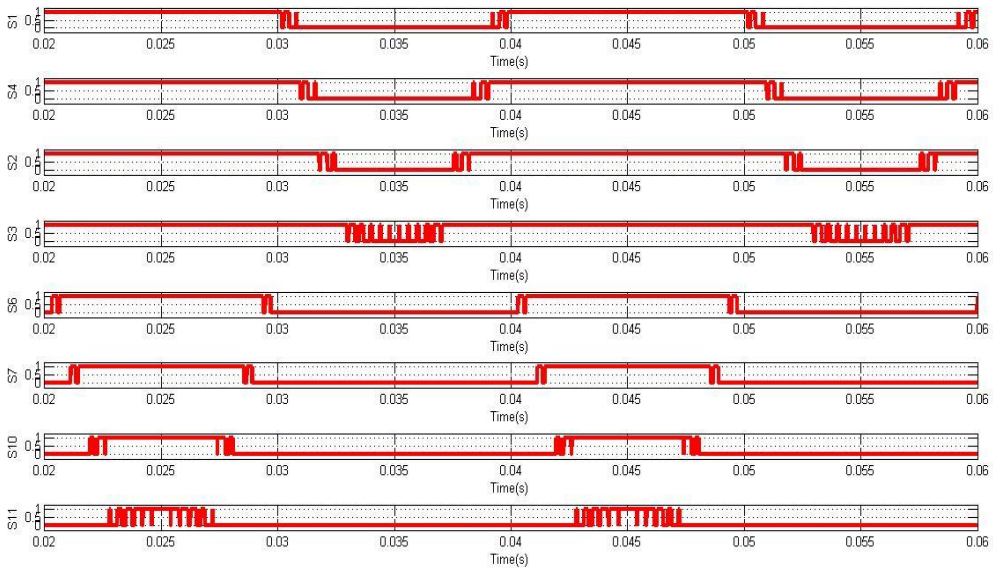

Fig.5.11 Gating pulses for positive half cycle of 9 Level CHB

The gating pulses required to get the positive half cycle of 9 level output is shown in fig 5.11

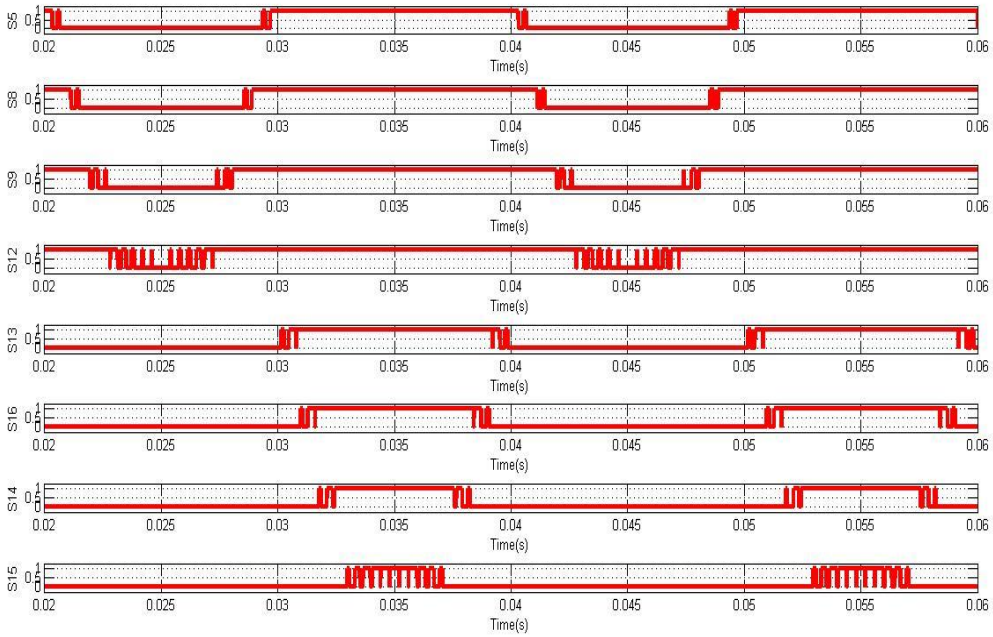

Fig.5.12 Gating pulses for negative half cycle of 9 Level CHB

The gating pulses required to get the negative half cycle of 9 Level output is shown in fig.5.12

5.3 5 Level cascaded switched-Diode multilevel inverter

The following are the results of 5 Level cascaded switched-Diode multilevel inverter

Table 5.3 Design parameters of 5 Level CSD

Parameter	Value
Input voltage	115V
Output voltage	230V
Output current	2.55A
Load resistor	90Ω
Filter inductor	35mH
Filter capacitor	5.5µF
Operating frequency of inverter	2500Hz
Output frequency	50Hz
Modulation index (m_a)	0.85

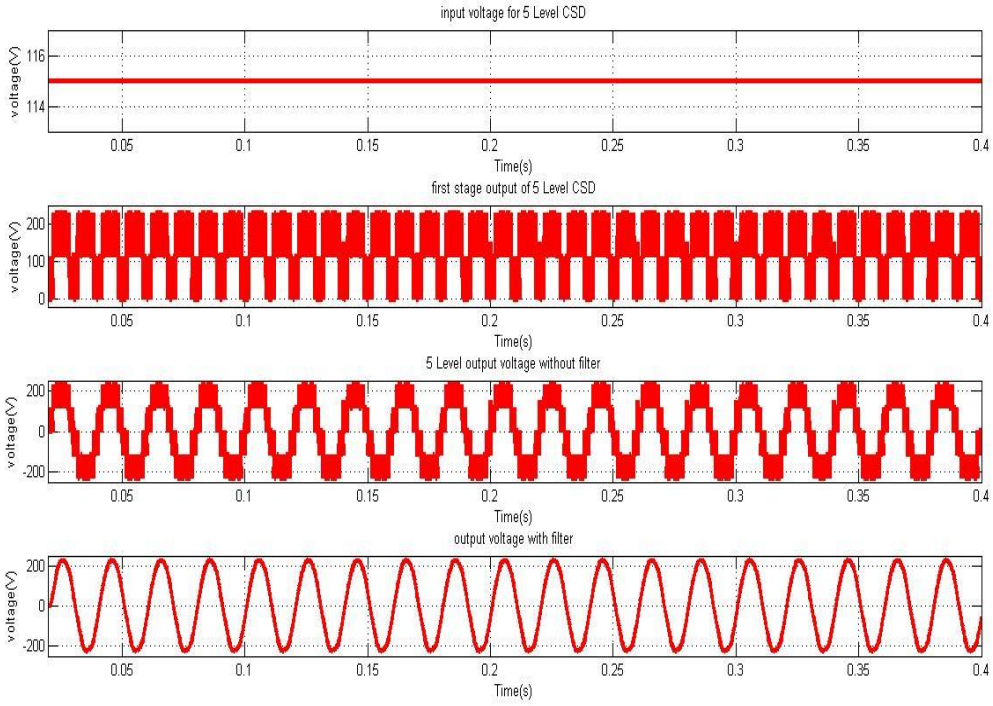

Fig.5.13 CSD 5 Level ouput voltage waveforms

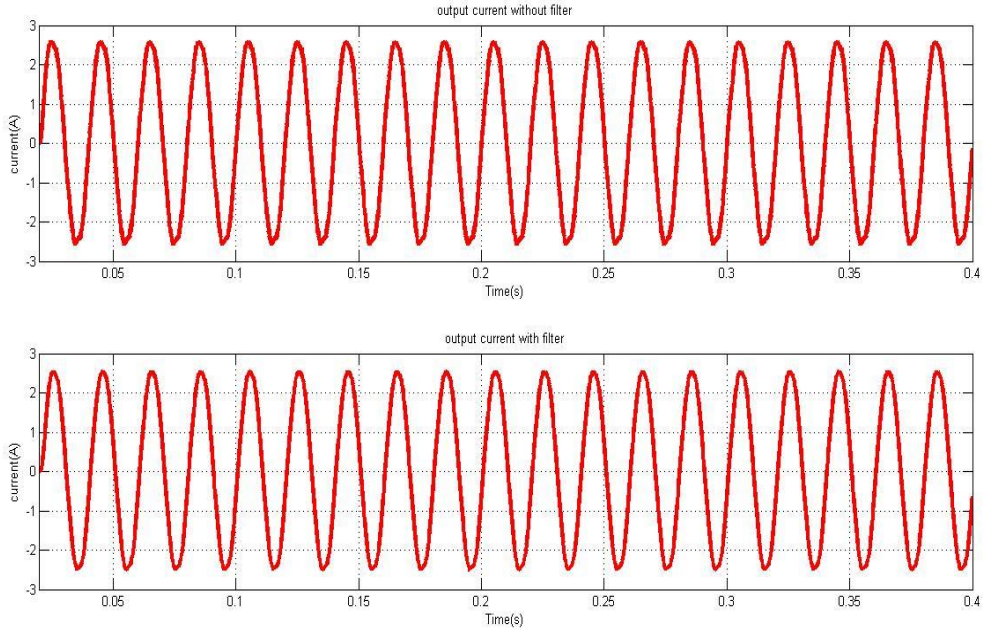

Fig.5.14 CSD 5 Level output current waveforms

To get the 5 Level output of Cascaded switched-Diode multilevel inverter the following switching sequences are followed. To get $+V_{dc}$ the switches S_{11}, S_1, S_2 are turned on. To get $+2V_{dc}$ the switches S_{11}, S_{12}, S_1, S_2 are turned on.

To get $-V_{dc}$ the switches S_{11}, S_3, S_4 are turned on. To get $-2V_{dcc}$ the switches S_{11}, S_{12}, S_3, S_4 are turned on. The load impedance of a 5 Level cascaded switche-Diode multilevel inverter is Z = 90Ω. The output of first stage 5 Leve CSD is shown in fig.5.13(b). in first stage only positive waveforms are obtained. In second stage positive waveforms can be converted into sinusoidal waveforms by using inverter. The final 5 Level stepped output waveform is shown in fig.5.13(c). after passing that stepped waveform into filter the smooth waveform is obtained as shown in fig.5.13(d). the output load current is shown in fig.5.14.

The total harmonic distortion of stepped 5 Level CSD output without filter is shown in fig.5.15 and with filter is shown in fig.5.16

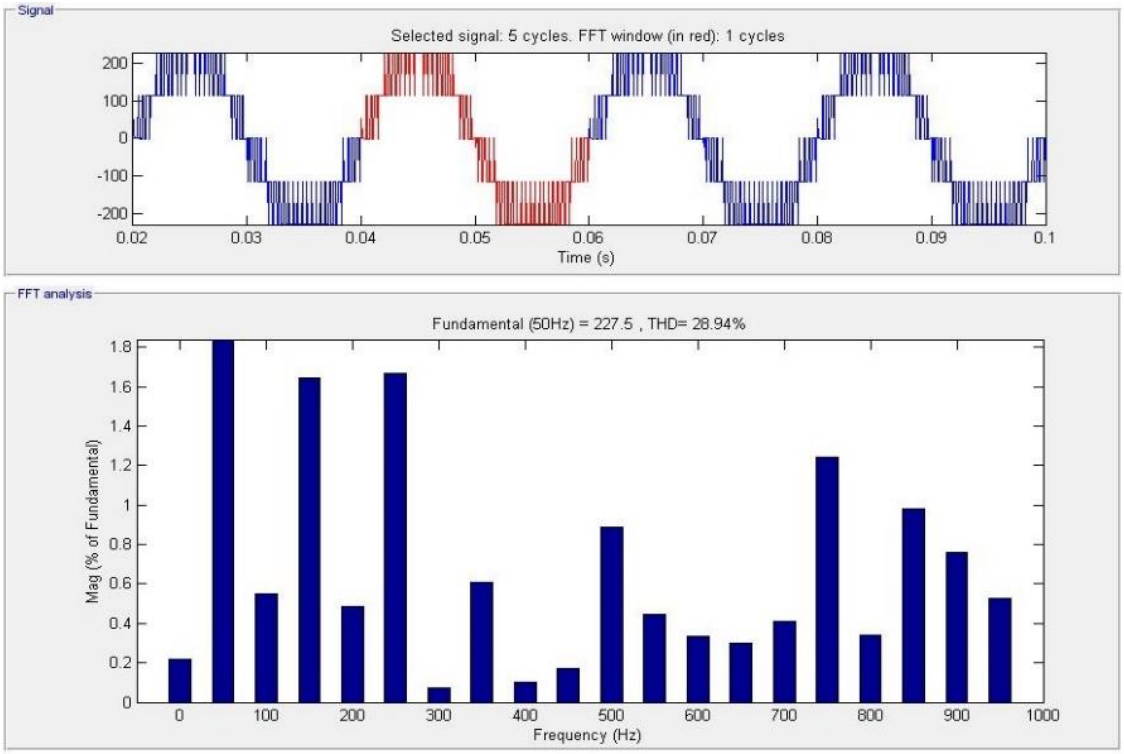

Fig.5.15 THD for CSD 5 Level output without filter

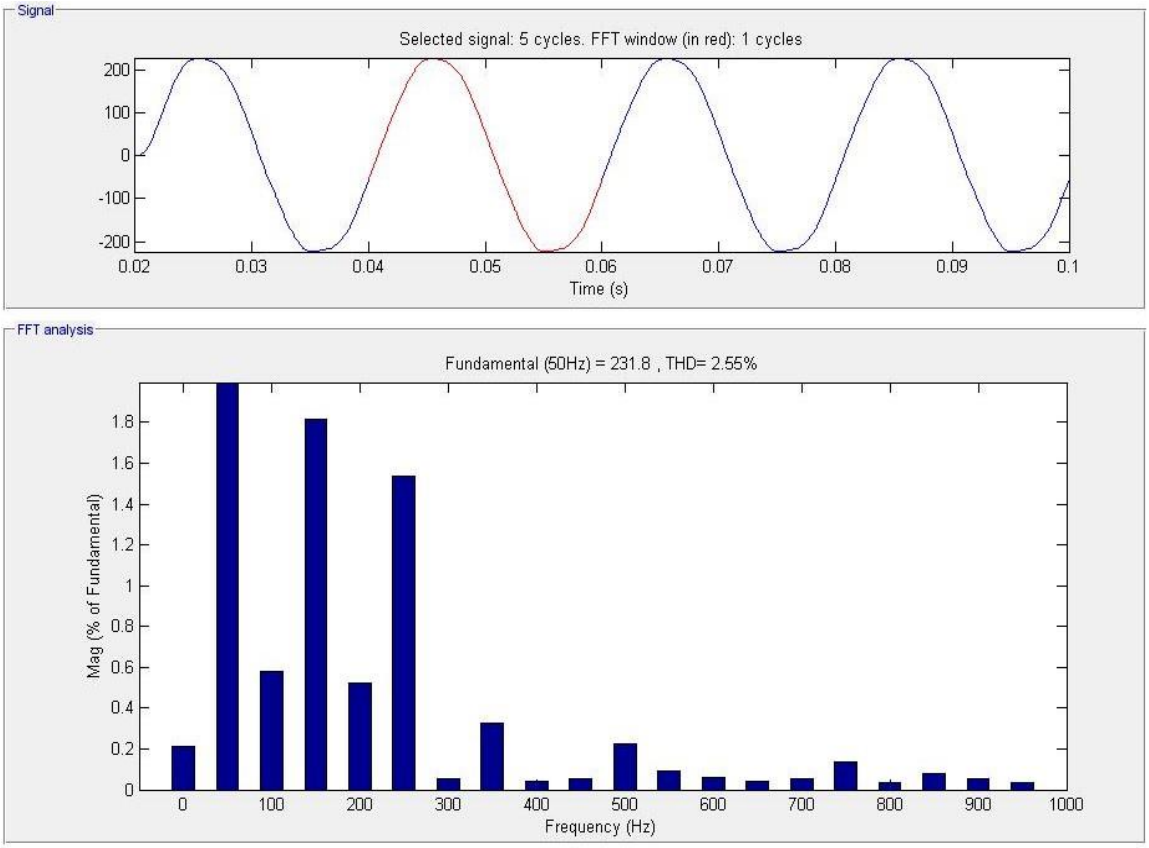

Fig.5.16 THD for CSD 5 Level output with filter

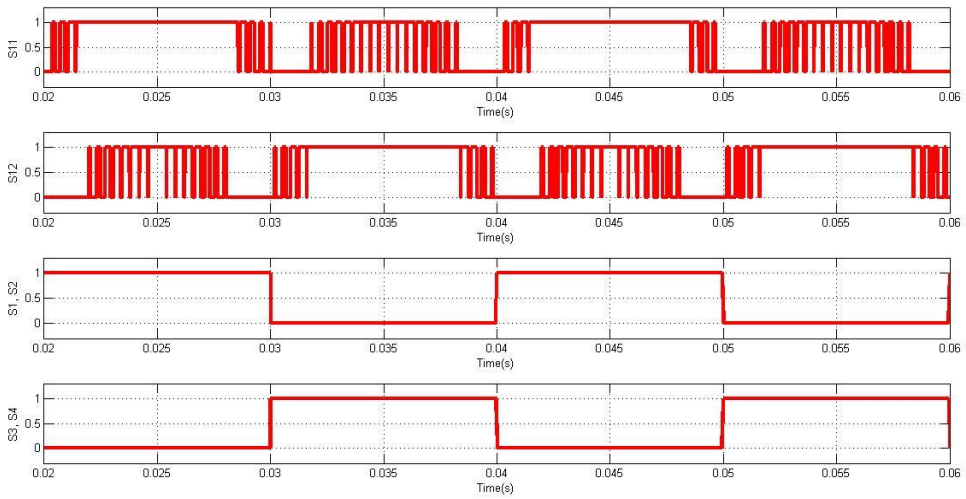

Fig.5.17 Gating pulses for 5 Level CSD

The gating pulses for CSD 5 Level are shown in fig.5.17

5.4 9 Level Cascaded Switched-Diode multilevel inverter

The following are the results of 9 Level cascaded switched-Diode multilevel inverter

To get the 9 Level output the switches of CSD are turned on in the following sequence. To get $+V_{dc}$ the switches S_{11}, S_1, S_2 are turned on. To get $+2V_{dc}$ the switches S_{11}, S_{12}, S_1, S_2 are turned on. To get $+3V_{dc}$ the switches S_{11}, S_{12}, S_{13}, S_1, S_2 are turned on. To get $+4V_{dc}$ the switches S_{11}, S_{12}, S_{13}, S_{14}, S_1, S_2 are turned on.

Table 5.4 Design parameters of 9 Level CSD

Parameter	Value
Input voltage	57.5V
Output voltage	230V
Output current	2.55A
Load resistor	90Ω
Filter inductor	20mH
Filter capacitor	3.5µF
Operating frequency of inverter	2500Hz
Output frequency	50Hz
Modulation index (m_a)	0.85

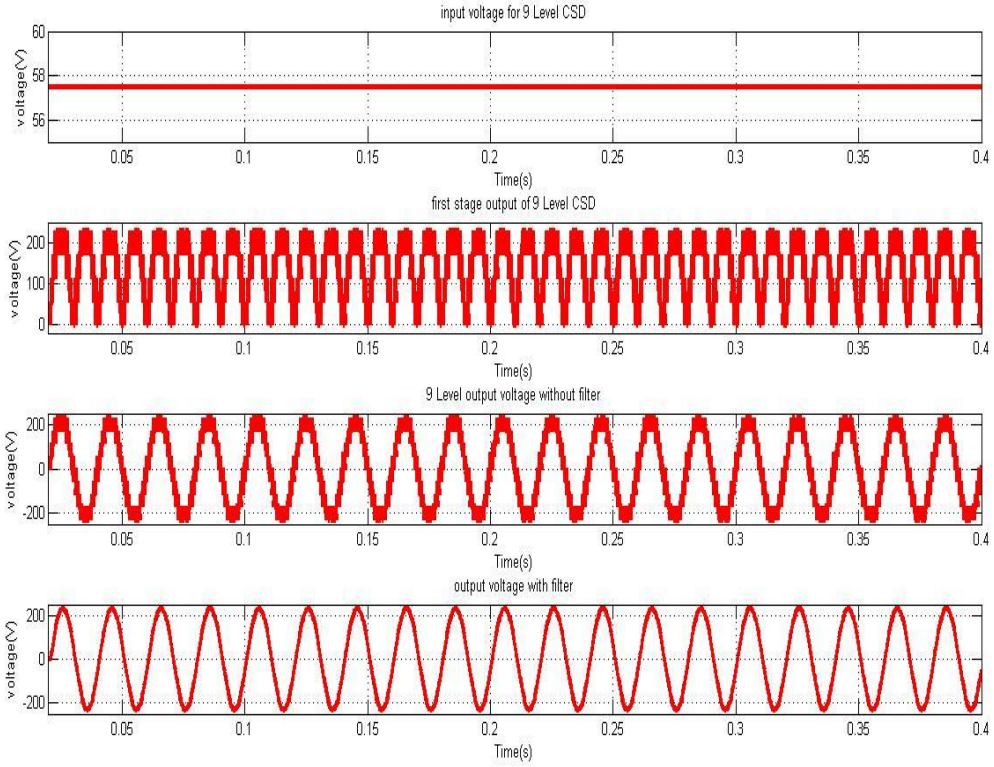

Fig.5.18 CSD 9 Level output voltage waveforms

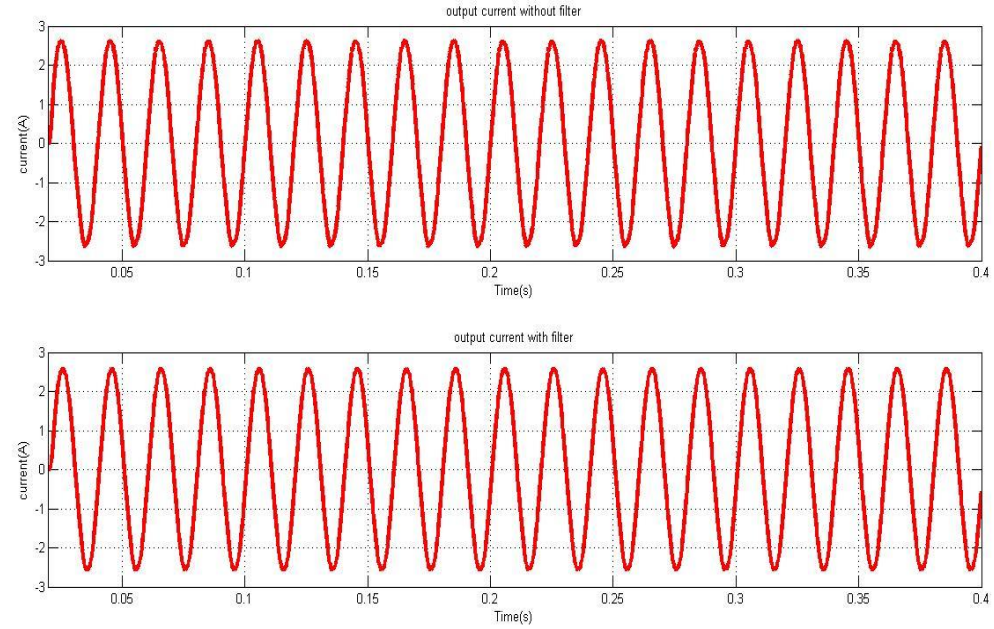

Fig.5.19 CSD 9 Level output current waveforms

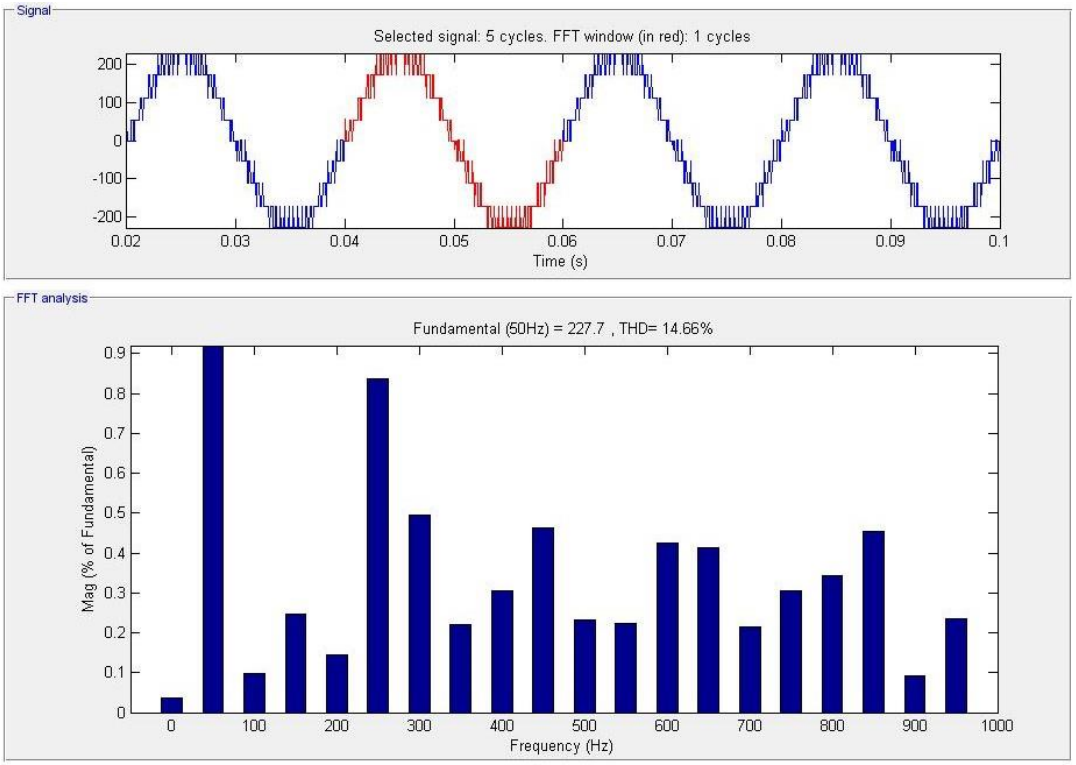

Fig.5.20 THD for CSD 9 Level output without filter

To get $-V_{dc}$ the switches S_{11}, S_3, S_4 are turned on. To get $-2V_{dc}$ the switches S_{11}, S_{12}, S_3, S_4 are turned on. To get $-3V_{dc}$ the switches S_{11}, S_{12}, S_{13}, S_3, S_4 are turned on. To get $-4V_{dc}$ the switches S_{11}, S_{12}, S_{13}, S_{14}, S_3, S_4 are turned on. The load impedance of a 5 Level CSD is Z = 90 Ω. The 9 Level CSD first stage stepped output is shown in fig.5.18(b). the second stage 9 Level stepped CSD output is shown in fig.5.18(c). the stepped output after passing through filter becomes smooth as shown in fig.5.18(d). the load current of 9 Level CSD is as shown in fig.5.19.

Total harmonic distortion for CSD 9 Level Stepped output without filter is shown in fig.5.20 and with filter is shown in fig.5.21

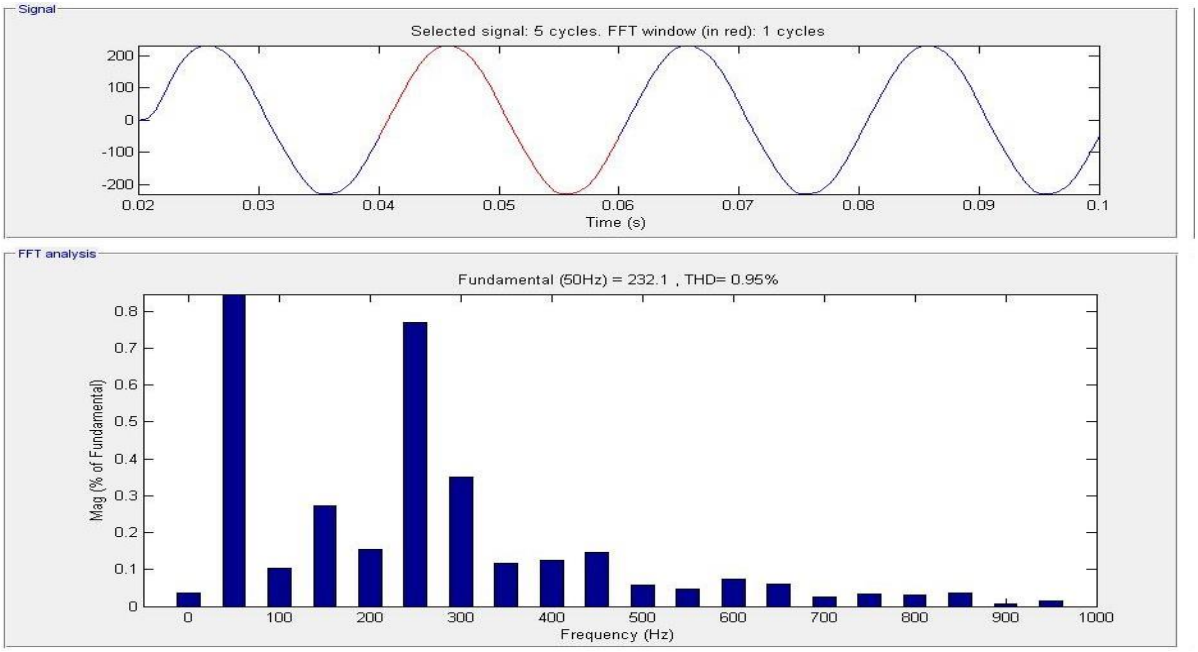

Fig.5.21 THD for CSD 9 Level output with filter

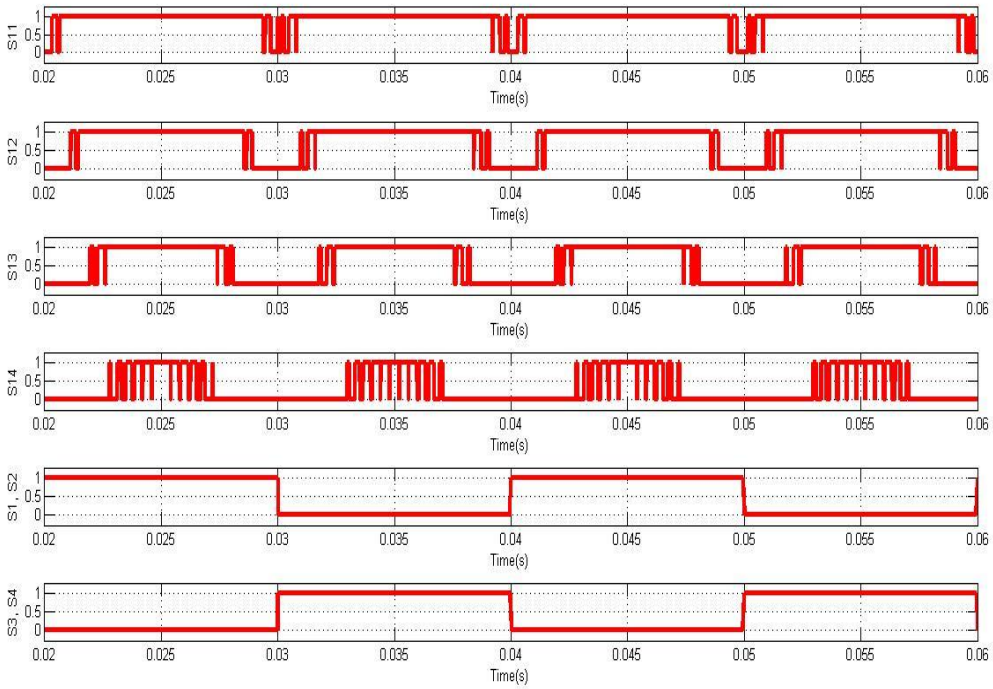

Fig.5.22 Gating pulses for 9 Level CSD

The gating pulses required to get first stage output waveform is as shown in fig.5.22.