CHAPTER 4

CASCADED SWITCHED DIODE MLI OPERATION AND CONTROL

4.1 Introduction

As the multilevel inverter classified into three main types in the cascaded version, the third main type is the cascaded switched diode multilevel inverter which is used in renewable energy integration. The input energy sources are like solar, fuel cell, wind, tidal, etc. In this project the input energy sources used are solar and fuel cells. By taking the wind and tidal energy sources as input sources the complexity of the Simulink model increases very high. In the past decade, many multilevel inverter topologies were used or studied for renewable energy integration by taking input sources like wind, tidal, fuel cell, solar energies, etc. High-quality voltage waveforms can be obtained from these multilevel inverters where the frequency required for power switches involved in the Simulink model is very low when compared to the other conventional inverters. Due to the simple structure of the cascaded switched diode multilevel inverter, it has attracted more attention and also had an advantage like it has individual dc power sources for each cascaded unit. The cascaded switched diode multilevel inverter has a great potential to be employed in renewable energy integration. In the previous version or type of cascaded MLI, the cascaded H-bridge requires more switches and its related gate drivers when compared to cascaded switched diode multilevel inverter which may lead to an expensive and complex overall system. Then the second type of cascade MLI, cascade half-bridge MLI introduced with less number of switches and gate drivers which produces more voltage levels when compared to the cascade H-bridge MLI but due to the lack of a path for reverse load currents under R-L loads, high voltage spikes occur at the base of stepped output voltage, which tends to deteriorate the power quality. Therefore the cascaded switched diode multilevel inverter is implemented to overcome the difficulties obtained by using the previous version topologies of a cascaded multilevel inverter.

4.2 Topology of cascaded switched diode multilevel inverter

The cascaded switched diode is done under two stages like the first stage and second stage respectively.

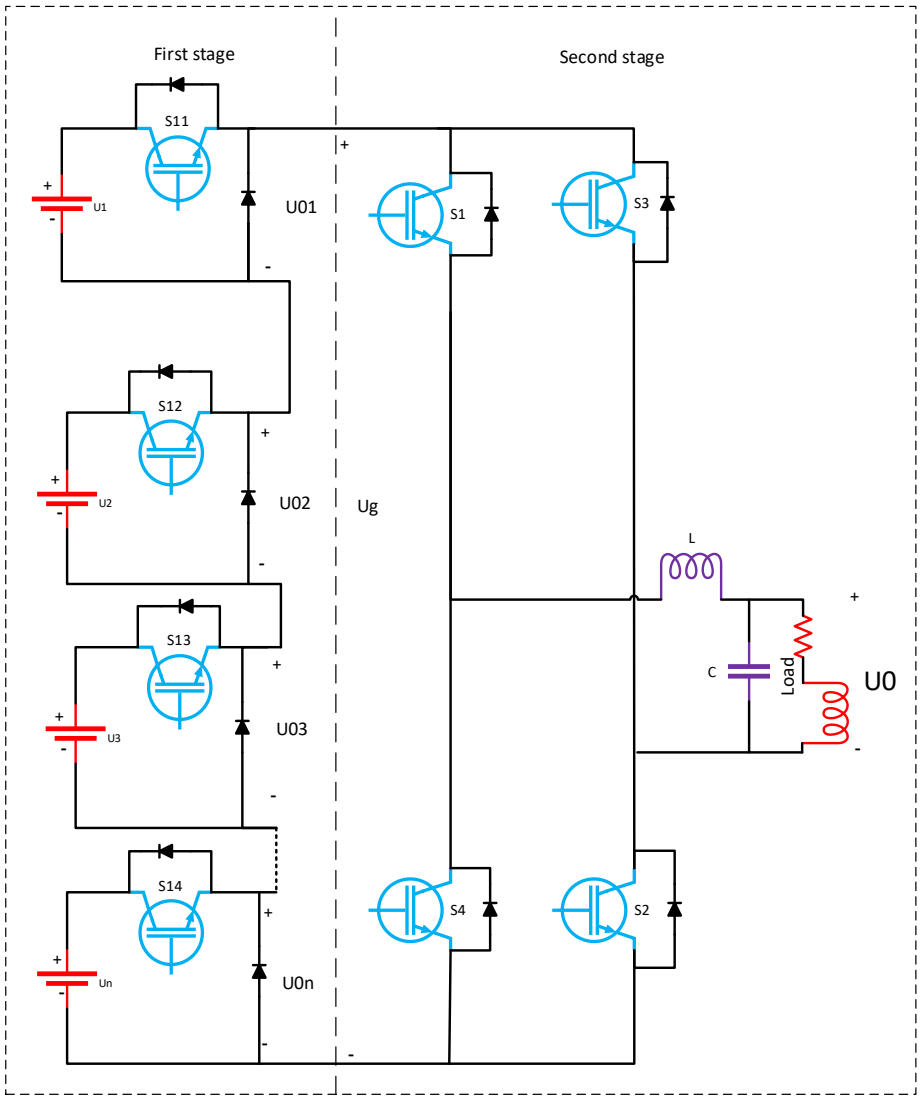

Fig 4.1 The structure of the developed two-staged CSD Topology.

Renewable energy sources act as the DC power sources of multilevel inverter in renewable energy integration as shown in fig 1.1. In practical conditions, because of all sorts of complex factors, the DC supply always fluctuates. For example, the outputs of the solar cell can change depending on factors like temperature, light intensity and so on, which results in the output mixed with low-frequency ripples. When using a DC supply with low-frequency ripples as the input of multilevel inverters, conventional modulation techniques are unable to meet the need for industrial applications. Therefore, a technique that can be used to meet the needs is to be

developed and also for the accurate static performance and a strong suppression ability against the interference in DC sources. The SPWM technique is introduced for controlling the proposed CSD multilevel topology. The staircase like output voltage waveforms will be obtained and a strong inhibition ability against the interferences in DC sources is achieved.

4.3 Switching states for positive and negative output voltage waveform.

Fig 4.1 shows the proposed two-stage CSD topology. The proposed topology had a cascaded switched-diode converter with a full-bridge inverter, where n is the number of the cascaded basic units. The basic unit 1 consists of the DC voltage source or a capacitor with a DC voltage equal to u_1 and a switch S_{11} with its internal reverse diode and a separate diode named D_1 as shown in fig 4.1. It is also known that the parallel connection of the diode D_1 avoids the shoot-through phenomenon of a bridge arm. The voltage obtained at the basic unit 1 is u_{o1} and it is the combination of the input voltage u_1 and the voltage at the switch S_{11}. If the switch is open voltage is present and if the switched is closed the voltage is zero. When S11 is on, S12 ⋯ S1n is off. The cascading layout of n basic units form the first stage, as shown in Fig. 4.1. The maximum output voltage of the first stage is given as follows:

$$u_g = u_{o1} + u_{o2} + \cdots + u_{on} \tag{4.1}$$

The first stage converter always produces the positive staircase waveform and for both the positive and negative output voltage waveforms both the converters are to be operated. for states of switches S_{11}, S_{12}, ⋯, $S_{1(n-1)}$, S_{1n}, 2^n different values of u_g are obtained, as listed in Table 4.1. Table 4.2 lists the switch state analysis with respect to the positive sign or negative sign of a reference voltage u_{ref}. It is clear that the employment of the second-stage achieves both the positive and negative halves of the output voltage. All the Dc voltage sources are equal to u_{dc} under the symmetric case, the number of output voltage levels N_{level} and the total number of switches N_{IGBT} required are calculated as follows:

$$N_{level} = 2n + 1 \tag{4.2}$$

then the number of the required switches for a N_{Level} output voltage is derived as follows:

$$N_{IGBT} = (N_{level} + 7)/ 2 \tag{4.3}$$

Table 4.1 Values of u_g w.r.t switching states of the first stage.

State	Switches states						u_g
	S_{11}	S_{12}	S_{13}	…….	$S_{1(n-11}$	S_{1n}	
1	off	off	off	…….	off	off	0
2	on	off	off	…….	off	off	u_1
……	…..	…..	….	…….	…..	…..	……
n	off	Off	off	…….	off	on	u_n
n+1	on	on	off	…….	off	off	u_{1+} u_2
……	…..	…..	……	…….	…….	…	…….
2^n	on	on	on	…….	on	on	$\sum_{i=1}^{n} Ui$

Table 4.2 Values of u_o w.r.t switching states of second stage

State	Switched states				u_o
	S_1	S_2	S_3	S_4	
1	On	On	Off	Off	u_g
2	Off	Off	On	On	$-u_g$

Table 4.1 consists of the values of the u_g with respect to switch states of the first stage and table 4.2 consists of the values of the u_o with respect to switch states of the second stage. The tables are as follows:

The 5-level reduced switch multilevel inverter i.e. cascaded switched diode structure is shown in fig.4.2.

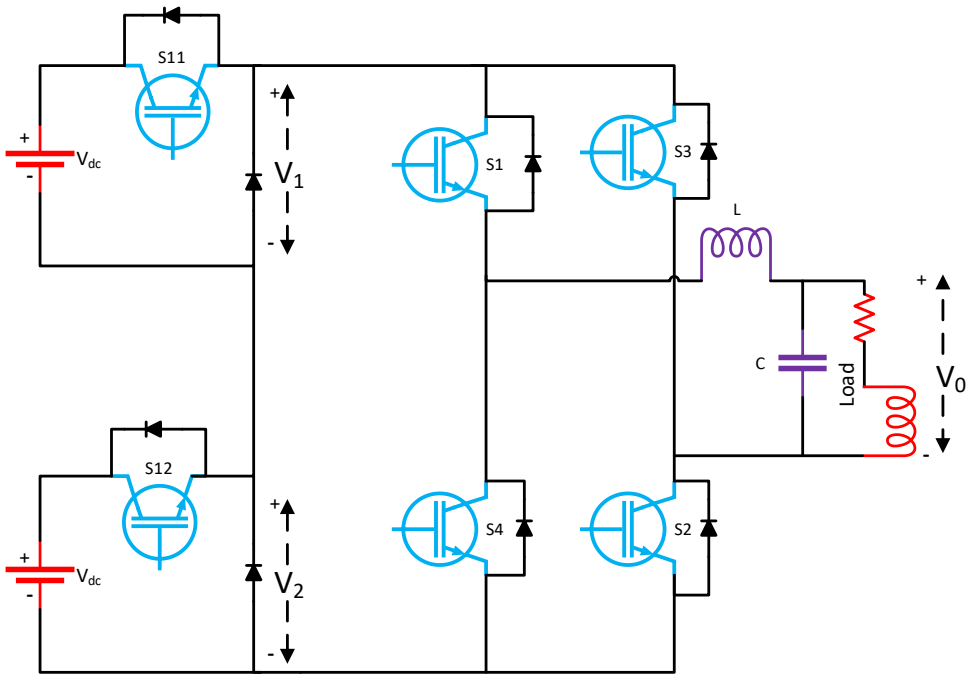

Fig. 4.2 5 Level CSD Structure

To get five level stepped waveform in the output the switches are turned on and off accordingly. The modes of operation of 5 Level CSD is as shown in table.4.3.

Table.4.3 Modes of operation of 5 Level CSD

	S11	S12	S1	S2	S3	S4
V_{dc}	1	0	1	1	0	0
$2V_{dc}$	1	1	1	1	0	0
0	0	0	0	0	0	0
$-V_{dc}$	1	0	0	0	1	1
$-2V_{dc}$	1	1	0	0	1	1

The 9 level cascaded switched diode structure is shown in fig.4.3

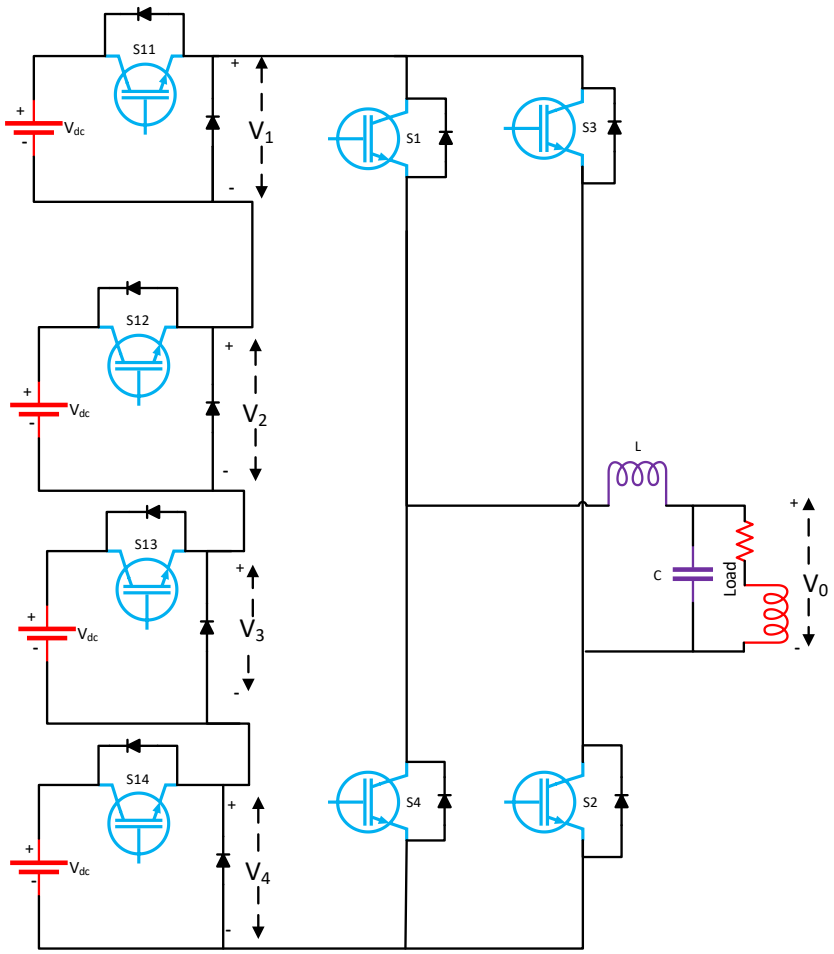

Fig.4.3 9 Level CSD structure

To get nine level stepped waveform in the output the switches are turned on and off accordingly. The modes of operation of 5 Level CSD is as shown in table.4.4.

Table.4.4 modes of operation of 9 Level CSD

	S11	S12	S13	S14	Sg	S1	S2	S3	S4
V_{dc}	1	0	0	0	1	1	1	0	0
$2V_{dc}$	1	1	0	0	0	1	1	0	0
$3V_{dc}$	1	1	1	0	0	1	1	0	0
$4V_{dc}$	1	1	1	1	0	1	1	0	0
0	0	0	0	0	0	0	0	0	0
$-V_{dc}$	1	0	0	0	1	0	0	1	1
$-2V_{dc}$	1	1	0	0	0	0	0	1	1
$-3V_{dc}$	1	1	1	0	0	0	0	1	1
$-4V_{dc}$	1	1	1	1	0	0	0	1	1

4.4 Carrier based PWM Techniques

There are different types of inverters and these inverters are used in their respective applications. To control switching pattern of these inverters, different PWM techniques are used such as SPWM, SVPWM, Selective Harmonic Elimination (SHE). SPWM is simplest method that can be implemented for inverters. The principle of SPWM is illustrated as follow, where sinusoidal modulating wave is compared with triangular carrier wave to give two stage (high or low). The modulating wave is compared with triangular wave, if the modulating wave amplitude is greater than amplitude of carrier wave results in high state otherwise remains at low state. At high state switch becomes on and at low state it will be turn off. SPWM technique is used to control the switching pattern of inverter which results in reduction of THD for output voltage. Any change in modulating waveform results in load current harmonics and causes EMI (Electro-Magnetic Interference), power loss, etc. PWM technique is effective modulation technique and it does not require any additional components and eliminates lower harmonics easily.

For multi carrier SPWM technique (m-1) carrier waves are required for m-Level inverter. The amplitude and frequency all carrier waves must be same.

The frequency modulation index is given by

$$m_f = {f_c}/{f_m} \tag{4.4}$$

Where f_c is carrier wave frequency and f_m is modulating wave frequency

$$m_a = {V_m}/{V_c} \tag{4.5}$$

Where V_m is the peak value of modulating wave and V_c is peak value of each carrier wave.

Multi carrier PWM technique is used to control switching pattern of multilevel inverters. For MLI's carrier based PWM techniques are classified as

1. Single-carrier SPWM
2. Multi-carrier SPWM

The multi-carrier SPWM control techniques are further categorized as

A. Phase shifted SPWM
B. Level shifted SPWM
C. Hybrid (combination of level and phase shifted)

A. Phase shifted SPWM

In the phase shifted SPWM technique all carrier wave has same peak-peak amplitude and same frequency, but there is phase shift between adjacent carrier signals. Phase shift between two carrier waves is given by

$$\emptyset_c = {}^{360}/_{(m-1)} \qquad 4.6$$

B. Level shifted SPWM

Level shifted SPWM technique is categorized as

1. In phase disposition
2. Phase opposition disposition
3. Alternate phase opposition disposition

In phase disposition requires the carrier waves have same amplitude and frequency, where as there is no phase shift between them. But this carrier waves are at different offset value. It is observed that this method has lowest harmonic distortion with high modulation indices as compared to other SPWM methods

In phase opposition disposition technique for m-level inverter m-1 carrier waves are used. In which the carrier wave above the zero reference are in same phase and the carrier waves below the zero reference are also in phase, but the carrier waves below zero reference are mirror image of carrier waves above zero reference. This method has better harmonic performances at lower modulation indices.

In alternate phase opposition disposition technique for m- level inverter, (m-1) carrier waves are 180-degree phase shifted from each other. This means that adjacent carrier waves are mirror image each other.