

A Project Report On

**RENEWABLE ENERGY INTEGRATION USING TWO STAGE
CASCADED SWITCHED DIODE MULTILEVEL INVERTER**

Submitted in Partial Fulfillment of the Requirements For

The Award Of

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IN

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RENEWABLE ENERGY INTEGRATION USING TWO STAGE CASCADED SWITCHED-DIODE MULTILEVEL INVERTER

ABSTRACT

Now a days People use electricity to do many jobs every day for lighting, heating and cooling etc. Despite its great importance in daily life. Most of the electricity is generating through non-renewable sources, as electricity demand is increasing day by day, to meet the demand non-renewable sources are not sufficient and also going to exhaust in future. So present generation technologies utilize renewable sources to reduce carbon emission and emission of other air pollutants, but renewable energy integration is complex.

In this project, a new topology of two-stage cascaded switched-diode multilevel inverter is proposed for medium-voltage renewable energy integration. First, it aims to reduce the number of switches along with its gate drivers. Thus, the installation space and cost of a multilevel inverter are reduced. The spike removal switch added in the first stage of the inverter provided a flowing path for the reverse load current, and as a result, high voltage spikes occurring at the base of the stepped output voltage based upon conventional multilevel inverter topologies are removed. Moreover, to resolve the problems related to DC source fluctuations of multilevel inverter used for renewable energy integration. Multicarrier in phase disposition SPWM technique is developed to control the two-stage cascaded switched-diode multilevel inverter. This new topology of two-stage cascaded switched-diode multilevel inverter is implemented using MATLAB/SIMULINK software.

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LIST OF ABBREVIATIONS

| Abbreviation | Description |
|---------------------|-------------------------------------|
| CHB | : Cascaded H-Bridge |
| CSD | : Cascaded Switched-Diode |
| DC | : Direct Current |
| AC | : Alternating Current |
| DTC | : Direct Torque Control |
| PWM | : Pulse Width Modulation |
| SPWM | : Sinusoidal Pulse Width Modulation |
| MLI | : Multi-Level Inverter |
| OCC | : One Cycle Control |

LIST OF SYMBOLS

| Symbol | : | Description |
|---------------|---|-------------------------|
| V_{dc} | | Input DC voltage |
| U_0 | | Output terminal voltage |
| M | | Meters |
| Ω | | Ohms |
| F | | Farads |
| H | | Henry |
| Hz | | Hertz |
| L | | Inductor |
| C | | Capacitor |
| R | | Resistor |

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CHAPTER 1

INTRODUCTION TO RENEWABLE ENERGY

1.1 Introduction

Electricity is the flow of electrons. Electricity is both a basic part of nature and one of the most commonly used forms of energy. Despite its great importance in routine life, few people maybe stop to think about what life would be like without electricity. Like air and water, people lean towards taking electricity from them. However, people use electricity to do many jobs every day for lighting, heating and cooling homes, powering televisions and computers. The electricity that we use is a secondary energy form because it is produced by converting main sources of energy such as coal, natural gas, nuclear energy, solar energy, and wind energy, into electrical power. Present most of the electricity production is done by using non-renewable resources like coal, gasoline, diesel, petrol, etc. in future non-renewable sources will exhaust. To overcome this problem production of electricity is done by renewable energy resources.

A renewable resource is a reserve that can be used repeatedly and substituted naturally. Renewable energy never runs out, for example, solar energy i.e. heat generates from the sun and never runs out. Examples include oxygen, water, solar energy, and biomass. Gasoline, diesel, natural gas, coal, plastics are other fossil fuels are not renewable. They take millions of years to be made, and cannot be renewed in a human's, or even a nation's generation. Renewable resources typically do not produce pollution or subsidize to global warming. The use of renewable resources and energy sources is increasing worldwide, with certain nations, such as Bhutan, and the US states, such as California, beginning to trust entirely on renewable energy. From 2008 to 2012, the U.S. doubled renewable generation from solar, wind, and geothermal bases. America and Britain are now home to some of the largest wind and solar farmhouses in the world. There are also things called human resources where human's waste is turned into energy. There are many other resources such as water power and Tidal power.

Renewable Energy Integration focuses on integrating renewable energy, distributed generation, energy-storing, thermally stimulated technologies, and demand response into the electric distribution and transmission system. A systems method is being used to conduct

integration advancement and demonstrations to address practical, economic, governing, and institutional barriers for using renewable and distributed systems. In addition to fully addressing functioning issues, the integration also establishes feasible business models for integrating these technologies into bulk planning, grid operations, and demand-side supervision.

The goal of Renewable energy integration is to develop the system design, planning, and process of the electric grid to:

- Decrease carbon productions and releases of other air contaminants through increased use of renewable energy and other clean distributed generation.
- Increase the benefit of use through the integration of distributed systems and customer loads to condense peak load and thus reduced the costs of electricity.
- Support the accomplishment of renewable energy collection standards for renewable energy and energy efficiency.
- Increase consistency, safety, and resiliency from microgrid in dangerous infrastructure protection and highly controlled areas of the electric grid.

Renewable energy sources produce Direct Current (DC), but most of the appliances using Alternating Current (AC) to work. Replacing the AC devices with DC devices is very difficult and it is not economical. To overcome this challenge the DC produced by the renewable energy sources will be converted to AC by using inverters.

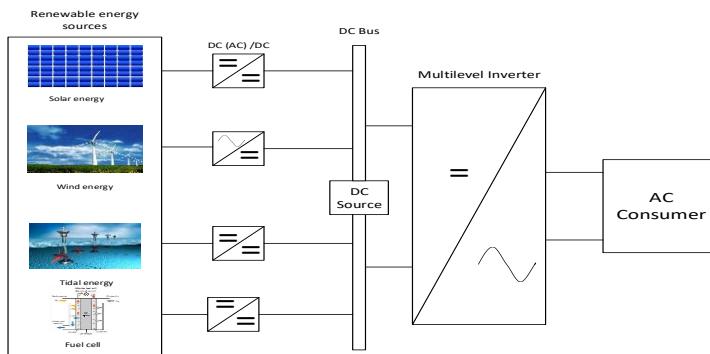


Fig.1.1 Renewable energy generation system with the multilevel inverter.

Basic inverters convert DC to AC (square waveform), but the required AC output is in pure/smooth sinusoidal. To get smooth sinusoidal output waveform multilevel inverters came into the picture, it can convert the fixed DC into multiple level output, if the levels of the inverter increase the output waveform is almost equal to sinusoidal.

Fig.1.1 shows the block diagram of a renewable energy generation system using a multilevel inverter. It integrates a variety of renewable sources, such as solar energy, wind energy, tide energy and so on and they are connected to a converter to generate DC power, which is stored in a capacitor or battery. After connected to a multilevel inverter, DC power is converted into AC power. The multilevel inverter capable of converting a single DC voltage source from a capacitor or battery into an AC voltage source is a key element of most stand-alone renewable energy generation systems. The multilevel inverter topologies, in general, can generate high-quality voltage waveforms, where power switches are operated at a very low frequency.

1.2 Solar energy

A number of different technologies and appliances are available for harnessing solar energy several of which are very relevant for meeting energy needs of developed and developing countries. Passive solar heating and cooling of buildings is being followed world over from time immemorial and interest in it has been revived in recent years. These techniques have been perfected over the years by applying modern scientific principles and computational aids.

Solar water heaters provide a very inexpensive way of meeting hot water needs of households, groups and the community at large. The technology is simple, proven and affordable. These systems are very appropriate for hotels, hostels, guesthouses and community centres. They make hot water available at zero operating costs. Efforts are however needed to reduce cost of equipment and organizing efficient installation and maintenance services.

Crop drying is an important operation in the agricultural economies of both developing and developed countries. Solar crop driers are an effective answer to meet these needs. A number of designs of solar driers have been developed in India, China, Philippines, Thailand and several other countries. They can be built using simple schemes and local materials. They can easily replace electricity-operated or oil-fired crop driers dispensing with open air-drying which is best with post -harvest losses. Seasoning of timber can be inexpensively carried out in solar kilns, a number of designs of which have been developed by the Forest Research Institute, Dehradun. Central Building Research Institute, Roorkee and Allahabad Polytechnic, Allahabad. Hundreds of such solar Kilns designed and installed by these institutions are satisfactorily functioning in different parts of the country, saving electricity or precious fossil-fuels, and ensuring favourable returns on investment. Having these ideas in our mind, we tried

to convert a solar box cooker in to a passive solar drier and its performance was quite appreciable. This dryer can be used for a family to dry their vegetables fruits and can preserve it.

The sun is a sphere of intensely hot gaseous matter with a diameter of 1.39×10^9 m and is on the average, 1.5×10^{11} m from earth. The sun is a continuous fusion reactor with its constituent gases as the "containing vessel" retained by gravitational forces. Several fusion reactions have been suggested to supply the energy radiated by the sun. The one considered the most important is a process in which hydrogen (i.e. four protons) combines to form helium (i.e. one helium nucleus); The mass of the helium nucleus is less than that of the four protons, mass having been lost in the reaction and converted to energy. The sun produces heat by nuclear fusion reactions. The thermal energy radiated by sun is inexhaustible hence the solar energy is called renewable source of energy. The energy produced in the interior of the solar sphere at temperature of millions of degrees must be transferred out to the surface and then be radiated into space. A succession of radiative and convective processes occurs successive emission, absorption, and reradiation; the radiation in the sun's core is in the x-ray and gamma-ray parts of the spectrum, with the wavelength of the radiation increasing as the temperature drops at large radial distances

1.3 Fuel cell

Fuel cells generate electricity by an electrochemical reaction in which oxygen and a hydrogen-rich fuel combine to form water. Unlike internal combustion engines, the fuel is not combusted, the energy instead being released electrocatalytically. This allows fuel cells to be highly energy efficient, especially if the heat produced by the reaction is also harnessed for space heating, hot water or to drive refrigeration cycles.

A fuel cell is like a battery in that it generates electricity from an electrochemical reaction. Both batteries and fuel cells convert chemical potential energy into electrical energy and also, as a by-product of this process, into heat energy. However, a battery holds a closed store of energy within it and once this is depleted the battery must be discarded, or recharged by using an external supply of electricity to drive the electrochemical reaction in the reverse direction. A fuel cell, on the other hand, uses an external supply of chemical energy and can run indefinitely, as long as it is supplied with a source of hydrogen and a source of oxygen (usually air).

There are several different types of fuel cell but they are all based around a central design. A fuel cell unit consists of a stack, which is composed of a number of individual cells. Each cell within the stack has two electrodes, one positive and one negative, called the cathode and the anode. The reactions that produce electricity take place at the electrodes. Every fuel cell also has either a solid or a liquid electrolyte, which carries ions from one electrode to the other, and a catalyst, which accelerates the reactions at the electrodes. The electrolyte plays a key role it must permit only the appropriate ions to pass between the electrodes. If free electrons or other substances travel through the electrolyte, they disrupt the chemical reaction and lower the efficiency of the cell.

Fuel cells are generally classified according to the nature of the electrolyte (except for direct methanol fuel cells which are named for their ability to use methanol as a fuel), each type requiring particular materials and fuel. Each fuel cell type also has its own operational characteristics, offering advantages to particular applications. This makes fuel cells a very versatile technology.

As a result, fuel cells have a broader range of application than any other currently available power source - from toys to large power plants, from vehicles to mobile chargers, and from household power to battlefield power.

1.4 Wind energy

In recent years, wind energy has become one of the most economical renewable energy technologies. Today, electricity generating wind turbines employ proven and tested technology, and provide a secure and sustainable energy supply. At good, windy sites, wind energy can already successfully compete with conventional energy production. Many countries have considerable wind resources, which are still untapped.

The technological development of recent years, bringing more efficient and more reliable wind turbines, is making wind power more cost-effective. In general, the specific energy costs per annual kWh decrease with the size of the turbine notwithstanding existing supply difficulties.

Many African countries expect to see electricity demand expand rapidly in coming decades. At the same time, finite natural resources are becoming depleted, and the

environmental impact of energy use and energy conversion have been generally accepted as a threat to our natural habitat. Indeed these have become major issues for international policy.

Many developing countries and emerging economies have substantial unexploited wind energy potential. In many locations, generating electricity from wind energy offers a cost-effective alternative to thermal power stations. It has a lower impact on the environment and climate, reduces dependence on fossil fuel imports and increases security of energy supply.

For many years now, developing countries and emerging economies have been faced with the challenge of meeting additional energy needs for their social and economic development with obsolete energy supply structures. Overcoming supply bottlenecks through the use of fossil fuels in the form of coal, oil and gas increases dependency on volatile markets and eats into valuable foreign currency reserves. At the same time there is growing pressure on emerging newly industrialised countries in particular to make a contribution to combating climate change and limit their pollutant emissions.

In the scenario of alternatives, more and more developing countries and emerging economies are placing their faith in greater use of renewable energy and are formulating specific expansion targets for a ‘green energy mix’. Wind power, after having been tested for years in industrialised countries and achieving market maturity, has a prominent role to play here. In many locations excellent wind conditions promise inexpensive power generation when compared with costly imported energy sources such as diesel. Despite political will and considerable potential, however, market development in these countries has been relatively slow to take off. There is a shortage of qualified personnel to establish the foundations for the exploitation of wind energy and to develop projects on their own initiative. The absence of reliable data on wind potential combined with unattractive energy policy framework conditions deters experienced international investors, who instead focus their attention on the expanding markets in Western countries.

It is only in recent years that appreciable development of the market potential in developing countries and emerging economies has taken place. The share of global wind generating capacity accounted for by Africa, Asia and Latin America reached about 20% at the end of 2008, with an installed capacity of 26 GW. This is attributable above all to breath taking growth in India and China: these two countries alone are responsible for 22 GW. This proves that economic use of wind energy in developing countries and emerging economies is possible, and also indicates that there is immense potential that is still unexploited

1.5 Tidal energy

Tidal energy is produced by the surge of ocean waters during the rise and fall of tides. Tidal energy is a renewable source of energy.

During the 20th century, engineers developed ways to use tidal movement to generate electricity in areas where there is a significant tidal range the difference in area between high tide and low tide. All methods use special generators to convert tidal energy into electricity.

Tidal energy production is still in its infancy. The amount of power produced so far has been small. There are very few commercial-sized tidal power plants operating in the world. The first was located in La Rance, France. The largest facility is the Sihwa Lake Tidal Power Station in South Korea. The United States has no tidal plants and only a few sites where tidal energy could be produced at a reasonable price. China, France, England, Canada, and Russia have much more potential to use this type of energy.

In the United States, there are legal concerns about underwater land ownership and environmental impact. Investors are not enthusiastic about tidal energy because there is not a strong guarantee that it will make money or benefit consumers. Engineers are working to improve the technology of tidal energy generators to increase the amount of energy they produce, to decrease their impact on the environment, and to find a way to earn a profit for energy companies.

There are currently three different ways to get tidal energy: tidal streams, barrages, and tidal lagoons.

For most tidal energy generators, turbines are placed in tidal streams. A tidal stream is a fast-flowing body of water created by tides. A turbine is a machine that takes energy from a flow of fluid. That fluid can be air (wind) or liquid (water). Because water is much more dense than air, tidal energy is more powerful than wind energy. Unlike wind, tides are predictable and stable. Where tidal generators are used, they produce a steady, reliable

stream of electricity. Placing turbines in tidal streams is complex, because the machines are large and disrupt the tide they are trying to harness. The environmental impact could be severe, depending on the size of the turbine and the site of the tidal stream. Turbines are

most effective in shallow water. This produces more energy and allows ships to navigate around the turbines. A tidal generator's turbine blades also turn slowly, which helps marine life avoid getting caught in the system.

The world's first tidal power station was constructed in 2007 at Strangford Lough in Northern Ireland. The turbines are placed in a narrow strait between the Strangford Lough inlet and the Irish Sea. The tide can move at 4 meters (13 feet) per second across the strait.

Another type of tidal energy generator uses a large dam called a barrage. With a barrage, water can spill over the top or through turbines in the dam because the dam is low. Barrages can be constructed across tidal rivers, bays, and estuaries.

Turbines inside the barrage harness the power of tides the same way a river dam harnesses the power of a river. The barrage gates are open as the tide rises. At high tide, the barrage gates close, creating a pool, or tidal lagoon. The water is then released through the barrage's turbines, creating energy at a rate that can be controlled by engineers.

The environmental impact of a barrage system can be quite significant. The land in the tidal range is completely disrupted. The change in water level in the tidal lagoon might harm plant and animal life. The salinity inside the tidal lagoon lowers, which changes the organisms that are able to live there. As with dams across rivers, fish are blocked into or out of the tidal lagoon. Turbines move quickly in barrages, and marine animals can be caught in the blades. With their food source limited, birds might find different places to migrate.

A barrage is a much more expensive tidal energy generator than a single turbine. Although there are no fuel costs, barrages involve more construction and more machines. Unlike single turbines, barrages also require constant supervision to adjust power output.

The tidal power plant at the Rance River estuary in Brittany, France, uses a barrage. It was built in 1966 and is still functioning. The plant uses two sources of energy: tidal energy from the English Channel and river current energy from the Rance River. The barrage has led to an increased level of silt in the habitat. Native aquatic plants suffocate in silt, and a flatfish called plaice is now extinct in the area. Other organisms, such as cuttlefish, a relative of squids, now thrive in the Rance estuary. Cuttlefish prefer cloudy, silty ecosystems.

CHAPTER 2

EVOLUTION OF MULTILEVEL INVERTERS AND LITERATURE SURVEY

2.1 Inverter

The Inverter is an electrical device that converts direct current (DC) to alternate current (AC). The inverter is used for backup power in a home. The AC power is used mostly for electrical devices like lights, radar, radio, motor, and other devices.

2.2 Multilevel inverter

J. Rodriguez, J. S. Lai, and F. Z. Peng (2002) was proposed a Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. J. Rodriguez, J. S. Lai, and F. Z. Peng presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multicell with separate dc sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. And also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation. Special attention is dedicated to the latest and more relevant applications of these converters such as laminators, conveyor belts, and unified power-flow controllers. The need of an active front end at the input side for those inverters supplying regenerative loads is also discussed, and the circuit topology options are also presented. Finally, the peripherally developing areas such as high-voltage high-power devices and optical sensors and other opportunities for future development are addressed.

F. S. Kang et al. (2005) was proposed a new multilevel pulse width-modulation (PWM) inverter scheme for the use of stand-alone photovoltaic systems. It consists of a PWM inverter, an assembly of LEVEL inverters, generating staircase output voltages, and cascaded transformers. To produce high-quality output voltage waves, it synthesizes a large number of output voltage levels using cascaded transformers, which have a series-connected secondary. By a suitable selection of the secondary turn-ratio of the transformer, the amplitude of an output

voltage appears at the rate of an integer to an input dc source. Operational principles and analysis are illustrated in depth. The validity of the proposed system is verified through computer-aided simulations and experimental results using prototypes generating output voltages of an 11 level and a 29 level, respectively, and their results are compared with conventional counterparts

B. P. McGrath and D. G. Holmes (2002) proposed an analytical solutions of pulse width-modulation (PWM) strategies for multilevel inverters are used to identify that alternative phase opposition disposition PWM for diode-clamped inverters produces the same harmonic performance as phase-shifted carrier PWM for cascaded inverters, and hybrid PWM for hybrid inverters, when the carrier frequencies are set to achieve the same number of inverter switch transitions over each fundamental cycle. Using this understanding, a PWM method is then developed for cascaded and hybrid inverters to achieve the same harmonic gains as phase disposition PWM achieves for diode-clamped inverters

Now a day's numerous industrial applications have started to involve high power appliances in the industries, still, they require medium or low power for their process. Using a high-power source for all industrial loads may show advantageous to some motors demanding high power, while it may harm the other loads. Some medium voltage motor and home applications need medium voltage. The multilevel inverter has been introduced since 1975 as a substitute in high power and medium voltage situations. The Multilevel inverter is similar to an inverter and it is used for industrial applications as a substitute in high power and medium voltage conditions.

The need for the multilevel converter is to give high output power from a medium-voltage source. Sources like batteries, supercapacitors, the solar panels are medium voltage sources. The multilevel inverter consists of several switches. In the multilevel inverter, the arrangement switches' angles are very important.

Multilevel inverters are three types.

- Diode clamped multilevel inverter
- Flying capacitors multilevel inverter
- Cascaded multilevel inverter

2.2.1 Diode clamped multilevel inverter

The key perception of this inverter is to use diodes and sends the multiple voltage levels through the different phases to the capacitor banks which are in series. A diode allows a limited amount of voltage, so dipping the stress on other electrical devices. The diode clamped multilevel inverter topology as shown in Fig. 2.1. The applied DC voltage is divided into various levels via capacitors, for N level inverter $N-1$ capacitors are essential. Diodes are used to clamp the output voltages.

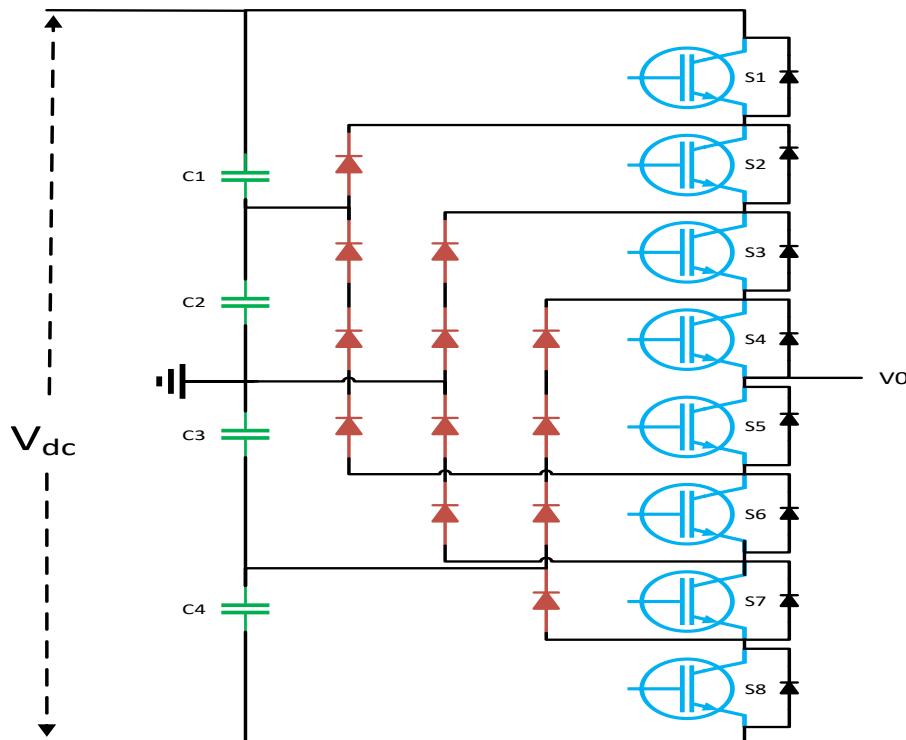


Fig. 2.1 Diode clamped multilevel inverter

Table.2.1 Modes of operation of diode clamped multilevel inverter

| V0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| $V_{dc}/2$ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $V_{dc}/4$ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $-V_{dc}/4$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| $-V_{dc}/2$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

This type of multilevel inverter is used in

- Static var compensation
- Variable speed motor drives
- High voltage system interconnections
- High voltage DC and AC transmission lines

The main advantages of using this multilevel inverter are:

- More efficiency for switching at the fundamental frequency.
- Pre charging of capacitors is done in groups.
- Efficient for back to back high-power connections.
- Lesser number of components.
- Low cost.

Disadvantages of using this multilevel inverter are:

Quadratic relation between the number of diodes and the number of levels is difficult to calculate, especially when the number of levels gets higher it becomes stressful and you would surely want to avoid it.

- Maintaining certain charging and discharging is difficult.
- Charge equilibrium gets disturbed for more than three levels.
- Limited output voltage.

2.2.2 Flying capacitors multilevel inverter

The main perception of this inverter is to use capacitors. It is of a series connection of capacitor clamped switching cells. The capacitors allow a limited amount of voltage to electrical devices. In this inverter switching states are similar in the diode clamped inverter. Clamping diodes are not needed in this type of multilevel inverters. Each leg consists of switching devices which are normally transistors. Every inverter limb contains cells connected in inward nested series. Every single cell has a single capacitor and two power switches. The power switch is a combination of a transistor connected with an anti-parallel diode. Like diode clamped inverter, this topology uses capacitors for clamping. An inverter with N cell will have $2N$ switches and $N+1$ different voltage level including zero. We can also have negative voltage levels, and so, all in all, we can say that N cell multilevel inverter can give a $2N+1$ voltage level. Capacitors nearer to the load have lower voltage. Capacitors nearer to the source voltage (V_{dc}) have a higher voltage. The number of levels depends upon the

number of conducting switches in each limb. They are called Flying Capacitor Multilevel Inverter because the capacitors float concerning to earth's potential. The main advantage of this multilevel inverter is each branch can be analysed separately and individually. The flying capacitor multilevel inverter topology is shown in Fig. 2.2.

Voltage balancing of capacitors:

One of the main advantages of using a Flying capacitor multilevel inverter is it's able to work at voltages higher than the blocking ranges of each power cell consisting of a diode and switching elements. Current co-efficient of an individual limb is equal and opposite in polarity. So, there is no net change in charge of capacitors. The cell and capacitor voltage

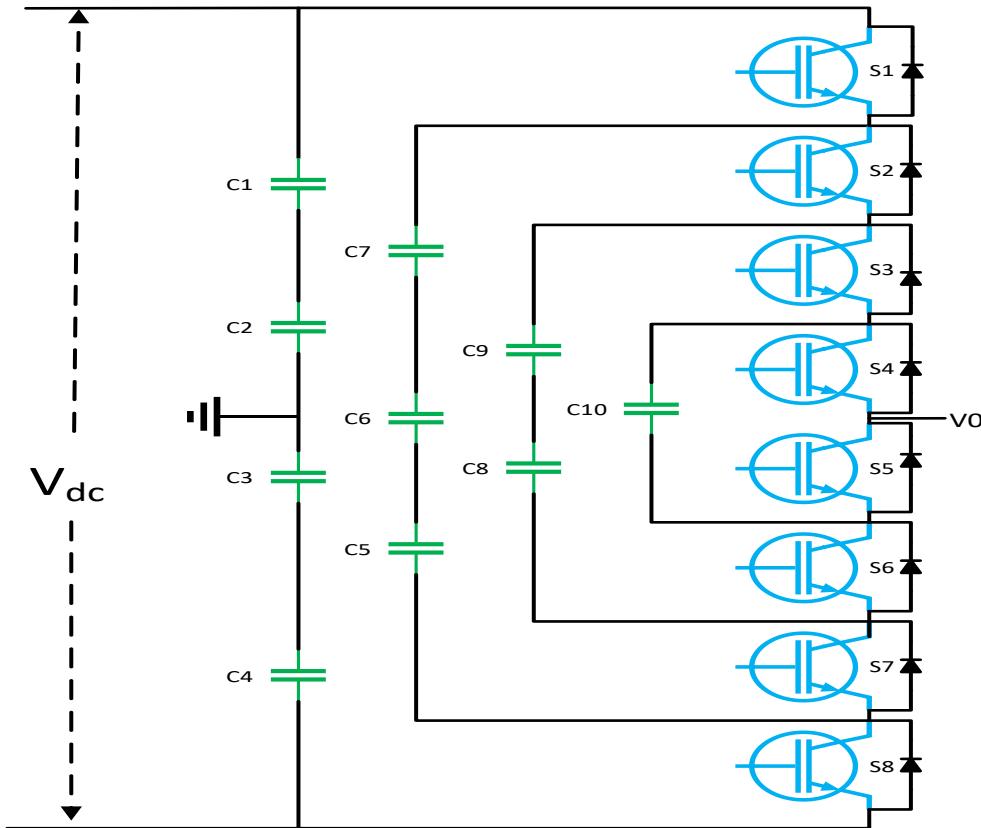


Fig.2.2 Flying capacitor multilevel inverter

Difference is sustained within a safe range and hence there is no chance of unbalancing the capacitor voltages.

Table.2.2 modes of operation of flying capacitor multilevel inverter

| V₀ | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
|--------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| V_{dc/2} | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| V_{dc/4} | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| -V_{dc/4} | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| -V_{dc/2} | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

Switching strategy:

To synthesize a sinusoidal waveform at the output, the switching strategy needs to be defined. It is quite simple. Every voltage is applied at the output with a certain electrical angle. Careful application of the angle gives low harmonic distortion and requires amplitude at the output.

More than one switching strategies are existing for a single voltage level. Three conditions should be shadowed for the right choice:

- For every change in the state, only one switch shift should be allowed.
- The capacitor's voltage balance should be maintained.
- All the switching devices are used equally.

The disadvantages of using this multilevel inverter is pre charging of capacitors is necessary and difficult

This multilevel inverter is used in:

- Induction motor control with DTC (Direct Torque Control) circuit
- Static var generation
- Both AC-DC and DC-AC conversion applications
- Converters with Harmonic distortion capability
- Sinusoidal current rectifiers

2.2.3 Cascaded multilevel inverter

Cascaded multilevel inverters are classified into

- a) Cascaded H-Bridge multilevel inverter
- b) Cascade Half-Bridge multilevel inverter
- c) Cascaded switched Diode multilevel inverter

a) Cascaded H-Bridge multilevel inverter

The cascaded H-bridge multilevel inverter is to use capacitors and switches and requires a smaller number of components at each level. This topology consists of a series of power conversion cells and power can be easily scaled. The mixture of capacitors and switches pair is called an H-bridge and gives the distinct input DC voltage for each H-bridge. It consists of H-bridge cells and each cell can deliver the three different voltages like zero, positive DC and negative DC voltages. One of the advantages of this type of multilevel inverter is that it needs a smaller number of components compared with diode clamped and flying capacitor inverters. The cost and mass of the inverter are less than those of the two inverters. Soft-switching is possible by some of the new switching methods.

Multilevel cascade inverters are used to eradicate the bulky transformer required in case of conventional multi-phase inverters, clamping diodes required in case of diode clamped inverters and flying capacitors required in case of flying capacitor inverters. But these require a large number of isolated voltages to supply each cell.

The cascaded H-bridge inverter has drawn tremendous interest due to the greater demand for medium-voltage high-power inverters. The cascaded inverter uses series strings of single-phase full-bridge inverters to build multilevel phase legs with separate dc sources. A single H-bridge is shown in Fig. 2.3. The output of individual H-bridge can have three discrete levels, in a staircase waveform that is closely sinusoidal even without filtering. A single H-bridge is a three-level inverter. Individual single-phase full-bridge inverter generates three voltages at the output: V_{dc} , 0, $-V_{dc}$. The four switches $S1$, $S2$, $S3$, and $S4$ are controlled to generate three discrete outputs V_{out} with levels 0, V_{dc} and $-V_{dc}$. When $S1$ and $S2$ are on, the output is V_{dc} . When $S3$ and $S4$ are turned on, the output is $-V_{dc}$; when either pair $S1$ and $S3$ or $S2$ and $S4$ are on, the output is 0. Fig. 2.4 shows a single-phase, five-level cascaded H-bridge cell inverter realized by connecting two three-level conventional full-bridge inverters in series was presented in Tolbert et al (1999). The switch sets $S1$ and $S3$ and $S2$ and $S4$ are opposite

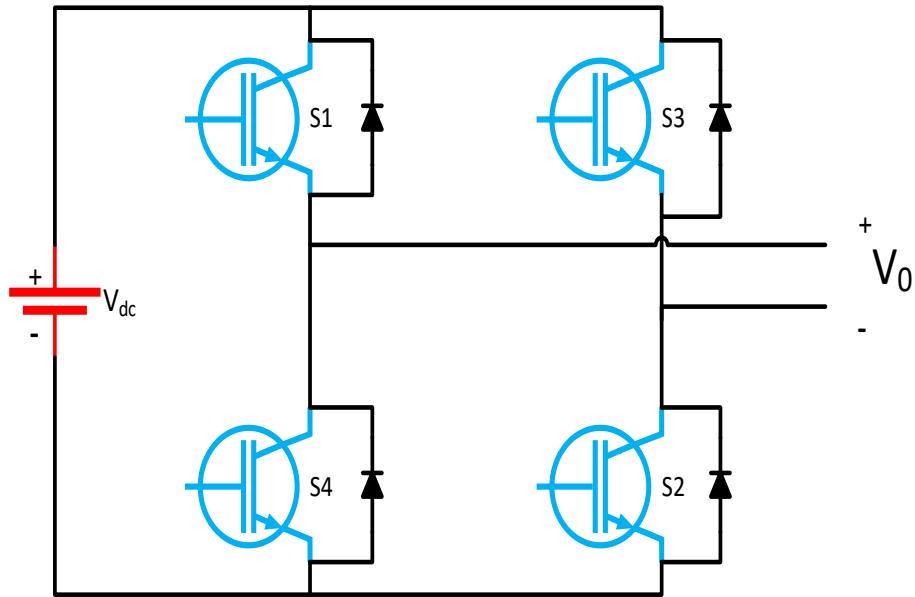


Fig. 2.3 Single H-Bridge Topology

to each other. The different voltage levels that can be obtained at the output terminals are $0, V_{dc}, -V_{dc}, 2V_{dc}, -2V_{dc}$. If the dc voltage sources in both the inverter circuits associated in series

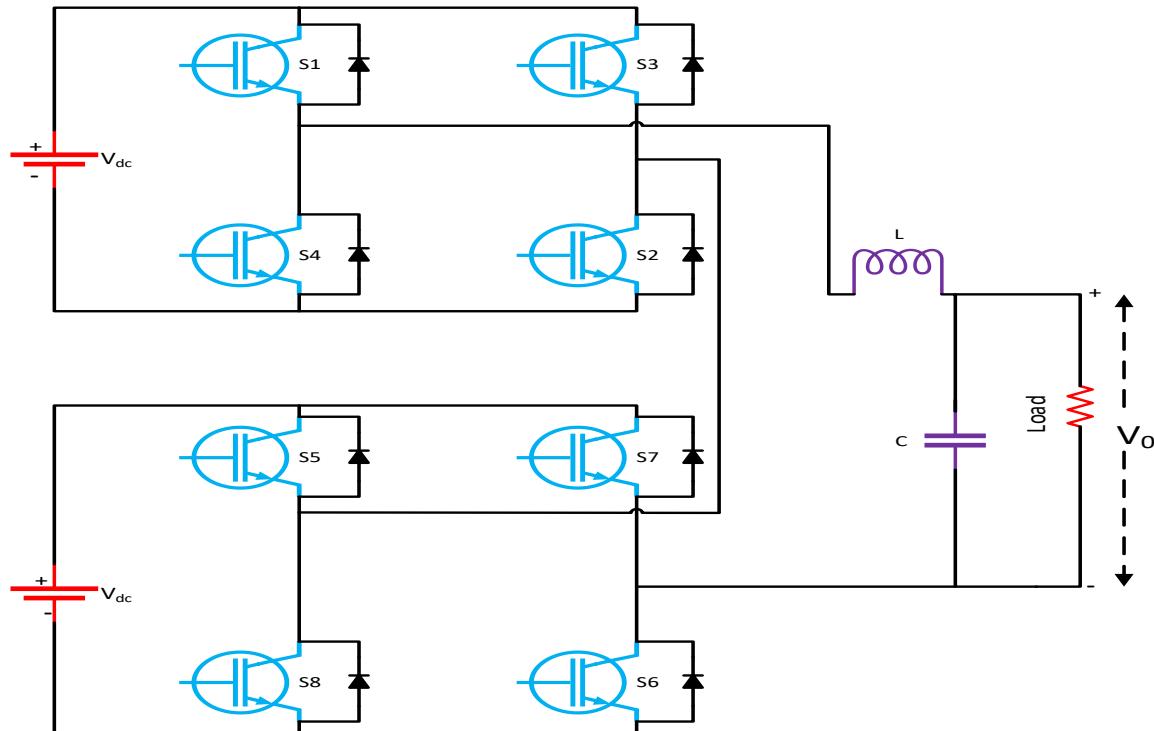


Fig. 2.4 5 Level Cascaded H-Bridge multilevel Inverter

are not equal to each other, then nine levels can be obtained at the output terminals. The number of levels in the output voltage can be amplified by two by adding a similar inverter in series. The n number of output phase voltage levels in a cascaded inverter with s separate dc sources

is $2s-1$ possible levels. Cascaded H-bridge cell inverters use the smallest number of power electronic devices when compared to any other topology. However, they require remote power sources in each cell which in turn needs a large isolating transformer. When the switches S_{a1} , S_{a2} , S_{b3} , and S_{b4} are on and S_{a3} , S_{a4} , S_{b1} , and S_{b2} are turned off, the corresponding output voltage of the cascaded H-bridge multilevel inverter is zero. The switches S_{a1} , S_{a2} , S_{b1} , and S_{b2} are turned on and S_{a3} , S_{a4} , S_{b3} , and S_{b4} are turned off, the corresponding output voltage of the cascaded H-bridge multilevel inverter is $2V_{dc}$. Similarly, the output voltages for additional switching stages are shown in Table 2.1.

Table 2.3 Switching States for 5 Level Cascaded H-Bridge

| V_o | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
|-------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| V_{dc} | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 2V_{dc} | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -V_{dc} | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| -2V_{dc} | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

The advantages of cascaded multilevel H-bridge inverter are the following:

- The series construction permits a scalable, modularized circuit layout and packaging due to the identical structure of each H-bridge.
- No additional clamping diodes or voltage balancing capacitors are necessary.
- Switching unnecessary usage for inner voltage levels is possible because the phase voltage is the sum of the output of each bridge.

The disadvantage of cascaded multilevel H-bridge inverter is the following:

- Needs separate DC sources.
- It requires more switching devices.

b) Cascaded Half-Bridge multilevel inverter

The basic unit of novel cascaded multilevel inverter is half-bridge. Fig. 2.6 shows the configuration of the half-bridge cascaded multilevel inverter. The maximum output voltage of the multilevel inverter is given by (1)

$$V_0 = V_{01} + V_{02} + \dots + V_{0n} \quad (2.1)$$

In the topology of Fig. 2.6, assuming that in each half-bridge unit the DC voltage is equal to E , the half-bridge only generates two kinds of voltage levels: $E, 0$; and all voltage levels generated by the half-bridge are synthesized before the H-bridge, therefore, the synthesized voltage levels become $nE, (n-1)E, \dots, 0$. The function of the H-bridge is flipping the polarity of the output voltage at the negative half, it means that, at the negative half cycle, the H-bridge turns synthesized voltage levels from positive to negative. Therefore, output voltage levels become $nE, (n-1)E, \dots, 0, \dots, -(n-1)E, -nE$.

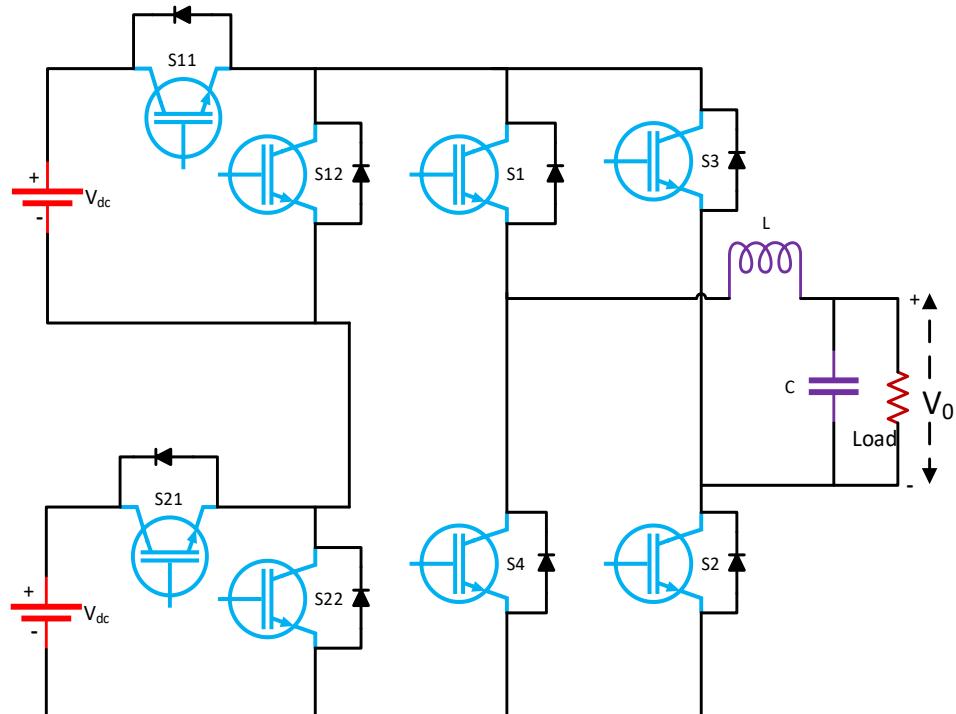


Fig.2.5 Cascaded Half-Bridge Multilevel Inverter

If all the DC voltage sources in Fig. 2.5 are equal to E , the inverter can also be called the symmetric multilevel inverter. The number of maximum output voltage steps of the N series basic units can be evaluated by (2) and the maximum output voltage is given by (3).

$$N_{step} = 2N + 1 \quad (2.2)$$

$$V_{omax} = NE \quad (2.3)$$

the novel topology of cascaded multilevel inverter reduces the number of devices without affecting the function of the electronic system. In Fig. 2.5, based on the same DC sources, the topology needs $2N+4$ semiconductor devices to realize the N_{step} staircase output waveform and in Fig. 2.4, the topology needs $4N$ semiconductor devices to realize the N_{step} staircase output waveform. With the increase of the number of cascaded units, the novel topology needs fewer semiconductor devices compared with cascaded H-bridge multilevel inverter. It compared the novel topology with the conventional cascaded multilevel inverter topology at the power component requirements, the standing voltage of switches, and the number of switches. Through the comparison, the novel topology needs fewer switches to realize the same output voltage, reduces the installation area and the number of gate drivers, so the cost is less.

CHAPTER 3

CASCADED H-BRIDGE MULTILEVEL INVERTER

3.1 Introduction

Multilevel inverters have been widely used in many applications since the technology is advantageous to increase the converter capability as well as to improve the output voltage quality. Multilevel inverters are able to produce a staircase output waveform, that is more approaching sinusoidal and produce a smaller number of harmonics compare to the conventional inverter output voltage. There are mainly three types of multi-level inverters, Diode clamped, Flying capacitor inverter and cascaded h- bridge multi-level inverter

Cascaded h-bridge multilevel inverters have been developed for utility applications including utility interface of renewable energy, voltage regulation, VAR compensation, and harmonic filtering in power systems. A modified cascaded H-bridge multilevel inverter (MLI) is implemented for solar applications. A new design of asymmetric cascaded H-bridge multilevel inverter is implemented in the grid side of the wind energy conversion system. A Five level cascaded H-bridge multilevel Inverter is also designed for induction motor drive.

The structure of the cascaded H-bridge (CHB) may consist of two or more H-bridge inverters. The CHB inverter can be supplied by separated DC sources or a single DC source. This type of inverter consists of two cells H-bridge inverter hence employs 8 power electronic switches. The modulation technique that applies to each cell of inverter may be the same or different. It varies from fundamental switching frequency PWM, carrier based PWM or combination of the two different PWM methods (known as mixed / hybrid PWM method)

3.2 5 Level cascaded H-Bridge

The modes of operation of 5 Level Cascaded H-Bridge is discussed in chapter 2 for each mode turned on switching devices and the current flow is discussed below. In mode-1 the output voltage across the load will be $+V_{dc}$ and the switches S_1 , S_2 , and S_6 are turned on, the

current will flow from source-1 to load in $+V_{dc1}$, S_1 , $+V_0$, $-V_0$, S_6 , S_2 , $-V_{dc1}$, the current flow is shown in fig.3.1

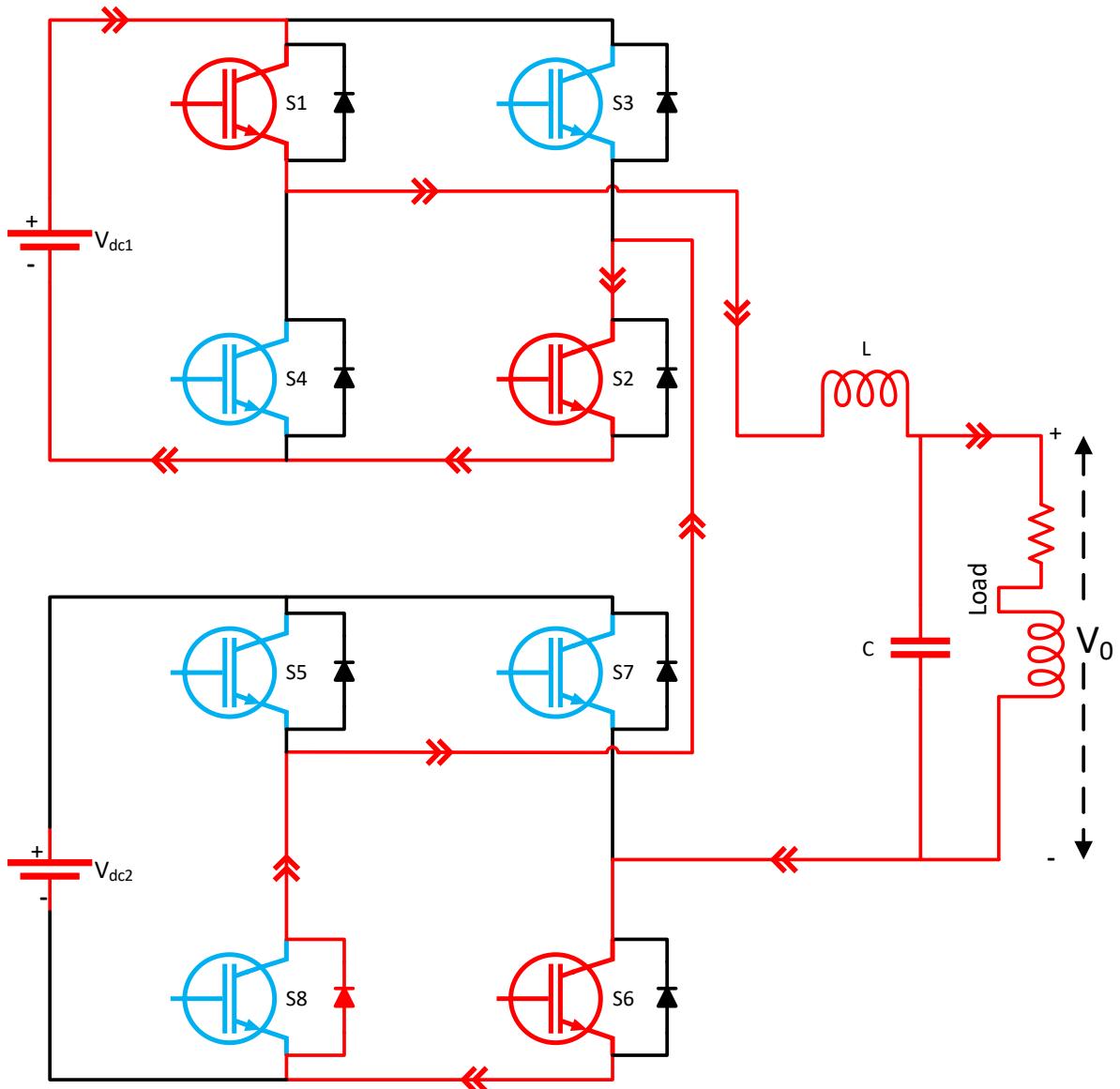


Fig. 3.1 5 Level CHB in Mode-1 ($+V_{dc}$)

In mode-2 the output voltage across the load will be $+2V_{dc}$ and the switches S_1 , S_2 , S_5 , S_6 are turned on, the current will flow in $+V_{dc1}$, S_1 , $+V_0$, $-V_0$, S_6 , $-V_{dc2}$, $+V_{dc2}$, S_5 , S_2 , $-V_{dc1}$, the current flow is shown in fig.3.2

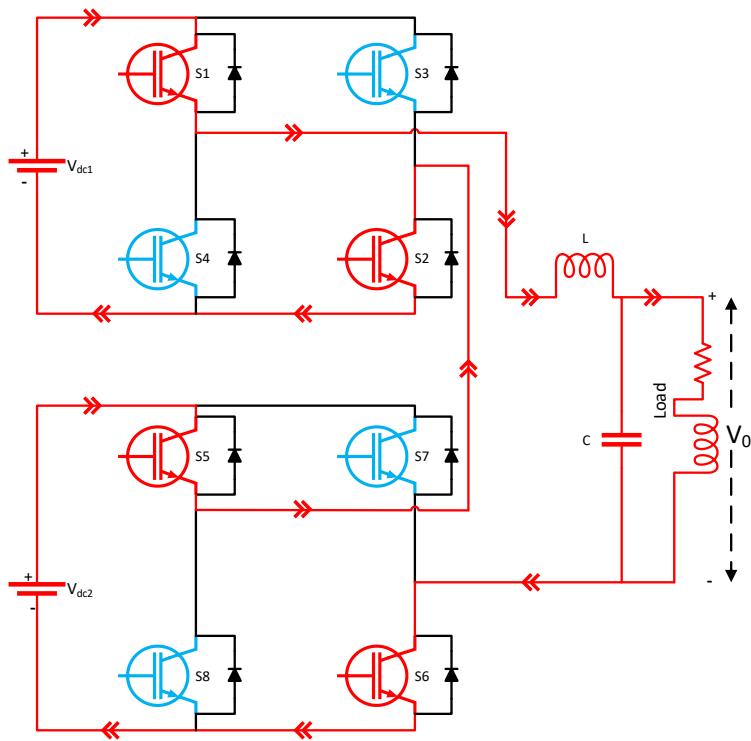


Fig. 3.2 5 Level CHB in Mode-2 ($+2V_{dc}$)

In mode-3 all the switches are in off position and the output voltage across the load will be zero. As shown in fig.3.3.

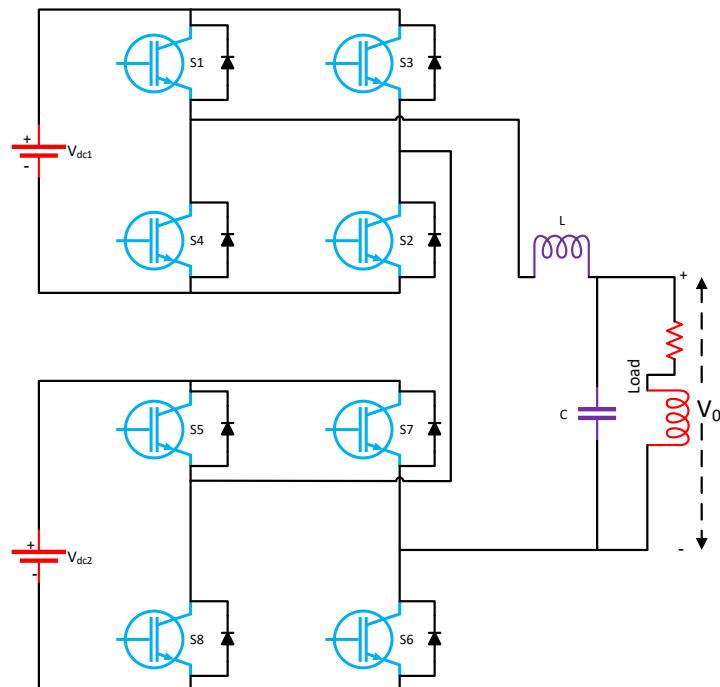


Fig.3.3 5 Level CHB in Mode-3 (0 Volts)

In mode-4 the output voltage across the load will be $-V_{dc}$ and the switches S_4 , S_7 , and S_8 are turned on, the current will flow from source to load in $+V_{dc2}$, S_7 , $-V_0$, $+V_0$, S_4 , S_8 , $-V_{dc2}$, the current flow is shown in fig.3.1

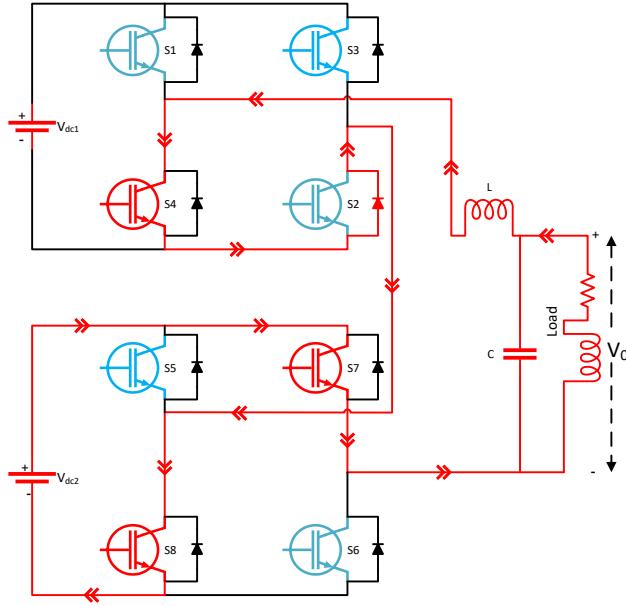


Fig.3.4 5 Level CHB in Mode-4 ($-V_{dc}$)

In mode-5 the output voltage across the load will be $-2V_{dc}$ and the switches S_3 , S_4 , S_7 , S_8 are turned on, the current will flow from source to load in $+V_{dc2}$, S_7 , $-V_0$, $+V_0$, S_4 , $-V_{dc1}$, $+V_{dc1}$, S_3 , S_8 , $-V_{dc2}$, the current flow is shown in fig.3.5

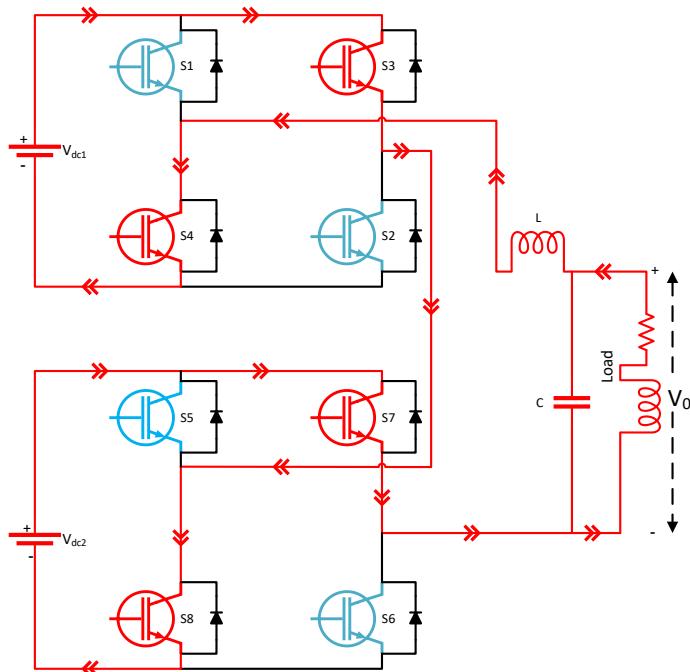


Fig.3.5 5 Level CHB in Mode-5 ($-2V_{dc}$)

3.3 9 Level Cascaded H-Bridge

In 5 Level cascaded H-Bridge the stepped output waveform contains harmonics to reduce that harmonics to some extent the levels of the CHB has been increased to 9 Level. For 9 Level inverter modes are discussed in detail and as shown in fig.5.6. In mode-1 the output voltage across the load will be $+V_{dc}$ the switches $S_1, S_2, S_6, S_{10}, S_{14}$ are turned on, the current will flow from source to load in $+V_{dc1}, S_1, +V_0, -V_0, S_{14}, S_{10}, S_6, S_2, -V_{dc1}$.

In mode-2 the output voltage across the load will be $+2V_{dc}$ and the switches $S_1, S_2, S_6, S_{10}, S_{13}, S_{14}$ are turned on. The current will flow from source to load in $+V_{dc1}, S_1, +V_0, -V_0, S_{14}, -V_{dc4}, +V_{dc4}, S_{10}, S_6, S_2, -V_{dc1}$.

In mode-3 the output voltage across the load will be $+3V_{dc}$ and the switches $S_1, S_2, S_6, S_9, S_{10}, S_{13}, S_{14}$ are turned on. The current will flow from source to load in $+V_{dc1}, S_1, +V_0, -V_0, S_{14}, -V_{dc4}, +V_{dc4}, S_{10}, -V_{dc3}, +V_{dc3}, S_9, S_6, S_2, -V_{dc1}$.

In mode-4 the output voltage across the load will be $+4V_{dc}$ and the switches $S_1, S_2, S_5, S_6, S_9, S_{10}, S_{13}, S_{14}$ are turned on. The current will flow from source to load in $+V_{dc1}, S_1, +V_0, -V_0, S_{14}, -V_{dc4}, +V_{dc4}, S_{10}, -V_{dc3}, +V_{dc3}, S_9, S_6, -V_{dc2}, +V_{dc2}, S_5, S_2, -V_{dc1}$.

In mode-5 the output voltage zero will appear across the load in this all the switching devices in off position.

In mode-6 the output voltage across the load will be $-V_{dc}$ and the switches $S_4, S_8, S_{12}, S_{15}, S_{16}$ are turned on. The current will flow from source to load in $+V_{dc4}, S_{15}, -V_0, +V_0, S_4, S_8, S_{12}, S_{16}, -V_{dc4}$.

In mode-7 the output voltage across the load will be $-2V_{dc}$ and the switches $S_3, S_4, S_8, S_{12}, S_{15}, S_{16}$ are turned on. The current will flow from source to load in $+V_{dc4}, S_{15}, -V_0, +V_0, S_4, -V_{dc1}, +V_{dc1}, S_3, S_8, S_{12}, S_{16}, -V_{dc4}$.

In mode-8 the output voltage across the load will be $-3V_{dc}$ and the switches $S_3, S_4, S_7, S_8, S_{12}, S_{15}, S_{16}$ are turned on. The current will flow from source to load in $+V_{dc4}, S_{15}, -V_0, +V_0, S_4, -V_{dc1}, +V_{dc1}, S_3, S_8, -V_{dc2}, +V_{dc2}, S_7, S_{12}, S_{16}, -V_{dc4}$.

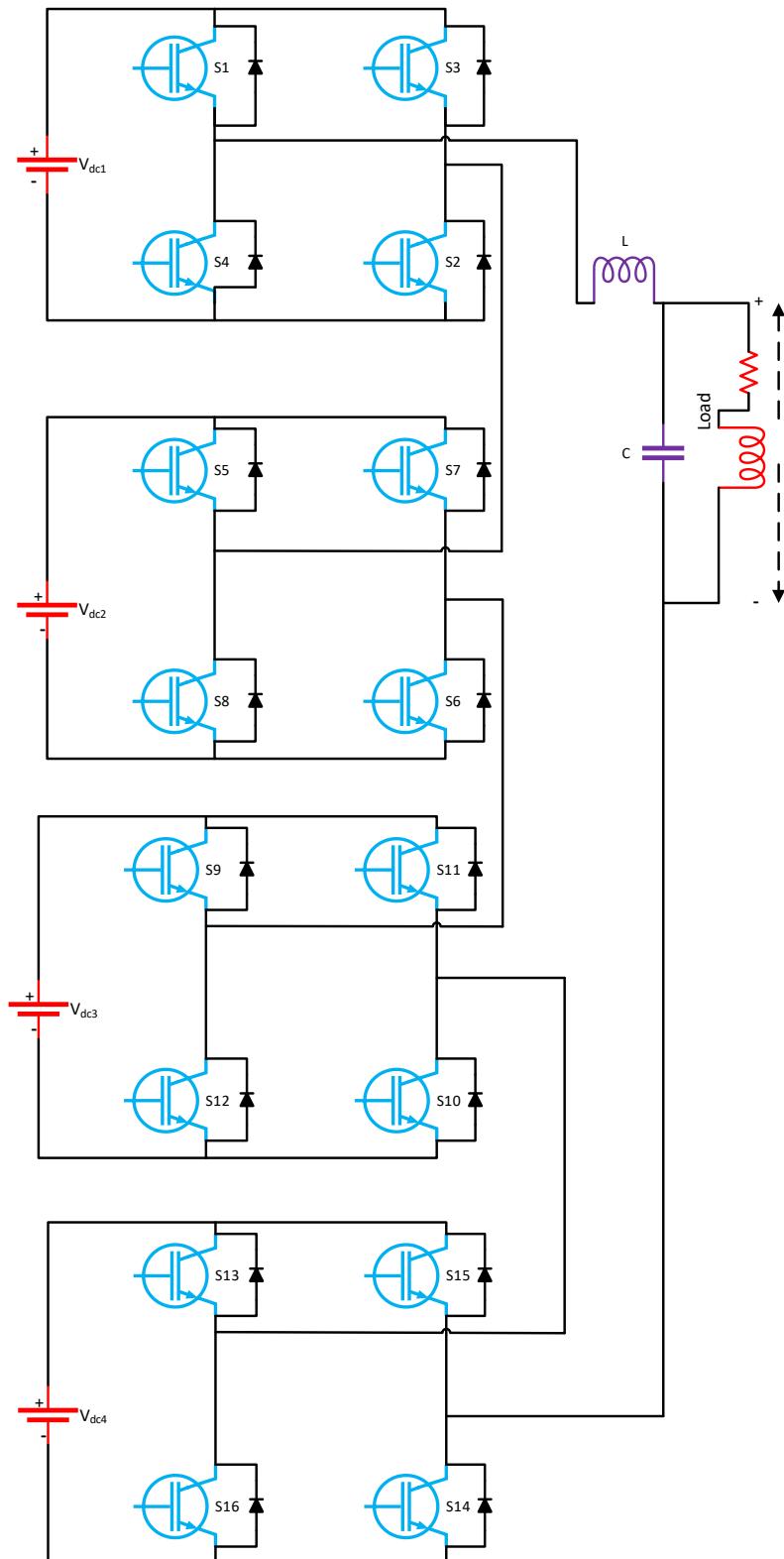


Fig.3.6 9 Level Cascaded H-Bridge

In mode-9 the output voltage across the load will be $-4V_{dc}$ and the switches $S_3, S_4, S_+, S_8, S_{11}, S_{12}, S_{15}, S_{16}$ are turned on. The current will flow from source to load in $+V_{dc4}, S_{15}, -V_0, +V_0, S_4, -V_{dc1}, +V_{dc1}, S_3, S_8, -V_{dc2}, +V_{dc2}, S_7, S_{12}, -V_{dc3}, +V_{dc3}, S_{11}, S_{16}, -V_{dc4}$.

The modes of operation of 9 Level cascaded H-Bridge is shown in table.3.1

Table.3.1 Mode of operation of 9 Level CHB

| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | S13 | S14 | S15 | S16 |
|-------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|------------|------------|------------|------------|------------|------------|------------|
| V_{dc} | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 2V_{dc} | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 3V_{dc} | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 4V_{dc} | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -V_{dc} | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| -2V_{dc} | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| -3V_{dc} | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| -4V_{dc} | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

For 5 Level CHB the output waveform contains 5 stages i.e. $+V_{dc}$, $+2V_{dc}$, 0 , $-V_{dc}$, $-2V_{dc}$, the output waveform looks nearer to sinusoidal, but because of the less no of steps in the output the total harmonic distortion will be more the output and that is not preferable for integration. So to reduce that harmonics the number of steps in the output will increase to 9, the output waveform is similar to sinusoidal and also the total harmonics distortion will be reduced to more than half as compared to 5 Level.

CHAPTER 4

CASCADED SWITCHED DIODE MLI

OPERATION AND CONTROL

4.1 Introduction

As the multilevel inverter classified into three main types in the cascaded version, the third main type is the cascaded switched diode multilevel inverter which is used in renewable energy integration. The input energy sources are like solar, fuel cell, wind, tidal, etc. In this project the input energy sources used are solar and fuel cells. By taking the wind and tidal energy sources as input sources the complexity of the Simulink model increases very high. In the past decade, many multilevel inverter topologies were used or studied for renewable energy integration by taking input sources like wind, tidal, fuel cell, solar energies, etc. High-quality voltage waveforms can be obtained from these multilevel inverters where the frequency required for power switches involved in the Simulink model is very low when compared to the other conventional inverters. Due to the simple structure of the cascaded switched diode multilevel inverter, it has attracted more attention and also had an advantage like it has individual dc power sources for each cascaded unit. The cascaded switched diode multilevel inverter has a great potential to be employed in renewable energy integration. In the previous version or type of cascaded MLI, the cascaded H-bridge requires more switches and its related gate drivers when compared to cascaded switched diode multilevel inverter which may lead to an expensive and complex overall system. Then the second type of cascade MLI, cascade half-bridge MLI introduced with less number of switches and gate drivers which produces more voltage levels when compared to the cascade H-bridge MLI but due to the lack of a path for reverse load currents under R-L loads, high voltage spikes occur at the base of stepped output voltage, which tends to deteriorate the power quality. Therefore the cascaded switched diode multilevel inverter is implemented to overcome the difficulties obtained by using the previous version topologies of a cascaded multilevel inverter.

4.2 Topology of cascaded switched diode multilevel inverter

The cascaded switched diode is done under two stages like the first stage and second stage respectively.

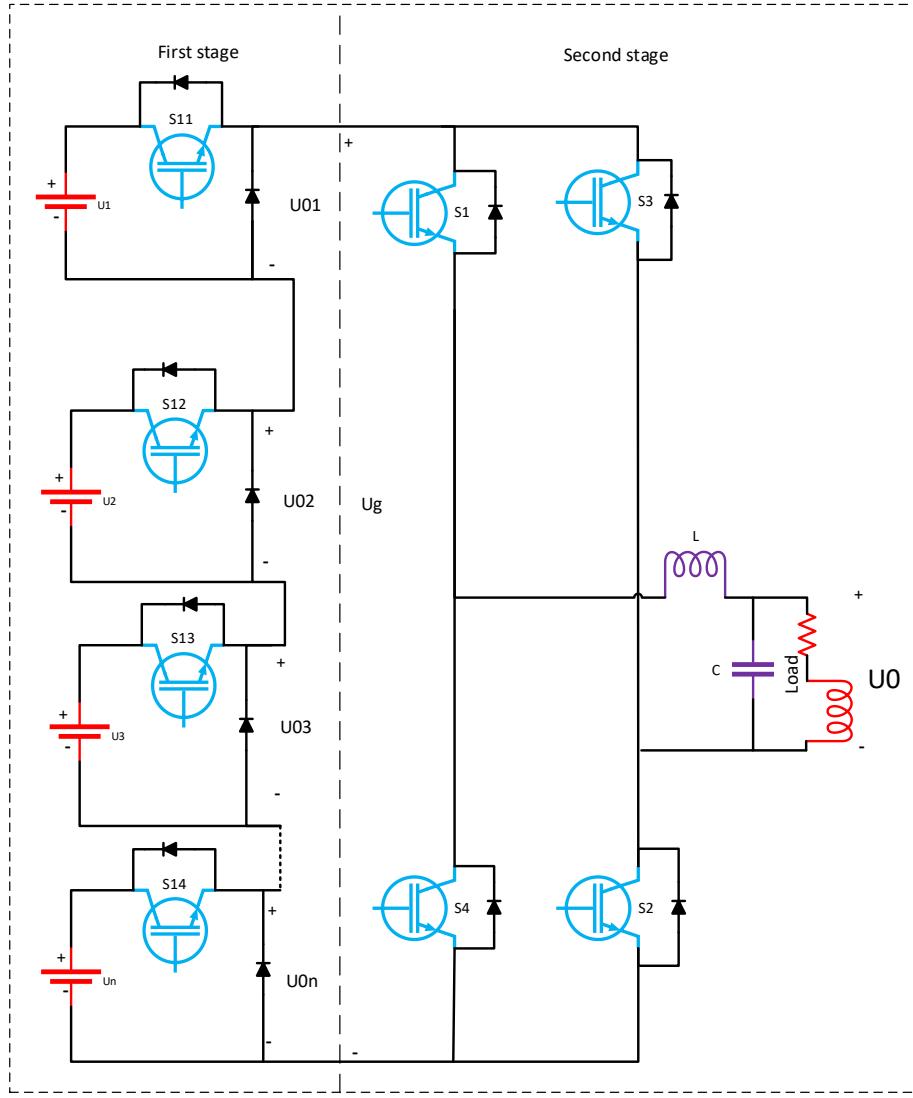


Fig 4.1 The structure of the developed two-staged CSD Topology.

Renewable energy sources act as the DC power sources of multilevel inverter in renewable energy integration as shown in fig 1.1. In practical conditions, because of all sorts of complex factors, the DC supply always fluctuates. For example, the outputs of the solar cell can change depending on factors like temperature, light intensity and so on, which results in the output mixed with low-frequency ripples. When using a DC supply with low-frequency ripples as the input of multilevel inverters, conventional modulation techniques are unable to meet the need for industrial applications. Therefore, a technique that can be used to meet the needs is to be

developed and also for the accurate static performance and a strong suppression ability against the interference in DC sources. The SPWM technique is introduced for controlling the proposed CSD multilevel topology. The staircase like output voltage waveforms will be obtained and a strong inhibition ability against the interferences in DC sources is achieved.

4.3 Switching states for positive and negative output voltage waveform.

Fig 4.1 shows the proposed two-stage CSD topology. The proposed topology had a cascaded switched-diode converter with a full-bridge inverter, where n is the number of the cascaded basic units. The basic unit 1 consists of the DC voltage source or a capacitor with a DC voltage equal to u_1 and a switch S_{11} with its internal reverse diode and a separate diode named D_1 as shown in fig 4.1. It is also known that the parallel connection of the diode D_1 avoids the shoot-through phenomenon of a bridge arm. The voltage obtained at the basic unit 1 is u_{o1} and it is the combination of the input voltage u_1 and the voltage at the switch S_{11} . If the switch is open voltage is present and if the switch is closed the voltage is zero. When S_{11} is on, $S_{12} \dots S_{1n}$ is off. The cascading layout of n basic units form the first stage, as shown in Fig. 4.1. The maximum output voltage of the first stage is given as follows:

$$u_g = u_{o1} + u_{o2} + \dots + u_{on} \quad (4.1)$$

The first stage converter always produces the positive staircase waveform and for both the positive and negative output voltage waveforms both the converters are to be operated. for states of switches $S_{11}, S_{12}, \dots, S_{1(n-1)}, S_{1n}$, 2^n different values of u_g are obtained, as listed in Table 4.1. Table 4.2 lists the switch state analysis with respect to the positive sign or negative sign of a reference voltage u_{ref} . It is clear that the employment of the second-stage achieves both the positive and negative halves of the output voltage. All the Dc voltage sources are equal to u_{dc} under the symmetric case, the number of output voltage levels N_{level} and the total number of switches N_{IGBT} required are calculated as follows:

$$N_{level} = 2n + 1 \quad (4.2)$$

then the number of the required switches for a N_{Level} output voltage is derived as follows:

$$N_{IGBT} = (N_{level} + 7)/2 \quad (4.3)$$

Table 4.1 Values of u_g w.r.t switching states of the first stage.

| State | Switches states | | | | | | u_g |
|-------|-----------------|----------|----------|-------|--------------|----------|--------------------|
| | S_{11} | S_{12} | S_{13} | | $S_{1(n-1)}$ | S_{1n} | |
| 1 | off | off | off | | off | off | 0 |
| 2 | on | off | off | | off | off | u_1 |
| | | | | | | | |
| n | off | Off | off | | off | on | u_n |
| n+1 | on | on | off | | off | off | $u_1 + u_2$ |
| | | | | | | | |
| 2^n | on | on | on | | on | on | $\sum_{i=1}^n U_i$ |

Table 4.2 Values of u_o w.r.t switching states of second stage

| State | Switched states | | | | u_o |
|-------|-----------------|-------|-------|-------|--------|
| | S_1 | S_2 | S_3 | S_4 | |
| 1 | On | On | Off | Off | u_g |
| 2 | Off | Off | On | On | $-u_g$ |

Table 4.1 consists of the values of the u_g with respect to switch states of the first stage and table 4.2 consists of the values of the u_o with respect to switch states of the second stage. The tables are as follows:

The 5-level reduced switch multilevel inverter i.e. cascaded switched diode structure is shown in fig.4.2.

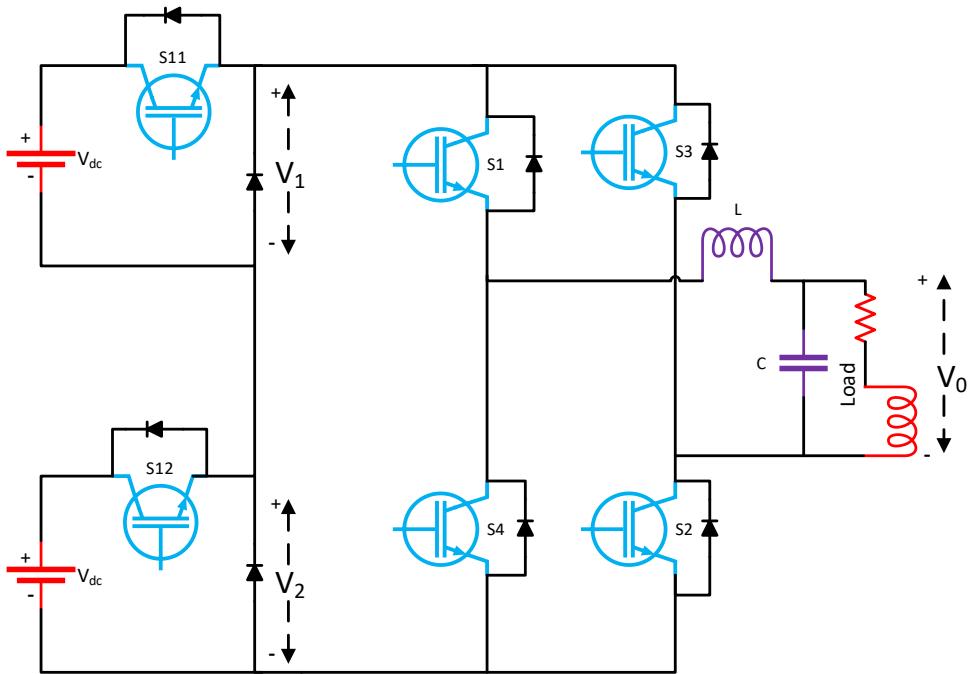


Fig. 4.2 5 Level CSD Structure

To get five level stepped waveform in the output the switches are turned on and off accordingly. The modes of operation of 5 Level CSD is as shown in table.4.3.

Table.4.3 Modes of operation of 5 Level CSD

| | S11 | S12 | S1 | S2 | S3 | S4 |
|-------------------------|------------|------------|-----------|-----------|-----------|-----------|
| V_{dc} | 1 | 0 | 1 | 1 | 0 | 0 |
| 2V_{dc} | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -V_{dc} | 1 | 0 | 0 | 0 | 1 | 1 |
| -2V_{dc} | 1 | 1 | 0 | 0 | 1 | 1 |

The 9 level cascaded switched diode structure is shown in fig.4.3

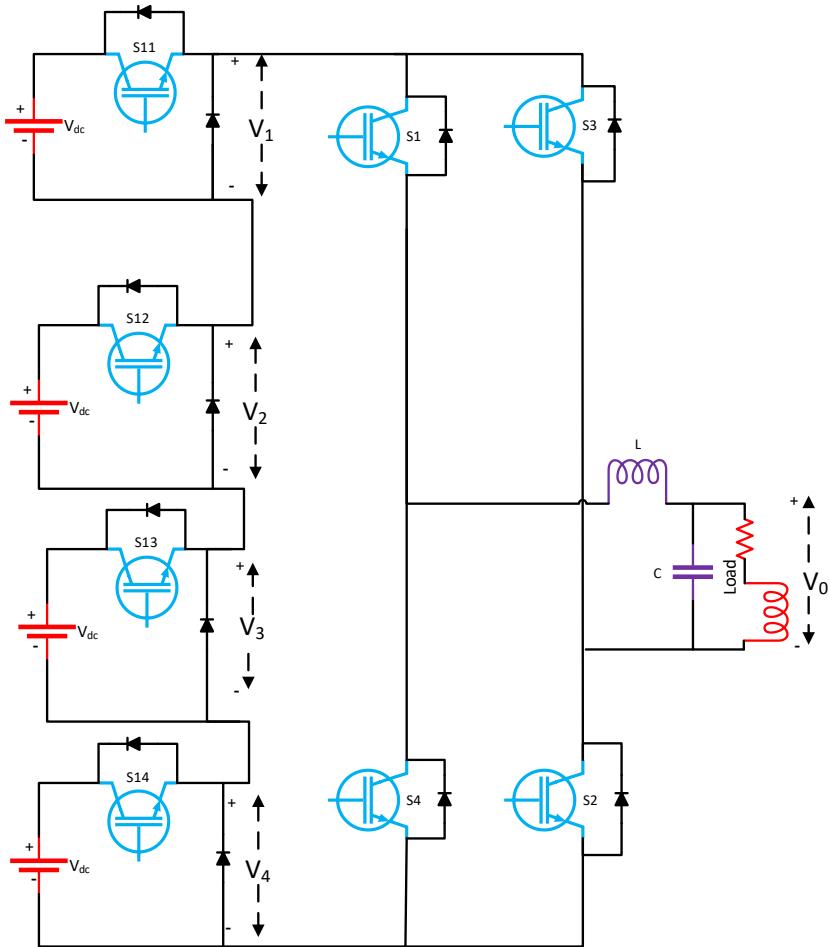


Fig.4.3 9 Level CSD structure

To get nine level stepped waveform in the output the switches are turned on and off accordingly. The modes of operation of 5 Level CSD is as shown in table.4.4.

Table.4.4 modes of operation of 9 Level CSD

| | S11 | S12 | S13 | S14 | Sg | S1 | S2 | S3 | S4 |
|--------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|
| Vdc | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 2Vdc | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 3Vdc | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 4Vdc | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -Vdc | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| -2Vdc | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| -3Vdc | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| -4Vdc | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

4.4 Carrier based PWM Techniques

There are different types of inverters and these inverters are used in their respective applications. To control switching pattern of these inverters, different PWM techniques are used such as SPWM, SVPWM, Selective Harmonic Elimination (SHE). SPWM is simplest method that can be implemented for inverters. The principle of SPWM is illustrated as follow, where sinusoidal modulating wave is compared with triangular carrier wave to give two stage (high or low). The modulating wave is compared with triangular wave, if the modulating wave amplitude is greater than amplitude of carrier wave results in high state otherwise remains at low state. At high state switch becomes on and at low state it will be turn off. SPWM technique is used to control the switching pattern of inverter which results in reduction of THD for output voltage. Any change in modulating waveform results in load current harmonics and causes EMI (Electro-Magnetic Interference), power loss, etc. PWM technique is effective modulation technique and it does not require any additional components and eliminates lower harmonics easily.

For multi carrier SPWM technique $(m-1)$ carrier waves are required for m -Level inverter. The amplitude and frequency all carrier waves must be same.

The frequency modulation index is given by

$$m_f = f_c / f_m \quad 4.4$$

Where f_c is carrier wave frequency and f_m is modulating wave frequency

$$m_a = V_m / V_c \quad 4.5$$

Where V_m is the peak value of modulating wave and V_c is peak value of each carrier wave.

Multi carrier PWM technique is used to control switching pattern of multilevel inverters. For MLI's carrier based PWM techniques are classified as

1. Single-carrier SPWM
2. Multi-carrier SPWM

The multi-carrier SPWM control techniques are further categorized as

- A. Phase shifted SPWM
- B. Level shifted SPWM
- C. Hybrid (combination of level and phase shifted)

A. Phase shifted SPWM

In the phase shifted SPWM technique all carrier wave has same peak-peak amplitude and same frequency, but there is phase shift between adjacent carrier signals. Phase shift between two carrier waves is given by

$$\phi_c = 360/(m - 1) \quad 4.6$$

B. Level shifted SPWM

Level shifted SPWM technique is categorized as

1. In phase disposition
2. Phase opposition disposition
3. Alternate phase opposition disposition

In phase disposition requires the carrier waves have same amplitude and frequency, where as there is no phase shift between them. But this carrier waves are at different offset value. It is observed that this method has lowest harmonic distortion with high modulation indices as compared to other SPWM methods

In phase opposition disposition technique for m-level inverter m-1 carrier waves are used. In which the carrier wave above the zero reference are in same phase and the carrier waves below the zero reference are also in phase, but the carrier waves below zero reference are mirror image of carrier waves above zero reference. This method has better harmonic performances at lower modulation indices.

In alternate phase opposition disposition technique for m- level inverter, (m-1) carrier waves are 180-degree phase shifted from each other. This means that adjacent carrier waves are mirror image each other.

CHAPTER 5

SIMULATION RESULTS

5.1 5 Level Cascaded H-Bridge multilevel inverter

The following are the results for the 5 Level casade H-Bridge multilevel inverter

To get the 5 level output waveform in CHB Topology the switches S₁, S₂, S₆ are turned on to get +V_{dc}. S₁, S₂, S₅, S₆ are turned on to get +2V_{dc}. S₄, S₇, S₈ are turned on to get -V_{dc}. S₃, S₄, S₇, S₈, are turned on to get -2V_{dc}. And to get smooth waveforms at the output LC filter is designed, and having a load of impedance Z = 90 Ω.

Table 5.1 Design parameters of 5 Level CHB

| Parameter | Value |
|---------------------------------|--------|
| Input voltage | 115V |
| Output voltage | 230V |
| Output current | 2.55A |
| Load resistor | 90Ω |
| Filter inductor | 35mH |
| Filter capacitor | 5.5μF |
| Operating frequency of inverter | 2500Hz |
| Output frequency | 50Hz |
| Modulation index (m_a) | 0.85 |

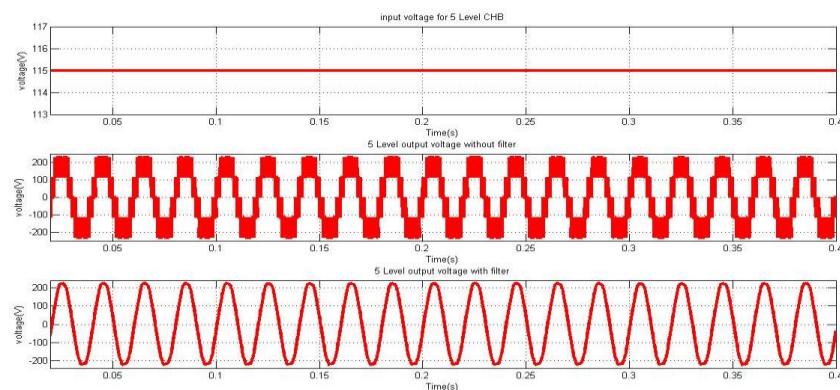


Fig.5.1 CHB 5 Level output voltage waveforms

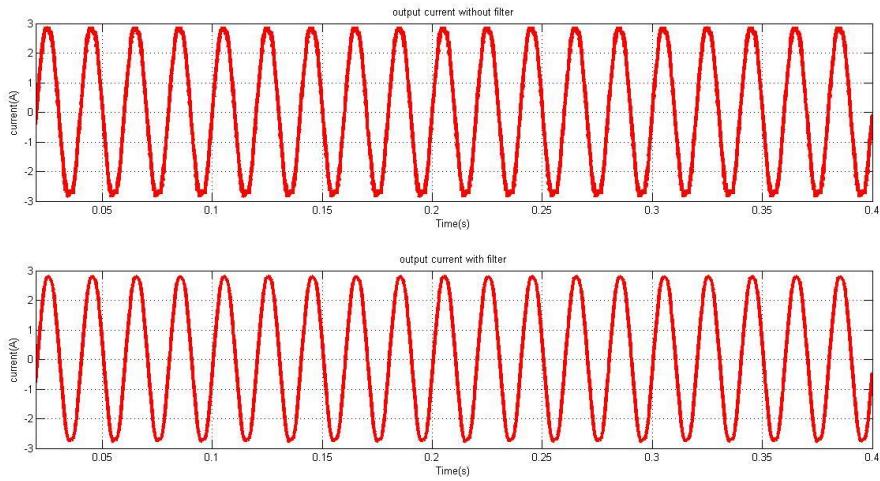


Fig.5.2 CHB 5 Level output current waveforms

The stepped 5 Level output voltage across the load is shown in fig 5.1(b), after passing that stepped waveform through LC filter the smooth 5 Level output waveform is obtained as shown in fig 5.1(c), the output current waveform for the 5 Level CHB without filter is shown in fig 5.2(a) and with filter is shown in fig.5.2(b). The input voltage given to the 5 Level CHB is 115V is as shown in fig.5.1(a).

The total harmonic distortion obtained for 5 Level CHB stepped output is 28.79% as shown in fig 5.3 and reduced to 2.99% as shown in fig.5.4 using LC filter

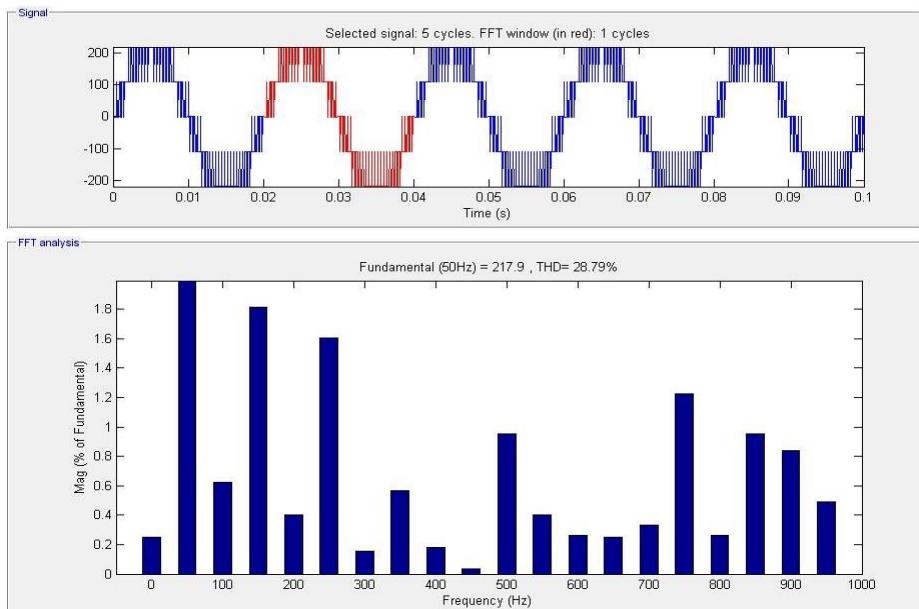


Fig.5.3 THD for CHB 5 Level output without filter

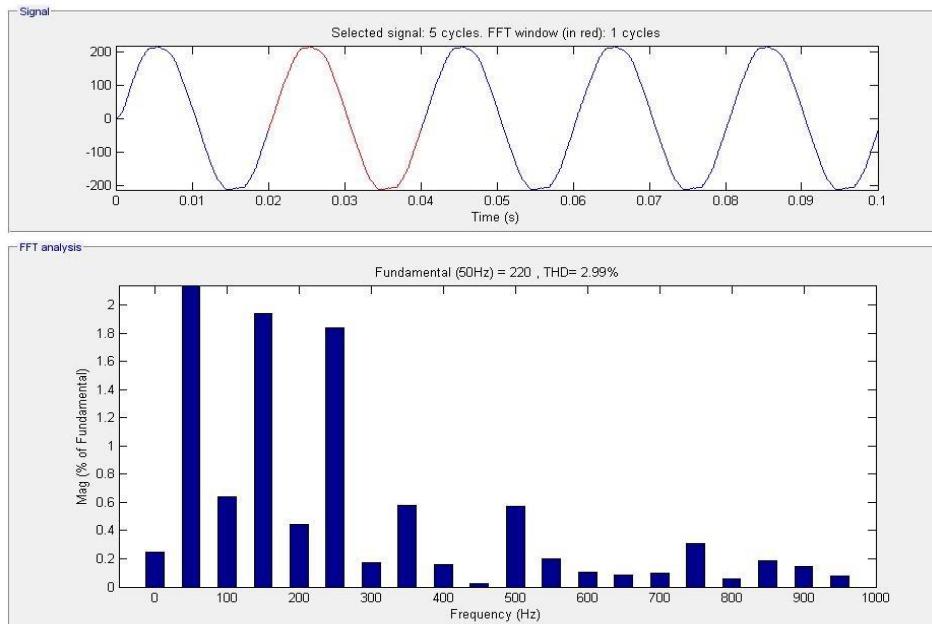


Fig.5.4 THD for CHB 5 Level output with filter

The gating pulse given the switches to get 5 Level positive cycle is shown in the fig.5.5

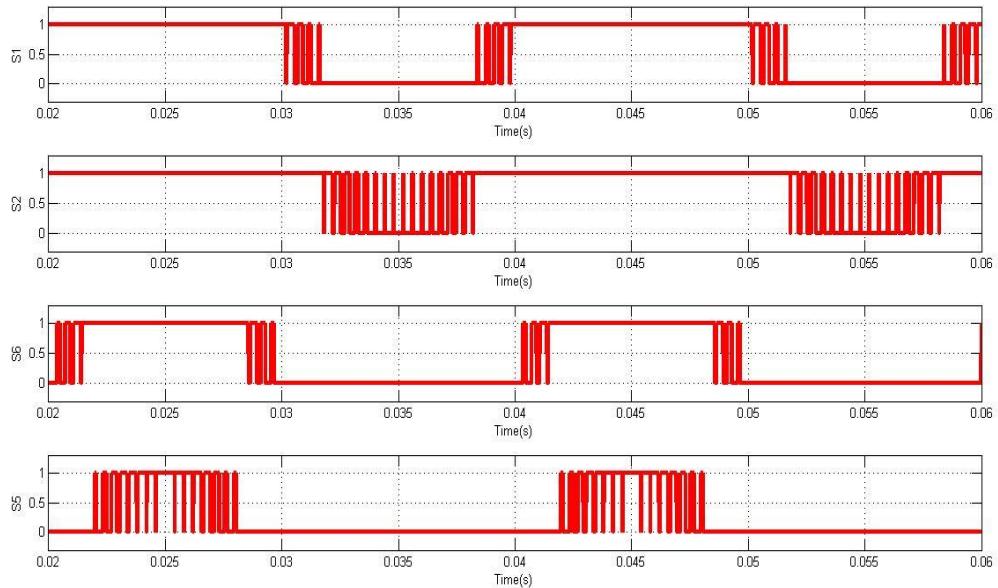


Fig 5.5 Gating pulses for positive half cycle of 5 Level CHB

The gating pulses given to the switches to get 5 Level negative cycle is shown in fig 5.6

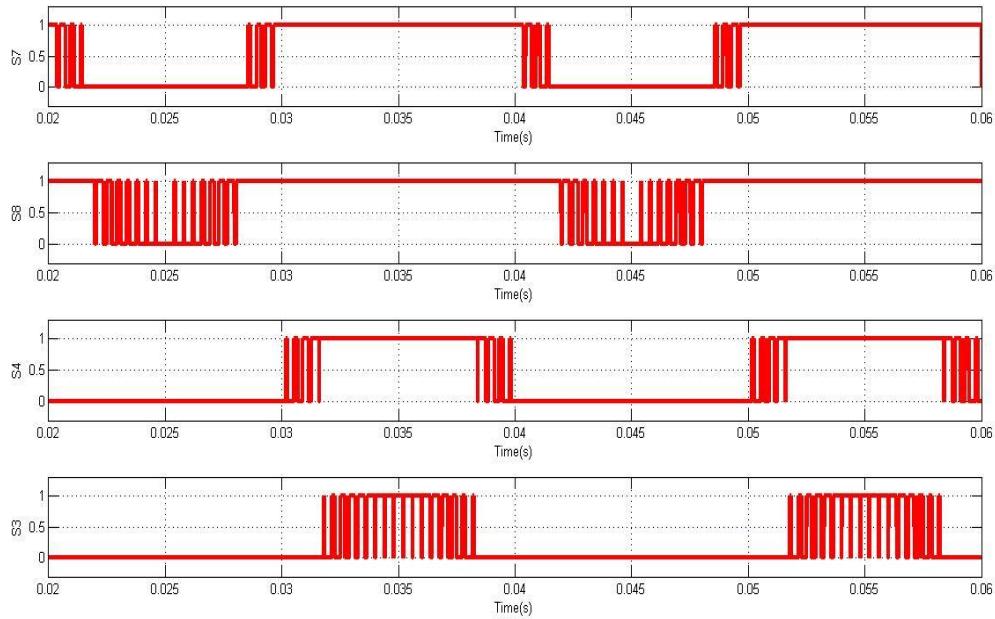


Fig. 5.6 Gating pulse for negative half cycle of 5 Level CHB

5.2 9 Level Cascaded H-Bridge multilevel inverter

The following are the results of the 9 Level Cascade multilevel inverter topology

To get 9 Level output the switches of CHB are turned on and off accordingly. To get $+V_{dc}$ the switches $S_1, S_2, S_6, S_{10}, S_{14}$ are turned on.

Table 5.2 Design parameters of 9 Level CHB

| Parameter | Value |
|---------------------------------|--------|
| Input voltage | 57.5V |
| Output voltage | 230V |
| Output current | 2.55A |
| Load resistor | 90Ω |
| Filter inductor | 20mH |
| Filter capacitor | 3.5μF |
| Operating frequency of inverter | 2500Hz |
| Output frequency | 50Hz |
| Modulation index (m_a) | 0.85 |

To get $2V_{dc}$ the switches $S_1, S_2, S_6, S_{10}, S_{13}, S_{14}$ are turned on To get $3V_{dc}$ the switches $S_1, S_2, S_6, S_9, S_{10}, S_{13}, S_{14}$ are turned on. To get $4V_{dc}$ the switches $S_1, S_2, S_5, S_6, S_9, S_{10}, S_{13}, S_{14}$ are turned on.

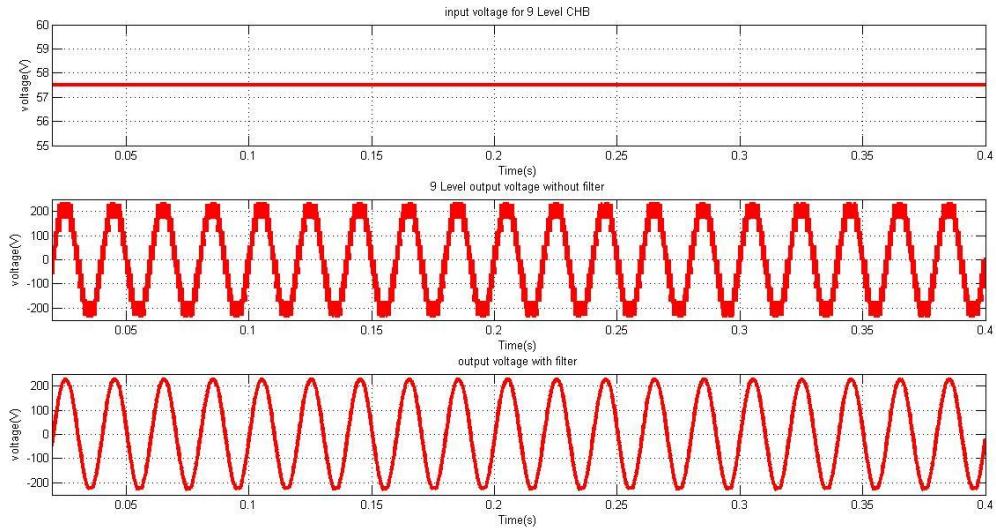


Fig.5.7 CHB 9 Level output voltage waveforms

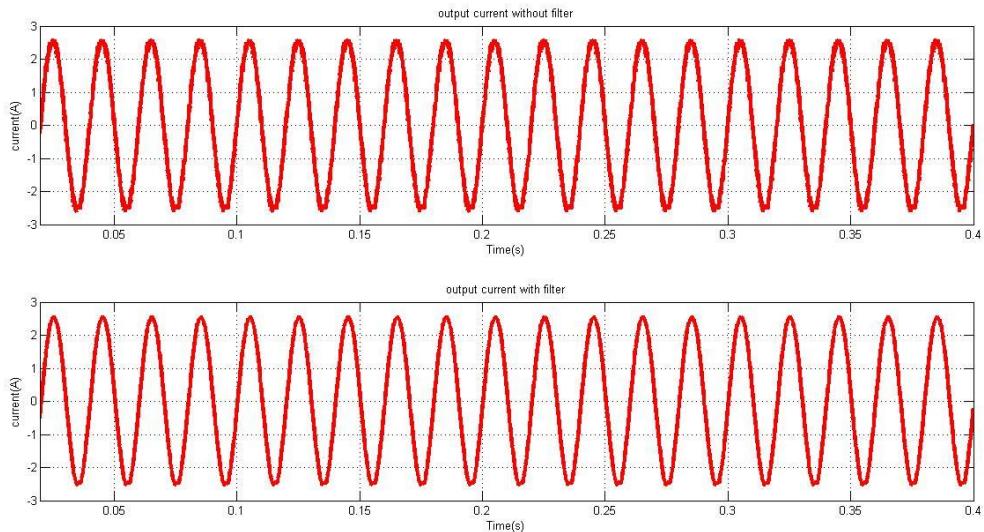


Fig.5.8 CHB 9 Level output current waveforms

To get $-V_{dc}$ the switches $S_4, S_8, S_{12}, S_{15}, S_{16}$ are turned on. To get $-2V_{dc}$ the switches $S_3, S_4, S_8, S_{12}, S_{15}, S_{16}$ are turned on. To get $-3V_{dc}$ the switches $S_3, S_4, S_7, S_8, S_{12}, S_{15}, S_{16}$ are turned on. To get $-4V_{dc}$ the switches $S_3, S_4, S_7, S_8, S_{11}, S_{12}, S_{15}, S_{16}$ are turned on. The load impedance of the CHB 9 Level multilevel inverter is $Z = 90\Omega$. The filter design is same as the design of CHB 5 Level multilevel inverter.the 9 level CHB output waveforms are shown in fig.5.7 and fig.5.8.

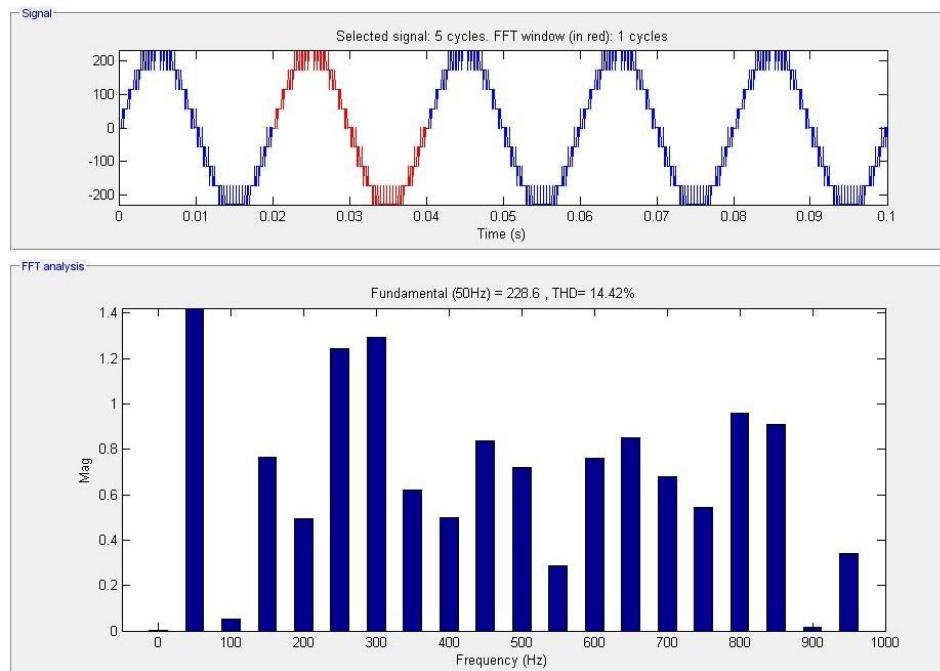


Fig.5.9 THD for CHB 9 Level output without filter

the 9 Level stepped output voltage is shown in fig 5.7(b), after passing that stepped output through filter the smooth sinusoidal waveform is obtained as shown in fig.5.7(c), the load current of CHB (level inverter is shown in fig.5.8) The total harmonic distortion for the CHB 9 Level inverter without filter is shown in fig.5.9 and with filter is shown in fig.5.10

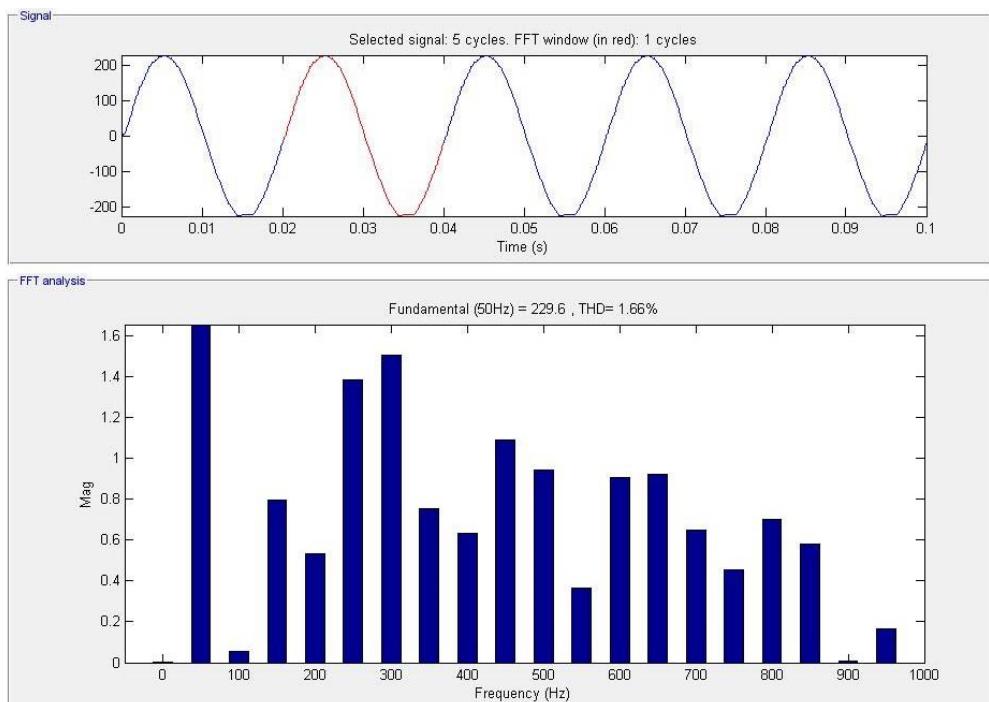


Fig.5.10 THD for CHB 9 Level output with filter

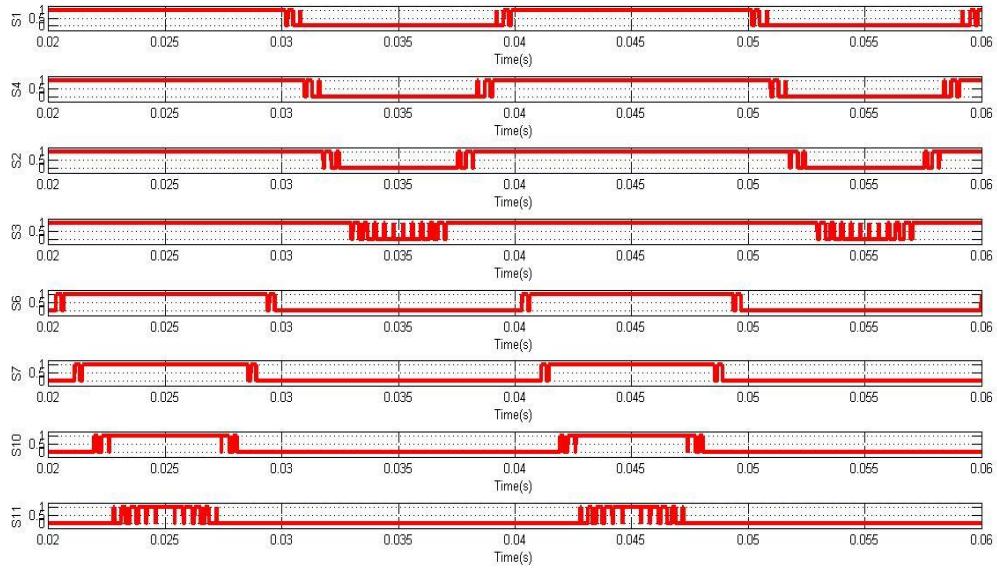


Fig.5.11 Gating pulses for positive half cycle of 9 Level CHB

The gating pulses required to get the positive half cycle of 9 level output is shown in fig 5.11

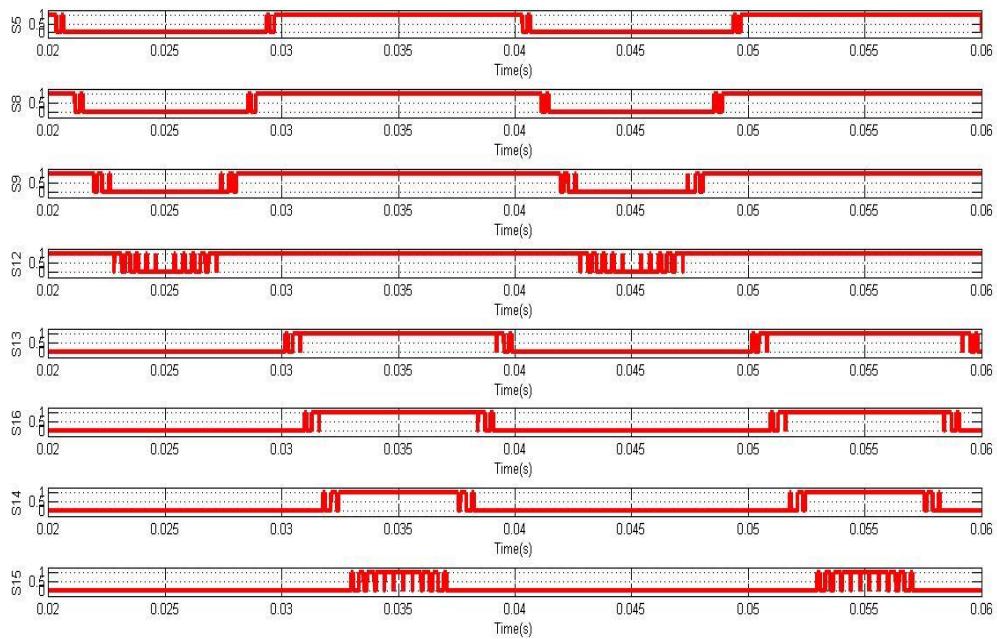


Fig.5.12 Gating pulses for negative half cycle of 9 Level CHB

The gating pulses required to get the negative half cycle of 9 Level output is shown in fig.5.12

5.3 5 Level cascaded switched-Diode multilevel inverter

The following are the results of 5 Level cascaded switched-Diode multilevel inverter

Table 5.3 Design parameters of 5 Level CSD

| Parameter | Value |
|---------------------------------|--------|
| Input voltage | 115V |
| Output voltage | 230V |
| Output current | 2.55A |
| Load resistor | 90Ω |
| Filter inductor | 35mH |
| Filter capacitor | 5.5μF |
| Operating frequency of inverter | 2500Hz |
| Output frequency | 50Hz |
| Modulation index (m_a) | 0.85 |

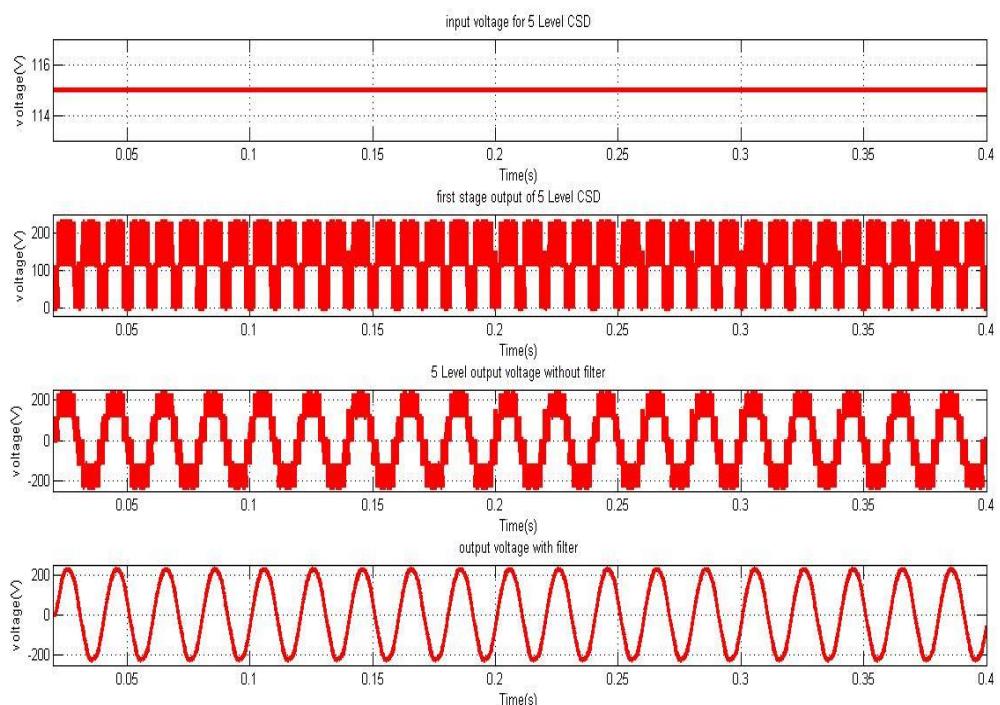


Fig.5.13 CSD 5 Level ouput voltage waveforms

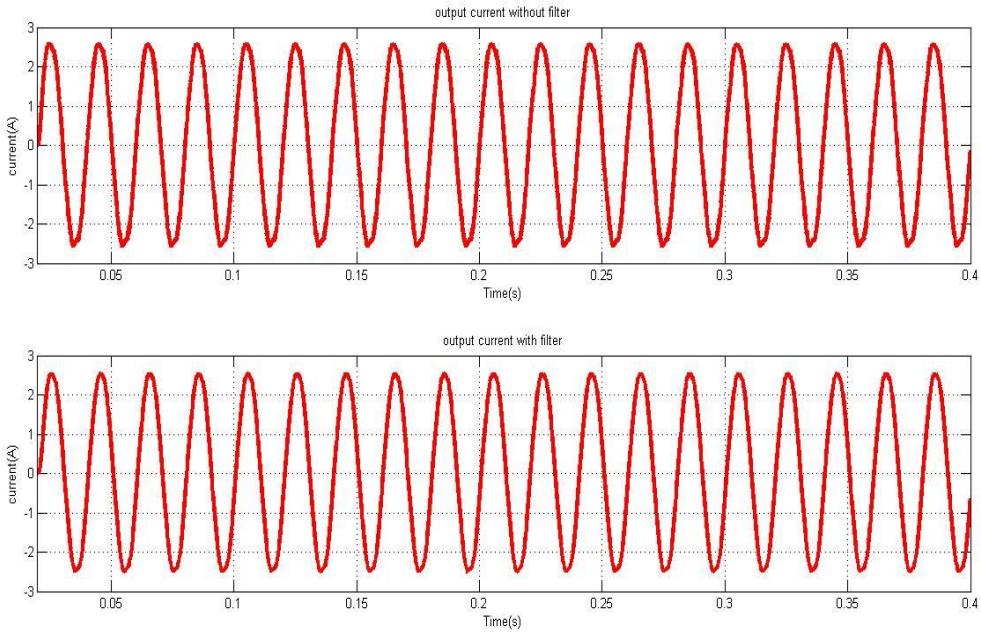


Fig.5.14 CSD 5 Level output current waveforms

To get the 5 Level output of Cascaded switched-Diode multilevel inverter the following switching sequences are followed. To get $+V_{dc}$ the switches S_{11}, S_1, S_2 are turned on. To get $+2V_{dc}$ the switches S_{11}, S_{12}, S_1, S_2 are turned on.

To get $-V_{dc}$ the switches S_{11}, S_3, S_4 are turned on. To get $-2V_{dc}$ the switches S_{11}, S_{12}, S_3, S_4 are turned on. The load impedance of a 5 Level cascaded switch-Diode multilevel inverter is $Z = 90\Omega$. The output of first stage 5 Leve CSD is shown in fig.5.13(b). in first stage only positive waveforms are obtained. In second stage positive waveforms can be converted into sinusoidal waveforms by using inverter. The final 5 Level stepped output waveform is shown in fig.5.13(c). after passing that stepped waveform into filter the smooth waveform is obtained as shown in fig.5.13(d). the output load current is shown in fig.5.14.

The total harmonic distortion of stepped 5 Level CSD output without filter is shown in fig.5.15 and with filter is shown in fig.5.16

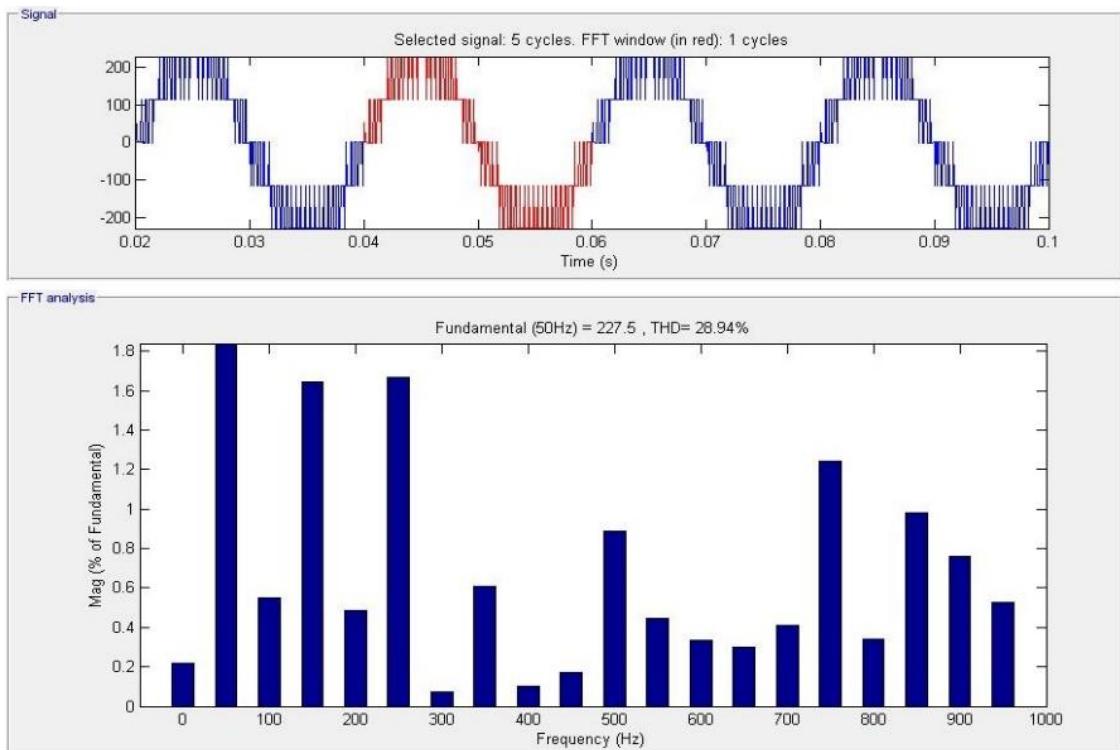


Fig.5.15 THD for CSD 5 Level output without filter

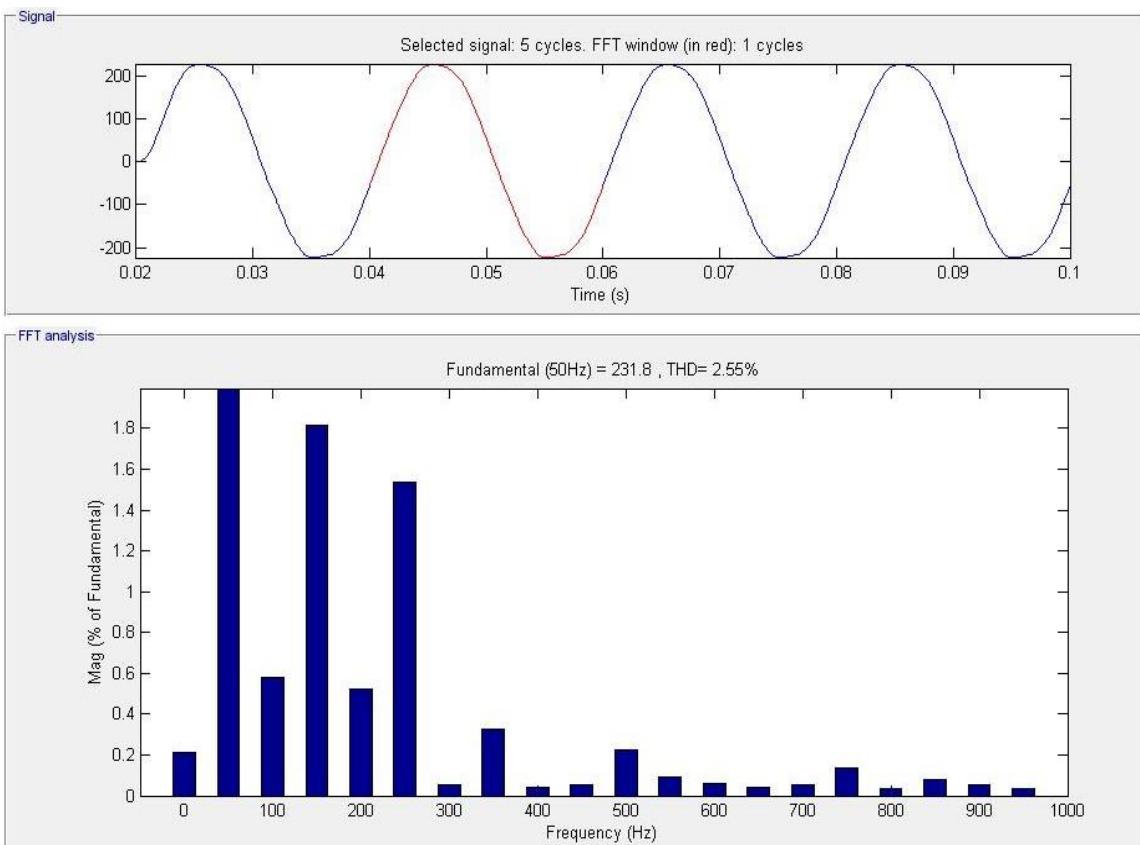


Fig.5.16 THD for CSD 5 Level output with filter

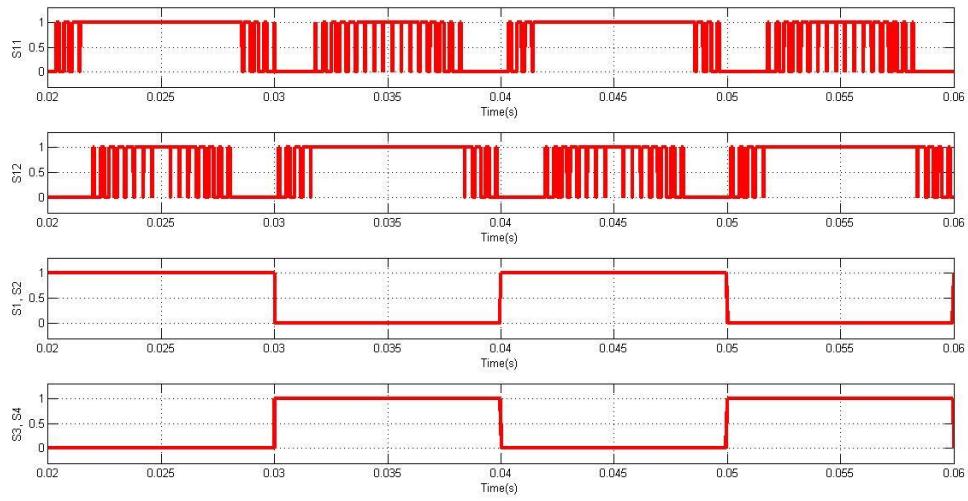


Fig.5.17 Gating pulses for 5 Level CSD

The gating pulses for CSD 5 Level are shown in fig.5.17

5.4 9 Level Cascaded Switched-Diode multilevel inverter

The following are the results of 9 Level cascaded switched-Diode multilevel inverter

To get the 9 Level output the switches of CSD are turned on in the following sequence. To get $+V_{dc}$ the switches S_{11}, S_1, S_2 are turned on. To get $+2V_{dc}$ the switches S_{11}, S_{12}, S_1, S_2 are turned on. To get $+3V_{dc}$ the switches $S_{11}, S_{12}, S_{13}, S_1, S_2$ are turned on. To get $+4V_{dc}$ the switches $S_{11}, S_{12}, S_{13}, S_{14}, S_1, S_2$ are turned on.

Table 5.4 Design parameters of 9 Level CSD

| Parameter | Value |
|---------------------------------|--------|
| Input voltage | 57.5V |
| Output voltage | 230V |
| Output current | 2.55A |
| Load resistor | 90Ω |
| Filter inductor | 20mH |
| Filter capacitor | 3.5μF |
| Operating frequency of inverter | 2500Hz |
| Output frequency | 50Hz |
| Modulation index (m_a) | 0.85 |

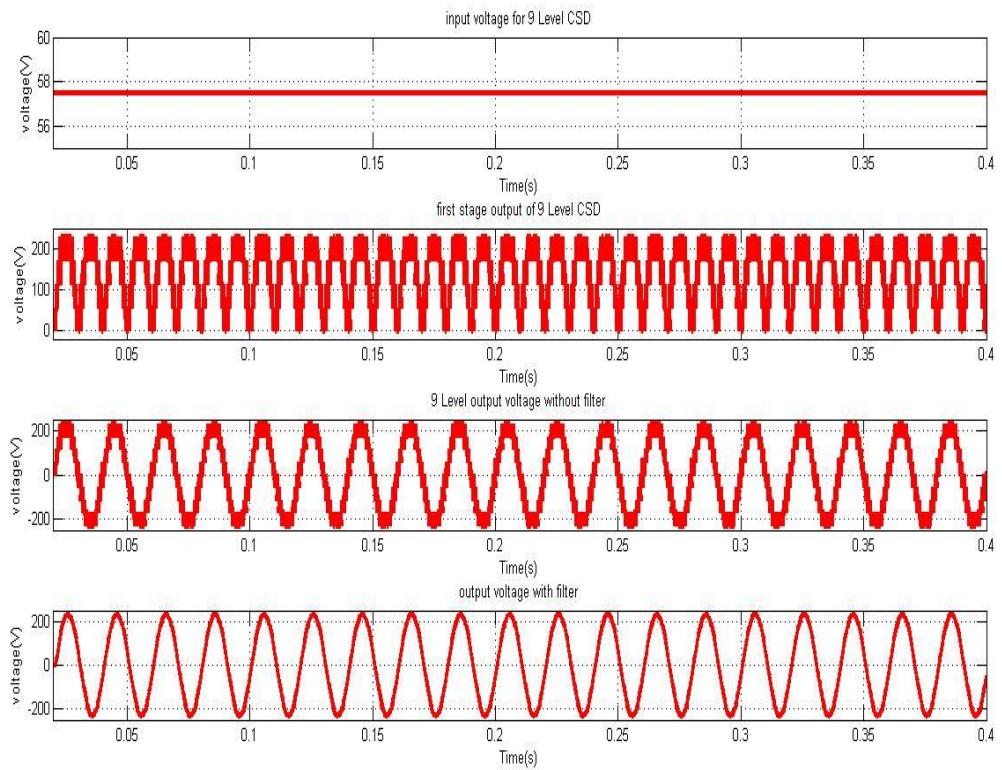


Fig.5.18 CSD 9 Level output voltage waveforms

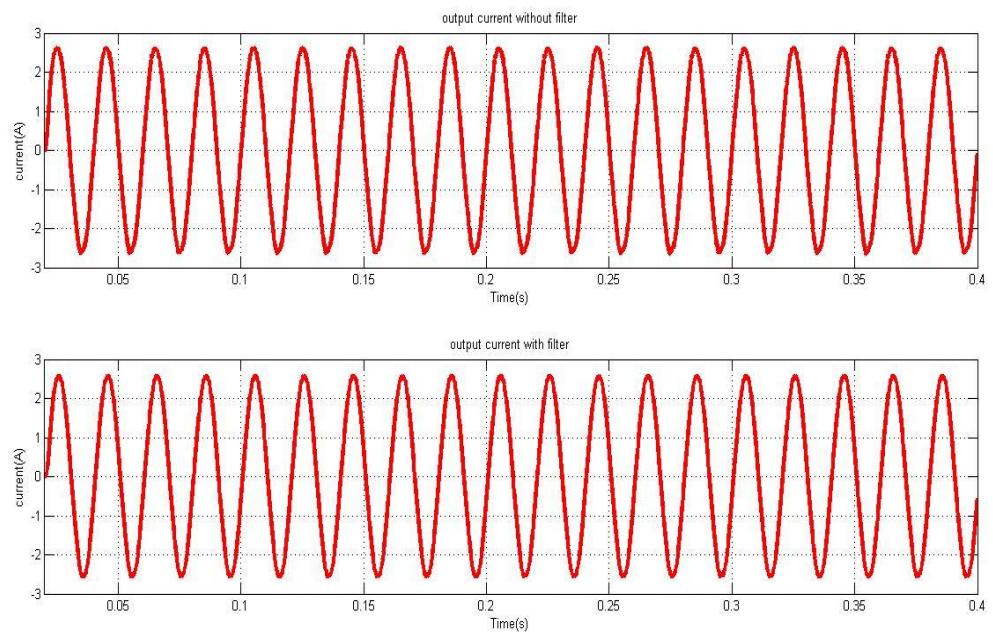


Fig.5.19 CSD 9 Level output current waveforms

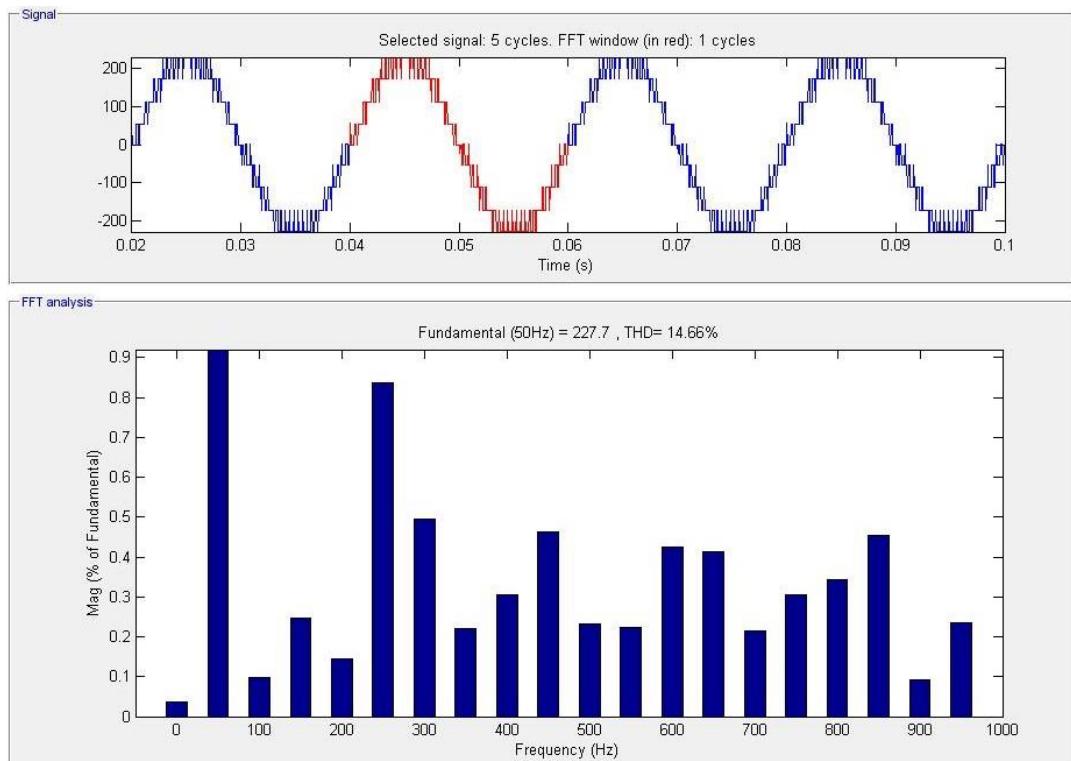


Fig.5.20 THD for CSD 9 Level output without filter

To get $-V_{dc}$ the switches S_{11}, S_3, S_4 are turned on. To get $-2V_{dc}$ the switches S_{11}, S_{12}, S_3, S_4 are turned on. To get $-3V_{dc}$ the switches $S_{11}, S_{12}, S_{13}, S_3, S_4$ are turned on. To get $-4V_{dc}$ the switches $S_{11}, S_{12}, S_{13}, S_{14}, S_3, S_4$ are turned on. The load impedance of a 5 Level CSD is $Z = 90 \Omega$. The 9 Level CSD first stage stepped output is shown in fig.5.18(b). the second stage 9 Level stepped CSD output is shown in fig.5.18(c). the stepped output after passing through filter becomes smooth as shown in fig.5.18(d). the load current of 9 Level CSD is as shown in fig.5.19.

Total harmonic distortion for CSD 9 Level Stepped output without filter is shown in fig.5.20 and with filter is shown in fig.5.21

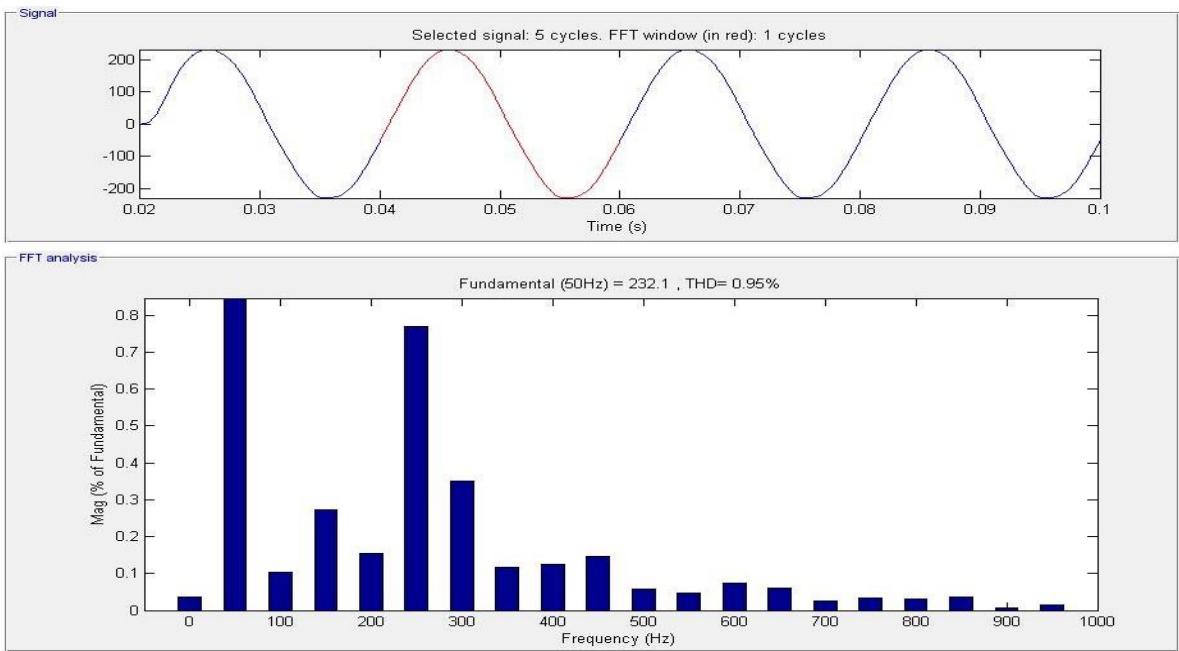


Fig.5.21 THD for CSD 9 Level output with filter

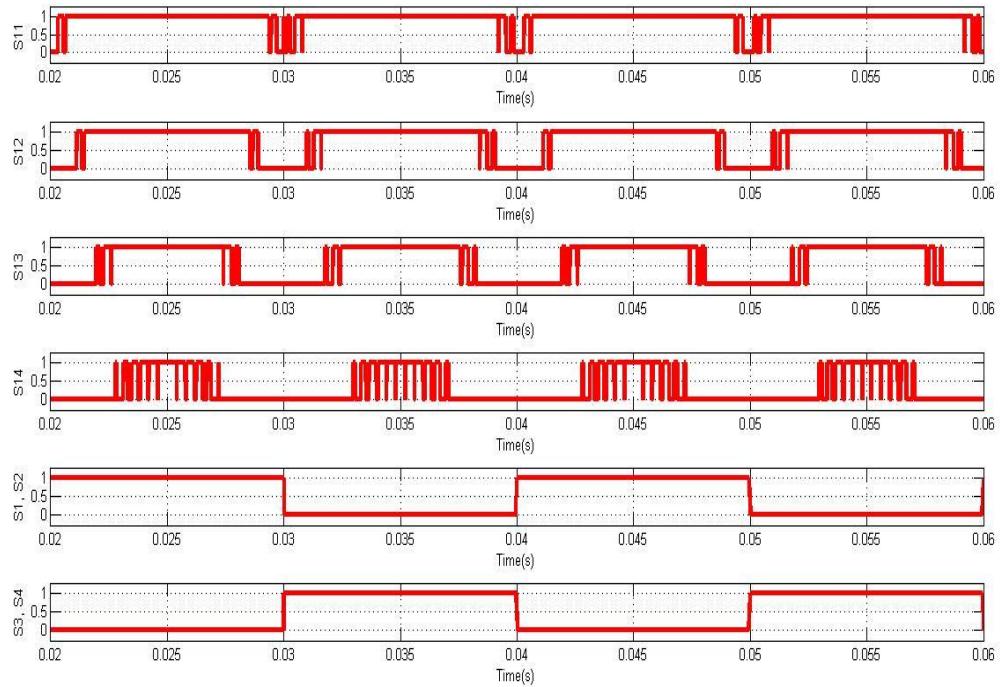


Fig.5.22 Gating pulses for 9 Level CSD

The gating pulses required to get first stage output waveform is as shown in fig.5.22.

CHAPTER 6

COMPARISION OF CHB AND CSD MULTILEVEL INVERTERS

6.1 Introduction

A recent study on the consumption of electrical energy shows that consumption is rapidly increasing due to the increase in energy demand. Therefore, resulting in the extinction of fossil fuels. So, the requirement for fossil fuels is increased largely. By using renewable energy sources, the control of the energy demand is possible. There are several multilevel inverter topologies present for renewable energy integration. But the cascaded version of the multilevel inverters gives a lot of advantages over other topologies. There are three main types in the cascaded form of multilevel inverters. They are as follows:

- 1)cascaded H-bridge multilevel inverter.
- 2)cascaded half-bridge multilevel inverter.
- 3)cascaded switched diode multilevel inverter.

These three types have a lot of advantages over the diode clamped multilevel inverter and flying capacitor multilevel inverter. In renewable integration, the cascaded switched diode multilevel inverter can yield the best results out of the three multilevel inverters mainly because of the advantages it gets over the other two topologies of multilevel inverters. In today's modern world, a conventional two-level inverter is not very efficient when compared to the cascaded switched diode multilevel inverter. As the name suggests the conventional two-level inverter comes with only two levels which is a major drawback considering the levels required nowadays. The conventional inverters are replaced by the multilevel inverters because of the good power quality, low switching losses, and high voltage capability. The main aim of the multilevel inverters is to produce multiple output voltage levels with less power switching losses and less harmonic distortion losses. The cascaded H-bridge multilevel inverter has a major disadvantage that requires a greater number of switches which results in more switching losses. The cascaded H-bridge multilevel inverter is an expensive multilevel inverter and has a

complex system. Then the cascaded half-bridge multilevel inverter is introduced which reduces the consumption of switches and reduces the switching losses very less when compared to the cascaded H-bridge. The cascaded half-bridge topology also produces more voltage levels than the CHB topology. Under the R-L load, there will be high voltage spikes occurring at the stepped output voltage but by using the cascaded half-bridge topology, there will be no path to flow these reverse currents resulting in deteriorated power quality which is considered as a major disadvantage in cascaded half-bridge topology. Therefore, the cascaded switched diode multilevel inverter is introduced which eliminates the disadvantage that occurs at the previous topology by adding a path for reverse currents to flow and also produce more voltage levels. By comparing the cascaded H-bridge multilevel inverter with the cascaded switched diode multilevel inverter gives the idea that why it's better to use cascaded switched diode topology for renewable energy integration.

6.2 Topology of the cascaded H-bridge multilevel inverter

By developing better power conversion converters, a lot of electrical energy can be saved and can be used efficiently in transmission, distribution, consumption sectors. The conventional inverter comes with the two levels generates the average voltage equal to the reference. But the losses in the conventional topology are very high. Therefore, multilevel inverters are introduced to eliminate these issues. The main theme of these multilevel inverters is to develop the desired output voltage from several input DC voltage sources. Several types of multilevel inverters are mentioned in the previous chapters i.e., diode clamped MLI, flying capacitor MLI, cascaded topologies. Cascaded H-bridge MLI topology is one of the most attractive topologies in MLI's. The cascaded H-bridge MLI has simple construction and control with many control techniques. The configuration of CHB MLI is a series-connected two-level H-bridge inverter with a separate DC source for each one. The topology of the cascaded H-bridge multilevel inverter is as follows:

The major disadvantages of CHB topology are as follows:

- (a) increased number of isolated input DC voltage sources.
- (b) increased number of switching devices which increase significantly MLI overall cost compared to conventional two levels inverters topology.

Resulting in developing of variety of techniques to reduce the number of utilized DC sources by selecting their values. Therefore, MLIs are classified based on the selection of utilized DC sources values. In the symmetric multilevel inverters, all DC sources have the same

amplitude. Therefore, the MLI output voltage is generated by directly adding all the V_{dcn} sources, resulting in number DC sources equal to the number of required output levels. This method is not an efficient method to select and utilize the DC sources in MLI.

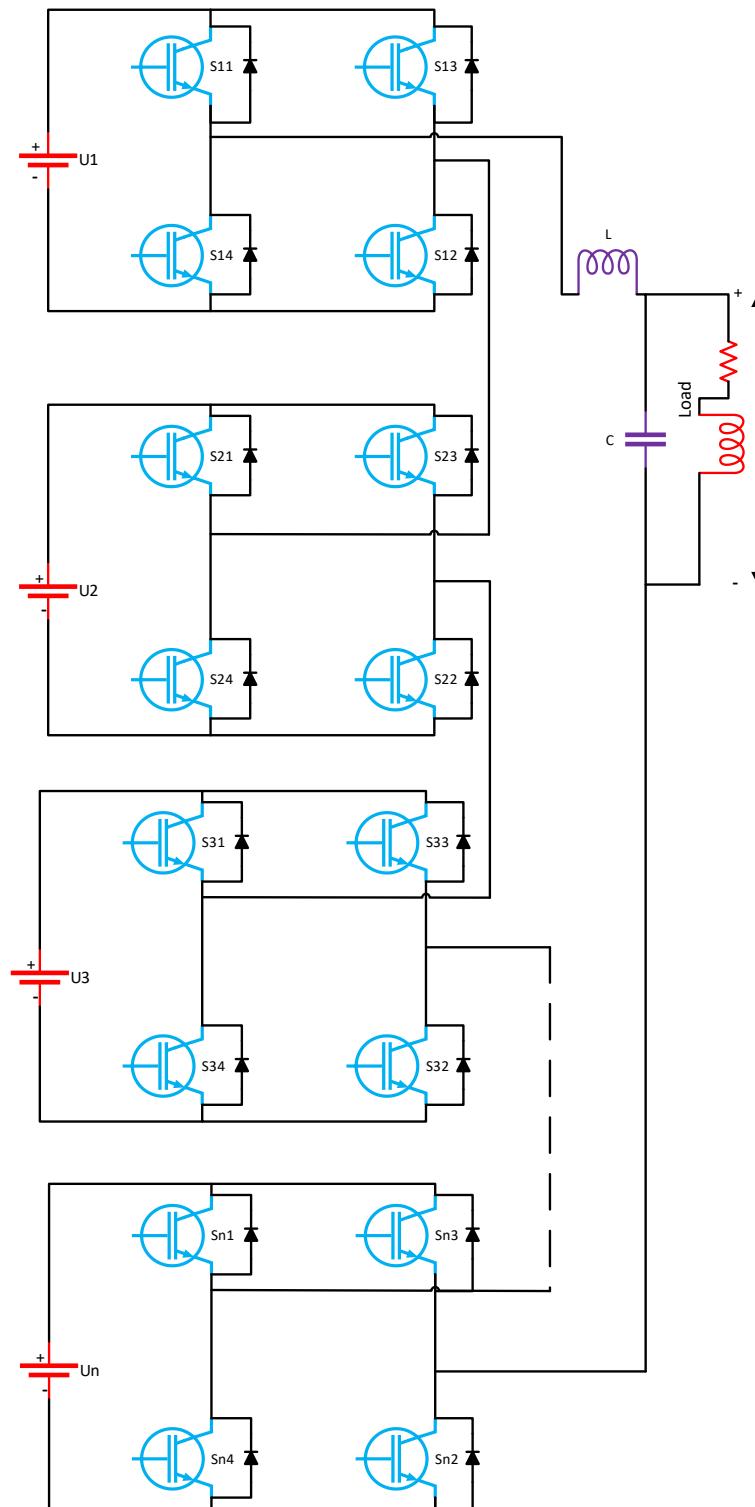


Fig.6.1 Topology of the cascaded H-bridge multilevel inverter

There are n DC sources present at the CHB topology each connected to an inverter called H-bridge inverter, as shown in Fig.6.1. Three levels of the output voltage can be generated from each H-bridge i.e., u_{dc} , 0 , $-u_{dc}$. In the case of symmetric, the number of required switches for a N_{level} output voltage is obtained as follows:

$$N_{IGBT} = 2N_{Level} - 2 \quad (6.1)$$

6.3 Topology of Cascaded Switched Diode

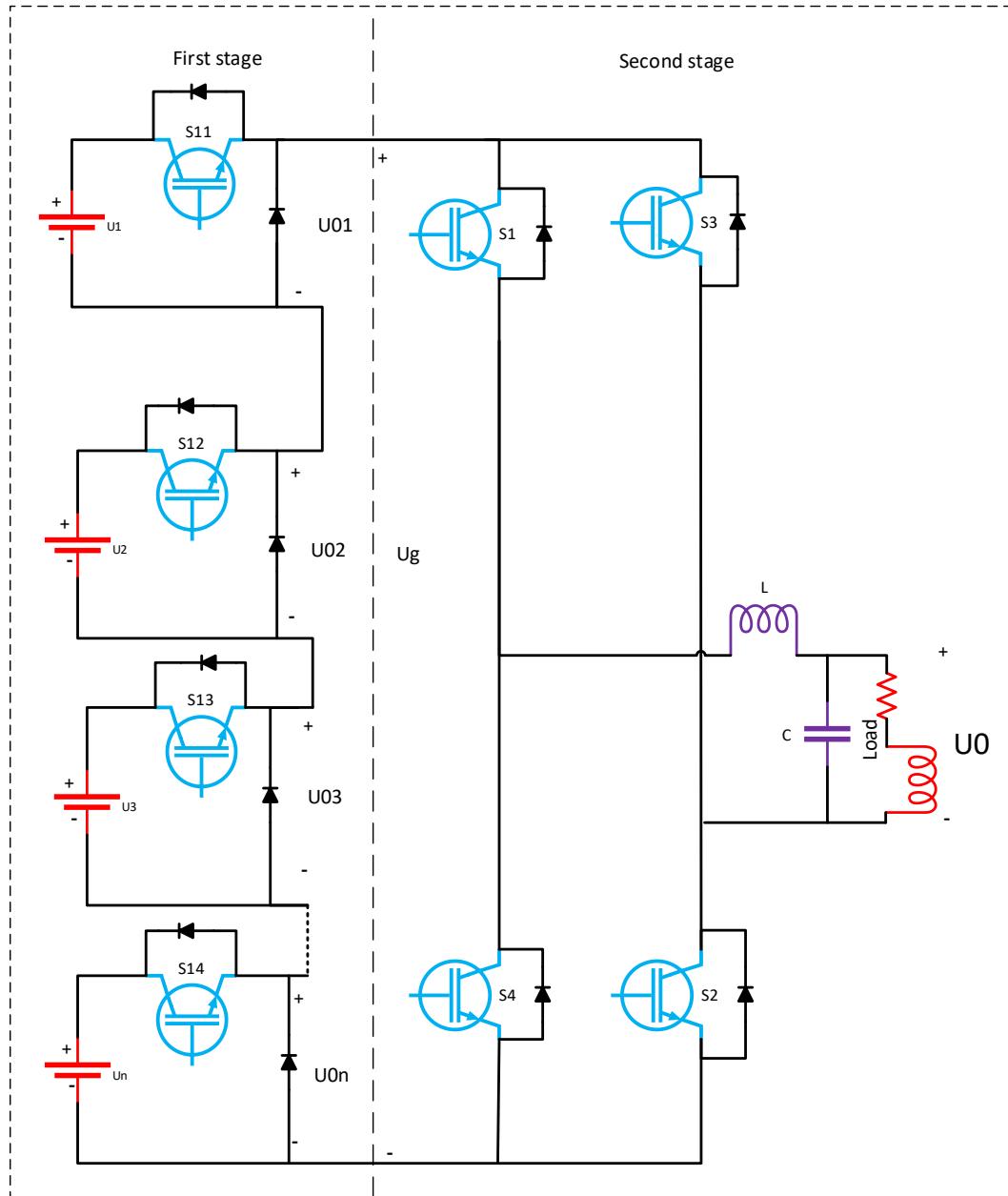


Fig.6.2 The structure of the proposed two-staged CSD topology

The cascaded switched diode topology which is shown in fig 6.2 overcomes all the disadvantages obtained during the cascaded H-bridge and cascade half-bridge multilevel inverters. The CSD topology has a switch S_g is connected between unit 2 and unit n which blocks the high voltage. This switch is considered a spike removal switch in CSD topology. The voltage and current ratings are very important in designing the inverters. Also, the proposed CSD topology has the highest voltage rating. The number of the required switches for a N_{level} output voltage is derived as follows:

$$N_{\text{IGBT}} = (N_{\text{level}} + 7)/2 \quad (6.2)$$

So, as the levels started to increase, the required number of switches started to decrease a lot when compared to the CHB topology. The main aim of this proposed CSD topology is to reduce the number of required switches and produce more voltage levels. The reliability, cost, circuit size, and control complexity are always based on the switches. The important factor in designing a multilevel converter is the rating of switches. In the above-mentioned topologies, the currents of all devices are equal to the rated currents of the loads. Therefore, the power component requirements among the CHB and the proposed CSD topologies are listed in Table 6.1 concerning the number of required switches and voltage rating of all the devices. And the fig.6.3 showing the difference between the CHB topology and cascaded switched diode topology is as follows:

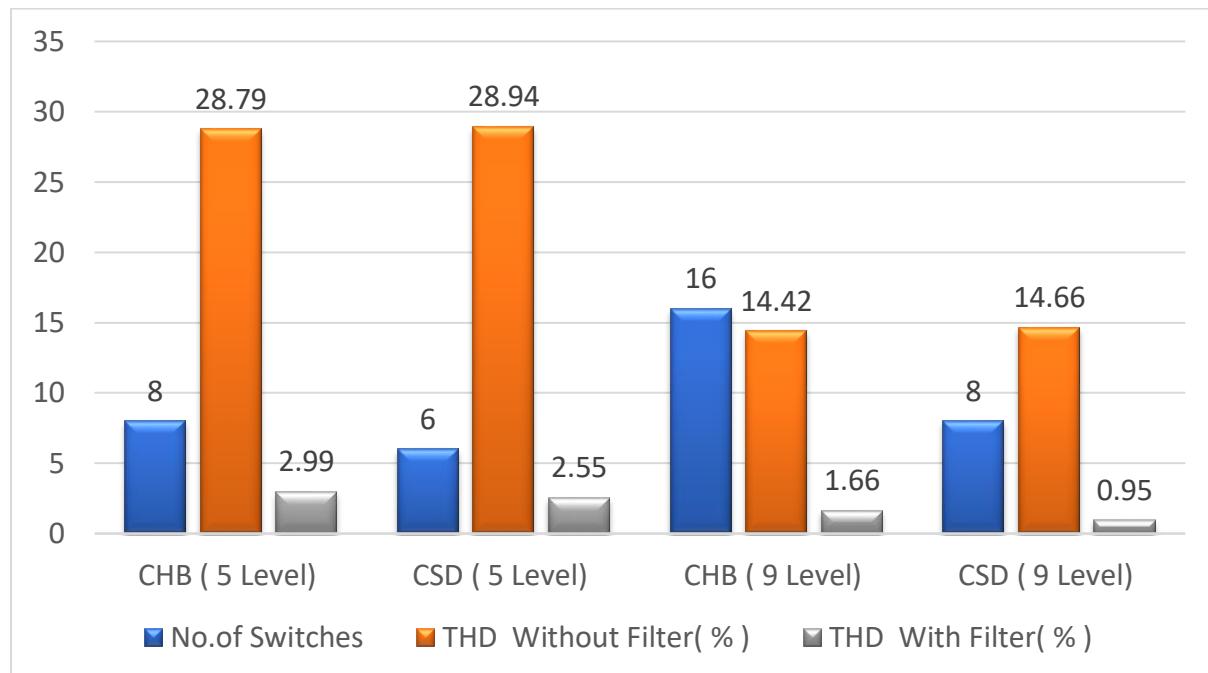


Fig.6.3 Comparison of CHB and CSD Topologies.

In the case of the 5-level, the number of switches required by CHB topology is 8 but in CSD topology the number is reduced to 6 and in the case of 9-level, the number is greatly reduced from 16 to 8. The THD levels with and without filters are relatively high in CHB topology when compared to CSD topology. The harmonic distortions produced in the process are very less in CSD topology which makes it more suitable for renewable energy integration. The mathematical equations of the maximum output voltage, no. of required switches, voltage rating of Sg and all the switches and diodes are presented below.

Therefore, by comparing these two topologies of cascaded multilevel inverters in different sectors, the CSD topology is more efficient than the CHB topology which makes it more suitable for renewable energy integration.

Therefore, the power component requirements are listed in table 6.1 as follows:

Table 6.1 comparison of CHB and CSD

| | CHB | CSD |
|---|---------------------------|--|
| Maximum output Voltage | $U_{dc}((N_{level}-1)/2)$ | $U_{dc}((N_{level}-1)/2)$ |
| No. of required switches | $2(N_{level}-1)$ | $(N_{level}+7)/2$ |
| Voltage rating of Sg (CSD) | N/A | $u_{dc}((N_{level}-3)/2)$ |
| Voltage rating of all the switches and diodes | $2u_{dc}(N_{level}-1)$ | $3u_{dc}(N_{level}-3)+(u_{dc}(N_{level}-1)/2)$ |

CONCLUSION

In this project, a new topology of cascaded switched diode multilevel inverter is designed for renewable energy integration. The topologies of cascaded H-Bridge and cascaded switched diode multilevel inverters have been analyzed for both 5 and 9 levels, sinusoidal pulse width modulation technique is used to generate gating pulses. To reduce the THD of the developed topology multicarrier in phase disposition SPWM technique and LC filter is used. 5 and 9 Level output is observed in respective topology. The number of switches used in the topology is less which in turn reduced the corresponding gate driving circuitry and made the circuit compact size. The circuit of developed multilevel inverter is simulated in MATLAB/SIMULINK and the total harmonic distortions for CHB and CSD are obtained by using FFT analysis window. The lowest THD observed with LC filter is 0.95%. In phase level shifting SPWM is used for pulse generation

REFERENCES

- [1] Lei Wang, Q.H.Wu, Wenhua Tang, “Novel Cascaded Switched-Diode Multilevel Inverter for Renewable Energy Integration,” *IEEE Trans. Energy convers.*, vol. 32, no.4, pp.1574-1582, Dec. 2017
- [2] F. S. Kang, S. J. Park, S. E. Cho, C. U. Kim, and T. Ise, “Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems,” *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906–915, Dec. 2005.
- [3] L. V. Nguyen, H.-D. Tran, and T. T. Johnson, “Virtual prototyping for distributed control of a fault-tolerant modular multilevel inverter for photovoltaics,” *IEEE Trans. Energy Convers.*, vol. 29, no. 4, pp. 841–850, Dec. 2014.
- [4] J. Rodriguez, J. S. Lai, and F. Z. Peng, “Multilevel inverters: A survey of topologies, controls, and application,” *IEEE Trans. Ind. Electron.*, vol.49, no. 4, pp. 724–738, Aug. 2002.
- [5] F. Z. Peng and J. S. Lai, “Multilevel converters—A new breed of power converters,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun.1996.
- [6] E.Villanueva, P. Correa, J. Rodriguez, and M. Pacas, “Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.
- [7] F.Khoucha, M.S.Lagoun, A.Kheloui, and M.E.H.Benbouzid,“A comparison of symmetrical and asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives,” *IEEE Trans. Energy Convers.*, vol. 26, no. 1, pp. 64–72, Mar. 2011.
- [8] M. Hamzeh, A. Ghazanfari, H. Mokhtari, and H. Karimi, “Integrating hybrid power sources into an islanded MV micro grid using CHB multilevel inverter under unbalanced and nonlinear load conditions,” *IEEE Trans. Energy Convers.*, vol. 28, no. 3, pp. 643–651, Sep. 2013.
- [9] S.A. Khajehhosseni, A. Bakhshai, and P. K. Jain, “A simple voltage balancing scheme for m-level diode-clamped multilevel converters based on a generalized current flow model,” *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2248–2259, Sep. 2008.

- [10] H.Sepahvand, K.A.Corzine, M.Ferdowsi, and M.Khazraei, “Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 769–778, Feb. 2012
- [11] A. Khoshkbar Sadigh, V. Dargabi, and K. Corzine, “New flying-capacitor based multilevel converter with optimized number of switches and capacitors for renewable energy integration,” *IEEE Trans. Energy Convers.*, vol. 31, no. 3, pp. 846–859, Sep. 2016.
- [12] E.Babaei and S.H.Hosseini, “New cascaded multilevel inverter topology with minimum of switches,” *Energy Convers. Manage.*, vol. 50, no. 4, pp. 2761–2767, 2009.
- [13] D. N. R. S. Alishah and S. H. Hosseini, “Novel topologies for symmetric, asymmetric, and cascade switched-diode multilevel converter with minimum number of power electronic components,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5300–5310, Oct. 2014.
- [14] B. P. McGrath and D. G. Holmes, “Multicarrier PWM strategies for multilevel inverters,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.