CSCE 312 – Lab 4 Individual Report

Texas A&M University

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Poyi Ou

Group 26 – Logic Wizard

Members:
Poyi Ou
Evan Ethington
Oscar Tsai

Part Designed Individually

I was responsible for designing the InputModule and OutputModule for Problem 1, the 1-bit Full Adder, 8-bit Full Adder, and 8-bit Subtractor for Problem 2, as well as the finite state machine for Problem 3.

Advantage Obtained

After completing this lab, I gained a deeper understanding of each component's functionality and learned how to apply them to real-world scenarios.

Disadvantage Observed

There is not much of a disadvantage within this lab, I enjoyed it and learned a lot from it.

Difficulties Encountered

The most challenging aspect of this lab was interpreting the functionality of each component in this microcontroller and figuring out how to utilize various controllers and logic to achieve the desired results.

Most Significant Design

I would say Evan's CPU design was the most impressive among all of us. He accurately utilized each component, understanding their intended functions, and ensured an efficient overall design. Evan also provided assistance to me and Oscar in our respective parts, guiding us through the logic of each component to achieve the desired outcomes.