

CSCE 312 – Lab 6 Individual Report

Texas A&M University

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Poyi Ou

Group 26 – Logic Wizard

Members:

Poyi Ou

Evan Ethington

Oscar Tsai

Part Designed Individually

I was responsible for designing the Split and Align and their subcircuits for the Fetch module, as well as the entire Execution Module and the assembly code for checking Palindrome.

Advantage Obtained

After completing this lab, I gained a deeper understanding of each module's functionality and how each module works together to create our Y86 RISC CPU.

Disadvantage Observed

There is not much of a disadvantage within this lab, I enjoyed it and learned a lot from it.

Difficulties Encountered

The most challenging aspect of this lab was designing different components separately and ensuring that the data passed in matches the required result needed. Additionally, figuring out how to utilize various controllers and designing respective assembly code to achieve the desired results presented another challenge.

Most Significant Design

I would say Evan's Clock timing module design was really impressive. He went through the thinking process of determining how many clock cycles each module needs to compute their respective values, and combined all of them to generate a working CPU. However, Oscar's design on the memory state is also quite impressive. He correctly handled every piece of data and stored them in the correct memory location, making the process of reading and updating memory data more convenient.