ECEN 714 LAB 7

Name: Bidhan Poudel
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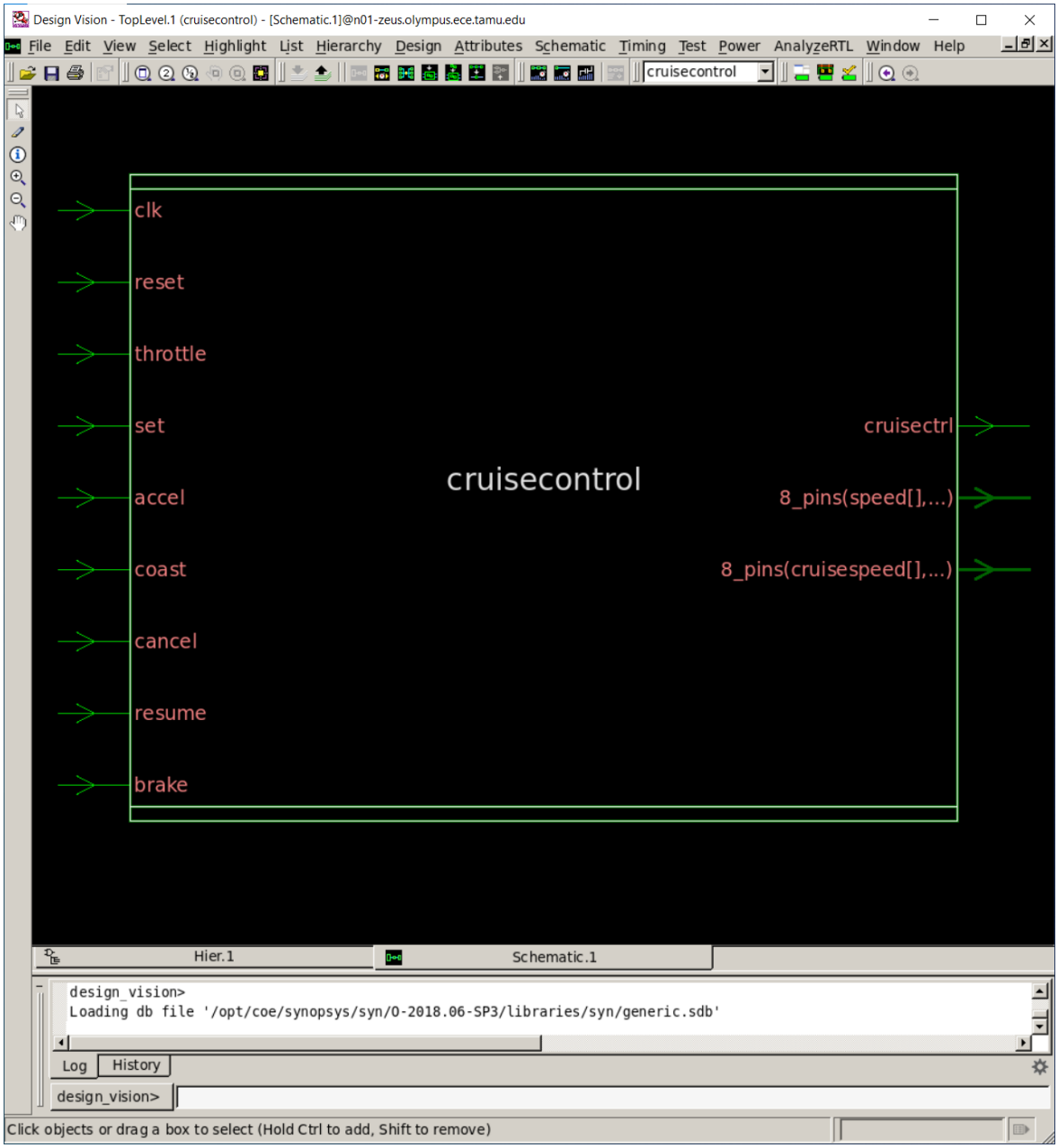
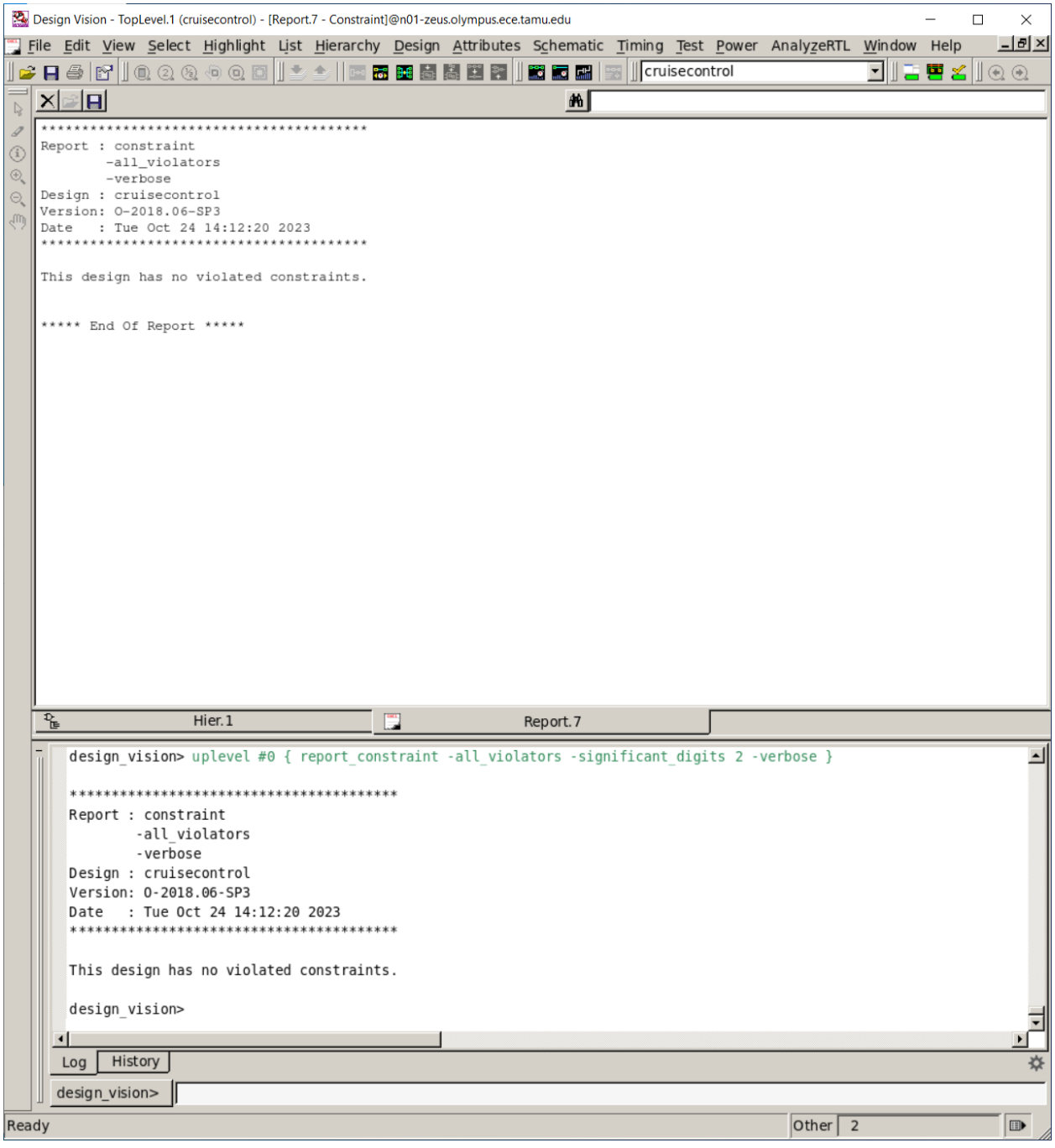
Lab section: 507/607 Tuesday 19:00
TA: Shejuti Shehreen

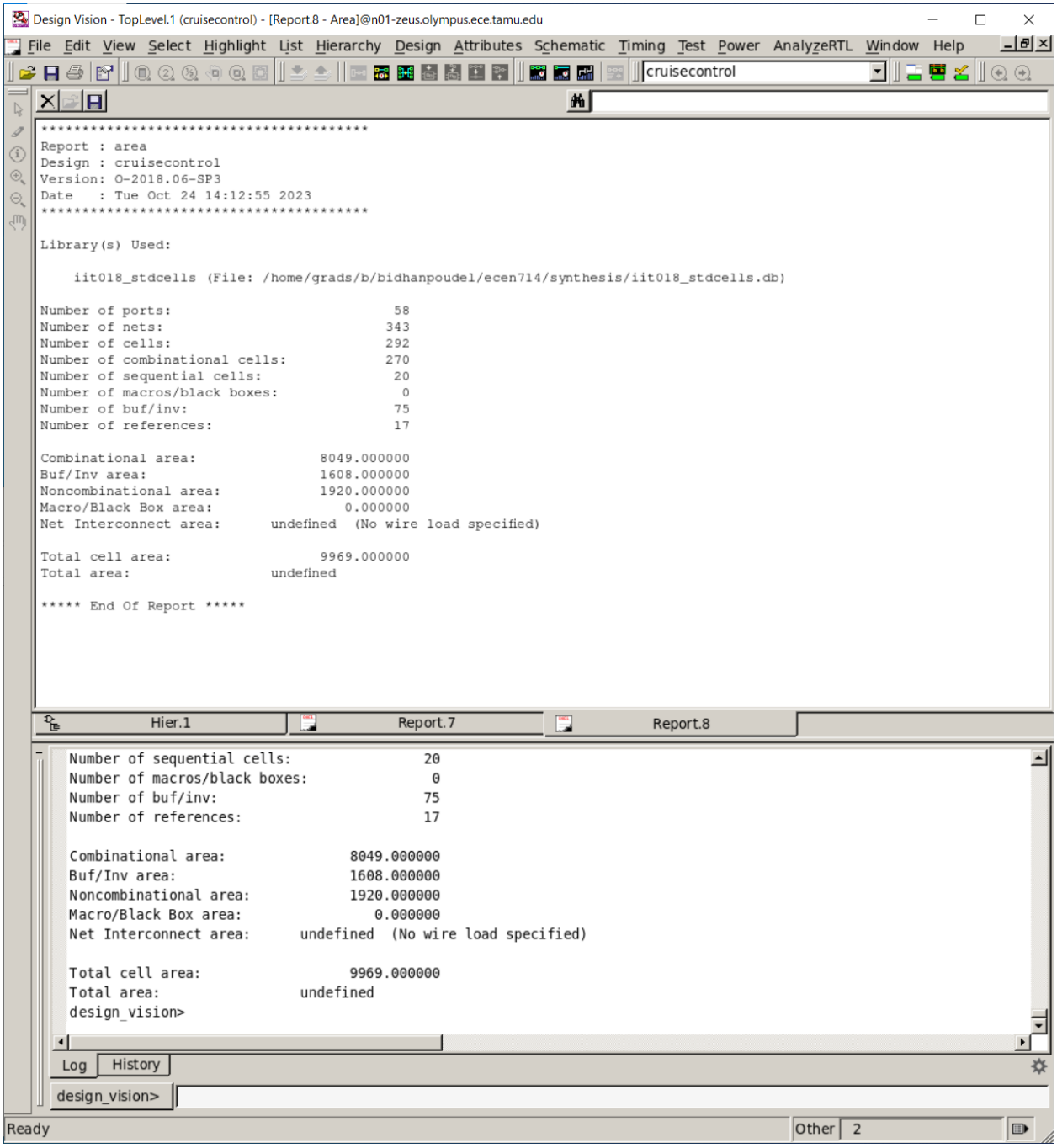
Part A: Logic Synthesis
Design Vision Symbol



Constraint Report



Area report:


Design Vision - TopLevel.1 (cruisecontrol) - [Report.8 - Area]@n01-zeus.olympus.ece.tamu.edu
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
cruisecontrol
****
Report : area
Design : cruisecontrol
Version: O-2018.06-SP3
Date : Tue Oct 24 14:12:55 2023
****
Library(s) Used:
iit018_stdcells (File: /home/grads/b/bidhanpoudel/ecen714/synthesis/iit018_stdcells.db)
Number of ports: 58
Number of nets: 343
Number of cells: 292
Number of combinational cells: 270
Number of sequential cells: 20
Number of macros/black boxes: 0
Number of buf/inv: 75
Number of references: 17
Combinational area: 8049.000000
Buf/Inv area: 1608.000000
Noncombinational area: 1920.000000
Macro/Black Box area: 0.000000
Net Interconnect area: undefined (No wire load specified)
Total cell area: 9969.000000
Total area: undefined
***** End Of Report *****
Hier.1
Report.7
Report.8
Number of sequential cells: 20
Number of macros/black boxes: 0
Number of buf/inv: 75
Number of references: 17
Combinational area: 8049.000000
Buf/Inv area: 1608.000000
Noncombinational area: 1920.000000
Macro/Black Box area: 0.000000
Net Interconnect area: undefined (No wire load specified)
Total cell area: 9969.000000
Total area: undefined
design_vision>
Log
History
design_vision>
Ready
Other
2

Verilog Netlist

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////////////////////////////////////////////////////////////
// Created by: Synopsys DC Expert(TM) in wire load mode
// Version   : O-2018.06-SP3
// Date      : Tue Oct 24 14:15:44 2023
////////////////////////////////////////////////////////////


module cruisecontrol_DW01_inc_4 ( A, SUM );
  input [7:0] A;
  output [7:0] SUM;

  wire   [7:2] carry;

  HAX1 U1_1_6 ( .A(A[6]), .B(carry[6]), .YC(carry[7]), .YS(SUM[6]) );
  HAX1 U1_1_5 ( .A(A[5]), .B(carry[5]), .YC(carry[6]), .YS(SUM[5]) );
  HAX1 U1_1_4 ( .A(A[4]), .B(carry[4]), .YC(carry[5]), .YS(SUM[4]) );
  HAX1 U1_1_3 ( .A(A[3]), .B(carry[3]), .YC(carry[4]), .YS(SUM[3]) );
  HAX1 U1_1_2 ( .A(A[2]), .B(carry[2]), .YC(carry[3]), .YS(SUM[2]) );
  HAX1 U1_1_1 ( .A(A[1]), .B(A[0]), .YC(carry[2]), .YS(SUM[1]) );
  XOR2X1 U2 ( .A(carry[7]), .B(A[7]), .Y(SUM[7]) );
  INVX1 U1 ( .A(A[0]), .Y(SUM[0]) );
endmodule


module cruisecontrol_DW01_inc_5 ( A, SUM );
  input [7:0] A;
  output [7:0] SUM;

  wire   [7:2] carry;

  HAX1 U1_1_6 ( .A(A[6]), .B(carry[6]), .YC(carry[7]), .YS(SUM[6]) );
  HAX1 U1_1_5 ( .A(A[5]), .B(carry[5]), .YC(carry[6]), .YS(SUM[5]) );
  HAX1 U1_1_4 ( .A(A[4]), .B(carry[4]), .YC(carry[5]), .YS(SUM[4]) );
  HAX1 U1_1_3 ( .A(A[3]), .B(carry[3]), .YC(carry[4]), .YS(SUM[3]) );
  HAX1 U1_1_2 ( .A(A[2]), .B(carry[2]), .YC(carry[3]), .YS(SUM[2]) );
  HAX1 U1_1_1 ( .A(A[1]), .B(A[0]), .YC(carry[2]), .YS(SUM[1]) );
  XOR2X1 U2 ( .A(carry[7]), .B(A[7]), .Y(SUM[7]) );
  INVX2 U1 ( .A(A[0]), .Y(SUM[0]) );
endmodule
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module cruisecontrol ( clk, reset, throttle, set, accel, coast, cancel,
resume,
        brake, speed, cruisespeed, cruisectrl );
  output [7:0] speed;
  output [7:0] cruisespeed;
  input clk, reset, throttle, set, accel, coast, cancel, resume, brake;
  output cruisectrl;
  wire   n300, n301, n302, n303, n304, n305, n306, n307, n308, n309, n310,
         n311, n312, n313, n314, n315, N128, N146, N147, N148, N149, N150,
         N151, N152, N153, n2, n3, n4, n5, n6, n7, n8, n9, n160, n161,
n162,
         n163, n164, n165, n166, n167, n168, n169, n171, n172, n173, n174,
         n175, n176, n177, n178, n179, n370, n371, n372, n373, n374, n375,
         n376, n377, n378, n379, n380, n381, n382, n383, n384, n385, n386,
         n387, n388, n389, n390, n391, n392, n393, n394, n395, n396, n397,
         n398, n399, n400, n401, n402, n403, n404, n405, n406, n407, n408,
         n409, n410, n411, n412, n413, n414, n415, n416, n417, n418, n419,
         n420, n421, n422, n423, n424, n425, n426, n427, n428, n429, n430,
         n431, n432, n433, n434, n435, n436, n437, n438, n439, n440, n441,
         n442, n443, n444, n445, n446, n447, n448, n449, n450, n451, n452,
         n453, n454, n455, n456, n457, n458, n459, n460, n461, n462, n463,
         n464, n465, n466, n467, n468, n469, n470, n471, n472, n473, n474,
         n475, n476, n477, n478, n479, n480, n481, n482, n483, n484, n485,
         n486, n487, n488, n489, n490, n491, n492, n493, n494, n495, n496,
         n497, n498, n499, n500, n501, n502, n503, n504, n505, n506, n507,
         n508, n509, n510, n511, n512, n513, n514, n515, n516, n517, n518,
         n519, n520, n521, n522, n523, n524, n525, n526, n527, n528, n529,
         n530, n531, n535, n540, n548, n550, n552, n554, n555, n556, n557,
         n558, n559, n560, n561, n562, n563, n564, n565, n566, n567, n568,
         n569, n570, n571, n572, n573, n574, n575, n576, n577, n578, n579,
         n580, n581, n582, n583, n584, n585, n586, n587, n588, n589, n590,
         n591, n592, n593, n594, n595, n596, n597, n598, n599, n600, n601,
         n602, n603, n604;
  wire   [2:0] state;

  DFFPOSX1 \cruisespeed_reg[0]  ( .D(n179), .CLK(clk), .Q(n314) );
  DFFPOSX1 \cruisespeed_reg[7]  ( .D(n178), .CLK(clk), .Q(n307) );
  DFFPOSX1 \cruisespeed_reg[6]  ( .D(n177), .CLK(clk), .Q(n308) );
  DFFPOSX1 \speed_reg[0]  ( .D(n176), .CLK(clk), .Q(N128) );
  DFFPOSX1 \state_reg[0]  ( .D(n175), .CLK(clk), .Q(state[0]) );
  DFFPOSX1 \speed_reg[1]  ( .D(n174), .CLK(clk), .Q(n306) );
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  DFFPOSX1 \speed_reg[7]  ( .D(n173), .CLK(clk), .Q(n300) );
  DFFPOSX1 \speed_reg[6]  ( .D(n172), .CLK(clk), .Q(n301) );
  DFFPOSX1 \speed_reg[5]  ( .D(n171), .CLK(clk), .Q(n302) );
  DFFPOSX1 \state_reg[1]  ( .D(n531), .CLK(clk), .Q(state[1]) );
  DFFPOSX1 \state_reg[2]  ( .D(n169), .CLK(clk), .Q(state[2]) );
  DFFPOSX1 \speed_reg[4]  ( .D(n168), .CLK(clk), .Q(n303) );
  DFFPOSX1 \speed_reg[3]  ( .D(n167), .CLK(clk), .Q(n304) );
  DFFPOSX1 \speed_reg[2]  ( .D(n166), .CLK(clk), .Q(n305) );
  DFFPOSX1 \cruisespeed_reg[4]  ( .D(n165), .CLK(clk), .Q(n310) );
  DFFPOSX1 \cruisespeed_reg[3]  ( .D(n164), .CLK(clk), .Q(n311) );
  DFFPOSX1 \cruisespeed_reg[2]  ( .D(n163), .CLK(clk), .Q(n312) );
  DFFPOSX1 cruisectrl_reg ( .D(n162), .CLK(clk), .Q(n315) );
  DFFPOSX1 \cruisespeed_reg[5]  ( .D(n161), .CLK(clk), .Q(n309) );
  DFFPOSX1 \cruisespeed_reg[1]  ( .D(n160), .CLK(clk), .Q(n313) );
  OR2X2 U168 ( .A(n472), .B(n473), .Y(n470) );
  OR2X2 U169 ( .A(resume), .B(state[1]), .Y(n463) );
  OR2X2 U170 ( .A(n602), .B(n485), .Y(n444) );
  AOI21X1 U225 ( .A(n370), .B(n371), .C(reset), .Y(n531) );
  NOR2X1 U226 ( .A(n372), .B(n581), .Y(n371) );
  AOI22X1 U227 ( .A(n373), .B(set), .C(n374), .D(n602), .Y(n370) );
  AND2X1 U228 ( .A(n375), .B(n579), .Y(n373) );
  NAND2X1 U229 ( .A(n376), .B(n377), .Y(n179) );
  AOI22X1 U230 ( .A(n576), .B(n568), .C(N146), .D(n580), .Y(n377) );
  AOI22X1 U231 ( .A(speed[0]), .B(n578), .C(n314), .D(n378), .Y(n376) );
  NAND2X1 U232 ( .A(n379), .B(n380), .Y(n178) );
  AOI22X1 U233 ( .A(n381), .B(n556), .C(cruisespeed[7]), .D(n382), .Y(n380)
);
  OAI21X1 U234 ( .A(n383), .B(n569), .C(n384), .Y(n382) );
  NOR2X1 U235 ( .A(n308), .B(cruisespeed[7]), .Y(n381) );
  AOI22X1 U236 ( .A(N153), .B(n580), .C(n300), .D(n578), .Y(n379) );
  NAND2X1 U237 ( .A(n385), .B(n555), .Y(n177) );
  OAI22X1 U238 ( .A(n387), .B(n308), .C(n569), .D(n384), .Y(n386) );
  AOI21X1 U239 ( .A(n576), .B(n309), .C(n388), .Y(n384) );
  AOI22X1 U240 ( .A(N152), .B(n580), .C(n301), .D(n578), .Y(n385) );
  OAI21X1 U241 ( .A(N128), .B(n560), .C(n389), .Y(n176) );
  AOI22X1 U242 ( .A(speed[0]), .B(n390), .C(n9), .D(n391), .Y(n389) );
  NAND2X1 U243 ( .A(n392), .B(n393), .Y(n390) );
  AOI21X1 U244 ( .A(n394), .B(n395), .C(reset), .Y(n175) );
  OAI21X1 U245 ( .A(state[0]), .B(n396), .C(n397), .Y(n395) );
  OAI21X1 U246 ( .A(brake), .B(n398), .C(n572), .Y(n397) );
  NAND2X1 U247 ( .A(n593), .B(n602), .Y(n396) );
  OAI21X1 U248 ( .A(n399), .B(n584), .C(n400), .Y(n174) );
  AOI22X1 U249 ( .A(n401), .B(n584), .C(n8), .D(n391), .Y(n400) );
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OAI21X1 U250 ( .A(speed[0]), .B(n560), .C(n393), .Y(n401) );
OAI22X1 U251 ( .A(n588), .B(n392), .C(n402), .D(n561), .Y(n173) );
AOI21X1 U252 ( .A(n2), .B(n403), .C(n404), .Y(n402) );
OAI21X1 U253 ( .A(n405), .B(n588), .C(n406), .Y(n404) );
NAND3X1 U254 ( .A(n588), .B(n589), .C(n567), .Y(n406) );
AOI21X1 U255 ( .A(n408), .B(n409), .C(n410), .Y(n405) );
OAI21X1 U256 ( .A(n411), .B(n566), .C(n412), .Y(n410) );
OAI21X1 U257 ( .A(n409), .B(n413), .C(n301), .Y(n412) );
OAI21X1 U258 ( .A(n414), .B(n589), .C(n415), .Y(n172) );
AOI22X1 U259 ( .A(n416), .B(n417), .C(n3), .D(n391), .Y(n415) );
NOR2X1 U260 ( .A(n301), .B(n407), .Y(n416) );
AOI21X1 U261 ( .A(n562), .B(n408), .C(n418), .Y(n414) );
OAI21X1 U262 ( .A(n411), .B(n560), .C(n392), .Y(n418) );
OAI21X1 U263 ( .A(n407), .B(n561), .C(n419), .Y(n171) );
AOI22X1 U264 ( .A(n4), .B(n391), .C(n302), .D(n420), .Y(n419) );
NAND2X1 U265 ( .A(n421), .B(n422), .Y(n420) );
AOI22X1 U266 ( .A(n562), .B(speed[4]), .C(n423), .D(n424), .Y(n421) );
AOI22X1 U267 ( .A(n409), .B(n586), .C(n413), .D(n411), .Y(n407) );
NAND3X1 U268 ( .A(n590), .B(n550), .C(n425), .Y(n408) );
AND2X1 U269 ( .A(n426), .B(n601), .Y(n169) );
OAI21X1 U270 ( .A(state[1]), .B(n592), .C(n583), .Y(n426) );
NAND2X1 U271 ( .A(n427), .B(n428), .Y(n168) );
AOI22X1 U272 ( .A(n429), .B(n562), .C(n303), .D(n430), .Y(n428) );
OAI21X1 U273 ( .A(n431), .B(n560), .C(n422), .Y(n430) );
AOI21X1 U274 ( .A(n585), .B(n562), .C(n563), .Y(n422) );
NOR2X1 U275 ( .A(n303), .B(n585), .Y(n429) );
AOI22X1 U276 ( .A(n5), .B(n391), .C(n423), .D(n570), .Y(n427) );
NAND2X1 U277 ( .A(n432), .B(n433), .Y(n167) );
AOI22X1 U278 ( .A(n6), .B(n391), .C(n304), .D(n434), .Y(n433) );
OAI21X1 U279 ( .A(n435), .B(n560), .C(n436), .Y(n434) );
AOI21X1 U280 ( .A(n562), .B(n587), .C(n563), .Y(n436) );
AOI22X1 U281 ( .A(n423), .B(n431), .C(n562), .D(n425), .Y(n432) );
NOR2X1 U282 ( .A(n587), .B(n304), .Y(n425) );
NAND2X1 U283 ( .A(n437), .B(n438), .Y(n166) );
AOI21X1 U284 ( .A(n7), .B(n391), .C(n439), .Y(n438) );
AOI21X1 U285 ( .A(n399), .B(n440), .C(n595), .Y(n439) );
OAI21X1 U286 ( .A(n562), .B(n423), .C(n306), .Y(n440) );
AOI21X1 U287 ( .A(speed[0]), .B(n423), .C(n563), .Y(n399) );
AND2X1 U288 ( .A(n417), .B(n403), .Y(n391) );
OAI21X1 U289 ( .A(n565), .B(n441), .C(n572), .Y(n403) );
NAND3X1 U290 ( .A(n443), .B(n444), .C(n445), .Y(n442) );
AOI22X1 U291 ( .A(accel), .B(n581), .C(throttle), .D(n579), .Y(n445) );
NAND3X1 U292 ( .A(n574), .B(n591), .C(n592), .Y(n443) );
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NAND2X1 U293 ( .A(n447), .B(n603), .Y(n441) );
AOI22X1 U294 ( .A(n562), .B(n449), .C(n423), .D(n435), .Y(n437) );
NOR2X1 U295 ( .A(n561), .B(n566), .Y(n423) );
NAND3X1 U296 ( .A(n450), .B(n394), .C(n451), .Y(n413) );
AOI22X1 U297 ( .A(n447), .B(n452), .C(n374), .D(n602), .Y(n451) );
NAND2X1 U298 ( .A(state[0]), .B(n453), .Y(n394) );
NAND3X1 U299 ( .A(n582), .B(n604), .C(cancel), .Y(n450) );
NAND2X1 U300 ( .A(n417), .B(n409), .Y(n393) );
OAI21X1 U301 ( .A(n398), .B(n604), .C(n454), .Y(n409) );
NOR2X1 U302 ( .A(n563), .B(reset), .Y(n417) );
NAND3X1 U303 ( .A(n455), .B(n456), .C(n457), .Y(n392) );
NOR2X1 U304 ( .A(n458), .B(n459), .Y(n457) );
NAND2X1 U305 ( .A(n573), .B(n460), .Y(n459) );
OAI21X1 U306 ( .A(n591), .B(n461), .C(n462), .Y(n374) );
NAND2X1 U307 ( .A(n574), .B(n593), .Y(n461) );
OAI21X1 U308 ( .A(n463), .B(n464), .C(n465), .Y(n458) );
OAI21X1 U309 ( .A(n452), .B(n466), .C(n582), .Y(n465) );
OAI21X1 U310 ( .A(throttle), .B(n448), .C(n603), .Y(n452) );
AOI21X1 U311 ( .A(n467), .B(n468), .C(n469), .Y(n448) );
OAI22X1 U312 ( .A(n470), .B(n471), .C(n589), .D(n308), .Y(n468) );
AOI21X1 U313 ( .A(speed[4]), .B(n596), .C(n474), .Y(n473) );
OAI22X1 U314 ( .A(n309), .B(n590), .C(n475), .D(n476), .Y(n474) );
OAI21X1 U315 ( .A(speed[3]), .B(n597), .C(n477), .Y(n476) );
OAI21X1 U316 ( .A(n312), .B(n595), .C(n478), .Y(n477) );
AOI22X1 U317 ( .A(n479), .B(n480), .C(speed[3]), .D(n597), .Y(n478) );
OAI21X1 U318 ( .A(n552), .B(n481), .C(n482), .Y(n480) );
NAND2X1 U319 ( .A(n483), .B(n568), .Y(n481) );
OAI21X1 U320 ( .A(n571), .B(n484), .C(state[0]), .Y(n464) );
NAND2X1 U321 ( .A(n588), .B(n589), .Y(n484) );
NOR2X1 U322 ( .A(n424), .B(n302), .Y(n411) );
NAND2X1 U323 ( .A(n431), .B(n550), .Y(n424) );
AND2X1 U324 ( .A(n435), .B(n548), .Y(n431) );
NOR2X1 U325 ( .A(n587), .B(speed[0]), .Y(n435) );
NOR2X1 U326 ( .A(n306), .B(n305), .Y(n449) );
AND2X1 U327 ( .A(n444), .B(n454), .Y(n456) );
NAND3X1 U328 ( .A(n574), .B(n591), .C(n446), .Y(n454) );
NOR2X1 U329 ( .A(n593), .B(resume), .Y(n446) );
AOI22X1 U330 ( .A(n593), .B(n574), .C(n603), .D(n447), .Y(n485) );
AOI21X1 U331 ( .A(n486), .B(n453), .C(n487), .Y(n455) );
AND2X1 U332 ( .A(n574), .B(n466), .Y(n486) );
OAI21X1 U333 ( .A(n469), .B(n488), .C(n467), .Y(n466) );
NAND2X1 U334 ( .A(cruisespeed[7]), .B(n588), .Y(n467) );
AOI21X1 U335 ( .A(n308), .B(n589), .C(n489), .Y(n488) );
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NOR2X1 U336 ( .A(n471), .B(n490), .Y(n489) );
OAI21X1 U337 ( .A(n309), .B(n590), .C(n491), .Y(n490) );
OAI21X1 U338 ( .A(speed[4]), .B(n596), .C(n492), .Y(n491) );
AOI21X1 U339 ( .A(n594), .B(n493), .C(n472), .Y(n492) );
NOR2X1 U340 ( .A(n599), .B(n302), .Y(n472) );
OAI21X1 U341 ( .A(speed[3]), .B(n564), .C(n494), .Y(n493) );
OAI21X1 U342 ( .A(n548), .B(n495), .C(n311), .Y(n494) );
OAI21X1 U343 ( .A(n305), .B(n598), .C(n496), .Y(n495) );
NAND2X1 U344 ( .A(n479), .B(n497), .Y(n496) );
OAI21X1 U345 ( .A(n568), .B(n498), .C(n483), .Y(n497) );
NAND2X1 U346 ( .A(n313), .B(n584), .Y(n483) );
NAND2X1 U347 ( .A(n482), .B(n552), .Y(n498) );
NAND2X1 U348 ( .A(n306), .B(n600), .Y(n482) );
XNOR2X1 U349 ( .A(n312), .B(n305), .Y(n479) );
XNOR2X1 U350 ( .A(n310), .B(n550), .Y(n475) );
XOR2X1 U351 ( .A(n308), .B(n301), .Y(n471) );
NOR2X1 U352 ( .A(n588), .B(cruisespeed[7]), .Y(n469) );
NAND2X1 U353 ( .A(n499), .B(n500), .Y(n165) );
AOI22X1 U354 ( .A(n310), .B(n501), .C(n557), .D(n576), .Y(n500) );
OAI21X1 U355 ( .A(n383), .B(n597), .C(n558), .Y(n501) );
AOI22X1 U356 ( .A(N150), .B(n580), .C(n303), .D(n578), .Y(n499) );
NAND2X1 U357 ( .A(n503), .B(n504), .Y(n164) );
AOI22X1 U358 ( .A(n505), .B(n559), .C(n311), .D(n502), .Y(n504) );
OAI21X1 U359 ( .A(n559), .B(n383), .C(n577), .Y(n502) );
NOR2X1 U360 ( .A(n311), .B(n383), .Y(n505) );
AOI22X1 U361 ( .A(N149), .B(n580), .C(n578), .D(n304), .Y(n503) );
NAND2X1 U362 ( .A(n506), .B(n507), .Y(n163) );
AOI22X1 U363 ( .A(n312), .B(n508), .C(n559), .D(n576), .Y(n507) );
OAI21X1 U364 ( .A(n383), .B(n600), .C(n554), .Y(n508) );
AOI22X1 U365 ( .A(N148), .B(n580), .C(n578), .D(n305), .Y(n506) );
AND2X1 U366 ( .A(n510), .B(n601), .Y(n162) );
OAI21X1 U367 ( .A(state[1]), .B(n575), .C(n511), .Y(n510) );
AOI21X1 U368 ( .A(cruisectrl), .B(n583), .C(n372), .Y(n511) );
AND2X1 U369 ( .A(resume), .B(n453), .Y(n372) );
NOR2X1 U370 ( .A(n593), .B(state[1]), .Y(n453) );
NAND2X1 U371 ( .A(n513), .B(n514), .Y(n161) );
AOI21X1 U372 ( .A(n309), .B(n388), .C(n556), .Y(n514) );
NAND3X1 U373 ( .A(n576), .B(n599), .C(n557), .Y(n387) );
OAI21X1 U374 ( .A(n557), .B(n383), .C(n577), .Y(n388) );
NAND3X1 U375 ( .A(n596), .B(n597), .C(n559), .Y(n515) );
NAND3X1 U376 ( .A(n600), .B(n568), .C(n598), .Y(n516) );
AOI22X1 U377 ( .A(N151), .B(n580), .C(n578), .D(n302), .Y(n513) );
NAND2X1 U378 ( .A(n517), .B(n518), .Y(n160) );
```

```
  AOI22X1 U379 ( .A(n519), .B(n576), .C(n313), .D(n509), .Y(n518) );
  OAI21X1 U380 ( .A(n383), .B(n568), .C(n577), .Y(n509) );
  NAND3X1 U381 ( .A(n577), .B(n601), .C(n447), .Y(n383) );
  NOR2X1 U382 ( .A(n520), .B(accel), .Y(n447) );
  NOR2X1 U383 ( .A(n314), .B(n313), .Y(n519) );
  AOI22X1 U384 ( .A(N147), .B(n580), .C(n578), .D(n306), .Y(n517) );
  OAI21X1 U385 ( .A(n487), .B(n579), .C(n522), .Y(n521) );
  NOR2X1 U386 ( .A(reset), .B(n378), .Y(n522) );
  NOR2X1 U387 ( .A(n512), .B(n523), .Y(n378) );
  OAI21X1 U388 ( .A(n398), .B(n603), .C(n460), .Y(n523) );
  AOI21X1 U389 ( .A(n582), .B(accel), .C(reset), .Y(n460) );
  OAI21X1 U390 ( .A(n524), .B(n525), .C(n583), .Y(n512) );
  NAND2X1 U391 ( .A(throttle), .B(set), .Y(n525) );
  NAND2X1 U392 ( .A(n579), .B(n375), .Y(n524) );
  OAI21X1 U393 ( .A(n526), .B(n590), .C(n527), .Y(n375) );
  NOR2X1 U394 ( .A(n301), .B(n300), .Y(n527) );
  AOI21X1 U395 ( .A(n528), .B(n306), .C(speed[4]), .Y(n526) );
  NOR2X1 U396 ( .A(n548), .B(n595), .Y(n528) );
  NAND3X1 U397 ( .A(n591), .B(n593), .C(state[0]), .Y(n462) );
  NOR2X1 U398 ( .A(n398), .B(n529), .Y(n487) );
  NAND3X1 U399 ( .A(n581), .B(n601), .C(accel), .Y(n530) );
  NAND2X1 U400 ( .A(n529), .B(n582), .Y(n520) );
  NAND3X1 U401 ( .A(state[0]), .B(n593), .C(state[1]), .Y(n398) );
  NOR2X1 U402 ( .A(brake), .B(cancel), .Y(n529) );
  cruisecontrol_DW01_inc_4 add_118 ( .A({cruisespeed[7], n308, n309, n310,
        n311, n312, n313, n314}), .SUM({N153, N152, N151, N150, N149, N148,
        N147, N146}) );
  cruisecontrol_DW01_inc_5 r118 ( .A({n300, n301, n302, speed[4:3], n305,
n306,
        speed[0]}), .SUM({n2, n3, n4, n5, n6, n7, n8, n9}) );
  INVX8 U403 ( .A(n588), .Y(speed[7]) );
  INVX1 U404 ( .A(n300), .Y(n588) );
  INVX8 U405 ( .A(n600), .Y(cruisespeed[1]) );
  INVX1 U406 ( .A(n313), .Y(n600) );
  INVX8 U407 ( .A(n568), .Y(cruisespeed[0]) );
  INVX1 U408 ( .A(n314), .Y(n568) );
  INVX2 U409 ( .A(n307), .Y(n535) );
  INVX8 U410 ( .A(n535), .Y(cruisespeed[7]) );
  INVX8 U411 ( .A(n599), .Y(cruisespeed[5]) );
  INVX1 U412 ( .A(n309), .Y(n599) );
  INVX8 U413 ( .A(n595), .Y(speed[2]) );
  INVX1 U414 ( .A(n305), .Y(n595) );
  INVX8 U415 ( .A(n589), .Y(speed[6]) );
```

```
INVX1 U416 ( .A(n301), .Y(n589) );
INVX2 U417 ( .A(n315), .Y(n540) );
INVX8 U418 ( .A(n540), .Y(cruisectrl) );
INVX8 U419 ( .A(n596), .Y(cruisespeed[4]) );
INVX1 U420 ( .A(n310), .Y(n596) );
INVX8 U421 ( .A(n597), .Y(cruisespeed[3]) );
INVX1 U422 ( .A(n311), .Y(n597) );
INVX8 U423 ( .A(n598), .Y(cruisespeed[2]) );
INVX1 U424 ( .A(n312), .Y(n598) );
INVX8 U425 ( .A(n590), .Y(speed[5]) );
INVX1 U426 ( .A(n302), .Y(n590) );
INVX8 U427 ( .A(n584), .Y(speed[1]) );
INVX1 U428 ( .A(n306), .Y(n584) );
INVX8 U429 ( .A(n569), .Y(cruisespeed[6]) );
INVX1 U430 ( .A(n308), .Y(n569) );
INVX2 U431 ( .A(n304), .Y(n548) );
INVX2 U432 ( .A(n303), .Y(n550) );
INVX2 U433 ( .A(N128), .Y(n552) );
INVX8 U434 ( .A(n548), .Y(speed[3]) );
INVX8 U435 ( .A(n550), .Y(speed[4]) );
INVX8 U436 ( .A(n552), .Y(speed[0]) );
INVX2 U437 ( .A(n509), .Y(n554) );
INVX2 U438 ( .A(n386), .Y(n555) );
INVX2 U439 ( .A(n387), .Y(n556) );
INVX2 U440 ( .A(n515), .Y(n557) );
INVX2 U441 ( .A(n502), .Y(n558) );
INVX2 U442 ( .A(n516), .Y(n559) );
INVX2 U443 ( .A(n423), .Y(n560) );
INVX2 U444 ( .A(n417), .Y(n561) );
INVX2 U445 ( .A(n393), .Y(n562) );
INVX2 U446 ( .A(n392), .Y(n563) );
INVX2 U447 ( .A(n495), .Y(n564) );
INVX2 U448 ( .A(n448), .Y(n565) );
INVX2 U449 ( .A(n413), .Y(n566) );
INVX2 U450 ( .A(n407), .Y(n567) );
INVX2 U451 ( .A(n424), .Y(n570) );
INVX2 U452 ( .A(n411), .Y(n571) );
INVX2 U453 ( .A(n442), .Y(n572) );
INVX2 U454 ( .A(n374), .Y(n573) );
INVX2 U455 ( .A(state[0]), .Y(n574) );
INVX2 U456 ( .A(n512), .Y(n575) );
INVX2 U457 ( .A(n383), .Y(n576) );
INVX2 U458 ( .A(n378), .Y(n577) );
```

```
  INVX2 U459 ( .A(n521), .Y(n578) );
  INVX2 U460 ( .A(n462), .Y(n579) );
  INVX2 U461 ( .A(n530), .Y(n580) );
  INVX2 U462 ( .A(n520), .Y(n581) );
  INVX2 U463 ( .A(n398), .Y(n582) );
  INVX2 U464 ( .A(n487), .Y(n583) );
  INVX2 U465 ( .A(n425), .Y(n585) );
  INVX2 U466 ( .A(n408), .Y(n586) );
  INVX2 U467 ( .A(n449), .Y(n587) );
  INVX2 U468 ( .A(state[1]), .Y(n591) );
  INVX2 U469 ( .A(n446), .Y(n592) );
  INVX2 U470 ( .A(state[2]), .Y(n593) );
  INVX2 U471 ( .A(n475), .Y(n594) );
  INVX2 U472 ( .A(reset), .Y(n601) );
  INVX2 U473 ( .A(throttle), .Y(n602) );
  INVX2 U474 ( .A(coast), .Y(n603) );
  INVX2 U475 ( .A(brake), .Y(n604) );
endmodule
```

Number of registers = 20

Part B: Static Time Analysis

Max_paths_txt

```
****************************************
Report : timing
      -path_type full
      -delay_type max
      -slack_lesser_than 5.00
      -max_paths 3
      -sort_by slack
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Tue Oct 24 14:53:12 2023
****************************************


  Startpoint: cruisespeed_reg[6]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed[6]
              (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                   Incr       Path

-------------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  cruisespeed_reg[6]/CLK (DFFPOSX1)                       0.00       0.00 r
  cruisespeed_reg[6]/Q (DFFPOSX1)                         0.18       0.18 r
  U176/Y (INVX1)                                          0.27       0.44 f
  U175/Y (INVX8)                                          0.77       1.21 r
  cruisespeed[6] (out)                                    0.00       1.21 r
  data arrival time                                                  1.21

  clock clk (rise edge)                                  10.00      10.00
  clock network delay (ideal)                             0.00      10.00
  clock reconvergence pessimism                           0.00      10.00
  output external delay                                  -5.00       5.00
  data required time                                                 5.00
```

```
--------------------------------------------------------------------------
---
  data required time                                                 5.00
  data arrival time                                                 -1.21

--------------------------------------------------------------------------
---
  slack (MET)                                                        3.79


  Startpoint: cruisespeed_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed[0]
              (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                   Incr       Path

--------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  cruisespeed_reg[0]/CLK (DFFPOSX1)                       0.00       0.00 r
  cruisespeed_reg[0]/Q (DFFPOSX1)                         0.14       0.14 r
  U184/Y (INVX1)                                          0.26       0.40 f
  U183/Y (INVX8)                                          0.77       1.17 r
  cruisespeed[0] (out)                                    0.00       1.17 r
  data arrival time                                                  1.17

  clock clk (rise edge)                                  10.00      10.00
  clock network delay (ideal)                             0.00      10.00
  clock reconvergence pessimism                           0.00      10.00
  output external delay                                  -5.00       5.00
  data required time                                                 5.00

--------------------------------------------------------------------------
---
  data required time                                                 5.00
  data arrival time                                                 -1.17

--------------------------------------------------------------------------
---
```

```
  slack (MET)                                                     3.83


  Startpoint: cruisespeed_reg[5]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed[5]
              (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                  Incr       Path

-----------------------------------------------------------------------------
---
  clock clk (rise edge)                                  0.00       0.00
  clock network delay (ideal)                            0.00       0.00
  cruisespeed_reg[5]/CLK (DFFPOSX1)                      0.00       0.00 r
  cruisespeed_reg[5]/Q (DFFPOSX1)                        0.14       0.14 r
  U182/Y (INVX1)                                         0.23       0.37 f
  U181/Y (INVX8)                                         0.76       1.12 r
  cruisespeed[5] (out)                                   0.00       1.12 r
  data arrival time                                                 1.12

  clock clk (rise edge)                                 10.00      10.00
  clock network delay (ideal)                            0.00      10.00
  clock reconvergence pessimism                          0.00      10.00
  output external delay                                 -5.00       5.00
  data required time                                                5.00

-----------------------------------------------------------------------------
---
  data required time                                                5.00
  data arrival time                                                -1.12

-----------------------------------------------------------------------------
---
  slack (MET)                                                     3.88

Warning: report_timing has satisfied the max_paths criteria. There are 33
further endpoints which have paths of interest with slack less than
5.00 that were not considered when generating this report. (UITE-502)

1
```

Min_path_txt

```
****************************************
Report : timing
       -path_type full
       -delay_type min
       -slack_lesser_than 5.00
       -max_paths 3
       -sort_by slack
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Tue Oct 24 14:53:29 2023
****************************************


  Startpoint: reset (input port clocked by clk)
  Endpoint: cruisectrl_reg
              (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.00       0.00 f
  reset (in)                               0.04       0.04 f
  U154/Y (OAI21X1)                         0.08       0.12 r
  cruisectrl_reg/D (DFFPOSX1)              0.00       0.12 r
  data arrival time                                   0.12

  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  clock reconvergence pessimism            0.00       0.00
  cruisectrl_reg/CLK (DFFPOSX1)                       0.00 r
  library hold time                        0.00       0.00
  data required time                                  0.00
  -----------------------------------------------------------
  data required time                                  0.00
```

```
  data arrival time                                  -0.12
  ------------------------------------------------------------
  slack (MET)                                         0.12


  Startpoint: cruisespeed_reg[3]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed_reg[3]
              (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                                 Incr       Path

-------------------------------------------------------------------------------
---
  clock clk (rise edge)                                 0.00       0.00
  clock network delay (ideal)                           0.00       0.00
  cruisespeed_reg[3]/CLK (DFFPOSX1)                     0.00       0.00 r
  cruisespeed_reg[3]/Q (DFFPOSX1)                       0.14       0.14 r
  U128/Y (AOI22X1)                                      0.06       0.19 f
  U126/Y (NAND2X1)                                      0.06       0.25 r
  cruisespeed_reg[3]/D (DFFPOSX1)                       0.00       0.25 r
  data arrival time                                                0.25

  clock clk (rise edge)                                 0.00       0.00
  clock network delay (ideal)                           0.00       0.00
  clock reconvergence pessimism                         0.00       0.00
  cruisespeed_reg[3]/CLK (DFFPOSX1)                                0.00 r
  library hold time                                     0.00       0.00
  data required time                                               0.00

-------------------------------------------------------------------------------
---
  data required time                                               0.00
  data arrival time                                               -0.25

-------------------------------------------------------------------------------
---
  slack (MET)                                                      0.25


  Startpoint: cruisespeed_reg[5]
```

```
               (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed_reg[5]
               (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                                   Incr       Path

-----------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  cruisespeed_reg[5]/CLK (DFFPOSX1)                       0.00       0.00 r
  cruisespeed_reg[5]/Q (DFFPOSX1)                         0.14       0.14 r
  U122/Y (AOI22X1)                                        0.06       0.19 f
  U120/Y (NAND2X1)                                        0.06       0.25 r
  cruisespeed_reg[5]/D (DFFPOSX1)                         0.00       0.25 r
  data arrival time                                                  0.25

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  clock reconvergence pessimism                           0.00       0.00
  cruisespeed_reg[5]/CLK (DFFPOSX1)                                  0.00 r
  library hold time                                       0.00       0.00
  data required time                                                 0.00

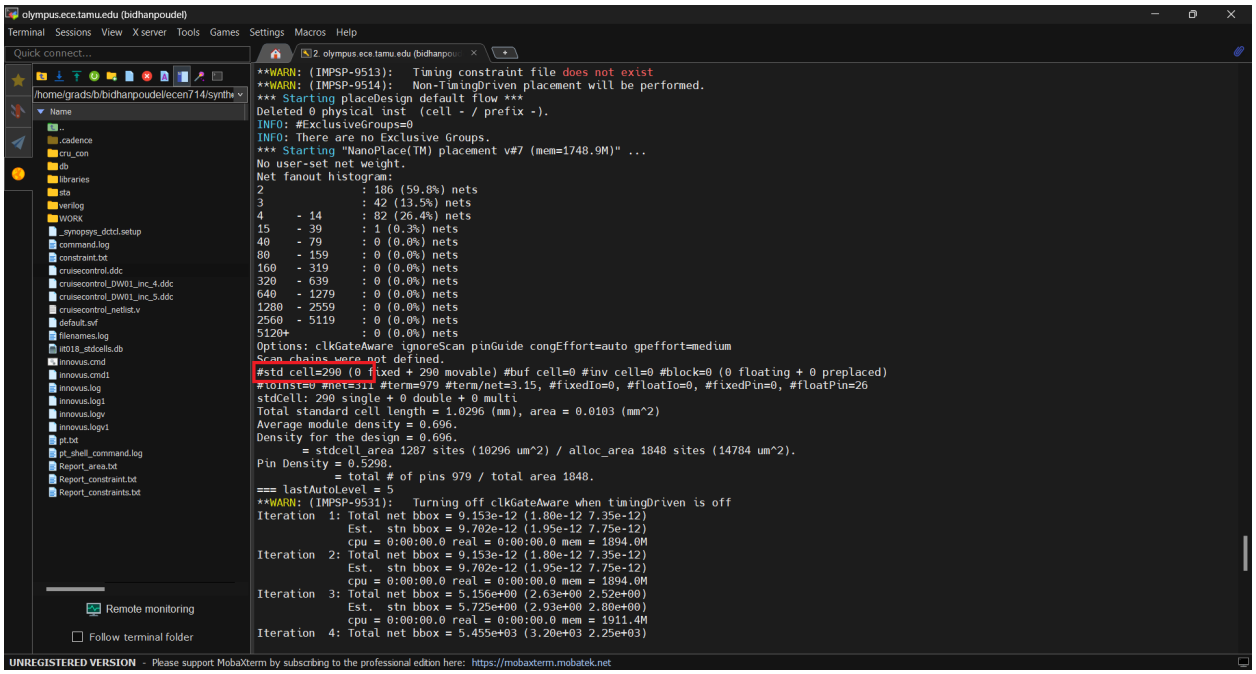
-----------------------------------------------------------------------------
---
  data required time                                                 0.00
  data arrival time                                                 -0.25

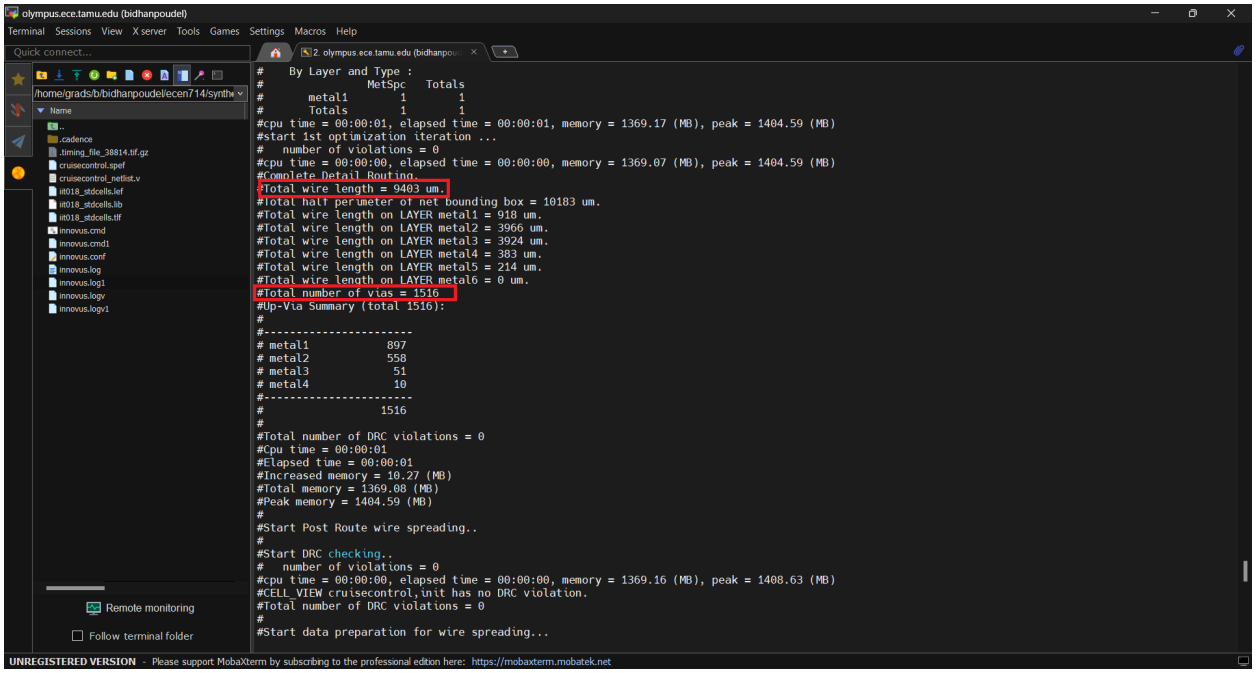
-----------------------------------------------------------------------------
---
  slack (MET)                                                        0.25

Warning: report_timing has satisfied the max_paths criteria. There are 17
further endpoints which have paths of interest with slack less than
5.00 that were not considered when generating this report. (UITE-502)

1
```

Part C: Automatic Place and Route





Total Wire Lengh: 9403 um
Number of Vias : 1516
Number of standard cells: 290

Generated Layout