Final Lab Report: IC Mems and Sensor Fabrication

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***Abstract*— This report presents the process flow and outcomes of microelectronic device fabrication through sequential laboratory experiments. The study focuses on the integration of key steps, including wafer preparation, oxidation, photolithography, doping, metallization, and device characterization. Each step is analyzed for its impact on device performance, with specific emphasis on physical data collection. The report synthesizes the process overview, procedure, and results.**

***Index Terms*— Device fabrication, Oxidation, Ion implantation, Semiconductor Processing, Microelectronic Devices, CMOS circuit, Device Characterization**

I. INTRODUCTION

Semiconductor device fabrication is a cornerstone of modern technology, enabling the production of microelectronic devices as transistor, sensors, and integrated circuits. The integration of process like oxidation, photolithography, and metallization is essential to achieve precise control over device characterization.

The labs in ECEN 688 focus on fabricating microelectronic devices using sequential processing steps, providing a hands-on understanding of the principles underlying semiconductor manufacturing.

The Primary objectives of this labs were to explore the key fabrication techniques, understand their individual roles, and analyze their combined impact on device performance.

This report documents the experimental methods, results, and analyses for each fabrication step.

II. WAFER HANDLING, PREPARATION, AND CHARACTERIZATION

Proper wafer Handling and preparation are critical for ensuring high-quality semiconductor device fabrication. Adhering to cleanroom protocols and employing precise cleaning methods are essentials to minimize contamination and maintain wafer integrity.

A. Objective

In this lab we learned how to handle wafers, how the fabrication process works, and how to safely perform the labs. We also used the four-point probe to measure the sheet resistivity of our silicon wafer.

B. Procedure

Upon receiving the wafer, its identifier and physical characteristics, such as resistivity, majority carrier type, and doping concentration, were recorded. Proper handling techniques were employed, including using tweezers to grip the wafer edges and adhering to cleanroom protocols to prevent contamination. The four-point probe method was used to measure sheet resistance at five distinct locations (center, top, bottom, left, and right), with readings averaged for accuracy. Oxide thickness was measured using an ellipsometer after calibration, ensuring proper wafer alignment and system functionality before collecting data

C. Results and Calculations

Specification	Details
Diameter	50.8 mm
Orientation	<100> OnO
Thickness	279±20 µm
Production Lot ID	1908-6604-22-295/2-1D
Type/Dopant	N/Phos
Resistivity	1-5 ohm cm
TTV (Total Thickness Variation)	< 5µm

Fig. 1. Wafer Characterization from Manufacturer

Point	X (mm)	Y (mm)	R (Ohm/sq)	Res (Ohm-cm)	V/I	Thickness (µm)
1	0	0	99.571762	0.005974	19.669867	0.6
2	90	0	85.617202	0.005192	21.440273	0.6
3	0	0	86.532402	0.005441	20.274214	0.6
4	-90	0	90.664394	0.004052	21.640006	0.6
5	0	-90	67.538399	0.005384	21.370295	0.6

Fig. 2. Four-point probe test result

Parameter	Value
Average Rs (Ohm/sq)	86.007335
Min Rs (Ohm/sq)	67.538399
Max Rs (Ohm/sq)	99.571762
Std Dev	10.561404
1 Sigma	12.661486

Fig. 3. Result Summary

D. Device Profile

Fig. 4. Lab1 device profile

III. Thermal Oxidation

Thermal oxidation is a critical step in semiconductor processing, used to grow a thin silicon dioxide (SiO_2) layer on the wafer surface. This layer serves as an insulator and a mask for subsequent processes such as ion implantation.

A. Objective

In this lab, we used thermal oxidation to grow the field oxide for our device.

B. Procedure

The thermal oxidation process began with wafer cleaning using a piranha solution (3:1 mixture of sulfuric acid and hydrogen peroxide) to remove biological contaminants, followed by rinsing in heated deionized water to eliminate impurities and prevent temperature shock. The furnace was stabilized at 1100°C with nitrogen (N_2) purging and oxygen (O_2) flows set according to specifications, while the DI water bubbler was heated to 98°C. Wafers were loaded into an oxidation boat with polished sides facing forward and placed into the furnace. The process started with a 30-minute dry oxygen flow to initiate oxide formation, followed by a 1-hour wet oxygen flow to achieve the target oxide thickness of 7000Å. After oxidation, the system was purged with nitrogen, and the wafers were carefully cooled in a laminar flow hood to complete the process.

C. Device Profile

Fig. 5. Lab2 device profile

IV. Photolithography and Etch

Photolithography and etching are essential processes in semiconductor fabrication used to define and transfer intricate patterns onto the wafer surface. Photolithography involves applying a photoresist layer, aligning a photomask, and using UV light to expose specific regions. Following this, etching selectively removes unwanted material, either through chemical (wet etching) or plasma-based (dry etching) methods, to create the desired features. These steps are critical for achieving precise patterning and preparing the wafer for subsequent fabrication stages.

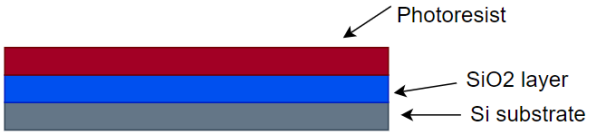
A. Objective

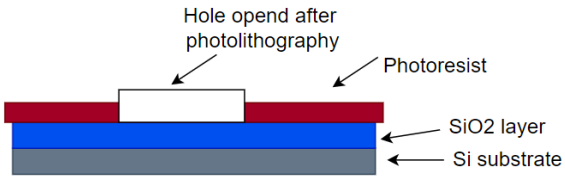
In this lab, we learned about photolithography and etching; how to accomplish it safely and how to get best results for our wafers.

B. Procedure

The photolithography and etching process began with the application of AZ5214-E positive photoresist onto the wafer using a spin coater at 4000 rpm for 40 seconds, achieving a uniform layer. The wafer was then soft baked at 120°C for 2 minutes to remove solvents and improve adhesion. Pattern exposure was performed using the MA6 Mask Aligner, with a 10-second exposure at 100 mJ/cm² through the photomask to transfer the pattern onto the photoresist. Development followed using AZ726MIF developer solution, removing the exposed areas of the photoresist and verifying the pattern accuracy under a microscope. The wafer was hard baked at 135°C for 8 minutes to prepare for etching. Etching was conducted using Buffered Oxide Etch (BOE) to remove the unprotected oxide layer, with the process monitored until the oxide was fully removed (approximately 8 minutes). Finally, the remaining photoresist was stripped by immersing the wafer in a stripping solution at 95°C.

C. Device Profile





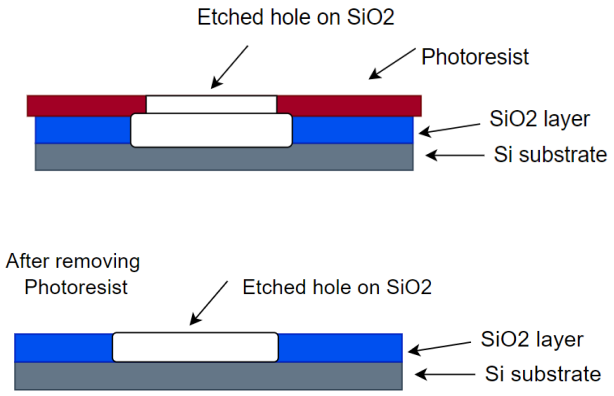


Fig. 5. Lab3 device profile

V. Gate Stack: Oxidation and Titanium Deposition

A. Objective

In this lab, we accomplished gate oxidation and titanium metal deposition. This was accomplished with the same means as the initial field oxidation process using dry oxidation. We used E-beam evaporator machine to deposit a thin film of titanium across the entire wafer.

B. Procedure

The process began by cleaning the wafers with Buffered Oxide Etch (BOE), deionized (DI) water, and nitrogen to remove any native oxide that had grown on the surface. The wafers were then placed at the edge of the furnace under a nitrogen atmosphere to heat up gradually. Once ready, the wafers were inserted into the furnace at 1000°C, where 40 nm of dry oxide was grown. One week later, the wafers were loaded into the E-beam evaporator deposition system, where a 300 nm layer of titanium metal was deposited, completing the preparation for subsequent device fabrication steps.

C. Device Profile

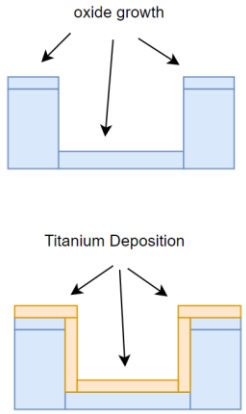


Fig. 6. Lab4 device profile

VI. Gate Patterning

A. Objective

The gate patterning process in this lab involves the use of photolithography and etching techniques to define the titanium gate stack, which consists of titanium deposited on a thin gate silicon oxide layer. During the photolithography step, a photomask is used to define the desired gate pattern, and the unpatterned titanium is subsequently removed through etching. Given the relatively small dimensions of the titanium gate region, measuring only 10 micrometers wide, achieving precise alignment and high resolution is crucial to ensure the accuracy and functionality of the patterned structures

B. Procedure

The gate patterning process began with wafer cleaning using the RCA cleaning method, followed by rinsing with deionized (DI) water to ensure a contaminant-free surface. A layer of photoresist was then applied by spin coating at 4000 RPM for 45 seconds, followed by a soft bake at 90°C for 1 minute to improve adhesion. Using a mask aligner, the wafer was aligned and exposed to UV light for 10 seconds to transfer the desired gate pattern onto the photoresist. After exposure, the wafer underwent a post-exposure bake at 90°C for 1 minute to stabilize the photoresist. The titanium layer was etched by immersing the wafer in a hydrofluoric acid solution for 35 seconds, followed by thorough rinsing with DI water to neutralize any residual acid. Residual photoresist was removed using a photoresist remover, and the wafer was rinsed and dried. The process concluded with a final inspection to verify alignment accuracy and etch quality.

C. Device Profile

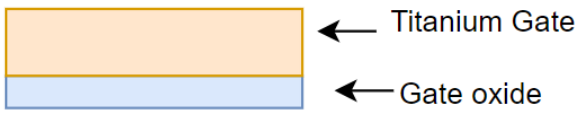


Fig. 7. Lab 5 device profile

VII. Diffusion and Ion Implantation

Diffusion and ion implantation are critical doping processes in semiconductor fabrication. Diffusion involves introducing dopants, such as boron or phosphorus, into the silicon wafer by heating in a high-temperature furnace, enabling the modification of electrical properties. Ion implantation, on the other hand, provides precise doping profiles by accelerating ions into the wafer at controlled energy levels.

A. Objective

In this lab we wanted to understand the principle and processes of doping silicon wafers to modify their electrical properties. This includes learning how diffusion and ion implantation techniques introduce dopants into the wafer.

For this lab, the wafers were sent to an offsite facility to perform the diffusion and ion implantation operations.

B. Procedure

The entire diffusion and ion implantation process was conducted at an offsite facility. The cleaned wafers were sent for processing, where diffusion was performed by placing the wafers in a high-temperature furnace, introducing dopants in a controlled environment to achieve the desired depth and concentration. Ion implantation followed, involving the acceleration of dopant ions into the wafer using a high-precision ion implanter. Post-implantation annealing was also conducted at the offsite facility to activate the dopants and repair implantation-induced damage. The processed wafers were then returned to the lab for inspection and characterization to confirm the effectiveness of the doping process.

C. Device Profile

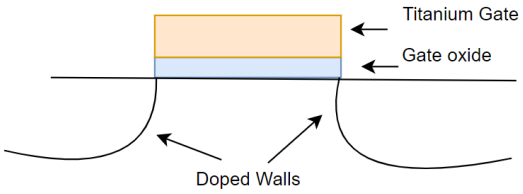


Fig. 8. Lab 6 device profile

VIII. Metallization

Metallization is a critical step in semiconductor fabrication that involves depositing a thin layer of metal, such as aluminum, onto the wafer to create electrical contacts and interconnects. This process ensures proper electrical connectivity between various device components and plays a vital role in the overall functionality and performance of the fabricated device.

A. Objective

In this lab use PVD to deposit the metal layer on our wafer. We deposited a layer of aluminum 300 nm thick using the same as method as poly si. The rate of deposition was 3 Å/s and the e-beam evaporator was operated at 6 kV and 600W.

B. Procedure

The metallization process began by loading the wafers into an electron-beam (e-beam) evaporator and placing aluminum pieces into the crucible. Once the system was securely closed, a vacuum was drawn to create the necessary deposition environment. The aluminum was then heated using a beam of electrons until it vaporized and deposited onto the wafer surface. The deposition process lasted approximately 30 minutes, resulting in a uniform aluminum layer for electrical contacts and interconnects.

C. Device Profile

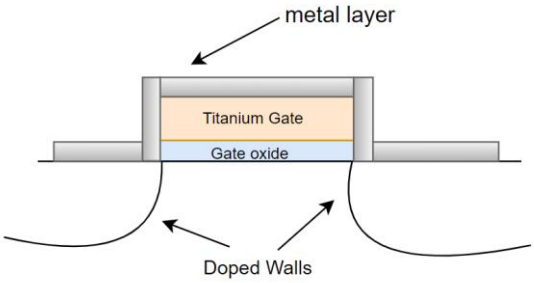


Fig. 9. Lab 7 device profile

IX. Metal patterning

A. Objective

This lab marked the final step in completing our wafers. Photolithography and etching were used to remove excess aluminum and pattern the metal layer, forming interconnects and contact pads for our devices. To ensure proper functionality, an annealing step was required to establish good ohmic contact with the doped source and drain regions.

B. Procedure

The metallization process began with cleaning the wafers using nitrogen gas to ensure a contaminant-free surface. The wafers were then spin-coated with a layer of positive photoresist and soft-baked on a hot plate at 120°C for 2 minutes to enhance adhesion. Next, the wafers were exposed to ultraviolet light using a lithography machine to define the desired pattern, followed by development in a solution for 4 minutes, rinsing in water for 2 minutes, and drying with nitrogen. A hard bake at 135°C for 8 minutes solidified the photoresist pattern. The final step involved etching the aluminum layer using a nitric and phosphoric acid solution for 7 minutes to remove excess aluminum, followed by a water rinse for 2 minutes, completing the patterning of the metal layer.

C. Device Profile

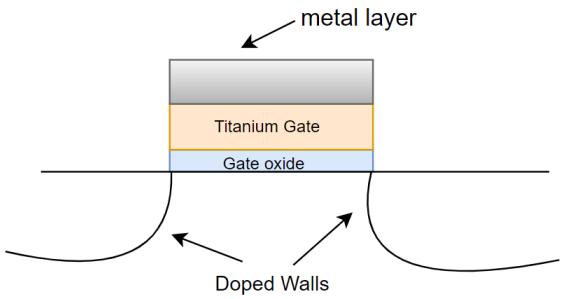


Fig. 10. Lab 8 device profile

X. Device Analysis

The Device Analysis process is a critical step in semiconductor fabrication, where the electrical and physical characteristics of the fabricated devices are evaluated to verify their functionality and performance. This involves measuring key parameters such as resistance, capacitance, and current-voltage behavior to ensure the devices meet design specifications. Device analysis provides insights into the quality of fabrication processes, identifies potential defects, and validates theoretical models with experimental results. By understanding the performance of devices like MOS capacitors and transistors, this step bridges the gap between fabrication and practical application, ensuring reliability and optimal performance in real-world scenarios.

A. Procedure

The device analysis began by placing the wafer on the chuck and positioning probes on the terminals of the devices under test. For resistors and diodes, one Source Measurement Unit (SMU) was set to ground while another performed a voltage sweep to generate I-V curves, with measurements repeated for all similar devices. For MOS transistors, additional steps included connecting a third SMU to the gate terminal and applying gate voltage values below and above the threshold voltage to observe off and on states. A fourth SMU was connected to the substrate or wafer backside and set to ground or the same voltage as the source terminal. To extract ID-VG curves for threshold voltage determination, the drain voltage was set for deep triode operation while the gate voltage was swept across a range capturing both ‘off’ and ‘on’ states. This procedure was repeated for all MOS transistors to ensure comprehensive analysis.

B. Results

Section 1: Tuesday 11 am

a. Mosfet1

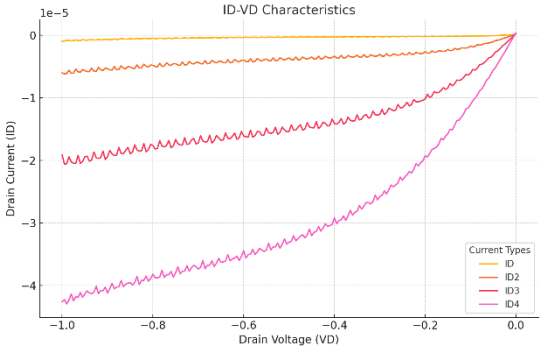


Fig. 11. ID-VD curve

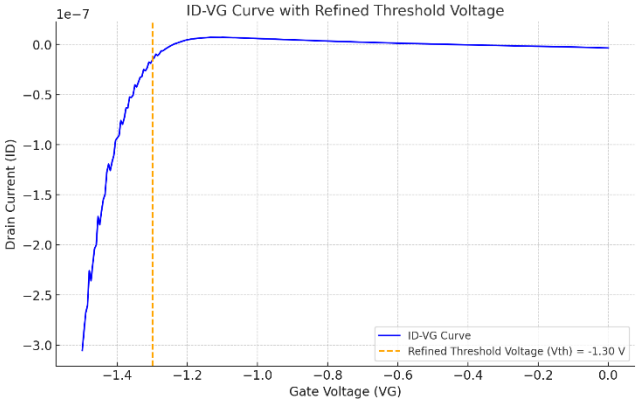


Fig. 12. ID-VG Curve

According to the IV characteristics curve, the mosfet is P-channel enhancement -mode MOSFET. And, the threshold voltage for this mosfet is around -1.30v.

a. MOSFET-2

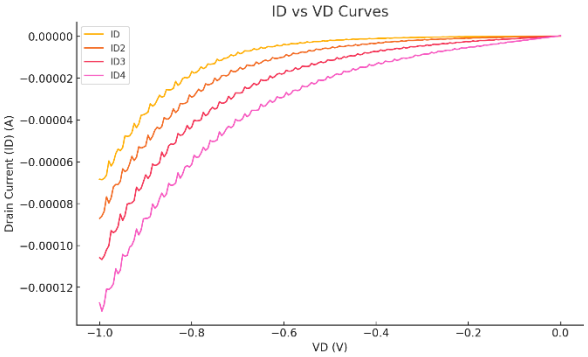


Fig. 13. Id -Vd curve

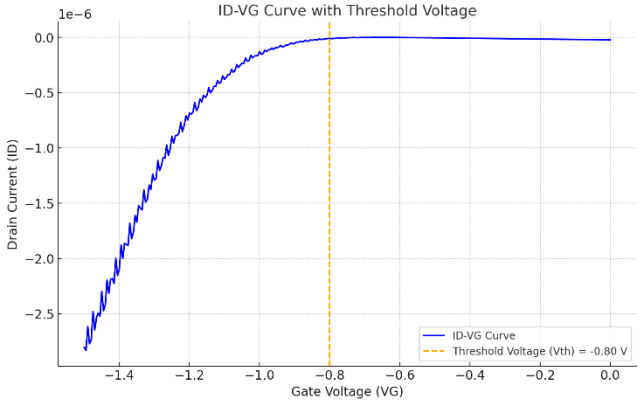


Fig. 14. Id -Vg curve

According to the IV characteristics curve, this is also P channel enhancement type mosfet.

b. MOSFET-3

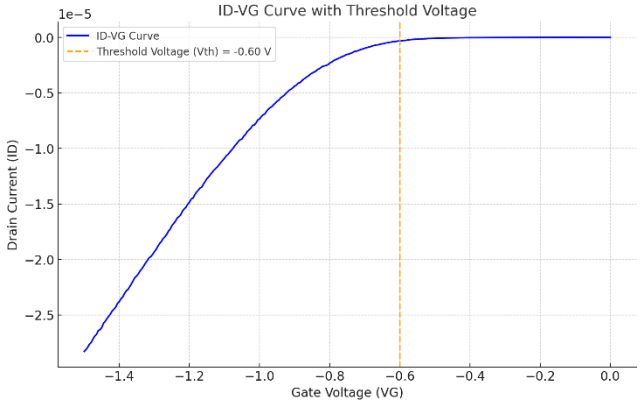


Fig. 15. Id -Vg curve

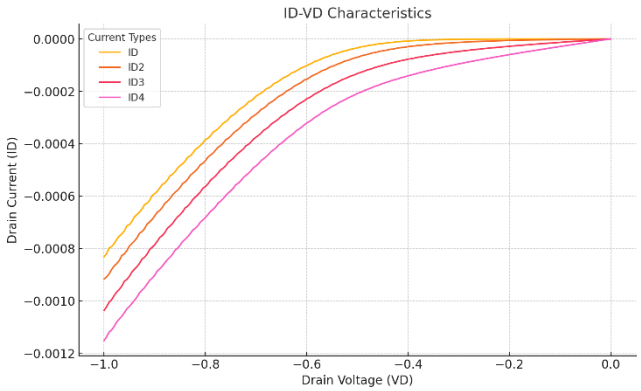


Fig. 16. Id -Vd curve

This is only P-channel Enhancement type mosfet.

Section 2: Tuesday 2pm

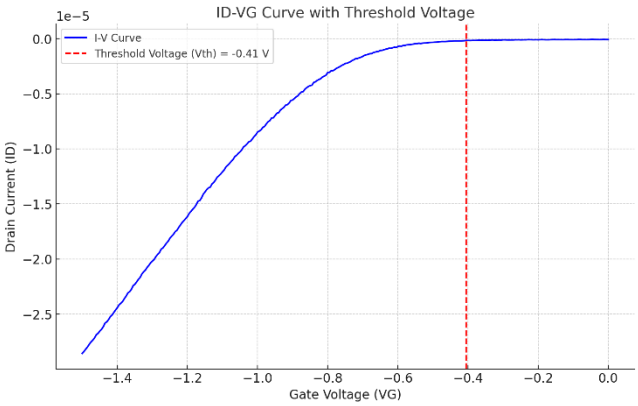


Fig. 17. Id -Vg curve

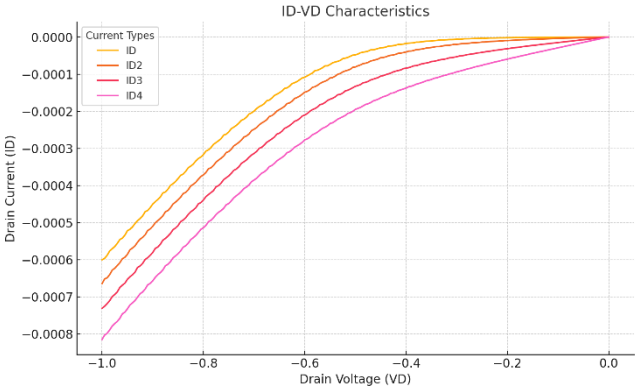


Fig. 18. Id -Vd curve

This is P-channel Enhancement type mosfet with threshold voltage of around -0.41v.

Section 3: Wednesday 11am

c. Mosfet1

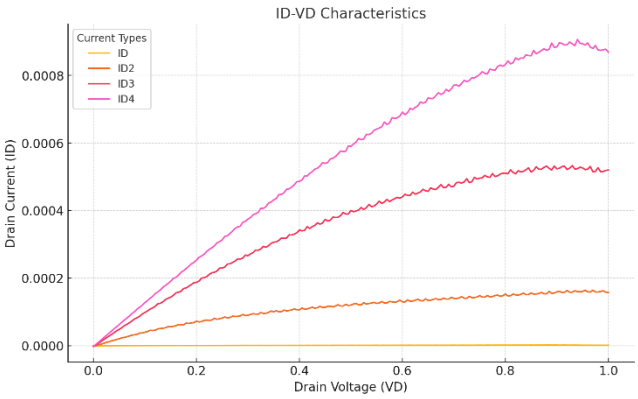


Fig. 19. Id -Vd curve

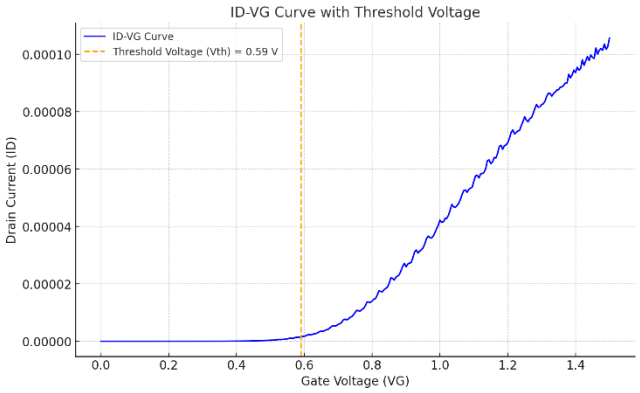


Fig. 15. Id -Vg curve

According to the IV characteristics curve for the mosfet, it is n-channel enhancement type mosfet. Here the threshold voltage is around 0.59v

d. MOSFET-2

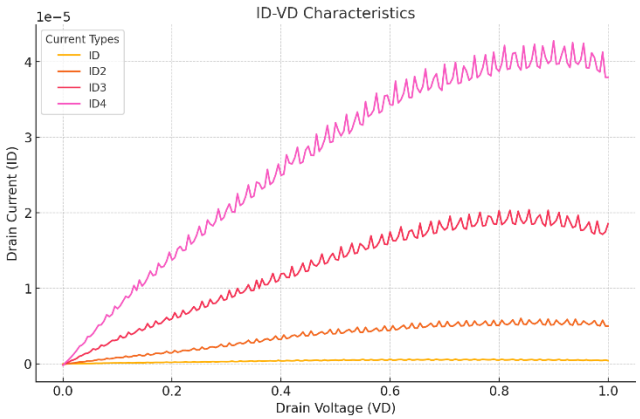


Fig. 16. Id -Vd curve

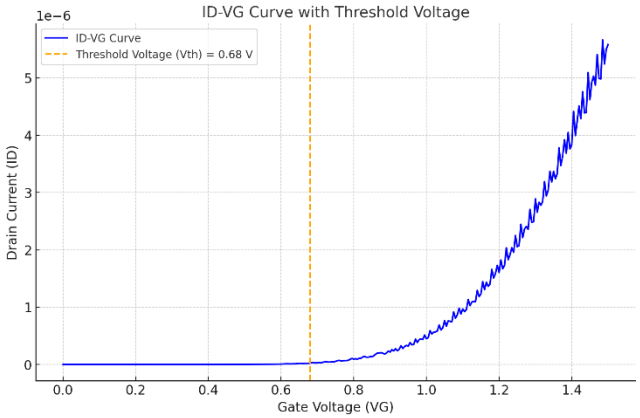


Fig. 17. Id -Vd curve

Section 4: Wednesday 8am

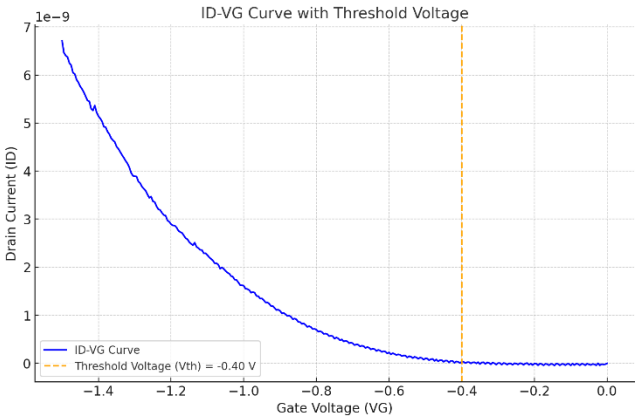


Fig. 18. Id -Vg curve

Section 5: Wednesday 5pm

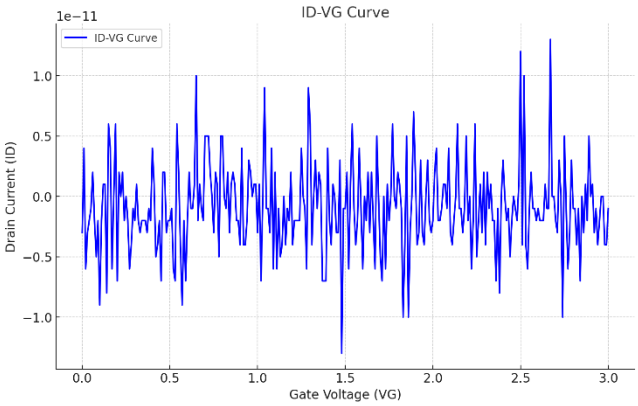


Fig. 19. Id -Vg curve

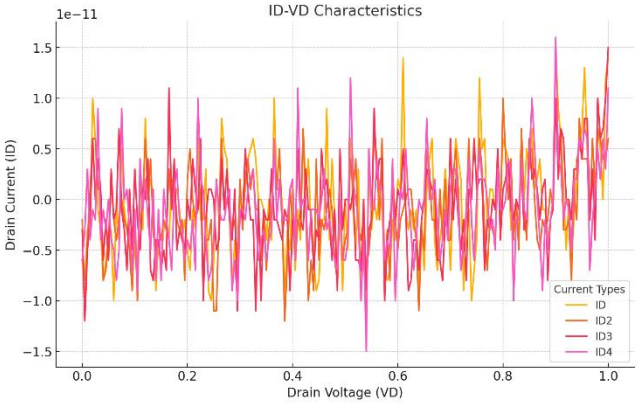


Fig. 20. Id -Vd curve

The IV characteristic curve for the device tested in this lab section shows an unusual behavior and doesn't represent any of the mosfet type. This device tested most probably be an

defective component. During the fabrication, there is a high possibility that there might be some defective components and this might be one of those.

V. Conclusion

This report provides a comprehensive overview of the fabrication process and analysis of semiconductor devices, emphasizing the integration of multiple steps including wafer preparation, oxidation, photolithography, doping, metallization, and device characterization. Through these laboratory experiments, we gained hands-on experience with the principles and techniques underlying semiconductor manufacturing.

Key observations include the successful fabrication of P-channel and N-channel enhancement-mode MOSFETs, with accurate characterization of their threshold voltages and current-voltage behavior. The processes demonstrated the critical role of precise control at every step, from thermal oxidation to metallization, to ensure device functionality and performance. However, the identification of a potentially defective MOSFET during analysis highlighted the importance of rigorous quality control and the potential for defects during fabrication.

Overall, these labs provided invaluable insights into the challenges and intricacies of semiconductor device fabrication. The results reinforced the importance of cleanroom protocols, precise equipment calibration, and a thorough understanding of material properties. This hands-on experience not only deepened our knowledge of CMOS fabrication techniques but also prepared us to address real-world challenges in microelectronic device production.

Acknowledgment

I would like to express my sincere gratitude to **Prof. H.R. Harris** for providing invaluable guidance and knowledge throughout the course and for offering an opportunity to gain hands-on experience in semiconductor device fabrication.

I would also like to extend my thanks to **Ryan Samuel**, the TA for my section, and **Jinyu Dai** for their support, assistance, and constructive feedback during the lab sessions. Their expertise and dedication were instrumental in ensuring the success of this project.