Instruction Set

Architecture

32 Bits CPU Based on MIPS

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# Instructions

## I)R-Type instructions

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALUop** |
| add | 000000 | 000000-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **000000** |
| sub | 000001 | 000001-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **000001** |
| mul | 000010 | 000010-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **000010** |
| div | 000011 | 000011-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **000011** |
| or | 000100 | 000100-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **000100** |
| and | 000101 | 000101-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **000101** |

## II)I-Type Instruction

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALUop** |
| addi | 000110 | 000110-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **000000** |
| subi | 000111 | 000111-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **000001** |
| muli | 001000 | 001000-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **000010** |
| divi | 001001 | 001001-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **000011** |
| ori | 001010 | 001010-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **000100** |
| andi | 001011 | 001011-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **000101** |

### Computational

### Load & Store

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALUop** |
| lw | 001100 | 000110-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **000000** |
| sw | 001101 | 001101-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **000000** |

### Branch

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALUop** |
| beq | 001110 | 001110-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **000001** |

## III)J-Type

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALUop** |
| jump | 001111 | 001111-xxxxxxxxxxxxxxxxxxxxxxxxxx | **X** |

# Signals of Control Unit

## R-Type Signals

|  |  |
| --- | --- |
| instruction | R-Type |
| RegDs | 1 |
| AluSrc | 0 |
| RgWrite | 1 |
| jump | 0 |
| Branch | 0 |
| MemWrite | 0 |
| MemRead | 0 |
| MemToReg | 0 |
| ExOp | X |

## I-Type Computational

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| instruction | addi | subi | muli | divi | ori | andi |
| RegDs | 0 | 0 | 0 | 0 | 0 | 0 |
| AluSrc | 1 | 1 | 1 | 1 | 1 | 1 |
| RgWrite | 1 | 1 | 1 | 1 | 1 | 1 |
| jump | 0 | 0 | 0 | 0 | 0 | 0 |
| Branch | 0 | 0 | 0 | 0 | 0 | 0 |
| MemWrite | 0 | 0 | 0 | 0 | 0 | 0 |
| MemToReg | 0 | 0 | 0 | 0 | 0 | 0 |
| ExOp | 0 | 0 | 0 | 0 | 0 | 0 |
| ALuOp | 000000 | 000001 | 000010 | 000011 | 000100 | 000101 |

## I-Type Load & Store

|  |  |  |
| --- | --- | --- |
| instruction | lw | sw |
| RegDs | 0 | Don’t care |
| AluSrc | 1 | 1 |
| RgWrite | 1 | 0 |
| jump | 0 | 0 |
| Branch | 0 | 0 |
| MemWrite | 0 | 1 |
| MemRead | 1 | 0 |
| MemToReg | 1 | Don’t care |
| ExOp | 1 | 1 |
| AluOP | 000000 | 000000 |

## I-Type Branch

|  |  |
| --- | --- |
| instruction | beq |
| RegDs | Don’t care |
| AluSrc | 0 |
| RgWrite | 0 |
| jump | 0 |
| Branch | 1 |
| MemWrite | 0 |
| MemToReg | Don’t care |
| ExOp | Don’t care |
| ALuOp | 000001 |

## Jump

|  |  |
| --- | --- |
| instruction | jump |
| RegDs | 0 |
| AluSrc | 0 |
| RgWrite | 0 |
| jump | 1 |
| Branch | 0 |
| MemWrite | 0 |
| MemToReg | 0 |
| ExOp | 0 |
| ALuOp | Don’t care |