Instruction Set

Architecture

32 Bits CPU Based on MIPS

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# Instructions

## R-Type instructions

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALU Op** |
| add | 100000 | 000000-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **Add** |
| sub | 100001 | 000001-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **Sub** |
| mul | 100010 | 000010-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **Multiply** |
| div | 100011 | 000011-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **Division** |
| or | 100100 | 000100-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **OR** |
| and | 100101 | 000101-xxxxx-xxxxx-xxxxx-xxxxxxxxxxx | **AND** |

## I-Type Instruction

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALUop** |
| addi | 000110 | 000110-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **Add** |
| subi | 000111 | 000111-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **Sub** |
| muli | 001000 | 001000-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **multiply** |
| divi | 001001 | 001001-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **Division** |
| ori | 001010 | 001010-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **OR** |
| andi | 001011 | 001011-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **AND** |

### Computational

### Load & Store

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALUop** |
| lw | 001100 | 000110-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **Add** |
| sw | 001101 | 001101-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **Add** |

### Branch

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALUop** |
| beq | 001110 | 001110-xxxxx-xxxxx-xxxxxxxxxxxxxxxx | **Sub** |

## J-Type

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | opcode | format | **ALUop** |
| jump | 001111 | 001111-xxxxxxxxxxxxxxxxxxxxxxxxxx | **X** |

# Signals of Control Unit

## R-Type Signals

|  |  |
| --- | --- |
| instruction | R-Type |
| RegDs | 1 |
| AluSrc | 0 |
| RgWrite | 1 |
| jump | 0 |
| Branch | 0 |
| MemWrite | 0 |
| MemRead | 0 |
| MemToReg | 0 |
| ExOp | X |

## I-Type Computational

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| instruction | addi | subi | muli | divi | ori | andi |
| RegDs | 0 | 0 | 0 | 0 | 0 | 0 |
| AluSrc | 1 | 1 | 1 | 1 | 1 | 1 |
| RgWrite | 1 | 1 | 1 | 1 | 1 | 1 |
| jump | 0 | 0 | 0 | 0 | 0 | 0 |
| Branch | 0 | 0 | 0 | 0 | 0 | 0 |
| MemWrite | 0 | 0 | 0 | 0 | 0 | 0 |
| MemToReg | 0 | 0 | 0 | 0 | 0 | 0 |
| ExOp | 0 | 0 | 0 | 0 | 0 | 0 |
| ALuOp | Add | Sub | mul | division | OR | AND |

## I-Type Load & Store

|  |  |  |
| --- | --- | --- |
| instruction | lw | sw |
| RegDs | 0 | Don’t care |
| AluSrc | 1 | 1 |
| RgWrite | 1 | 0 |
| jump | 0 | 0 |
| Branch | 0 | 0 |
| MemWrite | 0 | 1 |
| MemRead | 1 | 0 |
| MemToReg | 1 | Don’t care |
| ExOp | 1 | 1 |
| AluOP | Add | Add |

## I-Type Branch

|  |  |
| --- | --- |
| instruction | beq |
| RegDs | Don’t care |
| AluSrc | 0 |
| RgWrite | 0 |
| jump | 0 |
| Branch | 1 |
| MemWrite | 0 |
| MemToReg | Don’t care |
| ExOp | Don’t care |
| ALuOp | Sub |

|  |  |
| --- | --- |
| instruction | jump |
| RegDs | 0 |
| AluSrc | 0 |
| RgWrite | 0 |
| jump | 1 |
| Branch | 0 |
| MemWrite | 0 |
| MemToReg | 0 |
| ExOp | 0 |
| ALuOp | Don’t care |

## Jump