Module Name	Description	Create	Revision	HDL	Approach	Synthesizable	Errors	Warnings
Bit_Comp_Eq	Comparing two bits and determining whether they are equal	2016/08	2016/08	VHDL	Combinatorial	✓	x	x
Bit_Demux1_2	1-Bit 1x2 demultiplexer	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Bit_Flipflop_D_Async	1-Bit D Flip-Flop with asynchronous reset	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Bit_Flipflop_D_Async_FallEdge	1-Bit D Flip-Flop with asynchronous reset, which responds to the falling edge of the clock	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Bit_Flipflop_D_Sync	1-Bit D Flip-Flop with synchronous reset	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Bit_Mux2_1	1-Bit 2x1 multiplexer	2016/08	2016/08	VHDL	Combinatorial	✓	x	x
Edge_Detector	Rising edge detector based on emission delay technique	2016/08	2016/08	VHDL	Structural	✓	x	x
Edge_Detector_TB	Test bench for the rising edge detector that is based on emission delay technique UUT => Edge_Detector	2016/08	2016/08	VHDL	Behavioral	x	x	x
Flipflop_T_Async	T Flip-Flop with asynchronous reset	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Gen_Addr_Calc	Generic core to calculate the address of two cities' distance in the ROM (distance matrix)	2016/09	2016/09	VHDL	Structural	✓	x	Unconnected ports => 3 Warnings
Gen_Addr_Calc_TB	Test bench for the generic core that calculates the address of two cities' distance in the ROM UUT => Gen_Addr_Calc (Gen_Addr_Formula)	2016/09	2024/04/24	VHDL	Behavioral	x	x	x
Gen_Addr_Formula	Generic core to calculate the address of two cities' distance in the ROM (distance matrix)	2016/09	2024/05/22	VHDL	Moore FSM	✓	x	x
Gen_Bee_Async	Generic core to simulate the bee behavior, hold the path of TSP and make changes to it	2016/09	2024/06/12	VHDL	Moore FSM	✓	x	x
Gen_Bee_Sync	Generic core to simulate the bee behavior, hold the path of TSP and make changes to it	2016/09	2024/06/12	VHDL	Moore FSM	✓	x	x
Gen_Bee_TB	Test bench for the generic core simulating the bee behavior UUT => Gen_Bee_Async / Gen_Bee_Sync	2016/08	2016/09	VHDL	Behavioral	x	x	x
Gen_CNT	Generic core for an incremental counter	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Gen_Comp	Generic comparison core of two data	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Gen_Comp_Eq	Generic core for determining that two values are equal	2016/08	2016/08	VHDL	Combinatorial	✓	x	x
Gen_Comp_Less	Generic core for comparing two values and specifying the lesser one	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Gen_Demux1_2	Generic core for 1x2 demultiplexer	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Gen_Demux1_4	Generic core for 1x4 demultiplexer	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Gen_Euclidean_Distance	Generic core to calculate the Euclidean distance between two points on the 2D page (Altera SQRT IP core)	2024/07/15	2024/07/16	VHDL	Moore FSM	✓	x	x
Gen_Euclidean_Distance_Xilinx	Generic core to calculate the Euclidean distance between two points on the 2D page (Xilinx SQRT IP core)	2016/09	2024/07/10	VHDL	Moore FSM	✓	x	Instantiating black box module => 1 warning
Gen_Euclidean_Distance_TB	Test bench for the generic core calculating the Euclidean distance between two points on the 2D page UUT => Gen_Euclidean_Distance	2016/09	2024/07/10	VHDL	Behavioral	x	x	x
Gen_Flipflop_D_Async	Generic core for the D Flip-Flop with asynchronous reset	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Gen_HBA	Generic core for Hardware Bee Algorithm for solving the TSP	2016/09	2024/06/29	VHDL	Moore FSM	✓	x	Unconnected ports => 4 Warnings Unconnected signals => 208 Warnings (trimmed)
Gen_HBA_TB	Test bench for the generic core of Hardware Bee Algorithm which solves the TSP UUT => Gen_HBA	2016/09	2024/07/06	VHDL	Behavioral	x	x	x
Gen_Heuristic_Data_Constructor_P1	Generic core to construct the distances matrix on the RAM (RAM address and corresponding distance) ==> Based on synchronous one port ROM	2016/09	2024/07/15	VHDL	Structural	✓	x	Unconnected ports => 7 Warnings Instantiating black box module => 1 warning
Gen_Heuristic_Data_Constructor_P2	Generic core to construct the distances matrix on the RAM (RAM address and corresponding distance) ==> Based on synchronous dual port ROM	2016/09	2024/07/15	VHDL	Structural	✓	x	Unconnected ports => 7 Warnings Instantiating black box module => 1 warning
Gen_Heuristic_Data_Constructor_TB	Test bench for the generic core constructing the distances matrix on the RAM UUT => Gen_Heuristic_Data_Constructor	2016/09	2024/07/14	VHDL	Behavioral	x	x	x
Gen_Index_ij	Generic core for sequentially selecting two RAM addresses	2016/09	2024/05/05	VHDL	Structural	✓	x	Unconnected ports => 1 Warnings
Gen_Index_ij_Structural	Generic core for sequentially selecting two RAM addresses + case LAST_I (Gen_Index_ij + case LAST_I)	2016/09	2024/05/05	VHDL	Structural	✓	x	Unconnected ports => 1 Warnings
Gen_Index_ij_Behavioral	Generic core for sequentially selecting two RAM addresses (Complete cases)	2016/09	2024/05/04	VHDL	Behavioral	✓	x	x
Gen_Index_ij_TB	Test bench for sequentially selecting two RAM addresses UUT => Gen_Index_ij / Gen_Index_ij_Structural / Gen_Index_ij_Behavioral	2016/09	2016/09	VHDL	Behavioral	x	x	x
Gen_Index_ij_BRAM	Generic core for sequentially selecting two RAM addresses	2016/09	2024/07/14	VHDL	Structural	✓	x	Unconnected ports => 4 Warnings
Gen_Index_ij_BRAM_TB	Test bench for sequentially selecting two RAM addresses UUT => Gen_Index_ij_BRAM	2016/09	2016/09	VHDL	Behavioral	x	x	x
Gen_LFSR	Generic core for 8-Bit LFSR (Linear Feedback Shift Register)	2016/09	2024/04	VHDL	Behavioral	✓	x	x
Gen_LFSR_Old	Generic core for 8-Bit LFSR (Linear Feedback Shift Register)	2016/09	2016/09	VHDL	Behavioral	✓	x	x
Gen_LFSR_TB	Test bench for the generic core of 8-Bit LFSR (Linear Feedback Shift Register) UUT => Gen_LFSR / Gen_LFSR_Old	2016/09	2024/05/09	VHDL	Behavioral	x	x	x
Gen_Local_Search	Generic core for the 2-Opt local search	2016/09	2024/05/28	VHDL	Moore FSM	✓	x	Unconnected ports => 3 Warnings
Gen_Local_Search_TB	Test bench for the generic core, which is responsible for the 2 Opt local search UUT => Gen_Local_Search	2016/09	2024/05/12	VHDL	Behavioral	x	x	x
Gen_Mux2_1	Generic core for 2x1 multiplexer	2016/08	2016/08	VHDL	Combinatorial	✓	x	x
Gen_Mux4_1	Generic core for 4x1 multiplexer	2016/08	2016/08	VHDL	Combinatorial	✓	x	x
Gen_Nearest_City	Generic core for specifying and saving the nearest city from the current city in the nearest neighbor search	2016/09	2016/09	VHDL	Structural	✓	x	x
Gen_Nearest_City_TB	Test bench for the generic core that specifies and saves the nearest city from the current city in the nearest neighbor search UUT => Gen_Nearest_City	2016/09	2024/04/21	VHDL	Behavioral	x	x	x
Gen_Nearest_Neighbor	Generic core for specifying the nearest neighbor from the current city	2016/09	2016/09	VHDL	Structural	✓	x	Unconnected ports => 3 Warnings
Gen_Nearest_Neighbor_TB	Test bench for the generic core which specifys the nearest neighbor from the current city UUT => Gen_Nearest_Neighbor	2016/09	2024/05/07	VHDL	Behavioral	x	x	x

Gen_Nearest_Neighbor_Tour	Generic core for determining the nearest neighbor tour for the TSP	2016/09	2016/09	VHDL	Moore FSM	✓	x	Unconnected ports => 4 Warnings
Gen_Nearest_Neighbor_Tour_TB	Test bench for the generic core that determines the nearest neighbor tour for the TSP UUT => Gen_Nearest_Neighbor_Tour	2016/09	2024/05/09	VHDL	Behavioral	x	x	x
Gen_RAM_Heuristic_Data_Loader	Generic core to load an internal/external RAM with the distance matrix information	2024/07/14	2024/07/14	VHDL	Moore FSM	✓	x	Unconnected ports => 7 Warnings Instantiating black box module => 1 warning
Gen_RAM_Heuristic_Data_Loader_TB	Test bench for the generic core loading an internal/external RAM with the distance matrix information UUT => Gen_RAM_Heuristic_Data_Loader	2024/07/14	2024/07/14	VHDL	Behavioral	x	x	x
Gen_RNG_City_Set	Generic core for generating two pseudo-random city	2016/09	2024/05/23	VHDL	Moore FSM	✓	x	x
Gen_RNG_City_Set_TB	Test bench for the generic core that generats two pseudo-random city UUT => Gen_RNG_City_Set	2016/09	2024/05/10	VHDL	Behavioral	x	x	x
Gen_Sort_Permit	Generic core for the sort's permissions	2016/09	2024/06/13	VHDL	Behavioral	✓	x	x
Gen_Sort_Permit_TB	Test bench for the generic core of the sort's permission UUT => Gen_Sort_Permit	2016/09	2024/06/11	VHDL	Behavioral	x	x	x
Gen_SR_PIPO	Generic core for the Parallel-In and Parallel-Out Shift Register (PIPO SR)	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Gen_SR_SISO	Generic core for the Serial-In and Serial-Out Shift Register (SISO SR)	2016/08	2016/08	VHDL	Behavioral	✓	x	x
Gen_SR_SISO_TB	Test bench for generic core of the Serial-In and Serial-Out Shift Register (SISO SR) UUT => Gen_SR_SISO	2016/08	2016/08	VHDL	Behavioral	x	x	x
Gen_Tour_Async	Generic core to hold the path of TSP and make changes to it	2016/09	2024/05/19	VHDL	Moore FSM	✓	x	x
Gen_Tour_Sync	Generic core to hold the path of TSP and make changes to it	2016/09	2024/05/19	VHDL	Moore FSM	✓	x	x
Gen_Tour_TB	Test bench for the generic core to hold the path of TSP and make changes to it UUT => Gen_Tour_Async / Gen_Tour_Sync	2016/09	2024/05/19	VHDL	Behavioral	x	x	x
Gen_Update_Tour_V1	Generic core to update the TSP tour after a successful local 2-OPT search	2016/09	2024/05/17	VHDL	Moore FSM	✓	x	x
Gen_Update_Tour_V2	Generic core to update the TSP tour after a successful local 2-OPT search	2016/09	2024/05/17	VHDL	Moore FSM	✓	x	x
Gen_Update_Tour_TB	Test bench for generic core to update the TSP tour after a successful local 2-OPT search UUT => Gen_Update_Tour_V1 / Gen_Update_Tour_V2	2016/09	2024/05/12	VHDL	Behavioral	x	x	x
LFSR_8Bit	8-Bit Linear Feedback Shift-Register (LFSR) Xilinx application note 052 July 7,1996 (Version 1.1)	2016/08	2024/05/09	VHDL	Behavioral	✓	x	x
LFSR_8Bit_Old	8-Bit Linear Feedback Shift-Register (LFSR) Xilinx application note 052 July 7,1996 (Version 1.1)	2016/08	2016/09	VHDL	Behavioral	✓	x	x
LFSR_8Bit_TB	Test bench for 8-Bit Linear Feedback Shift-Register (LFSR) UUT => LFSR_8Bit / LFSR_8Bit_Old	2016/08	2016/09	VHDL	Behavioral	x	x	x
TSP_Dist_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM) berlin52 Database Distance matrix	2016/08	2024/07/08	VHDL	Behavioral	✓	x	x
TSP_Dist_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM) eil51 Database Distance matrix	2016/08	2024/07/08	VHDL	Behavioral	✓	x	x
TSP_Dist_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM) eil76 Database Distance matrix	2016/08	2024/07/08	VHDL	Behavioral	✓	x	x
TSP_Dist_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM) pr76 Database Distance matrix	2016/08	2024/07/08	VHDL	Behavioral	✓	x	x
TSP_Dist_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM) st70 Database Distance matrix	2016/08	2024/07/08	VHDL	Behavioral	✓	x	x
TSP_Dist_One_Port_ROM_Sync_TB	Test bench for single-port ROM with synchronous read (Block RAM) UUT => eil51 Database Distance matrix	2016/08	2024/04/24	VHDL	Behavioral	x	x	x
TSP_X_Dual_Port_ROM_Sync	Dual-port ROM with synchronous read (Block RAM) eil51 Database X Coordinates (24 Bit)	2016/08	2024/07/10	VHDL	Behavioral	✓	x	x
TSP_X_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM) eil51 Database X Coordinates (24 Bit)	2016/08	2024/07/10	VHDL	Behavioral	✓	x	x
TSP_X8bit_Dual_Port_ROM_Sync	Dual-port ROM with synchronous read (Block RAM) eil51 Database X Coordinates (8 Bit)	2016/08	2024/07/10	VHDL	Behavioral	✓	x	x
TSP_X8bit_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM) eil51 Database X Coordinates (8 Bit)	2016/08	2024/07/10	VHDL	Behavioral	✓	x	x
TSP_Y_Dual_Port_ROM_Sync	Dual-port ROM with synchronous read (Block RAM) eil51 Database Y Coordinates (24 Bit)	2016/08	2024/07/10	VHDL	Behavioral	✓	x	x
TSP_Y_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM) eil51 Database Y Coordinates (24 Bit)	2016/08	2024/07/10	VHDL	Behavioral	✓	x	x
TSP_Y8bit_Dual_Port_ROM_Sync	Dual-port ROM with synchronous read (Block RAM) eil51 Database Y Coordinates (8 Bit)	2016/08	2024/07/10	VHDL	Behavioral	✓	x	x
TSP_Y8bit_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM) eil51 Database Y Coordinates (8 Bit)	2016/08	2024/07/10	VHDL	Behavioral	✓	x	x
Xilinx_One_Port_RAM_Async	Single-port RAM with asynchronous read (Distributed RAM)	2016/08	2016/09	VHDL	Behavioral	✓	x	x
Xilinx_One_Port_RAM_Sync	Single-port RAM with synchronous read (Block RAM)	2016/08	2016/09	VHDL	Behavioral	✓	x	x
Xilinx_One_Port_ROM_Sync	Single-port ROM with synchronous read (Block RAM)	2016/08	2024/07/08	VHDL	Behavioral	✓	x	x
Xilinx_Dual_Port_RAM_Async	Dual-port RAM with asynchronous read (Distributed RAM)	2016/08	2016/09	VHDL	Behavioral	✓	x	x
Xilinx_Dual_Port_RAM_Sync	Dual-port RAM with synchronous read (Distributed RAM)	2016/08	2016/09	VHDL	Behavioral	✓	x	x
Xilinx_Dual_Port_RAM_TB	Test bench for dual-port RAM with synchronous/asynchronous read (Distributed RAM) UUT => Xilinx_Dual_Port_RAM_Sync / Xilinx_Dual_Port_RAM_Async	2016/08	2024/05/01	VHDL	Behavioral	x	x	x
Xilinx_Dual_Port_ROM_Sync	Dual-port ROM with synchronous read (Block RAM)	2016/08	2024/07/08	VHDL	Behavioral	✓	x	x