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Circuit Design of Weighted Order Statistics Filter Based on Neural Network in CMOS Process

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***Abstract*—In this paper a circuit of order statistics filter is proposed which is programmable as a result of weighting action. In this design a sign function circuit is offered based on the neural network structure. One of the main applications of the proposed filter is in the image processing and for this reason all examples and operations are assumed for images. The circuit has been designed in CMOS 0.35 µm process and good results have been achieved.**

***Keywords*—Neural Network; Weighted Order Statistics Filter; Sigmoid Function; Image Processing**

I. INTRODUCTION

Hardware and circuit implementation of various mathematical, control, pattern recognition, and many other techniques and operations seems an essential concern. Weighted order statistics (WOS) filters among other nonlinear filters have extensive usage such as impulsive noise filtering in signal and image processing. To preserve detail in the signal being filtered by an order statistics filter and also in order to have high performance noise filter, weighting property is needed [1].

Among circuit structures, analog approaches have higher speed and lower power consumption and oppositely, their digital counterparts are more accurate. For implementing WOS filter many digital [1, 2, 3, 4] and some analog formations [5, 6] have been devised. In this paper an analog circuit is designed in CMOS 0.35 µm process in the neural network form. The circuit contains an amplifier and a transconductance amplifier (TCA) for each input that reads input voltage values and then it stores filter's output value in a capacitor (as an analog memory). Basis of the presented design is on a two layer neural network that has adjustable weights in the second layer. Obtained results indicate that the circuit has good speed and high accuracy.

The rest of the paper is organized as follows. In section II, theory of the proposed neural network is illustrated. In section III, the proposed circuit is presented. In section IV, simulation results of the circuit are shown. Simple and famous states of weighted order statistics filters are median, min, and max filters and there are their simulation results in continuation of section IV. Finally, section V concludes the paper. All circuit simulations have been done by Hspice level 49 software.

II. FORMULATION

A WOS filter is described by the model shown in (1).

$$out = Kth\ largest\ of\ \{W_0\#X_0,..,W_i\#X_i,..,W_n\#X_n\} \quad (1)$$

where *out* is the output of WOS filter, K is rank of the filter, X_i is input, W_i is weight of X_i, and $W_i\#X_i$ means X_i repeated W_i times.

Mathematical form of WOS filter is explained as the below model:

$$\frac{dV_{out}}{dt} = I_p + \sum_{i\in G(i)} b_i \times sign(V_i - V_{out}) \quad (2)$$

where V_is are input voltage values, V_{out} is output voltage, and $G(i)$ is the set of inputs. Also b_is are coefficients that assign weight of each input. I_p is the rank selector which assigns how the filter operates (median, min, max, ...).

It is proved that after a while, V_{out} will converge to a quantity [7] as indicated in:

$$V_{out}\left(t \to \infty\right) = V^* \quad (3)$$

For actual realization of sign function we have used a sigmoid function with a high transference ramp, according to:

$$I_{out} = C \times \frac{dV_{out}}{dt} = I_p + \sum_{i\in G(i)} b_i \times sigfunc[a \times (V_i - V_{out})] \quad (4)$$

where *sigfunc(.)* is a sigmoid shape function. Also "*a*" should be large enough in order to have a *sigfunc* with large transference ramp. Therefore by having large "*a*", *sigfunc* always gives the answer equal to 1 or -1 and will not have a value between them.

In order to design the circuit of sigmoid function, a differential pair in the form of transconductance amplifier can be used. Equations (5), (6), (7) are related to the demonstrated circuit in Fig. 1.

$$I_{d1} = K \times (V_1 - V_x - V_t)^2, I_{d2} = K \times (V_2 - V_x - V_t)^2,$$
$$I = I_{d1} + I_{d2} \rightarrow$$
$$\sqrt{\frac{I_{d1}}{K}} - \sqrt{\frac{I_{d2}}{K}} = V_1 - V_2 \rightarrow$$
$$I_{d1} + I_{d2} - 2 \times \sqrt{I_{d1} \times I_{d2}} = (V_1 - V_2)^2 \times K \rightarrow$$
$$\sqrt{I_{d1} \times I_{d2}} = \frac{I - K \times (V_1 - V_2)^2}{2} \rightarrow$$
$$I_{d1} \times I_{d2} = \frac{\left(I - K \times (V_1 - V_2)^2\right)^2}{4} \quad (5)$$

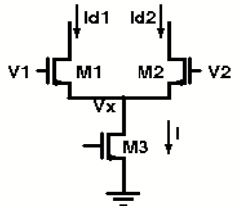

Fig. 1. Differential pair

As a result of (5) we can reach to (6), which this equation generates a sigmoid type shape. Equation (6) is valid while neither of transistors is off.

$$I_{d1}^2 + I_{d2}^2 + 2 \times I_{d1} \times I_{d2} = I^2 \rightarrow$$

$$I_{d1}^2 + I_{d2}^2 + 2 \times I_{d1} \times I_{d2} - 4 \times I_{d1} \times I_{d2} = I^2 - 4 \times$$

$$I_{d1} \times I_{d2} \rightarrow (I_{d1} - I_{d2})^2 = I^2 - \left(I - K \times V_{diff}^2\right)^2 = 2 \times$$

$$K \times I \times V_{diff}^2 - K^2 \times V_{diff}^4 \rightarrow$$

$$I_{d,diff} = V_{diff} \times \sqrt{2 \times K \times I - K^2 \times V_{diff}^2} \qquad (6)$$

Operation limit of transistors is defined as:

$$V_{diff}^4 - \frac{2 \times I}{K} \times V_{diff}^2 + \frac{I^2}{K^2} = 0 \rightarrow V_{diff} = \pm\sqrt{\frac{I}{K}} \qquad (7)$$

As mentioned before, it is desirable with turning off one of the transistors, input current (I_{diff}) become equal to I or -I.

Concerning to this points and assuming $K = 370 \times 10^{-6}$ and I=6.25 µA for differential pair's transistors, $I_{d,diff}$ variations for V_{diff} are shown in Fig. 2. This result has been obtained by Matlab software. It indicates that by using a circuit similar to the one exhibited in Fig. 1, we can reach to a sigmoid function and then realize the sign function by increasing its ramp.

Finally with consideration to (2) and (4) the neural network for realization of WOS filter is illustrated in Fig. 3. The number of first layer neurons is equal to the number of inputs. Second layer weights are same b_i coefficients. In addition, b is identical to the mentioned I_p. Note that second layer neuron just has the task of adding input currents and for this reason it is not anything except a simple connection of outputs of first layer neurons. Based on (4), at the output, capacitor C is for attaining output voltage (V_{out}) from second layer neuron's output current. Weights and bias of second layer of the neural network can be directly assigned (as we used) or network can be trained offline by use of a host machine.

III. CIRCUIT DESCRIPTION

The circuit of the first layer neuron is shown in Fig. 4. At first, the circuit amplifies (V_{out}-V_{in-i}) by transistors M12-M24, and then based on (6) it applies a sigmoid function on the amplified voltage by use of transistors

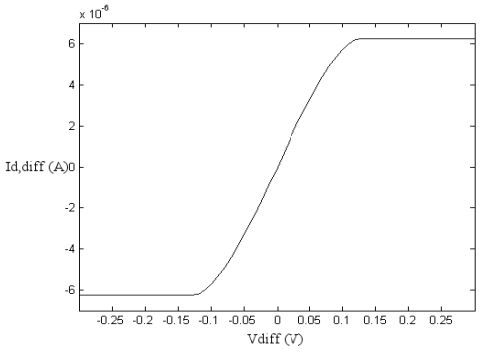

Fig. 2. $I_{d,diff}$ variations for V_{diff} in differential pair

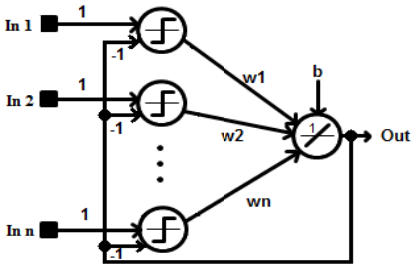

Fig. 3. The neural network of WOS filter

M1-M5. Thus, based on (7), after amplifying V_{diff}, transistor M1 or M2 goes to be turned off and so it makes total circuit to take $sign(V_{out} - V_{in-i})$.

Cascode structure is used for boosting amplifier's gain (M12-M15 and M16-M19). In order to have larger input range, only transistor M22 is used as current source of amplifier's differential pair instead of cascode structure (because it reduces swing of input voltages). In addition, bias circuit has been designed in the purpose of having least dependence to temperature variations. Transistors M6-M11 are used for biasing.

When one of the transistors M1 or M2 is off, I_{out} is linearly related to I_q. Thus, by changing the value of current source I_q we can assign neuron's output weight (w_i). Therefore WOS filter will have its weighting attribute.

Finally after using several circuits of Fig. 4 (as many as number of inputs) and connecting their outputs together, a capacitor is placed at the output to be charged by output currents, according to (4).

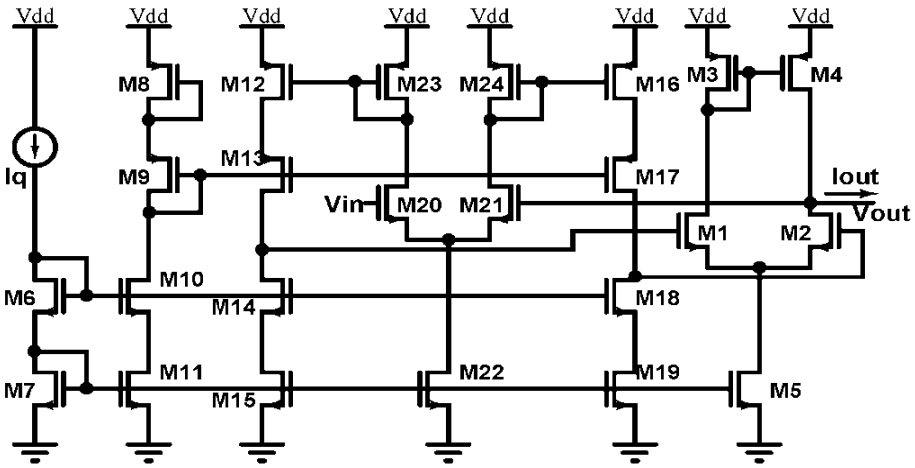

Fig. 4. The proposed circuit for implementation of WOS filter

Channel length and width of the transistors are shown in Table I. Layout of the presented circuit in Fig. 4 is shown in Fig. 5. Layout area of the proposed circuit (Fig. 4 and Fig. 5) is equal to 30×25 μm^2.

IV. Simulation Results

Considering dc sweep of (V_{in}-V_{out}), Output current (I_{out}) of first layer neuron with respect to I_q=0, 1, 2, 3, 4 μA is shown in Fig. 6. As we can see, circuit operates in the form of sign function. Because of the exploited techniques, we see steep ramp of Fig. 6 instead of gradual ramp of Fig. 2. This issue causes increasing of the accuracy of the whole neural network and this is an improvement compared to [7] (4 times steeper than [7]).

To observe general functionality of the proposed WOS filter, we review some famous cases of these filters (such as median, min, and max filters) by an example with application in the image processing. For a 3×3 mask we will need 9 neurons in first layer of the proposed neural network, hence we have used a structure like that shown in Fig. 7. Which each block is identical to the circuit of Fig. 4. A 3 pF capacitor was placed at the output. For biasing, a 2.3 V voltage source was used at the inputs and at the output too.

Table I. Channel length and width of transistors

Transistor	W(μm)	L(μm)
M1, M2, M6, M7, M10, M11, M14, M15, M18-M21	1	0.35
M5, M22	2	0.35
M3, M4, M8, M9, M12, M13, M16, M17, M23, M24	3	0.35

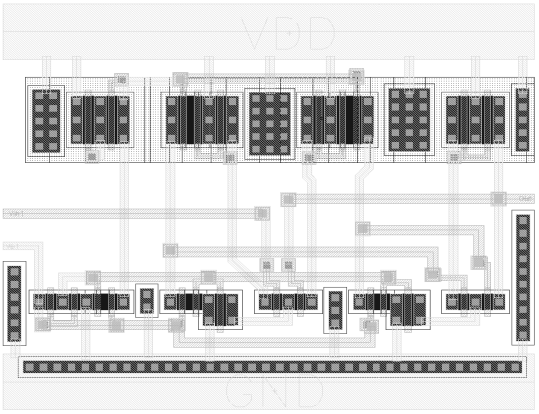

Fig. 5. Layout of the proposed circuit

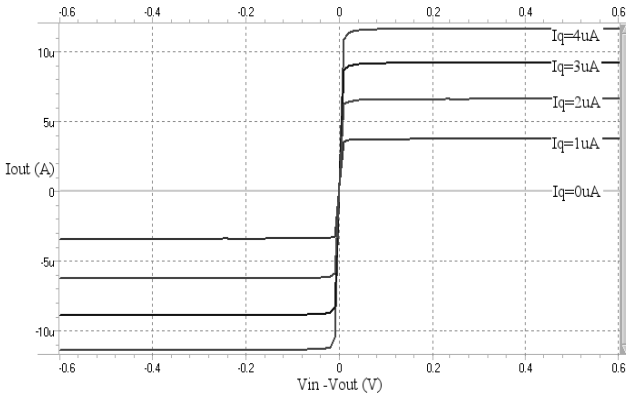

Fig. 6. Current output (I_{out}) as (V_{in} – V_{out}) swept for I_q = 0, 1, 2, 3, 4 μA

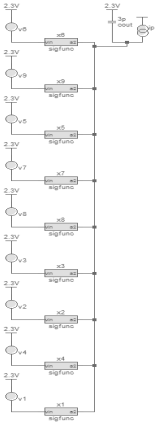

Fig. 7. Weighted order statistics filter with 9 inputs

Median filter is a special state of the presented filter and its conditions are:

$$\forall\ all\ i \in G(i): b_i = 1, I_p = 0 \qquad (8)$$

When all b_is are equal to 1, it means that I_q for all circuits is equivalent. I_q for all blocks is supposed to be 2 μA. Now if current source I_p has zero value then we have made a median filter.

Input voltages from 9 hypothetical pixels in the range of -0.5 V to 0.5 V, as a pulse with 1 MHz frequency, are shown in Table II. Result is exact median of input pulses with 1.5 mV and 3.5 mV errors in two levels of pulse that is indicated in Fig. 8 with all inputs. Also the output for dc sweeping of first input (input 1) is shown in Fig. 9 when other inputs are according to their first level values in Table II. It is indicative that the circuit has very good functionality.

Table II. Voltages of 9-input pulse

Input number	Pulse (V)		Input number	Pulse (V)	
	Second level	First level		Second level	First level
1	0.0	-0.4	6	-0.1	0.1
2	0.2	-0.37	7	-0.17	0.3
3	-0.5	-0.3	8	0.15	0.4
4	0.43	-0.25	9	-0.15	0.44
5	0.4	-0.15			

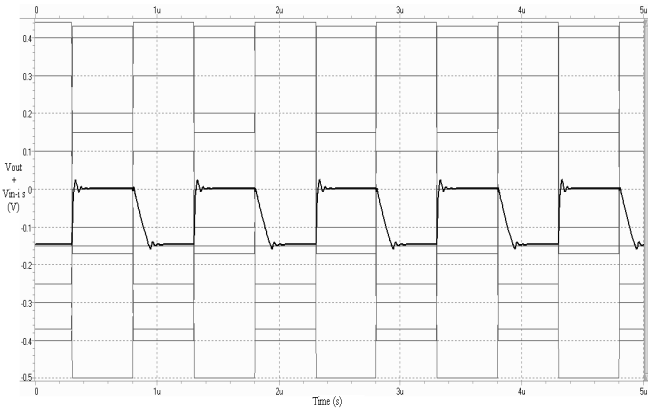

Fig. 8. Median output accompanied by inputs

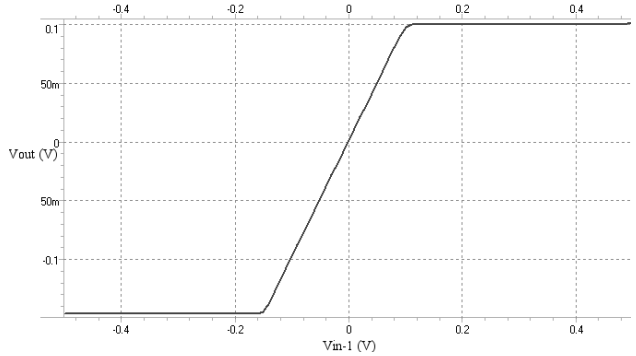

Fig. 9. Median output for dc sweep of first input

Now if we just change the value of I_p and injected current amount in the output be equal to 50 µA in this example, we will have a max circuit. Output with all inputs is illustrated in Fig. 10 with 880 µV and 820 µV errors in two levels of pulse. Fig. 11 has been obtained in the same manner that said for Fig. 9.

With changing I_p to -60 µA, we will have a min circuit which result of Fig. 12 shows its output beside inputs with 1.85 mV and 4.5 mV errors in two pulse levels. In addition, Fig. 13 shows output for dc sweeping of first input voltage when other inputs are according to their first level values in Table II.

Power consumption of the whole filter (containing 9 sign circuits) with I_p=0 in the 3×3 mask example is equal to 525 µW which is exhibited in Fig. 14. For median filter a dc sweep analysis of first input has been performed in corners ss, sf, fs, ff and in temperatures -40 ^oC, 125 ^oC when other inputs were according to their respective first level quantities in Table II. Result of this simulation can be seen in Fig. 15.

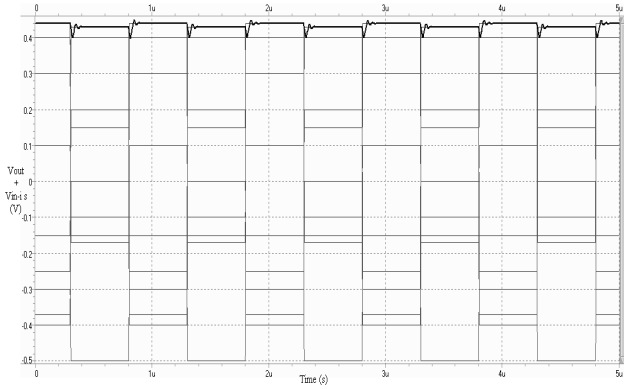

Fig. 10. Max output accompanied by inputs

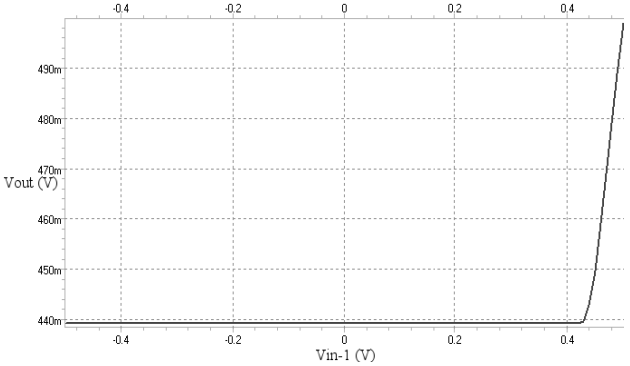

Fig. 11. Max output for dc sweep of first input

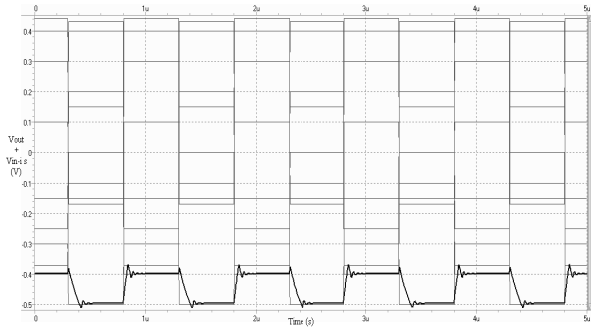

Fig. 12. Min output accompanied by inputs

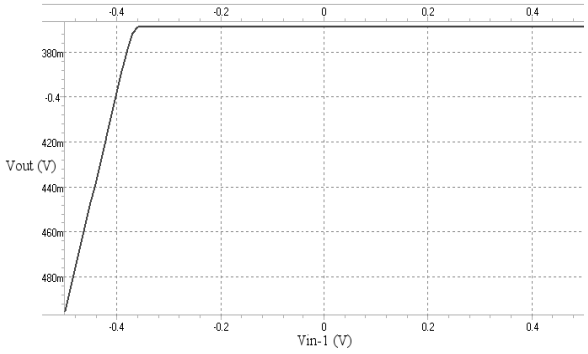

Fig. 13. Min output for dc sweep of first input

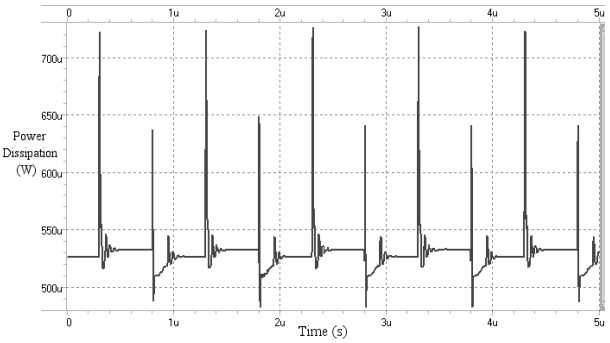

Fig. 14. Power dissipation of median filter

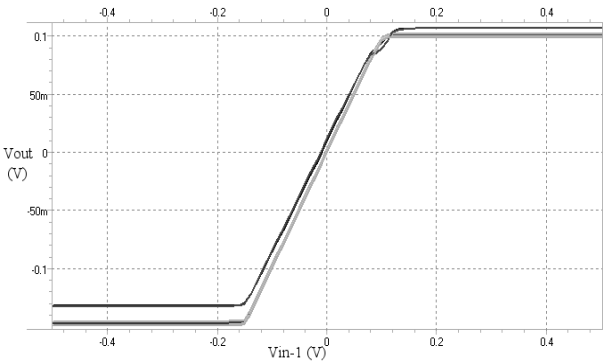

Fig. 15. Median output for dc sweep of first input in various corners and temperatures

At last for comparison to other works, Fig. 16 shows that in a min circuit with 3 displayed inputs, the worst error of the proposed circuit is 6 times lower compared to the measured results of the same inputs presented in [7].

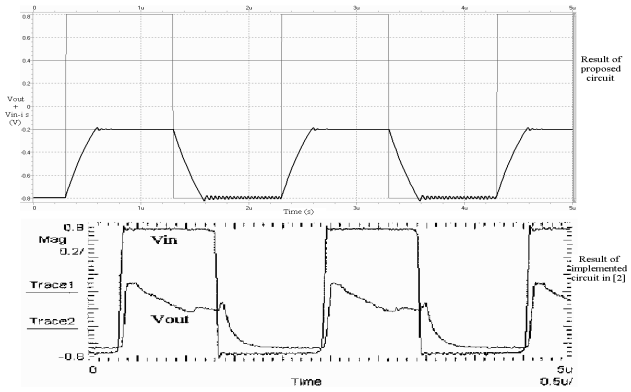

Fig. 16. Comparison with [7]

V. CONCLUSIONS

In this paper, a neural network was proposed for realization of weighted order statistics filter based on circuit of a neuron that it has improvements over earlier works. Good results have been achieved from the point of circuit power consumption and accuracy. With regard to output capacitor and bias current (I_q), high speed has been attained for the circuit. The circuit can be used for removing images' noise and has applications in other numerous fields.

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