

# گزارش پروژه تمرین جبرانی پایانترم

## حل سوال 7

(در میانترم سوالات 6 و 5 حل شده بود)

این تمرین به صورت انفرادی انجام شده است.

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من برای ساخت این پردازنده از 4 ماژول ALU ، RegisterFile ، Memory و در نهایت vectorprocessor ساختم. در ادامه کد های ماژول هر بخش نمایش میدهم.

## ماژول ALU:

```
1  module ALU (  
2      input clock,  
3      input operation,  
4      input [511 : 0] input_data_1, input_data_2,  
5      output reg [511 : 0] output_data_1, output_data_2  
6  );  
7  
8      localparam ADD = 1'b0;  
9      localparam MULL = 1'b1;  
10  
11     integer i;  
12  
13     always @(posedge clock) begin  
14         #3;  
15         case (operation)  
16             ADD: begin  
17                 for (i = 1; i < 17; i = i + 1) begin  
18                     {output_data_2[32*i-1 -: 32], output_data_1[32*i-1 -: 32]} <=  
19                         input_data_1[32*i-1 -: 32] + input_data_2[32*i-1 -: 32];  
20                 end  
21             end  
22  
23             MULL: begin  
24                 for (i = 1; i < 17; i = i + 1) begin  
25                     {output_data_2[32*i-1 -: 32], output_data_1[32*i-1 -: 32]} <=  
26                         input_data_1[32*i-1 -: 32] * input_data_2[32*i-1 -: 32];  
27                 end  
28             end  
29         endcase  
30     end  
31  
32 endmodule  
33  
34
```

## : RegisterFile ماژول

```
1  module RegisterFile (  
2      input clk,  
3      input read, write,  
4      input read_two, write_two,  
5      input [1 : 0] address,  
6      input [511 : 0] data_in,  
7      output reg [511 : 0] data_out,  
8      input [511 : 0] data_in_1, data_in_2,  
9      output reg [511 : 0] data_out_1, data_out_2  
10 );  
11     reg [511 : 0] registers [0 : 3];  
12  
13     always @(posedge clk) begin  
14         #1;  
15         if (read) begin  
16             data_out <= registers[address];  
17         end  
18  
19         if (read_two) begin  
20             data_out_1 <= registers[0];  
21             data_out_2 <= registers[1];  
22         end  
23     end  
24  
25     always @(negedge clk) begin  
26         if (write) begin  
27             registers[address] <= data_in;  
28         end  
29  
30         if (write_two) begin  
31             registers[2] <= data_in_1;  
32             registers[3] <= data_in_2;  
33         end  
34     end  
35  
36 endmodule  
37
```

## ماژول Memory :

```
1  module MainMemory (
2      input clk,
3      input read, write,
4      input [4 : 0] address,
5      input [511 : 0] data_in,
6      output reg [511 : 0] data_out
7  );
8      reg [31 : 0] mem [0 : 511];
9
10     integer i;
11
12     always @(posedge clk) begin
13         #1;
14         if (read) begin
15             for (i = 1; i < 17; i = i + 1) begin
16                 data_out[32*i-1 -: 32] <= mem[16 * address + i - 1];
17             end
18         end
19     end
20
21     always @(negedge clk) begin
22         if (write) begin
23             for (i = 1; i < 17; i = i + 1) begin
24                 mem[16 * address + i - 1] <= data_in[32*i-1 -: 32];
25             end
26         end
27     end
28
29 endmodule
30
31 |
```

## ماژول پردازنده آرایه ای vectorProcessor:

در این ماژول اصلی از ماژول های قبلی استفاده کردیم. ورودی operation مشخص می کند کدام یک از عملیات load store sum product انجام شود. فایل تمام ماژول ها قرار داده شده ( ولی تصویری از این ماژول در صفحه بعد قرار داده ام:

```

1  module VectorProcessor (
2      input [1 : 0] opcode, rf_address,
3      input [4 : 0] mem_address
4  );
5
6      // Initializing upcodes:
7      localparam ADDITION = 0;
8      localparam MULTIPLY = 1;
9      localparam LOAD = 2;
10     localparam STORE = 3;
11
12     // Control signals:
13     reg clk, mem_read, mem_write, rf_read, rf_write, read_two_regs, write_two_regs;
14
15     // Data :
16     reg [511 : 0] rf_in_1, rf_in_2;
17     wire [511 : 0] rf_out_1, rf_out_2;
18
19     wire [511 : 0] mem_data_in, mem_data_out, rf_data_in, rf_data_out;
20
21     // ALU Input & Outputs:
22     reg [511 : 0] alu_in_1, alu_in_2;
23     wire [511 : 0] alu_out_1, alu_out_2;
24
25     // Instancing modules:
26     ALU alu(clk, opcode[0], alu_in_1, alu_in_2, alu_out_1, alu_out_2);
27     MainMemory main_memory (clk, mem_read, mem_write, mem_address, mem_data_in, mem_data_out);
28     RegisterFile register_file (
29         .clk(clk),
30         .read(rf_read),
31         .write(rf_write),
32         .read_two(read_two_regs),
33         .write_two(write_two_regs),
34         .address(rf_address),
35         .data_in(rf_data_in),
36         .data_out(rf_data_out),
37         .data_in_1(rf_in_1),
38         .data_in_2(rf_in_2),
39         .data_out_1(rf_out_1),
40         .data_out_2(rf_out_2)
41     );
42
43     // Doing task:
44     assign mem_data_in = opcode[1] ? rf_data_out : {512{1'bz}};
45     assign rf_data_in = opcode[1] ? mem_data_out : {512{1'bz}};
46
47     always @(posedge clk) begin
48         case (opcode)
49
50             ADDITION, MULTIPLY : begin
51                 mem_read = 0; mem_write = 0;
52                 rf_read = 0; rf_write = 0;
53                 read_two_regs = 1; write_two_regs = 1;
54                 #2; // 2 units delay for register_file
55                 alu_in_1 <= rf_out_1;
56                 alu_in_2 <= rf_out_2;
57                 #2; // 2 units delay for alu
58                 rf_in_1 <= alu_out_1;
59                 rf_in_2 <= alu_out_2;
60                 // now the data is ready for write in registerfile before negedge of clock
61             end
62
63             LOAD: begin
64                 mem_read = 1; mem_write = 0;
65                 rf_read = 0; rf_write = 1;
66                 read_two_regs = 0; write_two_regs = 0;
67             end
68
69             STORE: begin
70                 mem_read = 0; mem_write = 1;
71                 rf_read = 1; rf_write = 0;
72                 read_two_regs = 0; write_two_regs = 0;
73             end
74
75         endcase
76     end
77
78     initial begin
79         clk = 1;
80         forever #5 clk = ~clk;
81     end
82

```

ابتدا ماژول بستر آزمون را مطابق زیر تعریف می کنیم و مقدار دهی میکنیم. و حالت های خواسته شده سوال را بررسی می کنیم.

```
1  module TestBenchProcessor;
2
3  reg [1 : 0] opcode, rf_address;
4  reg [4 : 0] mem_address;
5
6  integer i;
7
8  VectorProcessor vectorProcessor(opcode, rf_address, mem_address);
9
10 initial begin
11     for (i = 0; i < 32; i = i + 1) begin
12         vectorProcessor.main_memory.mem[i] = i;
13     end
14
15     for (i = 32; i < 512; i = i + 1) begin
16         vectorProcessor.main_memory.mem[i] = 2 ** (i % 32);
17     end
18     #100;
19
20     $monitor("Time: %t | opcode = %b | rf_address = %d | mem_address = %d"
21             , $time, opcode, rf_address, mem_address);
22
23     $display("Doing sum on first two vectors and write Results on last two vectors :\n");
24
25     opcode = 2; // Load
26     rf_address = 0; mem_address = 0;
27     #10;
28     rf_address = 1; mem_address = 1;
29     #10;
30
31     opcode = 0; // Sum
32     #10;
33
34     opcode = 3; // Store
35     rf_address = 2; mem_address = 31;
36     #10;
37     rf_address = 3; mem_address = 30;
38     #10;
39
40     $display("\nDoing multiply on second and third vectors and write Results on 15th and 16th vectors :\n");
41
42
43     opcode = 2; // Load
44     rf_address = 0; mem_address = 20;
45     #10;
46     rf_address = 1; mem_address = 21;
47     #10;
48
49     opcode = 1; // Multiply
50     #10;
51
52     opcode = 3; // Store
53     rf_address = 2; mem_address = 16;
54     #10;
55     rf_address = 3; mem_address = 15;
56     #10;
57
58     $display("\n Results of msb sum :\n");
59
60     for (i = 480; i < 496; i = i + 1) begin
61         $display("Reading data from address %d: %d", i, vectorProcessor.main_memory.mem[i]);
62     end
63
64     $display("\n Results of lsb sum :\n");
65
66     for (i = 496; i < 512; i = i + 1) begin
67         $display("Reading data from address %d: %d", i, vectorProcessor.main_memory.mem[i]);
68     end
69
70     $display("\n Results of msb multiply :\n");
71
72     for (i = 240; i < 256; i = i + 1) begin
73         $display("Reading data from address %d: %b", i, vectorProcessor.main_memory.mem[i]);
74     end
75
76     $display("\n Results of lsb multiply :\n");
77
78     for (i = 256; i < 272; i = i + 1) begin
79         $display("Reading data from address %d: %b", i, vectorProcessor.main_memory.mem[i]);
80     end
81 end
```



و نتیجه را مشاهده میکنیم:

```
Doing sum on first two vectors and write Results on last two vectors :
Time:          100 | opcode = 10 | rf_address = 0 | mem_address = 0
Time:          110 | opcode = 10 | rf_address = 1 | mem_address = 1
Time:          120 | opcode = 00 | rf_address = 1 | mem_address = 1
Time:          130 | opcode = 11 | rf_address = 2 | mem_address = 31
Time:          140 | opcode = 11 | rf_address = 3 | mem_address = 30

Doing multiply on second and third vectors and write Results on 15th and 16th vectors :
Time:          150 | opcode = 10 | rf_address = 0 | mem_address = 20
Time:          160 | opcode = 10 | rf_address = 1 | mem_address = 21
Time:          170 | opcode = 01 | rf_address = 1 | mem_address = 21
Time:          180 | opcode = 11 | rf_address = 2 | mem_address = 16
Time:          190 | opcode = 11 | rf_address = 3 | mem_address = 15
```

نتیجه جمع :

```
# Results of msb sum :
#
# Reading data from address      480:      0
# Reading data from address      481:      0
# Reading data from address      482:      0
# Reading data from address      483:      0
# Reading data from address      484:      0
# Reading data from address      485:      0
# Reading data from address      486:      0
# Reading data from address      487:      0
# Reading data from address      488:      0
# Reading data from address      489:      0
# Reading data from address      490:      0
# Reading data from address      491:      0
# Reading data from address      492:      0
# Reading data from address      493:      0
# Reading data from address      494:      0
# Reading data from address      495:      0
#
# Results of lsb sum :
#
# Reading data from address      496:     16
# Reading data from address      497:     18
# Reading data from address      498:     20
# Reading data from address      499:     22
# Reading data from address      500:     24
# Reading data from address      501:     26
# Reading data from address      502:     28
# Reading data from address      503:     30
# Reading data from address      504:     32
# Reading data from address      505:     34
# Reading data from address      506:     36
# Reading data from address      507:     38
# Reading data from address      508:     40
# Reading data from address      509:     42
# Reading data from address      510:     44
# Reading data from address      511:     46
#
```

## نتیجه ضرب :

```
# Results of msb multiply :
#
# Reading data from address      240: 00000000000000000000000000000000
# Reading data from address      241: 00000000000000000000000000000000
# Reading data from address      242: 00000000000000000000000000000000
# Reading data from address      243: 00000000000000000000000000000000
# Reading data from address      244: 00000000000000000000000000000000
# Reading data from address      245: 00000000000000000000000000000000
# Reading data from address      246: 00000000000000000000000000000000
# Reading data from address      247: 00000000000000000000000000000000
# Reading data from address      248: 00000000000000000000000000000001
# Reading data from address      249: 00000000000000000000000000000100
# Reading data from address      250: 0000000000000000000000000000010000
# Reading data from address      251: 000000000000000000000000000001000000
# Reading data from address      252: 00000000000000000000000000000100000000
# Reading data from address      253: 0000000000000000000000000000010000000000
# Reading data from address      254: 000000000000000000000000000001000000000000
# Reading data from address      255: 00000000000000000000000000000100000000000000
#
# Results of lsb multiply :
#
# Reading data from address      256: 00000000000000000000000000000000
# Reading data from address      257: 00000000000000000000000000000000
# Reading data from address      258: 00000000000000000000000000000000
# Reading data from address      259: 00000000000000000000000000000000
# Reading data from address      260: 00000000000000000000000000000000
# Reading data from address      261: 00000000000000000000000000000000
# Reading data from address      262: 00000000000000000000000000000000
# Reading data from address      263: 00000000000000000000000000000000
# Reading data from address      264: 00000000000000000000000000000000
# Reading data from address      265: 00000000000000000000000000000000
# Reading data from address      266: 00000000000000000000000000000000
# Reading data from address      267: 00000000000000000000000000000000
# Reading data from address      268: 00000000000000000000000000000000
# Reading data from address      269: 00000000000000000000000000000000
# Reading data from address      270: 00000000000000000000000000000000
# Reading data from address      271: 00000000000000000000000000000000
```