COMP 8551 Advanced Games Programment Exam Help Techniques //powcoder.com Add WeChat powcoder

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Hardware and Assembly Language

Overview

Hardware concepts

Assignment Project Exam Help

 Definitions https://powcoder.com

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Design and architectures

Hardware Concepts

CPU, GPU, GPGPU, FPGA

- All integrated circuits
- FPGA: programment Project Exam Help
- CPU/GPU/GPU/Ipplucgelee.compurpose or specialized microprocessors Add WeChat powcoder
- CPU: most general, FPU/GPU: most specific
- Traditionally: processing (physics, AI, etc.) on CPU, rendering (geometry, shading, lighting, etc.) on GPU

Hardware Concepts

CPU, GPU, GPGPU, FPGA

- Game engines used to process some graphics (e.g., lighting)none OPD; diethown bloke away from that: very efficient, empty refrigerator is useless
- CPU still important: concurrent desks (firewall, networking, I/O, etc.), physics, AI very efficient, full refrigerator still means bigger refrigerator may be needed

Hardware Concepts

CPU, GPU, GPGPU, FPGA

- Over past decade, graphics and gaming drove
 Moore's Assignment Project Exam Help
- Demand for hetter GRUs increased dramatically: GPUs became arguably more powerful thander became arguably more
- GPGPUs attempt to combine both, but require radical change in how one approaches programming

RISC, CISC, SIMD

CISC

- Complex instruction set computer
- CPU designsstratement Project Exam Help
- Single instructions execute several low-level operations https://powcoder.com

http://en.wikipedia.org/wiki/Complex instruction set computer Add WeChat powcoder

RISC

- Reduced instruction set computing
- CPU design strategy
- Small set of simple instructions that can run very fast

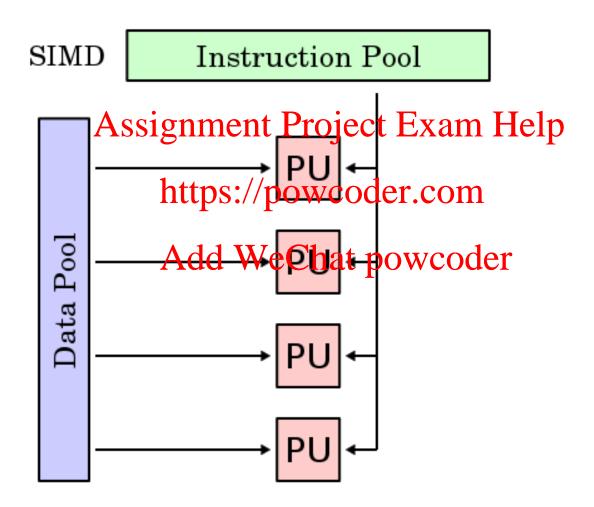
http://en.wikipedia.org/wiki/Reduced_instruction_set_computer

RISC, CISC, SIMD

SIMD

- Multiple processing elements that perform the same operation on the whiteless that perform the
- Examples: https://powcoder.com
 - Change image brightness: each pixel (RGB) read from memory, value added/subtracted/result written back to memory
 - Can process multiple pixels simultaneously: single instruction to fetch multiple memory locations
 - Value added to all locations referenced by instruction at the same time (high level of parallelism)

RISC, CISC, SIMD



Multiprocessor vs Multicore

- Traditionally, for true parallelism, needed multiple processors (CPUs)
- Allows each CPU to work independently Assignment Project Exam Help
 Data synchronization was always challenging
- https://powcoder.com
 Bottlenecks included bus speeds and lack of parallel code (ordgovote Compilers that balance loads)
- But, more CPUs always improves speed if they are utilized at all (even if not in the most efficient way): this is why multi-threading is so important!
- Main obstacle was cost

Multiprocessor vs Multicore

- Multicore means multiple processing units on a single chip
- In practice, lower the clock speed to save power Assignment Project Exam Help consumption and heat, but much lower cost, making it now afford pole for consumer-level products to have multiple "processors" Add WeChat powcoder.

 Turns out multicore is often more efficient (e.g.,
- Turns out multicore is often more efficient (e.g., share data bus)
- Newer game consoles (Xbox360, PS3) are multicore

Note: sometimes, bottleneck is not processing power, but bus speed/architecture and/or I/O

Instruction set

- Instructions: mnemonics (aka machine language or opcodes) used to identify commands to CPU Assignment Project Exam Help to carry out operations using transistors
- Native data types: Depende 56 System architecture bus widthat fowcoder
- Registers: on-chip memory reserved for operands of instructions
- Addressing modes: methods of accessing instructions and other memory (e.g., direct, indirect, offset, etc.)

Instruction set (cont'd)

- Interrupts and exceptions: mechanisms
 provided to allow change of regular sequential Assignment Project Exam Help flow of operations
- All of this is pared by the system clock and hardware logical WeChat powcoder
- Micro-architecture: microprocessor design techniques used to implement instruction set (different micro-architectures can share common instruction set).
- Micro-code: instructions broken down into suboperations that can be pipelined

Pipelining

- Instruction pipeline: overlapping execution of multiple instructions with Pharedeir cuitry (e.g., units for decoding used for one instruction while units for arithmetic or register fetch used for another).

Microcode

- Hardware instructions or data structures used to implement higher level machine code instructions
- Resides in specialized high-speed memory (not necessarily cadtteps://powcoder.com
- Provides layer of abstraction so instructions can be designed independently from underlying electronics
- Related terms: microprogramming, microprogram
- Can also be used for hardware emulation or support for legacy hardware without having to include old circuitry
- Sometimes used as synonym for firmware

Instruction set extensions

- MMX, SSE, SSE1-4, etc.
- With SIMD came various attempts to existing instruction sets
- They added https://powcoder.com
 - longer regis Acts (W.ge, Clast bit town Cocleit systems)
 - instructions to perform single operation on multiple memory locations simultaneously (vector operations)
 - more complex math operations at machine code level
 - DSP and thread management instructions
 - geometry instructions
 - complex integer arithmetic operations

CPU cache

- Cache: special, more expensive but much faster access memory Assignment Project Exam Help
- Used by CPU to reduce average time to access memory (which can be https://powive.dtepenting on the type of memory and bus architecture)
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 Stores copies of data from most frequently used
- Stores copies of data from most frequently used memory locations
- Various sophisticated heuristics and algorithms used to optimize cache performance (trade-off between keeping things around too long or not long enough)

CPU cache (cont'd)

- Instruction cache: fetching instructions stored in main memory Assignment Project Exam Help
- Data cache: transfer of data between main memory and internal registers://powcoder.com
- Translation lookaside buffer: virtual-physical address translation

Review

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Design and architectures

