University of Glasgow

Wednesday, 13 May 2015
2.00pm – 4.00pm

(Duration: 2 hours)

DEGREES OF MSc, MSci, MEng, BEng, BSc, MA and MA (Social Sciences)

Systems and Networks

Answer ALL 3 Questions

This examination paper is worth a total of 60 marks

INSTRUCTIONS TO INVIGILATORS

Please collect all exam question papers and exam answer scripts and retain for school to collect. Candidates must not remove exam question papers.

1. (a) What number does the codeword $FD represent in:

i. 8-bit unsigned code

ii. 8-bit two's complement code

Explain your reasoning in each case.

[4]

(b) Using a 32-bit binary word give the ranges of numbers that can be represented using: (a) an unsigned; and (b) a two's complement code. (You may express the answers in the form of powers of 2.)

[2]

(c) Explain how a 32-bit numeric codeword would be stored in memory in a Sigma16 system? How would it be stored in a 6811 system?

[3]

(d) A Sigma16 system has two arrays, X and Y, of 4 16-bit signed numbers in memory. Write an assembly language program to form a third array, Z, whose i^{th} element, z_i, is formed by multiplying the i^{th} elements of X and Y together, i.e. $z_i = x_i * y_i$

[6]

(e) With a view to maximising efficiency, modify your program in (d) to sum the elements of Z and put the result in a variable called SPRDT.

[5]

For reference, this is part of the instruction set of the Sigma16 CPU.

lea	Rd, x[Ra]	Rd:= x +Ra
load	Rd, x[Ra]	Rd:= mem[x+Ra]
store	Rd, x[Ra]	mem[x +Ra]:=Rd
add	Rd,Ra,Rb	Rd:= Ra+Rb
sub	Rd,Ra,Rb	Rd:= Ra-Rb
mul	Rd,Ra,Rb	Rd:= Ra*Rb
div	Rd,Ra,Rb	Rd:= Ra/Rb
cmplt	Rd,Ra,Rb	Rd:= Ra<Rb
cmpeq	Rd,Ra,Rb	Rd:= Ra=Rb
cmpgt	Rd,Ra,Rb	Rd:= Ra>Rb
jumpf	Rd, x[Ra]	If Rd=0 then PC:=x+Ra
jumpt	Rd, x[Ra]	If Rd<>0 then PC:=x+Ra
jal	Rd, x[Ra]	Rd:= pc, pc: =x +Ra
trap	Rd,Ra,Rb	PC:= interrupt handler
jump	x[Ra]	PC:= x +Ra

2. (a) In the memory hierarchy, explain how cache memory works. Clearly define the concepts of a cache miss, cache hit and replacement policy

[6]

(b) What does the following Sigma16 program do?

```
; Initialise registers

            LEA     R1,1[R0]        ; R1 = 1 (constant)
            LEA     R2,1[R0]        ; i = 1
            LOAD    R3,n[R0]        ; R3 = n
            LEA     R4,1[R0]        ; x = 1

; For loop follows

FORLOOP     CMPGT   R5,R2,R3        ; IF i>n
            JUMPT   R5,OUT[R0]      ; EXIT Loop
            MUL     R4,R4,R2        ; x = x*i
            ADD     R2,R2,R1        ; i = i + 1
            JUMP    FORLOOP[R0]     ; Loop again

; Exit Loop and store result.

OUT         STORE   R4,x[R0]        ; Store x
            TRAP    R0,R0,R0        ; Finish
; Data Area

n           DATA    5
x           DATA    0
```


[2]

(c) How many cycles are in the main loop?

[2]

(d) If a memory cycle takes 10ns, how long would this program take to execute?

[3]

(e) If a cache is introduced, how many hits will there be?

[2]

(f) If a cache cycle takes 1ns, how long would this program take to execute?

[2]

(g) Does it make sense to cache memory mapped I/O locations? Explain your answer.

[3]

3. (a) What is the difference between a circuit-switched and packet-switched network. Explain the role of the nodes in each case.

[4]

(b) Describe the layered structure of the Internet communications system, identifying the layers and their functions.

[8]

(c) In a packet-switched network packets occasionally arrive in the wrong order or are lost completely.

Explain how each of these problems might arise and how the communications system would fix them

[4]

(d) Explain how the problems discussed in (c) would impact the following user applications:

i. A file transfer application
ii. A music streaming application

[4]