



University
of Glasgow

Monday 9 May 2016

9:30 am – 11:30 am

(Duration: 2 hours)

DEGREES OF MSc, MSci, MEng, BEng, BSc, MA and MA (Social Sciences)

Systems and Networks (M)
Assignment Project Exam Help

<https://powcoder.com>
Answer ALL Questions

This examination paper is worth a total of 60 marks

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The use of a calculator is not permitted in this examination

INSTRUCTIONS TO INVIGILATORS

Please collect all exam question papers and exam answer scripts and retain for school to collect. Candidates must not remove exam question papers.

1. (a) In a 16-bit two's complement code what are the codewords for:

- i. 50
- ii. -15

Express your answers in hexadecimal.

[4]

(b) The current version of the Sigma16 processor does not have any equivalent of the Condition Code Register in the MC6811. What are the consequences of this?

[2]

(c) In the MC6811 the CCR has four status flags which are set by the ADD instructions: C (carry), V (two's complement overflow), Z(zero) and N(sign). If an ADD instruction is used to add the two 8-bit values, \$7F and \$80, which of these flags will be set following the operation? Explain your answer in each case.

[4]

(d) A Sigma16 system has two arrays, X and Y, of 4 16-bit signed numbers in memory. Write an assembly language program to swap the arrays, so that all elements of X end up in Y and vice versa.

[6]

(e) With a view to maximising efficiency, modify your program in (d) so that the *i*th elements of X and Y are only swapped if $x_i > y_i$.

[4]

For reference, this is part of the instruction set of the Sigma16 CPU:

lea	Rd, x[Ra]	Rd:= x +Ra
load	Rd, x[Ra]	Rd:= mem[x +Ra]
store	Rd, x[Ra]	mem[x +Ra]=Rd
add	Rd,Ra,Rb	Rd:= Ra+Rb
sub	Rd,Ra,Rb	Rd:= Ra-Rb
mul	Rd,Ra,Rb	Rd:= Ra*Rb
div	Rd,Ra,Rb	Rd:= Ra/Rb
cmplt	Rd,Ra,Rb	Rd:= Ra<Rb
cmpeq	Rd,Ra,Rb	Rd:= Ra=Rb
cmpgt	Rd,Ra,Rb	Rd:= Ra>Rb
jumpf	Rd, x[Ra]	If Rd=0 then PC:=x+Ra
jumpt	Rd, x[Ra]	If Rd<>0 then PC:=x+Ra
jal	Rd, x[Ra]	Rd:= pc, pc:=x +Ra
trap	Rd,Ra,Rb	PC:= interrupt handler
jump	x[Ra]	PC:= x +Ra

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- 2 (a) Explain what is meant by an *exception* and describe how such an event is handled by a typical operating system. [4]
- (b) Describe the following exceptions and outline briefly where they are used:
- i. Reset;
 - ii. Interrupt;
 - iii. Trap (Software Interrupt);
 - iv. Memory Fault.
- [10]
- (c) In the context of the MC6811 explain what will happen and why, if a programmer who has just written an interrupt routine fails to:
- i. Initialise the interrupt vector;
 - ii. Initialise the stack pointer.
- [6]
3. (a) In the Internet, explain why data is broken up into separate limited-size IP packets and why such packets are sometimes able to arrive in the wrong order at the destination. [6]
- (b) If two IP packets do arrive at their destination in the wrong order, discuss in detail how the destination should react. [6]
- (c) Another problem that may occur in IP transit is that packets could get destroyed. Give two reasons that might cause this? [4]
- (d) If a packet does get destroyed in transit what are the implications for the data transfer and how can the problem be rectified? [4]

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