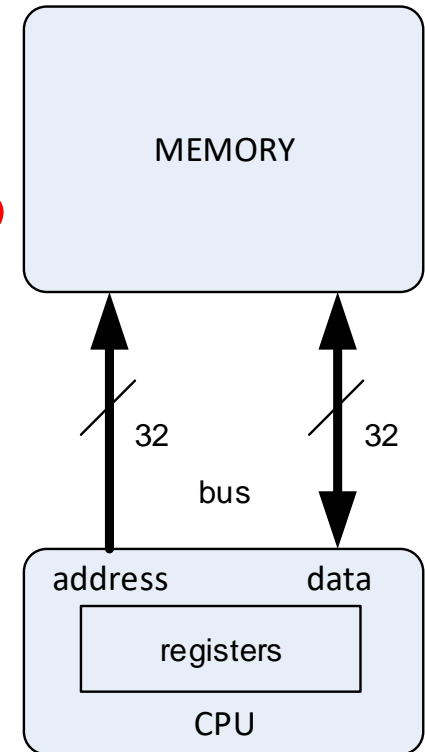


Simple Model of an ARM Microprocessor System

- comprises a central processing unit (CPU) and memory
- instructions and data are stored in memory
- the CPU reads instructions from memory (one after another) and executes them
- when the CPU executes an instruction
 - it performs operations between its registers OR
 - it reads data from memory and stores it in a register OR
 - it writes data from a register and stores it in memory



Memory

- memory comprises an array of memory locations
- each location stores 1 byte of data
- each location has a unique 32 bit address
0x00000000 to 0xFFFFFFFF
- the address space, 2^{32} bytes (4GB), is the amount of memory that can be physically attached to the CPU
- the byte stored at each location may be part of an instruction (as each instruction is 4 bytes) or data

0xFFFFFFFF

0xFFFFFFFFE

0xFFFFFFFFD

0xFFFFFFFFC

⋮

0x00000005

0x00000004

0x00000003

0x00000002

0x00000001

0x00000000

0xFF

0xEE

0xDD

0xCC

0x05

0x04

0x11

0x22

0x33

0x44

memory as an
array of BYTES

Memory

- often easier to view memory as an array of WORDs (32 bits) rather than an array of BYTES

- as each WORD location is aligned on a 4-byte boundary, the low order 2 bits of each address is 0

- making a comparison with the previous slide, the byte of data stored at memory location 0 is the least significant byte of the WORD stored in location 0

- this way of storing a WORD is termed LITTLE ENDIAN - the least significant byte is stored at the lowest address (the other way is BIG ENDIAN)

- ARM CPUs can be configured to be LITTLE ENDIAN or BIG ENDIAN (term from [Gulliver's Travels](#))

0xFFFFFFF8

0xFFFFFFF4

0x0000000C

0x00000008

0x00000004

0x00000000

0xCCDDEEFF

0xF8F8F8F8

⋮

0x876543210

0x8ABCDEFO

0x12345678

0x11223344

memory as an array of
WORDS

ARM CPU Registers

- the ARM CPU contains 16 x 32bit registers R0 to R15
- data can be read from memory and stored in a register
- data in a register can be written to memory
- arithmetic operations can be performed between the registers

ADD R0, R1, R2 ; R0 = R1 + R2

- R0 to R12 are considered general purpose registers
- R13, R14 and R15 are specialised
- registers are far quicker to access than memory

← 32 bits →

R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13 (SP)
R14 (LR)
R15 (PC)

stack pointer
link register
program counter

ARM CPU registers

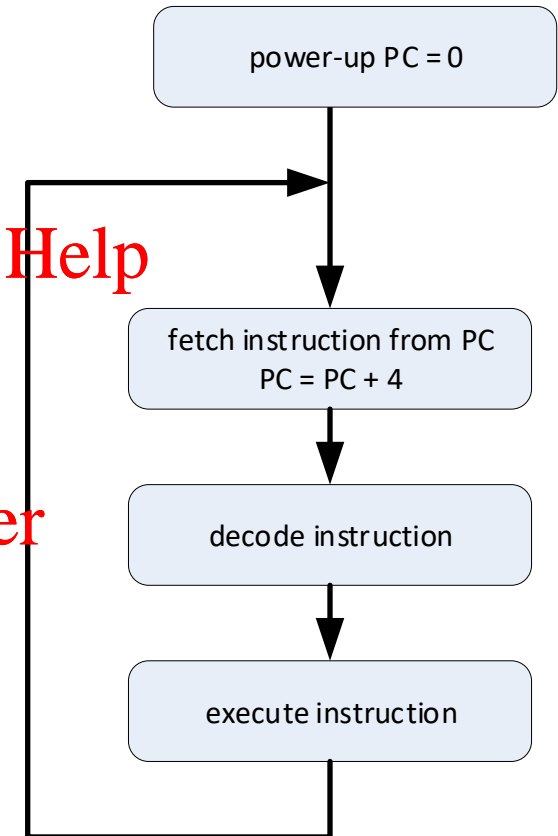
Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

Program Execution

- the CPU continuously fetches, decodes and executes instructions stored in memory at the address specified by the Program Counter (R15 or PC)
- on power-up, the PC is initialised to 0 so that the first instruction executed is a memory address 0
- after fetching each instruction, 4 is added to the PC so that the PC contains the address of the next sequential instruction (ALL instructions are 4 bytes)
- CPU keeps fetching, decoding and executing instructions until it is switched off



ARM data processing instructions

- consider the following ARM assembly language instructions

ADD - add

SUB - subtract

RSB - reverse subtract

MOV - move

MUL - multiply

Assignment Project Exam Help

<https://powcoder.com>

- three address instructions need to specify dst, src1 and src2 registers

ADD R0, R1, R2 ; R0 = R1 + R2 (R0:dst R1:src1 R2:src2)

SUB R0, R1, R2 ; R0 = R1 - R2

RSB R0, R1, R2 ; R0 = R2 - R1

MOV R0, R1 ; R0 = R1 (makes a copy of R1, src1 ignored)

MUL R0, R1, R2 ; R0 = R1 * R2 (NB: dst and src1 registers cannot be the same)

ADD R0, R0, R0 ; R0 = R0 + R0

Immediate src2 Operand

- the src2 operand can be a register OR a constant value
- there are limitations to the constant values that can “fit” in src2 field (these will be explained later)
- the fall-back position is to use a LDR instruction as it can load a register with any 32bit constant (also explained later)

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

ADD R0, R1, #1	; R0 = R1 + 1
ADD R2, R3, #0x0F	; R2 = R3 + 0x0F
SUB R1, R1, #2	; R1 = R1 - 2
MOV R0, #3	; R0 = 3

- note the # symbol – means an immediate constant
- MUL instruction is an exception, src2 cannot be an immediate constant

ARM LDR instruction

- LDR can be used to load an immediate (or constant) value into a register

```
LDR    R0, =0x1234    ; R0 = 0x1234
```

Assignment Project Exam Help

- = symbol for an immediate LDR operand, other instructions use the # symbol
- ; indicates the start of a comment

<https://powcoder.com>

Add WeChat powcoder

- LDR is not quite what it seems, explained in more detail later

ARM data processing example

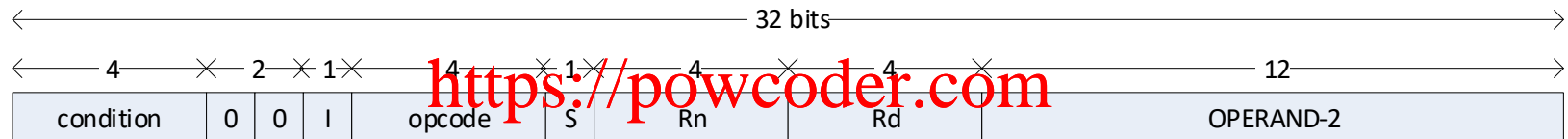
- if $x = 50$, compute $x^2 + 10x - 3$
- need to decide how best to use the registers
- compute result in R0
- use R1 to hold x
- use R2 as a temporary register for performing the computation

MOV R1, #50 ; R1 = $x = 50$
MUL R0, R1, R1 ; R0 = x^2
MOV R2, #10 ; R2 = 10
MUL R2, R1, R2 ; R2 = $10x$ (MUL R2, R2, R1 would not work)
ADD R0, R0, R2 ; R0 = $x^2 + 10x$
SUB R0, R0, #3 ; R0 = $x^2 + 10x - 3$

- work around limitations of MUL instruction
 - dst and src1 cannot be the same register
 - src2 cannot be an immediate constant

Assembly Language => Machine Code Example

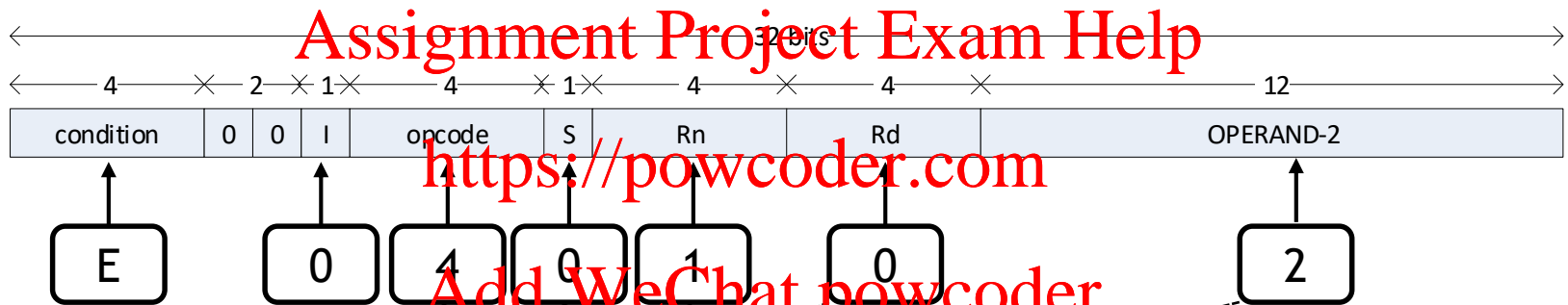
- assembly language instructions are converted into machine code by the assembler
- the CPU fetches, decodes and executes machine code instructions stored in memory
- each machine code instruction is 4 bytes (32 bits)
- the 32-bit machine code instruction encodes the operation (eg ADD) and operands



- 4 bit condition field (instruction can be conditionally executed, if value = 0xE instruction always executed)
- single I bit which determines how the OPERAND-2 field is interpreted
- 4 bit opcode field specifying the operation (16 possible operations)
- single S bit which determines if the instruction updates the condition codes
- 4 bit Rn field specifying src1 register (R0 .. R15)
- 4 bit Rd field specifying dst register (R0 .. R15)
- 12 bit src2 field (if I bit = 0 interpreted as a register or if I = 1 as an immediate value)
- fields will be described in more detail later in module

Assembly Language => Machine Code

- what is the machine code for ADD R0, R1, R2



- 1110 0000 1000 0001 0000 0000 0010₂
- 0xE0810002

- don't have to remember the machine code, but looking at how instructions are encoded can help with figuring out what the instruction can do

Writing Assembly Language Programs

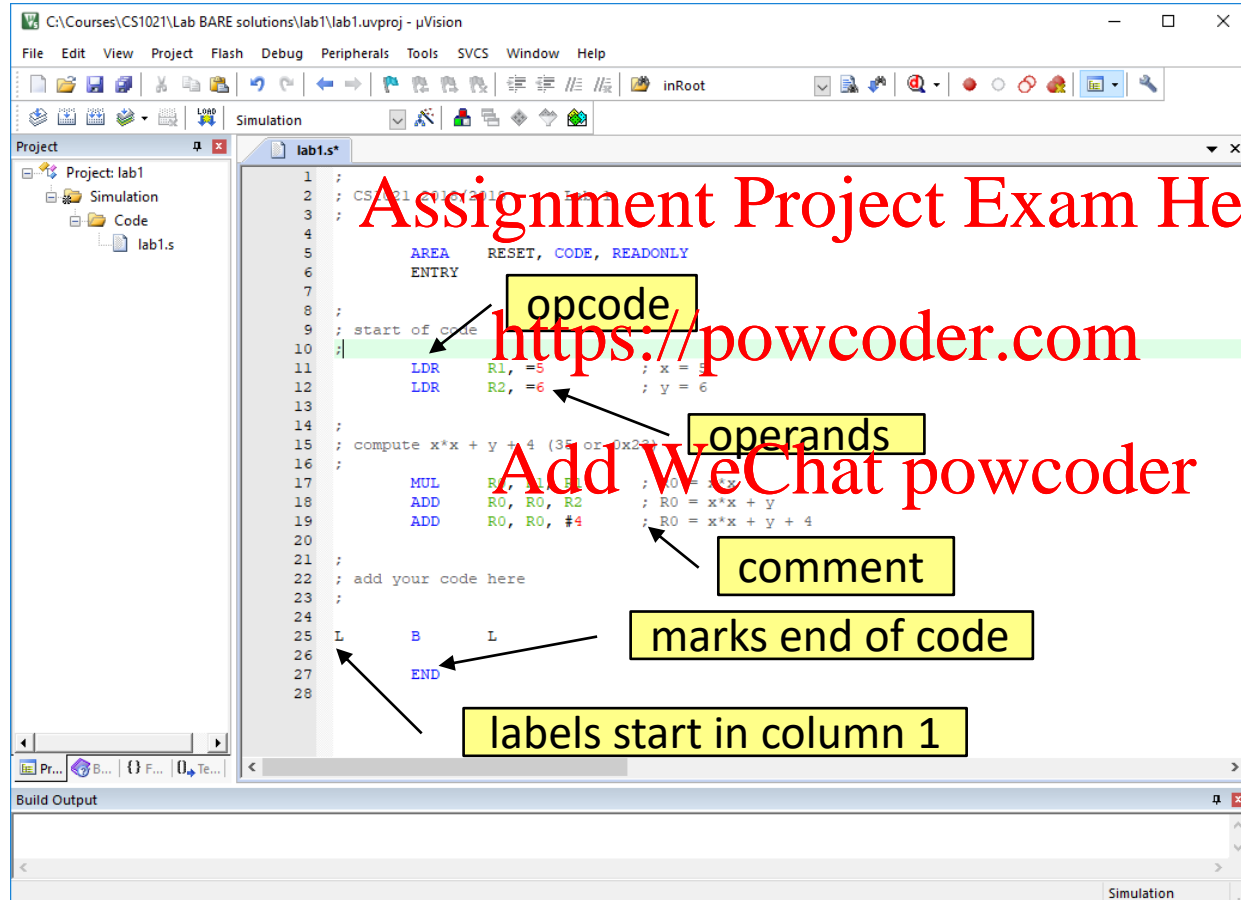
- writing programs using machine code is possible, but NOT practical
- much easier to write programs using assembly language
 - instructions are written using mnemonics (ADD instead of 0x04, R2 instead of 0x2, ...)
- assembly language translated into machine code by the assembler, stored in memory and then executed by CPU
- ARM assembly opcodes and operands NOT case sensitive
- one assembly language instruction per line
- labels start in column 1, otherwise leave blank except if a comment
- opcode followed by operands (separated by commas)
- comments start with a semicolon

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

Writing Assembly Language Programs



Executing/Debugging Assembly Language Programs

- build target [Project][Build Target]
- correct any assembly language errors and **REBUILD**

Assignment Project Exam Help

- run program [Debug][Start/Stop Debug Session]
- programs stops before first instruction executed

<https://powcoder.com>
Add WeChat powcoder

ARM ASSEMBLY LANGUAGE

Executing/Debugging Assembly Language Programs

address

machine code

registers

assembly language window

Breakpoint (click here to set or remove)

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

program stopped here

Registers

Register	Value
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x00000002
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC	0x00000000
Mode	Supervisor
States	0
Sec	0.00000000

Disassembly

```
0x00000000 E3A01005 MOV R1, #0x00000005
12: LDR R2, =6 ; y = 6
14: ; compute x*x + y + 4 (35 or 0x23)
15: MUL R0, R1, R1 ; R0 = x*x
17: ADD R0, R0, R2 ; R0 = x*x + y
18: ADD R0, R0, #4 ; R0 = x*x + y + 4
19: AREA RESET, CODE, READONLY
20: ENTRY
21: ; start of code
22: ; compute x*x + y + 4 (35 or 0x23)
23: MUL R0, R1, R1 ; R0 = x*x
24: ADD R0, R0, R2 ; R0 = x*x + y
25: ADD R0, R0, #4 ; R0 = x*x + y + 4
26: ; add your code here
27: ; infinite loop to end programme
28: L B L
```

Command

Running with Code Size Limit: 32K
Load "C:\Courses\CS1021\Lab BARE solutions\lab1\Objects\BS \lab1\lab1.s\25

ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE

Step out of the current function

Real-Time Agent: Target Reset

Simulation

t1: 0.00000000 sec

L11 C:1

CAP NUT

Executing/Debugging Assembly Language Programs

- press F11 or [Debug][Step] to single step one instruction at a time
- check instruction execution by examining register contents (remember register contents in hexadecimal)
- set breakpoints (red circle) by clicking on assembly language instruction (left hand side of assembly language window)
- press F5 or [Debug][Run] to run to next breakpoint (or forever if no breakpoint hit)
- check instruction execution by examining register contents
- break program in to sections and get each section working before moving on to next section
- [Debug][Start/Stop Debug Session] to exit debug session

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

Some Assembly Language Programming Guidelines

- comment every line of code with a helpful comment
- assume someone else may be reading your code

Assignment Project Exam Help

ADD R0, R0, R2 ; R0 = R0 + R2 - *poor*

ADD R0, R0, R2 <https://powcoder.com> - *better*

Add WeChat powcoder

- break your programs into small sections, separated by blank lines or comments
- try to keep your programs simple and easy to follow
- use TABs to align operator, operands and comments into columns
- tidy code = tidy mind
- remember to initialise values in registers and memory
- don't assume everything is set to zero when you start or switch on

Assembly Language Listing

```
ARM Macro Assembler Page 1
1 00000000
2 00000000
3 00000000
4 00000000
5 00000000 AREA RESET, CODE, READONLY
6 00000000 ENTRY
7 00000000
8 00000000 ; start of code
9 00000000
10 00000000
11 00000000 E3A01005 LDR R1, #5 ; x = 5
12 00000004 E3A02006 LDR R2, #6 ; y = 6
13 00000008
14 00000008 ;
15 00000008 ; compute x*x + y + 4
16 00000008
17 00000008 E0000191 MML R0, R1, R2, #0 ; R0 = x*x
18 0000000C E0800002 ADD R0, R0, R2 ; R0 = x*x + y
19 00000010 E2800004 ADD R0, R0, #4 ; R0 = x*x + y + 4
20 00000014
21 00000014 ;
22 00000014 ; add your code here
23 00000014 ;
24 00000014
25 00000014 EAF00000 L B L ; infinite loop to
; end programme

26 00000018
27 00000018 END
Command Line: --debug --xref --diag_suppress=9931 --apcs=interwork --depend=.\o
bjects\lab1.d -o-.\objects\lab1.o -IC:\Keil_v5\ARM\RV31\INC -IC:\Keil_v5\ARM\CMS
IS\Include -IC:\Keil_v5\ARM\INC\Philips --predefine=" EVAL SETA 1" --predefine
```

- code starts at 0x00000000
- code ends at 0x00000017
- ALL instructions start with 0xE... meaning that they are always executed

This week's Tutorial and Lab

- will put this week's lecture notes on CS1021 web site today
- look at the this week's notes before Thursday's tutorial
- lab1 this Friday - you'll write your first assembly language program
- will put the lab question on the CS1021 web site on Thursday, so take some time to look at it in advance so you know what you have to do

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder