Which of these expressions can bring to an overflow? Select all that apply. a + b, with a > 0 and b > 0

a + b, with a > 0 and b > 0

a + b, with a < 0 and b > 0

Assignment Project Exam Help

Flag this Questinttps://powcoder.com
Question 21 pts

If you have this code:

add \$a1, \$t1, \$zeko
addi \$a2, \$t2, 1 Add WeChat powcoder

jal Procedure

addi \$t1, \$v0, 1

Which instruction will be in the \$ra register after the jal instruction is executed? addi \$a2, \$t2, 1

add \$a1, \$t1, \$zero

jal Procedure

addi \$t1, \$v0, 1

#### Flag this Question

#### Question 31 pts

Immagine that you have a branch instruction with an offset equal to 1010(000000000010102), and the PC contains the address 3000010

## If the Arsisi gramentill Perojector Examin Help 30040

https://powcoder.com

Add WeChat powcoder

30014

#### Flag this Question

#### Question 41 pts

Which of these instructions could cause a Data Hazard? Select all that apply.

Remember: The instructions are intended "stand alone"; it's not a sequence of instructions from the same program.

sub

lw

add

jal

#### Flag this Question

#### **Question 51 pts**

Which Assignment of Project transame Helpat apply

sub

https://powcoder.com

lw

Add WeChat powcoder

beq

bne

#### Flag this Question

#### **Question 61 pts**

If you have a "lw" instruction, which will be the first pipeline register to contain the retrieved information?

ID/EX

IF/ID

EX/MEM

MEM/WB

#### Flag this Question

#### **Question 71 pts**

# Assignment Project Exam Help Do we have a Data Hazard in this situation?

https://powcoder.com

Add WeChat powcoder

EX/MEM.RegisterRd = \$t1 (address of register t1)

ID/EX.RegisterRd = \$t2 (address of register t2)

ID/EX.RegisterRt = \$t3 (address of register t3)

MEM/WB.RegisterRd = \$t1 (address of register t1) Yes

No

#### Flag this Question

#### **Question 81 pts**

Do we have a Data Hazard in this case?

EX/MEM.RegisterRd = ID/EX.RegisterRs

Yes Assignment Project Exam Help

https://powcoder.com

## Flag this Question dd WeChat powcoder

#### **Question 91 pts**

For a 2-way set associative cache with a 32-bit address, the following bits of the address are used to access the cache:

Tag: 31-10

Index: 9-5

Block Offset: 4-0

What is the block size (in words)?

2

16

4

8

## Assignment Project Exam Help

Plag this Question https://powcoder.com

Add WeChat powcoder
If a 16-way set-associative cache has 32 bit words, 2 words per block and

If a 16-way set-associative cache has 32 bit words, 2 words per block and 8192 sets, how big is the cache in bytes? 524,288 (2^19)

1,048,576 (2^20)

262,144 (2^18)

2,097,152 (2^21)

Flag this Question

**Question 111 pts** 

A 256kiB (2^18 bytes) cache has a block size of 32 bytes and is 32-way set-associative.

How many bits of a 32-bit address will be in the Tag, Index, and Bock Offset?

Tag: 19; Index: 8; Offset: 5

Tag: 14; Index: 13; Offset: 5

Tag: 18; Index: 9; Offset: 5

Tag: 19 Index: 9: Offset: 4nt Project Exam Help

Flag this Questibittps://powcoder.com

**Question 121 pts** 

Add WeChat powcoder

For a 2-way set associative cache, the following number of bits for each field of the 32-bit address are used to access the cache:

Tag: 17 bits

Index: 9 bits

Block Offset: 6 bits

What is the block size (in words)?
8 words
4 words
16 words

# ASSIGnment Project Exam Help Question 130 pts

https://powcoder.com
For a 4-way set associative cache, the following number of bits for each field of the 32-bit address are used to access the cache:

## Add WeChat powcoder

Tag: 17 bits

Index: 8 bits

Block Offset: 7 bits

How many sets are present in this cache? 256

128

64

#### Flag this Question

#### **Question 141 pts**

A 16kiB (214 bytes) cache has a block size of 8 bytes and is 2-way set-associative.

## Assignment Project Exam Help

How many bits of a 32-bit address will be in the Tag, Index, and Bock Offset? Tag: 20; Index: powcoder.com

Tag: 19; Index: A; add We Chat powcoder

Tag: 18; Index: 10; Block Offset: 4

Tag: 18; Index: 11; Block Offset: 3

#### Flag this Question

#### Question 151 pts

Given a 2-way set associative cache with this configuration:

Index: 10 bits

Block Offset: 6 bits

- a. How many words are in a block?
- b. How many bytes of data does this cache hold?
- a) 16 words per block; b) 65536 bytes (2^16)
- a) 8 words per block; a) 65536 bytes (2\.0016) Assignment Project Exam Help
- a) 16 words per block; b) 131072 bytes (2^17)

https://powcoder.com

a) 16 words per block; b) 32768 bytes (2^15)

## Add WeChat powcoder

Flag this Question

#### **Question 161 pts**

If you have this list of actual prediction from the same branch instruction, that is, the actual outcome of the branch instruction:

Т

Т

Т

NT

Т

NT

## Assignment Project Exam Help

# https://powcoder.com Add WeChat powcoder

Where T is for Taken, and NT for Not Taken.

What is the prediction accuracy using 3-bit Dynamic Branch Prediction starting from NT (100)?

Key:

000 - Taken

001 - Taken

010 - Taken	
011 - Taken	
100 - Not Ta	aken
101 - Not Ta	aken
110 - Not Ta	
	signment Project Exam Help
111 - Not Ta	aken
	https://powcoder.com
3/8	Add WeChat powcoder
4/8	
5/8	
2/8	
6/8	