

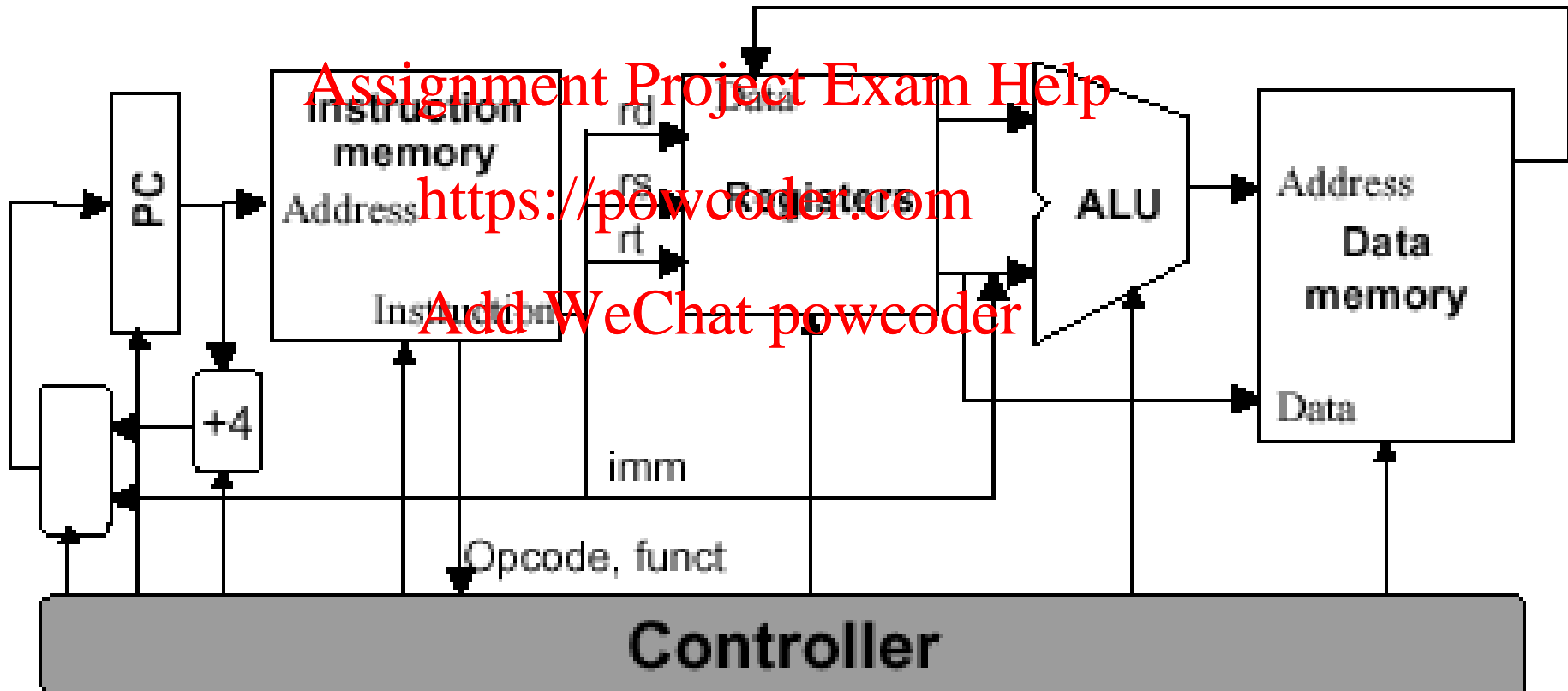
# ISA Hardware Diagrams

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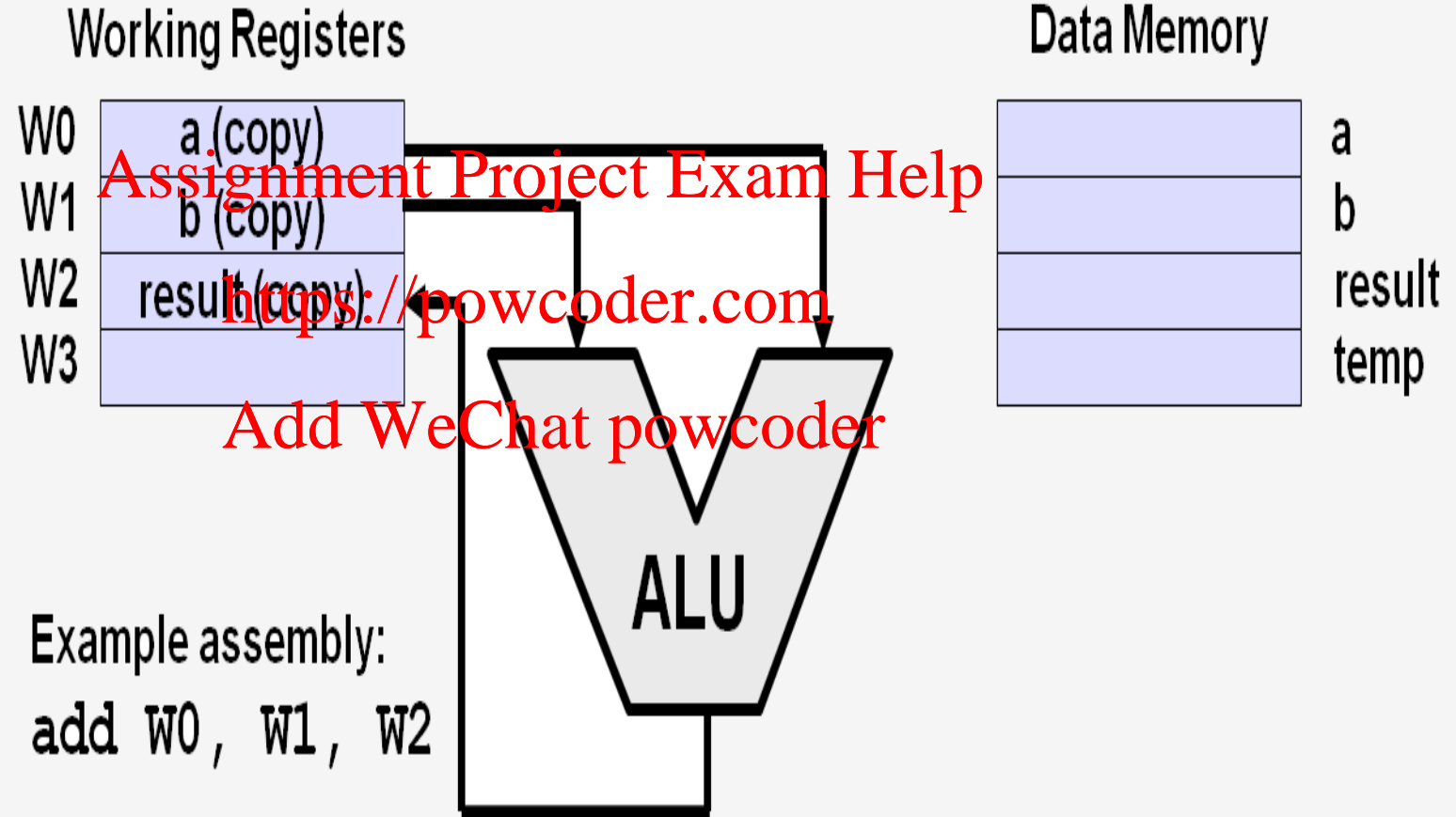
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# Load-Store = Reg-Reg (MIPS, ARM)



## 16-bit ALU Data Path (Register-Register Operation)



# Accumulator w/ DMA

Store:

Copy AC -> Mem

Load:

Mem -> ALU

AC = Accumulator

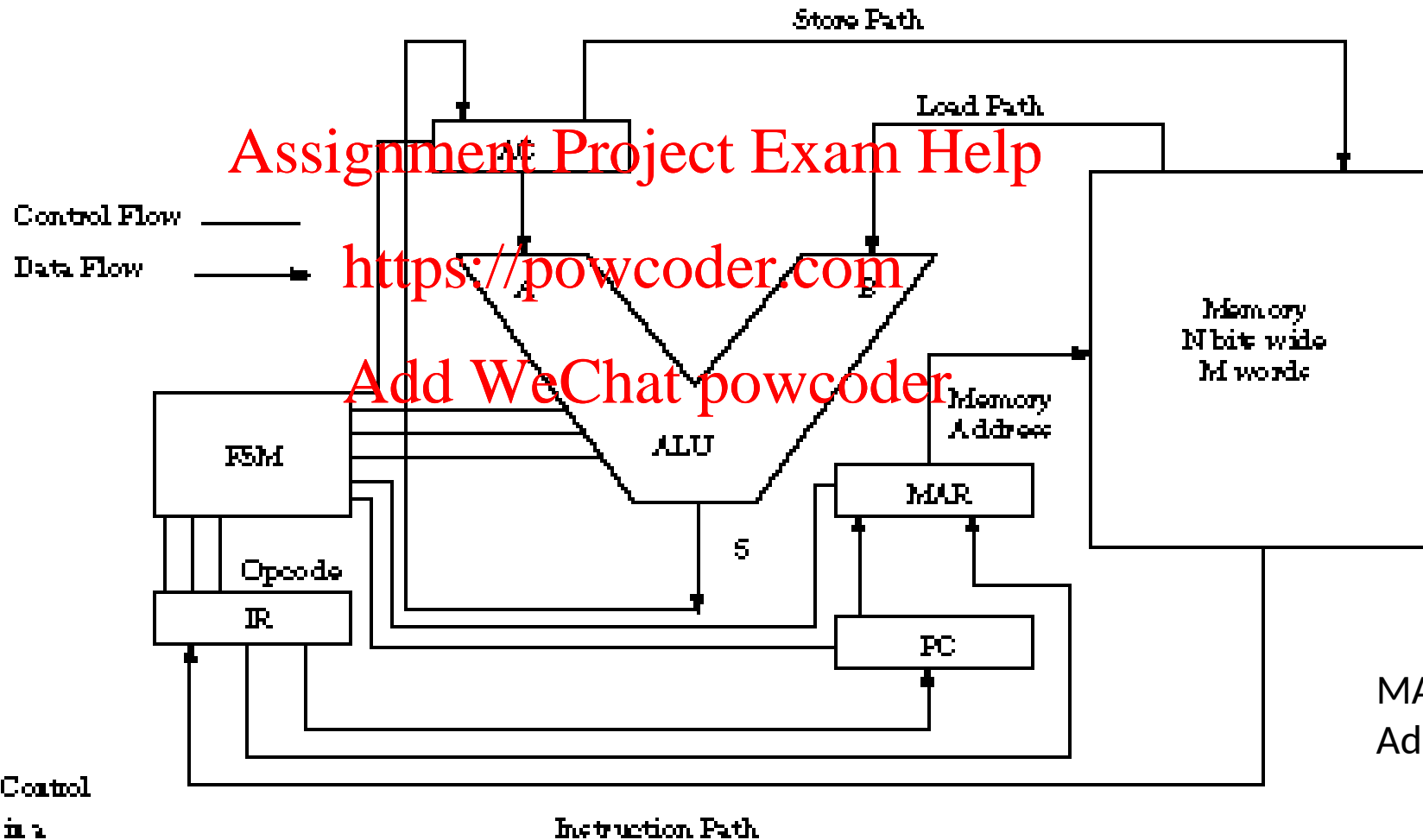
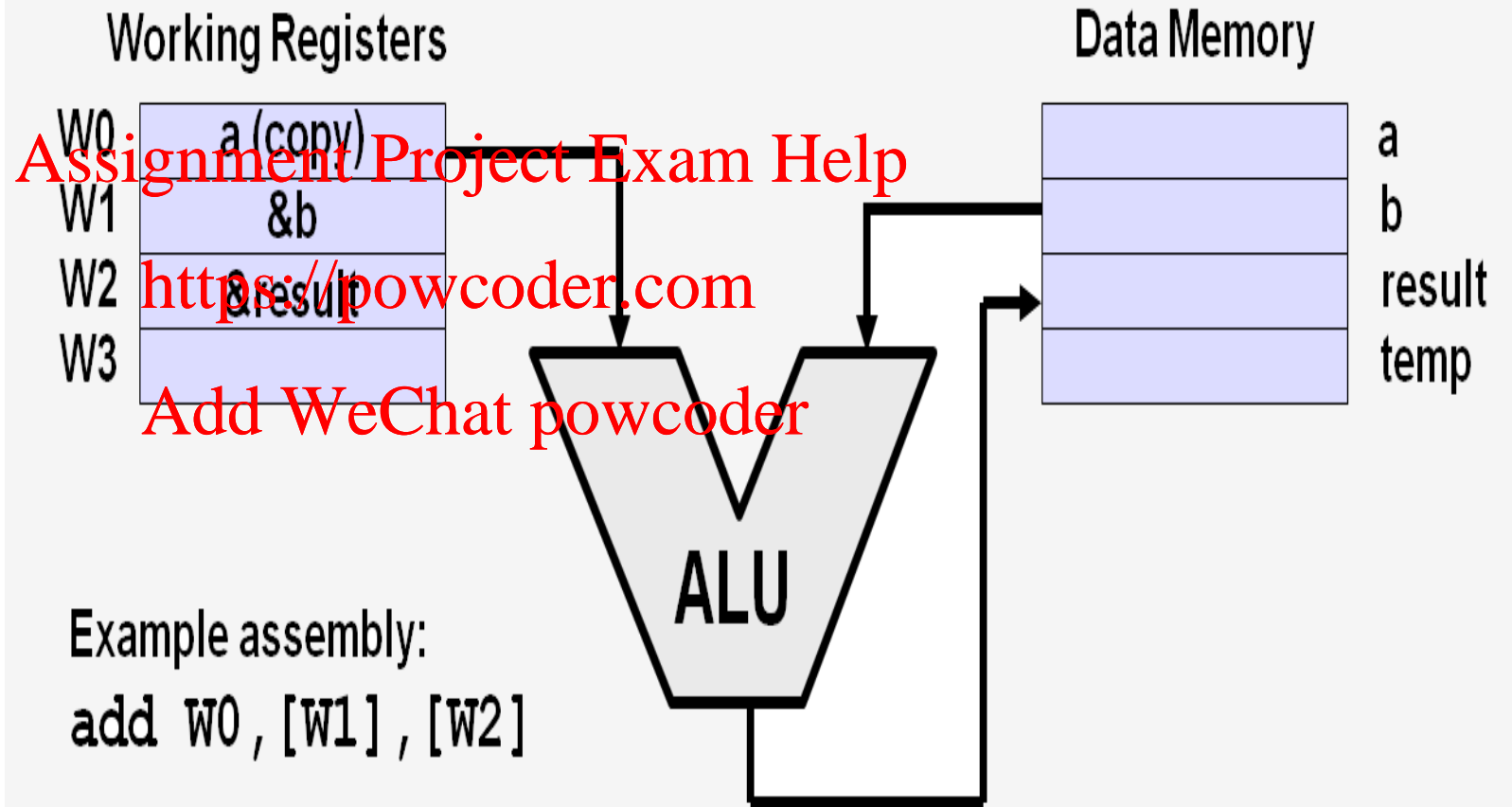


Figure 114 Control and data flows in a

MAR = Memory Address Register

# 16-bit ALU Data Path (Register-Memory Operation)



# Comparing the Number of Instructions

Code sequence for  $C = A + B$  for four classes of instruction sets:

<u>Stack</u>	<u>Accumulator</u>	<u>GP Register</u> (register-memory)	<u>GP Register</u> (load-store)
Push A	Load A	ADD C, A, B	Load R1,A
Push B	Add B		Load R2,B
Add	Store C		Add R3,R1,R2
Pop C			Store C,R3

- Accumulator: "B" comes from reg\_file or data\_mem
- Loads copy mem->acc; stores copy acc->mem
- "load-store" = ARM/MIPS-like

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