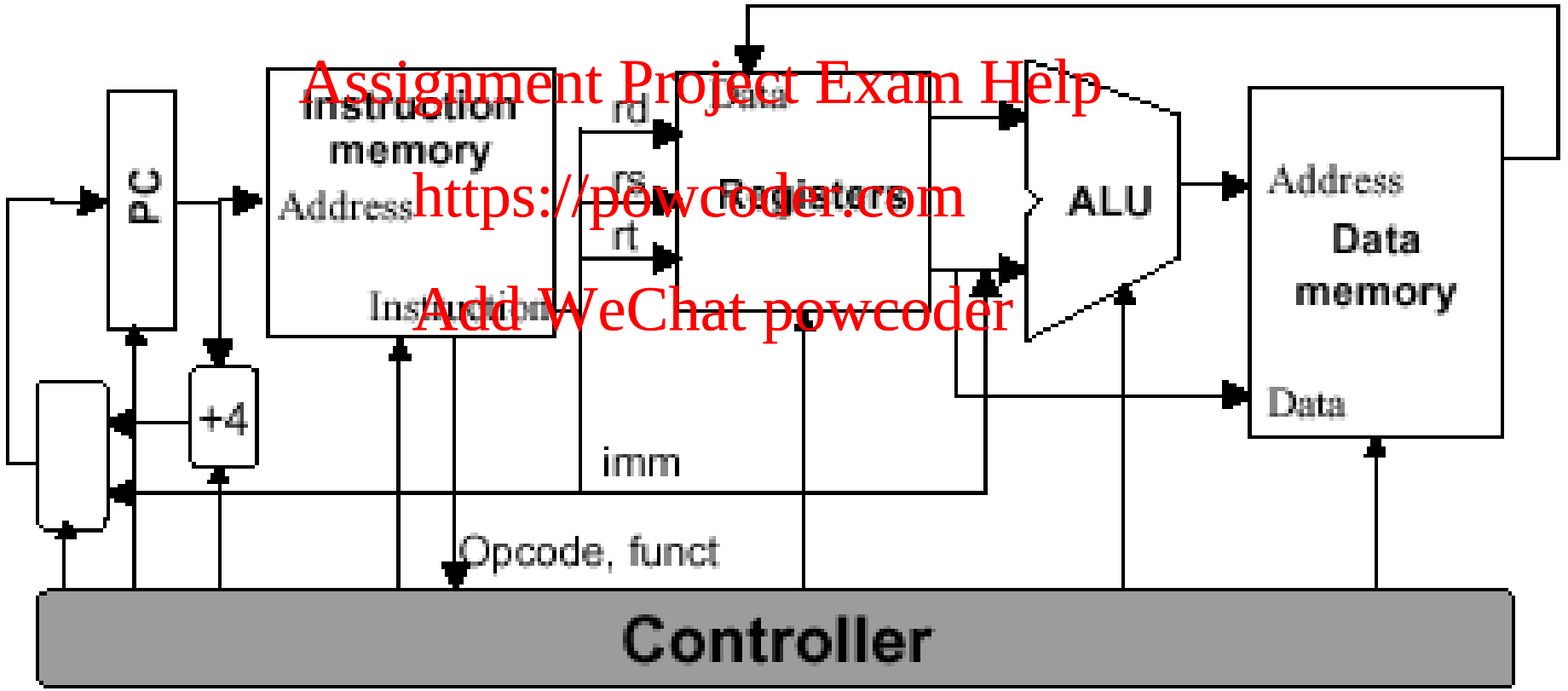
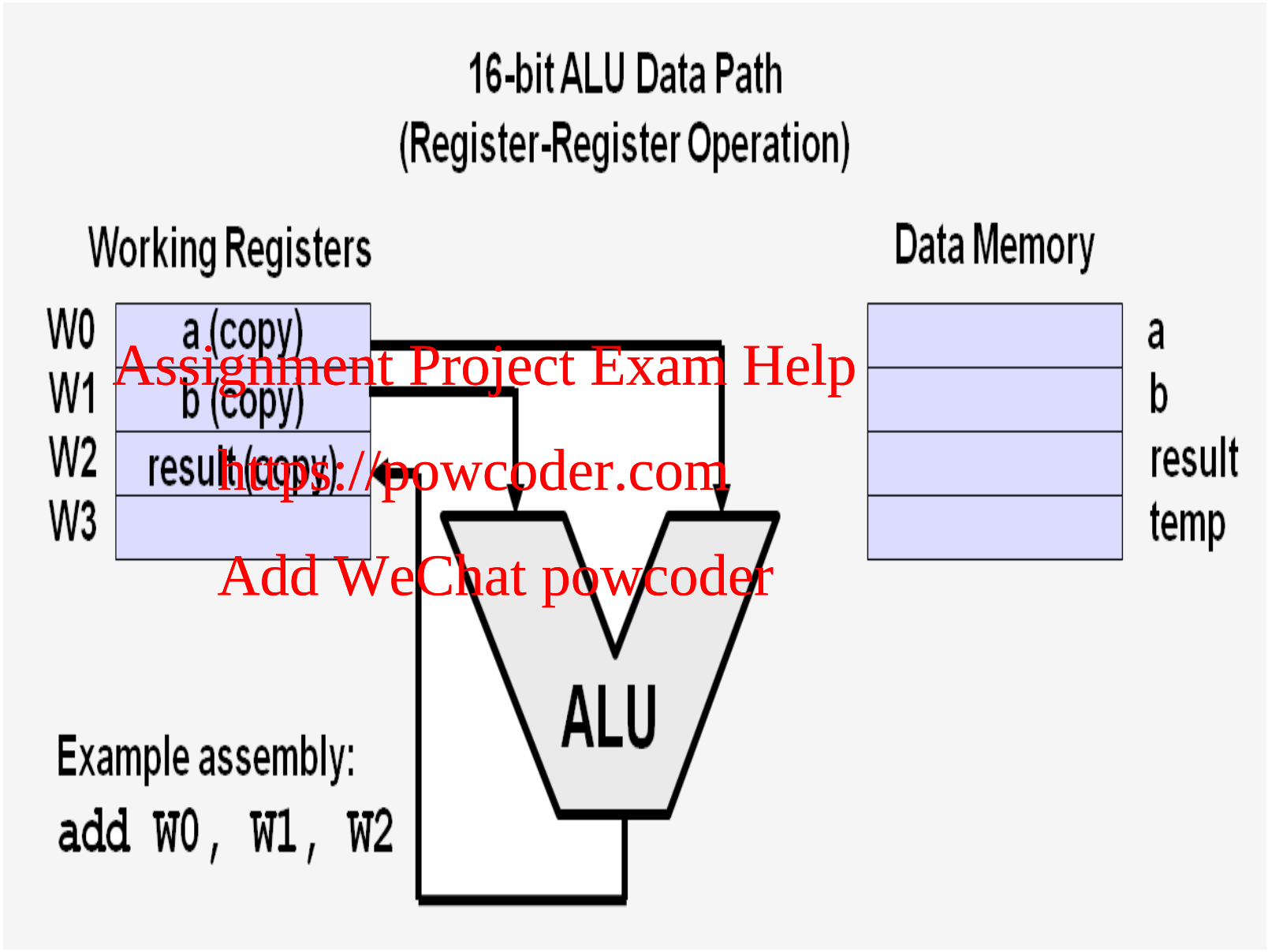
ISA Hardware Diagrams

Load-Store = Reg-Reg (MIPS, ARM)





Accumulator w/ DMA

Store:
Copy AC -> Mem
Load:
Mem -> ALU

AC = Accumulator

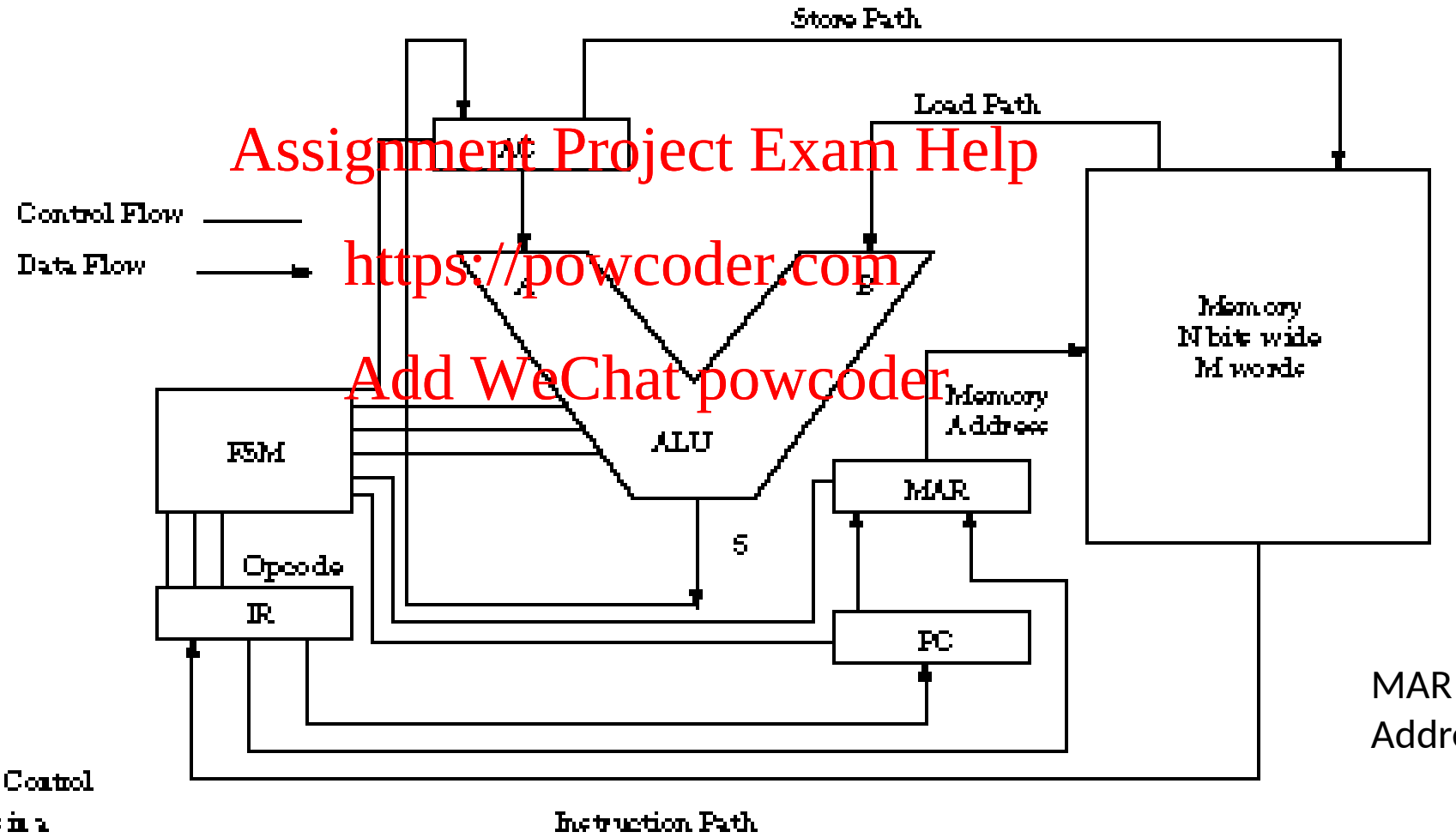
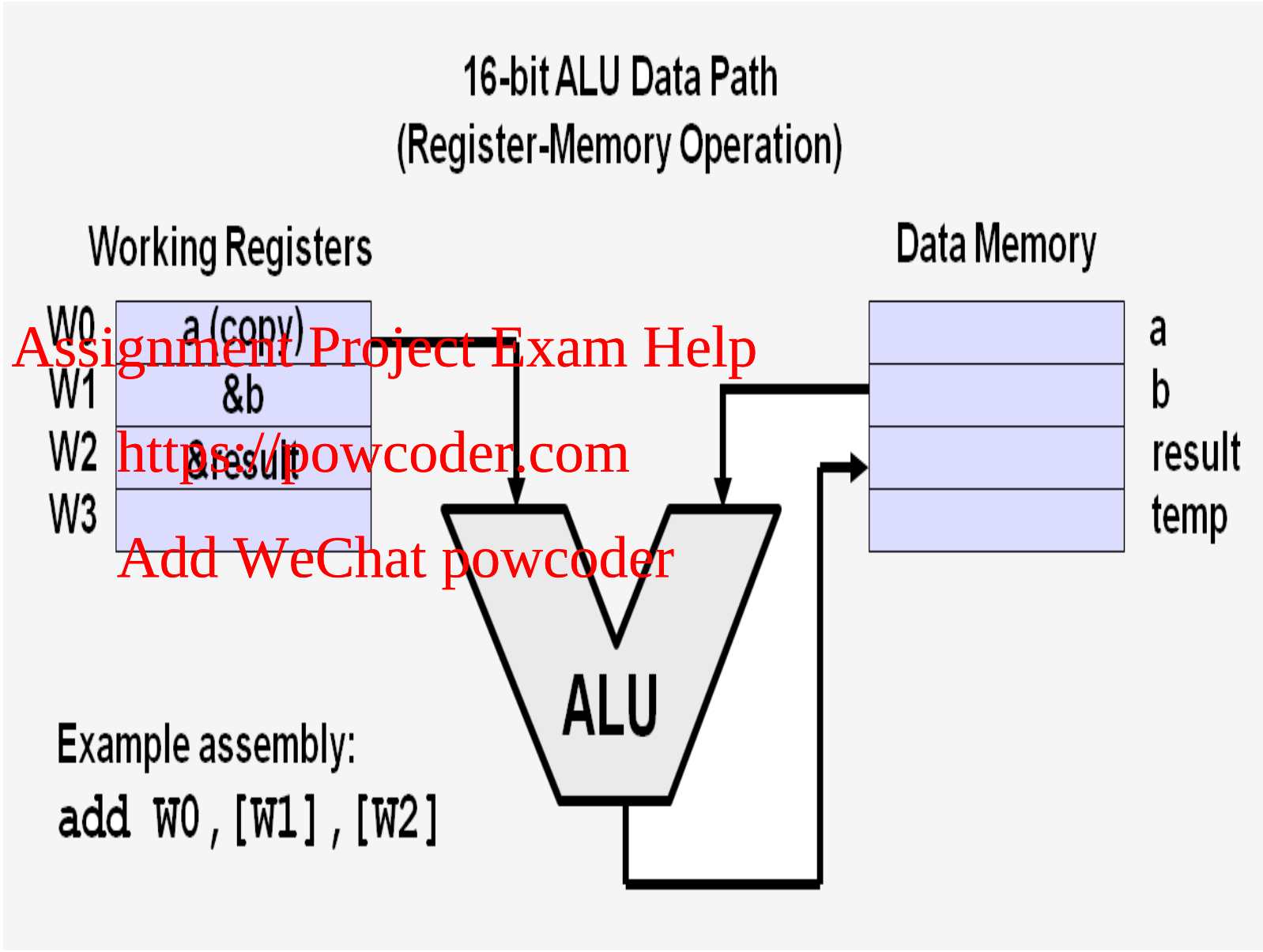


Figure 11.4 Control and data flows in a

MAR = Memory Address Register



Comparing the Number of Instructions

Code sequence for C = A + B for four classes of instruction sets:

Stack	Accumulator	GP Register (register-memory)	GP Register (load-store)
Push A	**Load A**	**ADD C, A, B**	**Load R1,A**
Push B	**Add B**		**Load R2,B**
Add	**Store C**		**Add R3,R1,R2**
Pop C			**Store C,R3**

- Accumulator: "B" comes from reg_file or data_mem
- Loads copy mem->acc; stores copy acc->mem
- "load-store" = ARM/MIPS-like