

# Assignment10 - Due: Friday, April 9th, 5pm

CSE/EEE230 Assignment10

Due: Friday, April 9th, 5pm

***Important: This is an individual assignment. Please do not collaborate. Do not share your solution with anyone.***

***Make sure to follow the academic integrity policies.***

It must be submitted on-line (course website)

Copying any part of this assignment, and providing them to another person or posting them on the Internet without a permission of the instructor will be a violation of its copyright.

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The document needs to be 100% typed (no hand written answers) If it is not typed, it will be zero on the assignment. (this is to check any academic integrity violation).

Add WeChat powcoder  
Upload your file containing your solution to the course website by the assignment deadline. PDF, word (.doc, docx), and power point (.ppt, pptx) files are accepted.

20 points total (This assignment will be counted towards your grade).

No late assignment will be accepted

## Assignment Description:

1. (6 pts)

a).For the following MIPS assembly code to be executed using the pipelined datapath, identify all of the data dependencies (which register in which instruction needs to read the result register value from which another instruction that is writing it?) and enumerate them (give data dependencies numbers as 1,2, ...).

b).Which dependencies are data hazards that will be resolved via forwarding and without a stall (you can specify the number(s) from

the part a)?

c). Which dependencies are data hazards that will cause a stall (you can specify the number(s) from the part a)?

```
add $t7, $t2, $t5  
lw $t6, 16($t7)  
sub $t4, $t6, $t5  
add $t3, $t1, $t7  
lw $t9, 8($t3)  
add $t3, $t9, $t8  
sub $t5, $t8, $t9
```

2. (6 pts) Consider executing the following code on the pipelined datapath that we discussed in class.

a). During the 5th cycle, which registers are being read and which register(s) will be written (using the register file)?

```
add $t1, $t3, $t2  
sub $t6, $t7, $t3  
sub $t9, $t8, $t7  
add $t8, $t5, $t9  
add $t5, $t6, $t5
```

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b). Explain what the forwarding unit is doing during the 5th cycle of execution. Which registers are being compared? List all pairs of registers that are compared during the 5th cycle for the forwarding unit. (First, you need to determine which instruction's values are in the EX/MEM, which instruction's values are in the MEM/WB register, and which instruction's values are read from the ID/EX register during the 5th cycle. Then check the conditions for forwarding.)

c). Explain what the hazard detection unit is doing during the 5th cycle of execution. Which registers are being compared? List all pairs of registers that are compared during the 5th cycle for the hazard detection unit. (You need to determine which instruction's values are in the IF/ID and which instruction's values are in the ID/EX register during the 5th cycle. Then check the conditions for the hazard detection.)

3. (4 pts) Assume that you have a direct-mapped cache with 16 one-word blocks that is initially empty, and that you will be given a series

of word address references in the following order. Label each reference as a hit or a miss and show the content of the cache in each step.

a). word address 70

Hit or Miss?

What is the cache content at this point?

Block number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Address																

b). word address 42 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Address																

c). word address 86 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Address																

d). word address 70 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Address																

Address														
---------	--	--	--	--	--	--	--	--	--	--	--	--	--	--

e). word address 42 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Address																

f). word address 28 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Address																

g). word address 42 (continuing from the previous step)

Add WeChat powcoder

Hit or Miss?

What is the cache content at this point?

Block number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Address																

h). word address 87 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Address																

4. (4pts) Assume that you have a direct-mapped cache with four-word blocks and a total size of 16 words that is initially empty, and that you will be given a series of word address references in the following order. Label each reference as a hit or a miss and show the content of the cache in each step.

a). word address 61

Hit or Miss?

What is the cache content at this point?

Block number	0 (00)	1 (01)	2 (10)	3 (11)
Address				

b). word address 39 (continuing from the previous step)

Hit or Miss? **Assignment Project Exam Help**

What is the cache content at this point?

Block number	0 (00)	1 (01)	2 (10)	3 (11)
Address		Add WeChat powcoder		

c). word address 63 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0 (00)	1 (01)	2 (10)	3 (11)
Address				

d). word address 14 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0 (00)	1 (01)	2 (10)	3 (11)

Address											
---------	--	--	--	--	--	--	--	--	--	--	--

e). word address 38 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0 (00)	1 (01)	2 (10)	3 (11)
Address				

f). word address 60 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0 (00)	1 (01)	2 (10)	3 (11)
Address				

g). word address 48 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0 (00)	1 (01)	2 (10)	3 (11)
Address				

h). word address 15 (continuing from the previous step)

Hit or Miss?

What is the cache content at this point?

Block number	0 (00)	1 (01)	2 (10)	3 (11)
Address				

**What to turn in:**

-Upload your file containing your solution to the course website by the assignment deadline. PDF, word (.doc, docx), and power point (.ppt, pptx) files are accepted. If you want to use other type of files, please check with the instructor. Make sure that your files have your name and email address.

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