Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
Ollscoil Átha Cliath | The University of Dublin

Faculty of Engineering, Mathematics and Science

School of Computer Science & Statistics

Integrated Computer Science Programme
Year 2

Michaelmas Term 2020

CSU22022 – Computer Architecture I

24 August 2020 at 09.00 - 25 August 2020 at 09.00

24-hour take-home exam

Prof. Michael Manzke

Answer Question 1 and 2. Please confirm in you answer that this is your own work and that you have not collaborated with other students.

Students who are registered with Disability Services and who are entitled to extra time in examinations will be granted 10 additional minutes per hour (i.e. a 28 hour period in which to complete the 24-hour take home exam).

Figure 1 depicts the processor we designed. You will need this diagram for all the questions.

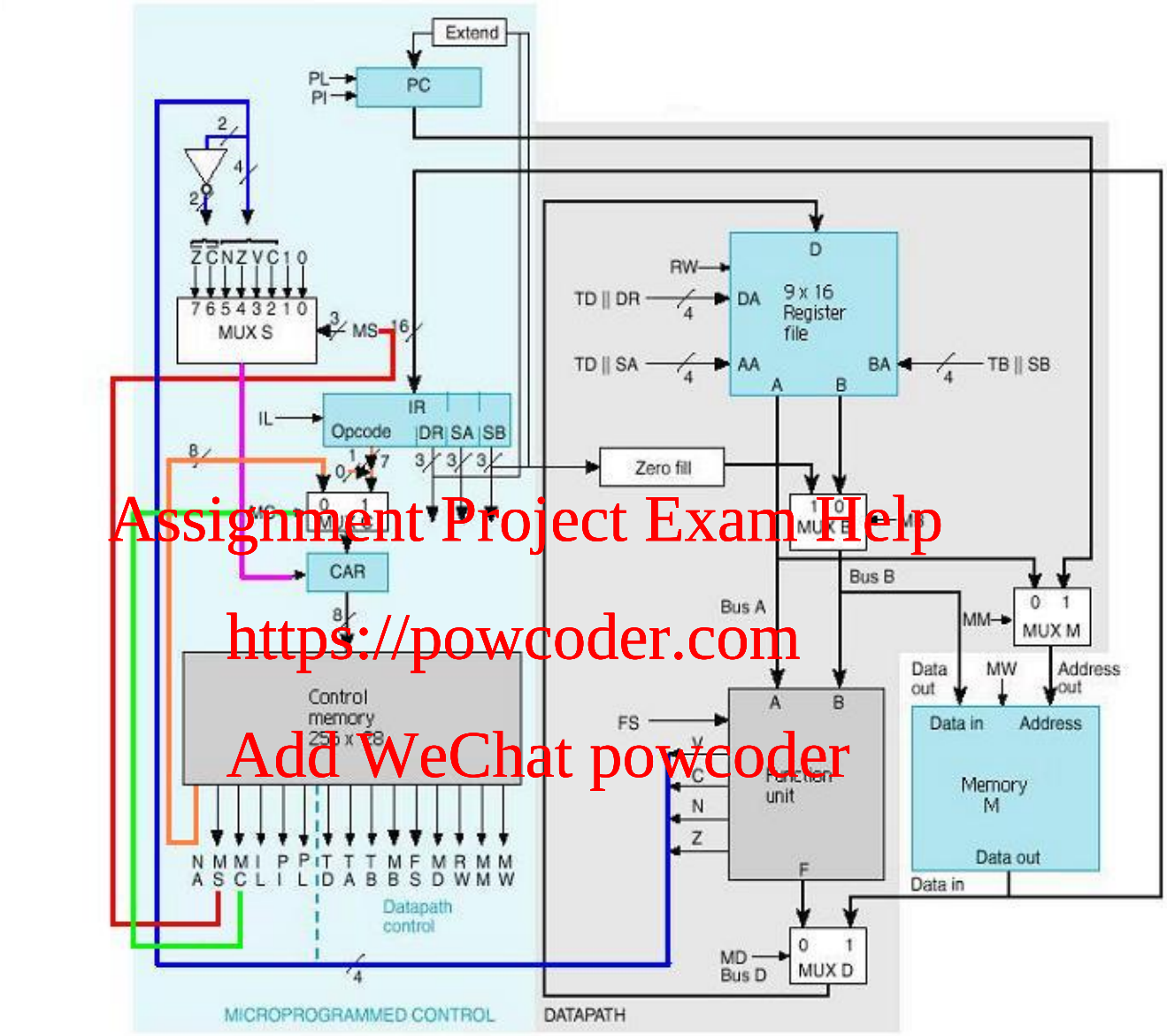


Figure 1 Processor block diagram

Figure 2 shows various instruction formats. These 16bit instructions (machine-code) are stored in the **Memory M** (see Figure 1) at particular addresses. The **PC** (Program Counter, see Figure 1) should point to the next to be executed instruction in **Memory M**. You require this information to program the **machine-code** in **Memory M** (see Figure 1).

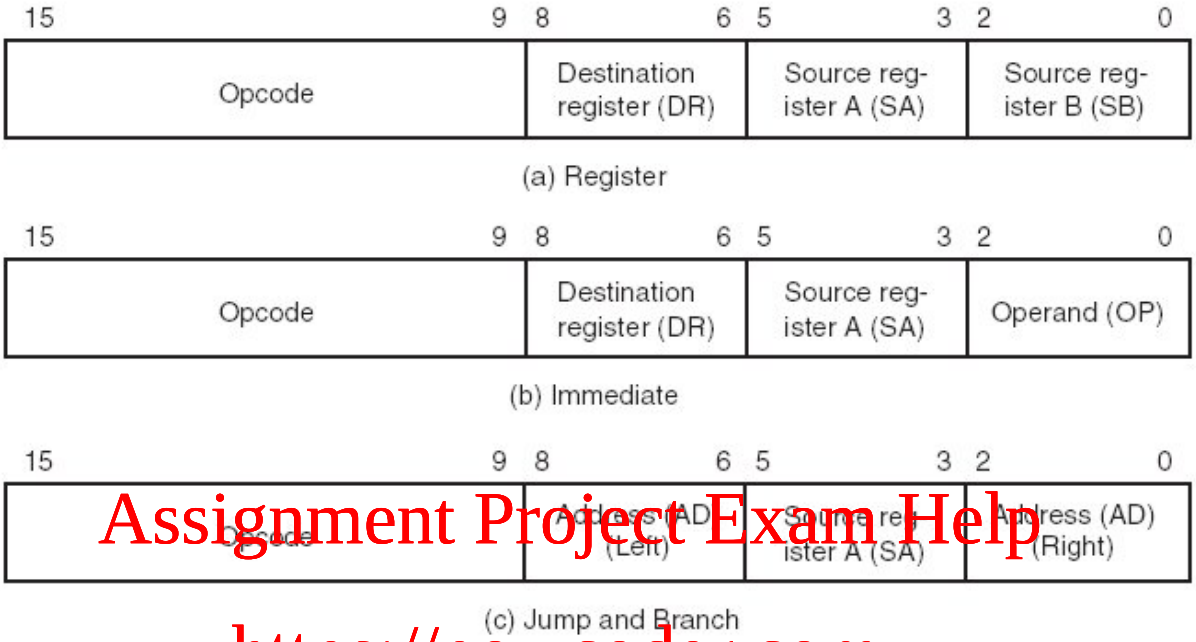


Figure 2

Figure 3 provides you with the binary code for all the operations of the **Function Unit** and other switches (see Figure 1). You need this information to program the **micro-code** in the **Control Memory** (see Figure 1).

TD	TA	TB	MB		FS		MD	RW	MM	MW	
Select	Select	Select	Select	Code	Function	Code	Select	Function	Select	Function	Code
R[DR]	R[SA]	R[SB]	Register	0	$F = A$	00000	FnUt	No write (NW)	Address	No write (NW)	0
$R8$	$R8$	$R8$	Constant	1	$F = A + 1$	00001	Data In	Write (WR)	PC	Write (WR)	1
					$F = A + B$	00010					
					$F = A + B + 1$	00011					
					$F = A + \overline{B}$	00100					
					$F = A + \overline{B} + 1$	00101					
					$F = A - 1$	00110					
					$F = A$	00111					
					$F = A \wedge B$	01000					
					$F = A \vee B$	01010					
					$F = A \oplus B$	01100					
					$F = \overline{A}$	01110					
					$F = B$	10000					
					$F = \text{sr } B$	10100					
					$F = \text{sl } B$	11000					

Figure 3

Figure 4 depicts the layout of all the memory locations in the in the **Control Memory** (see Figure 1). You need this information to program the micro-code in the **Control Memory** (see Figure 1). Figure 3 provides with all the information for programming bit 0 to 12. These bits determine the operations of the **datapath**. Bit 13 to 27 are needed for the sequencing of the **micro operations** and other operations in the processor's control.

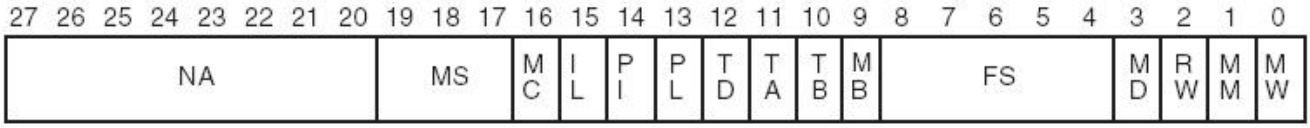
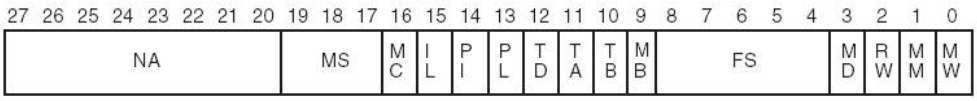


Figure 4

1. **Question**, please provide an algorithmic state machine chart for the implementation of the following **machine-code instructions**: ***IF***(Instruction Fetch), ***ADI***, ***LD***, ***ST***, ***INC***, ***NOT***, and ***ADD***. Please provide **micro-code** at the correct memory location in the **Control Memory** and **machine-code instructions** at the correct memory location in the **Memory M** that will use the **micro-code**. Please see below for the correct layout of you answer.

Your answer must provide **micro-code** for the **Control Memory** that implements your **algorithmic state machine chart.** The **micro-code** should have the following format for every memory address in the **Control Memory** that implements your **algorithmic state machine**.

For example:

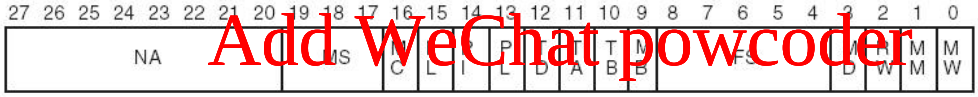


ADI

a) Control Memory Address

b) Binary code for bits 0 to 27

c) Providing written reasons for selecting these binary values for NA, MS, MC, IL, PI, PL, TD, TA, TB, MB, FS, MD, RW, MM, and MW.



LD

a) Control Memory Address

b) Binary code for bits 0 to 27

c) Providing written reasons for selecting these binary values for NA, MS, MC, IL, PI, PL, TD, TA, TB, MB, FS, MD, RW, MM, and MW.

… continue for all states in your algorithmic state machine.

[40 marks]

Your solution must also provide **machine-code instructions** at the correct memory location in the **Memory M**. The **machine-code instructions** should have the following format. You should execute the ***machine-code instructions*** in the following order ***LD***, ***NOT***, ***ADD***, ***INC***, ***ADI***, and ***ST***. Your first machine-code instructions (***LD***) should be at address 0000 0000 0000 0101

For example:

15 Opcode 9	8 6	5 3	2 0

LD

a) Memory M Address

b) Binary code for bits 0 to 15

c) Providing written reasons for selecting these binary values for the Opcode 15 to 9, 8 to 6, 5 to 3, and 2 to 0.

15 Opcode 9	8 6	5 3	2 0

INC

a) Memory M Address

b) Binary code for bits 0 to 15

c) Providing written reasons for selecting these binary values for the Opcode 15 to 9, 8 to 6, 5 to 3, and 2 to 0.

… continue for all six **machine-code instructions** (LD, NOT, ADD, INC, ADI,and ST)

You should assume the following values for the six **machine-code instructions** (***LD***, ***INC***, ***ADI***, ***NOT***, ***ADD***, and ***ST***)

a) ***ADI***: DR=001, SA=010, zfIR[2:0]=010

b) ***LD***: DR=111, SA=011

c) ***ST***: SA=101, SB=110

d) ***INC***: DR=010, SA=011

e) ***NOT***: DR=011, SA=010

f) ***ADD***: DR=101, SA=010, SB=010

[20 marks]

2. **Question**, this question builds on 1. Question. You must modify your **algorithmic state machine chart** from the 1.Question by incorporating the **algorithmic state machine chart** shown in Figure 5 (below) into your ASM chart.

   Please provide **micro-code** at the correct memory location in the **Control Memory** and a **machine-code instruction (IDA)** at the correct memory location in the **Memory M** that will invoke these **micro-code instructions**.

   You only need to provide **micro-code** at the correct memory location in the **Control Memory** for states**: IF, EXO, LRI0, and LRI1**

   Please follow 1. Question's format for the **micro-code** and **machine-code instructions**. Please see below Figure 5 for the correct layout of you answer.

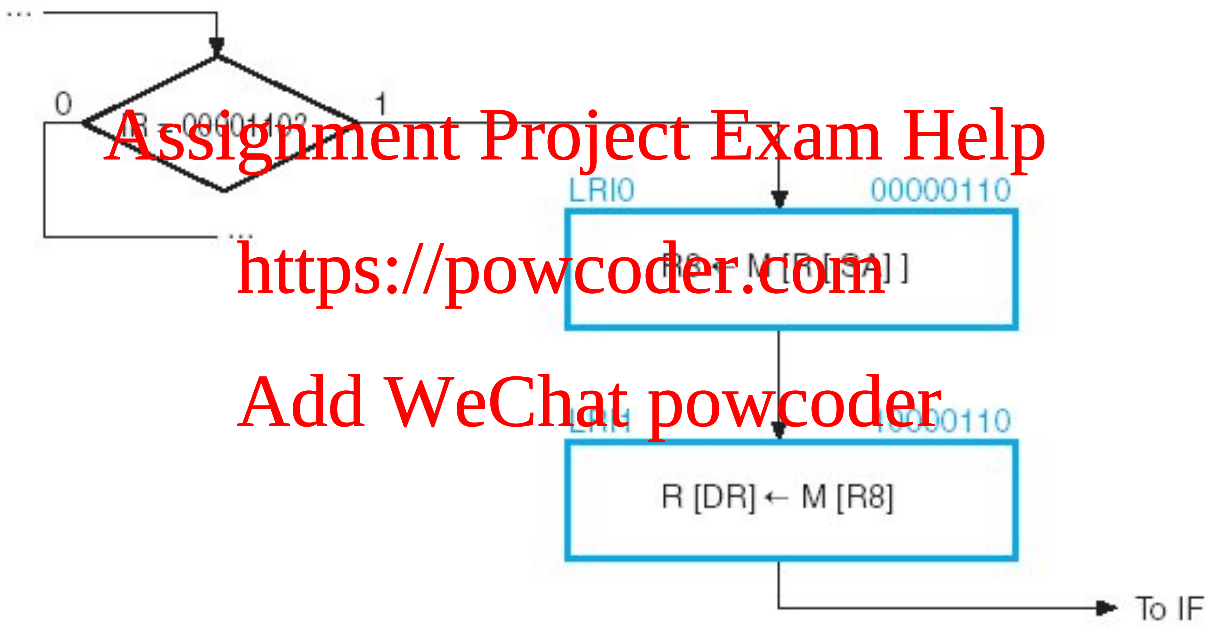
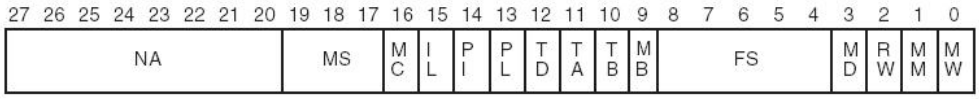


Figure 5

Your answer must provide **micro-code** for the **Control Memory** that implements the *modified* **algorithmic state machine chart.** The **micro-code** should have the following format for memory addresses in the **Control Memory** that implements your **algorithmic state machine: IF, EXO, LRI0, and LRI1.**

For example:

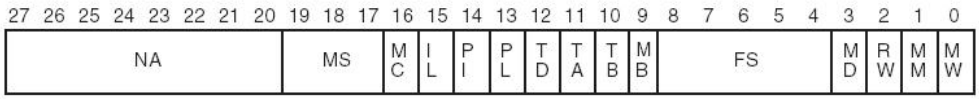


LRI0

a) Control Memory Address

b) Binary code for bits 0 to 27

c) Providing written reasons for selecting these binary values for NA, MS, MC, IL, PI, PL, TD, TA, TB, MB, FS, MD, RW, MM, and MW.



LRI1

a) Control Memory Address

b) Binary code for bits 0 to 27

c) Providing written reasons for selecting these binary values for NA, MS, MC, IL, PI, PL, TD, TA, TB, MB, FS, MD, RW, MM, and MW.

… continue for states: **IF and EXO** shown in your algorithmic state machine.

[35 marks]

Your solution must also provide a **machine-code instruction** at the correct memory location in the **Memory M**. The **machine-code instruction** should have the following format. You should execute this ***machine-code instructions*** *after* the ***ST*** **machine-code instruction** (1. Question).

15 Opcode 9	8 6	5 3	2 0

IDA(we call this instruction IDA)

a) Memory M Address

b) Binary code for bits 0 to 15

c) Providing written reasons for selecting these binary values for the Opcode 15 to 9, 8 to 6, 5 to 3, and 2 to 0.

You should assume the following values for the ***IDA*** **machine-code instruction**:

a) ***IDA***: DR=110, SA=010

[5 marks]

IMPORTANT ! : For Question 1 and 2, you must provide written reasons for selecting the binary values for NA, MS, MC, IL, PL, PE, TD, TA, TB, MB, FS, MD, RW, MM, and MW for the **micro-code** . Also written reasons for selecting the binary values for the Opcode 15 to 9, 8 to 6, 5 to 3, and 2 to 0 for the **machine-code instructions**.