The background of the slide is a detailed circuit board diagram. It features several integrated circuits (ICs) including a CPU (MC68008), an EEPROM (MC27C64), a GAL (GAL22V10), a counter (74LS393), and a crystal oscillator (XTAL1). The diagram shows various pins, power supply connections (5V, +V), and signal lines. A yellow brushstroke is drawn across the middle of the image, partially obscuring the circuit diagram.

► Synthesis produces a digital circuit that implements the behavior captured in the VHDL description.

Assignment Project Exam Help

<https://powcoder.com>

► VHDL is also the bases for a simulation.

► Characteristics of digital systems:

- Structural
- Behavioral
- Physical

Event, Propagation Delays and Concurrency

Event

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

Concurrency

Propagation delay

Signals



- ▶ May be 0, 1, or Z
- ▶ Equivalent to wires in digital circuits
- ▶ May be assigned values
- ▶ Signals are associated with time values
- ▶ Sequences of values determines the waveform
- ▶ Signal type depends on the level of abstraction
 - ▶ At gate level through wires (or, and, xor...)
 - ▶ At module level through integer (ALU...)

Shared Signals

► Hardware description languages must be expressive enough to describe signal that may be driven by one or more sources.

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

► Bus

Design Entity

► Design entities could be:

► Board

► Chip

► Gate

► Transistor

► This design component behavior must be:

► Described

► Simulated

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

Design Entity -Gate Level Example

► Half-Adder

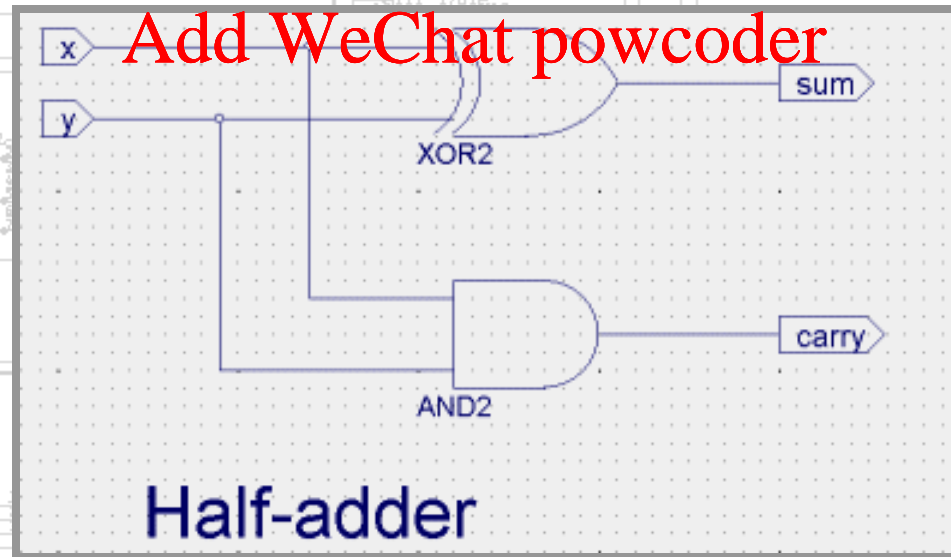
► Input signals: x, y

► Output signals: sum, carry

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder



Design Entity - Description

- ▶ Input signals
- ▶ Output signals
- ▶ Behavior
 - ▶ Truth table
 - ▶ Boolean equation
 - ▶ Wires between gates
- ▶ Two components in the design-entity description:
 - ▶ The interface
 - ▶ Internal behavior

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

Entity Declaration

▶ Interface to design entities through

▶ Entity Declaration:

Assignment Project Exam Help Keywords

<https://powcoder.com>

Design Entity Name

Add WeChat powcoder

```
entity half_adder is
  Port ( x : in bit;
         y : in bit;
         sum : out bit;
         carry : out bit);
end half_adder;
```

Port = input & output

Declaration Details

- ▶ **Blue bold** type denotes VHDL reserved keywords (entity, port, ...)
- ▶ VHDL is not case sensitive
 - ▶ Half-adder <https://powcoder.com>
- ▶ Ports define the input and output of the the design entity
 - Add WeChat powcoder**
- ▶ **Ports are signals** that enable communication between the design entity and other entities.
- ▶ Port signals must declare their types.

Port Declaration

- ▶ Signal types defined in the VHDL language

bit

Assignment Project Exam Help

- ▶ Represents a single-bit signal

bit_vector

<https://powcoder.com>

- ▶ Represents a vector of signal of type **bit**

- ▶ Bit and bit_vector are only two out of several other VHDL data types.

IEEE 1164 Signals Values

IEEE 1164 standard defines nine-value signals:

Assignment Project Exam Help

<https://powcoder.com>

Add WhatsApp powcoder

U	Uninitialised
X	Forcing Unknown
0	Forcing 0
1	Forcing 1
Z	High Impedance
W	Weak Unknown
L	Weak 0
H	Weak 1
-	Don't Care

Library IEEE

The following modifications are required to make the previous entity declaration IEEE compliant.

Assignment Project Exam Help

```
library IEEE;  
https://powcoder.com  
use IEEE.STD_LOGIC_1164.ALL;
```

Add WeChat powcoder
entity half_adder is

```
Port ( x : in std_logic;  
       y : in std_logic;  
       sum : out std_logic;  
       carry : out std_logic);  
end half_adder;
```

Signal Mode

▶ Port declaration distinguishes between:

▶ **in** - input signal

▶ **out** - output signal

▶ **inout** - bidirectional signal

Signal mode

```
entity half_adder is  
  Port ( x : in std_logic;
```

4 to 1 Multiplexer

This example uses `std_logic_vector(7 downto 0)`;

```
library IEEE;
```

```
use IEEE.STD_LOGIC_1164.ALL;
```

```
entity mux is
```

```
Port ( I0 : in std_logic_vector(7 downto 0);
```

```
      I1 : in std_logic_vector(7 downto 0);
```

```
      I2 : in std_logic_vector(7 downto 0);
```

```
      I3 : in std_logic_vector(7 downto 0);
```

```
      Sel : in std_logic_vector(1 downto 0);
```

```
      Z : out std_logic_vector(7 downto 0));
```

```
end mux;
```

<https://powcoder.com>

Bit vector

Add WeChat powcoder

std_logic_vector(7 downto 0)

```
entity mux is
    Assignment Project Exam Help
    std_logic_vector(7 downto 0);
```

<https://powcoder.com>

► This example refers to 8 bits long input vector.

► bit 7 - most significant bit

► bit 0 - least significant bit

Entity's Internal Behavior

```
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;
```

```
entity half_adder is  
  Port ( x : in std_logic;  
         y : in std_logic;  
         sum : out std_logic;  
         carry : out std_logic);  
end half_adder;
```

```
architecture Behavioral of half_adder is  
  -- declaration  
begin  
  -- description of behavior  
end Behavioral;
```

VHDL describes
the internal
behavior in the
architecture
construct.

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder

Architecture

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity half_adder is
    Port (
        x, y : in std_logic;
        sum, carry : out std_logic);
end half_adder;

architecture concurrent_behavior of half_adder is
begin
    sum <= (x xor y) after 5 ns;
    carry <= (x and y) after 5 ns;
end concurrent_behavior;
```

Assignment Project Exam Help

<https://powcoder.com>

Add WeChat powcoder