

Digital System Design

Functional Design

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Register Transfer Level Design

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Logic Design

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Circuit Design

Physical Design

Top-down
Digital
System
Design

Functional Design

► Functional design is based on:

- Requirement specification

► Target implementation influences the design flow

- CPU

- ASIC (Application Specific Integrated Circuits)

- FPGA (Field Programmable Gate Arrays)

► Requirements:

- Operation, Performance, Interface, Cost, Size, Power dissipation...

► Functional design may be verified through simulation

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Register Transfer Level Design (RTL)

- ▶ This step in the design flow transforms the high-level functional design into a description at the register level.
- ▶ The Register Transfer Level Design describes the design at the following level of abstraction:
 - ▶ Registers
 - ▶ Memory
 - ▶ Arithmetic Units
 - ▶ State Machines
- ▶ RTL designs are validated through simulation

Logic Design

- ▶ At this stage in the design flow the register level transfer design is compiled into logic design.
- ▶ Again the design may be verified through simulation.
- ▶ Please note:
 - ▶ Simulation may be used to guaranty that the design meets the specification.
 - ▶ The simulation in every step in the design flow allows for the interception of errors early in the design.

Circuit Design

- ▶ At this stage in the design flow the logic design is compiled into circuit design.
- ▶ The step is strongly influenced by the target implementation.
- ▶ Again the design may be verified through simulation specifically through:
 - ▶ Timing simulation
 - ▶ Circuit analysis.

Physical Design

► In the final step in the design flow the circuit design determines the physical chip layout.

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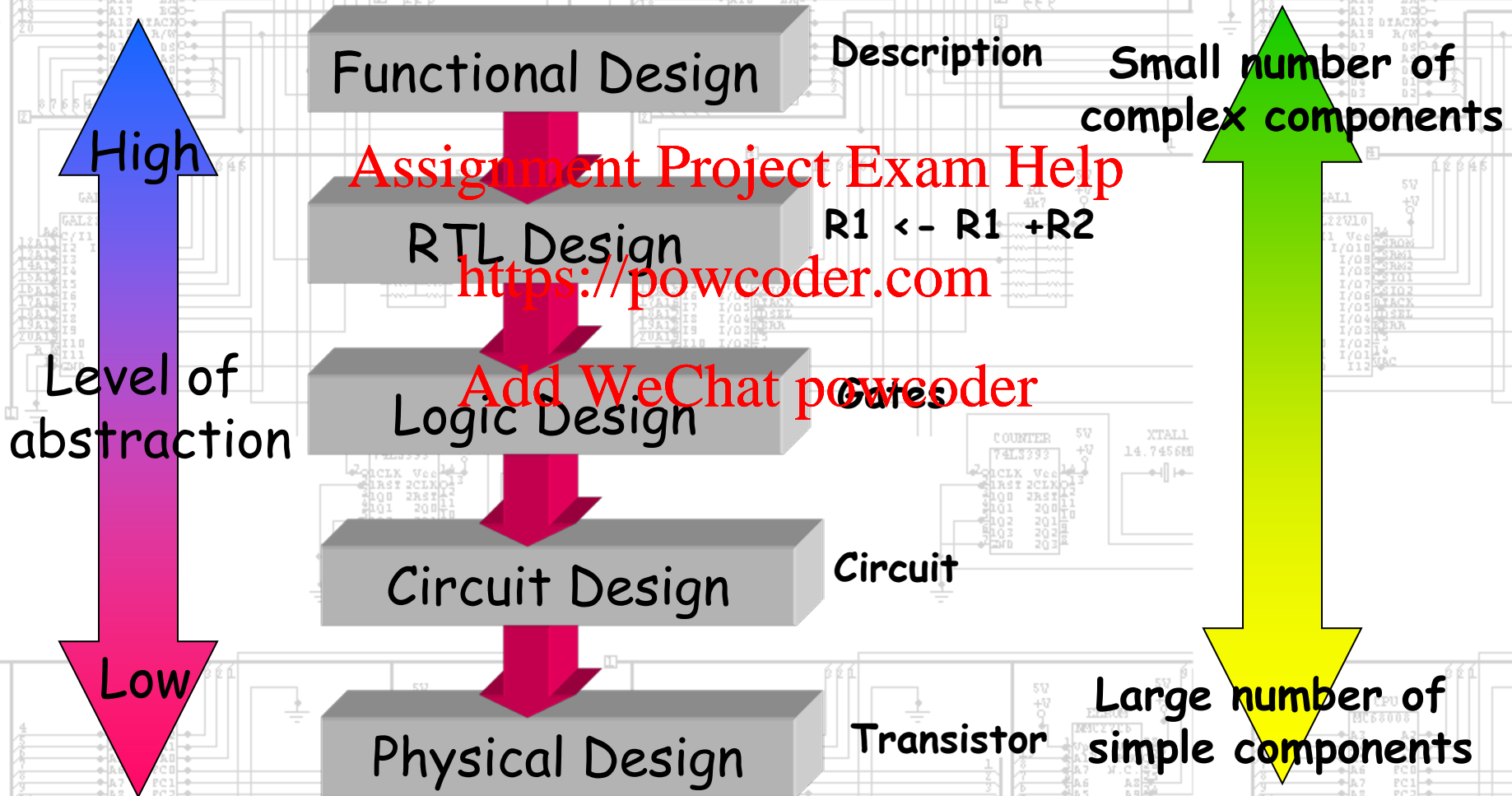
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► Physical properties may be verified:

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- Chip area
- Power dissipation
- Clock frequency

Digital System Design Hierarchy



Hardware Description Languages

▶ Hardware Description Languages are used to:

▶ Describe digital systems

▶ Model digital systems

▶ Design digital systems

▶ Hardware Description Languages:

▶ VHDL, Verilog and more

▶ **VHDL**

▶ **V**HSIC **H**ardware **D**escription **L**anguage

▶ **VHSIC**

▶ **V**ery **H**igh **S**peed **I**ntegrated **C**ircuit **L**anguage

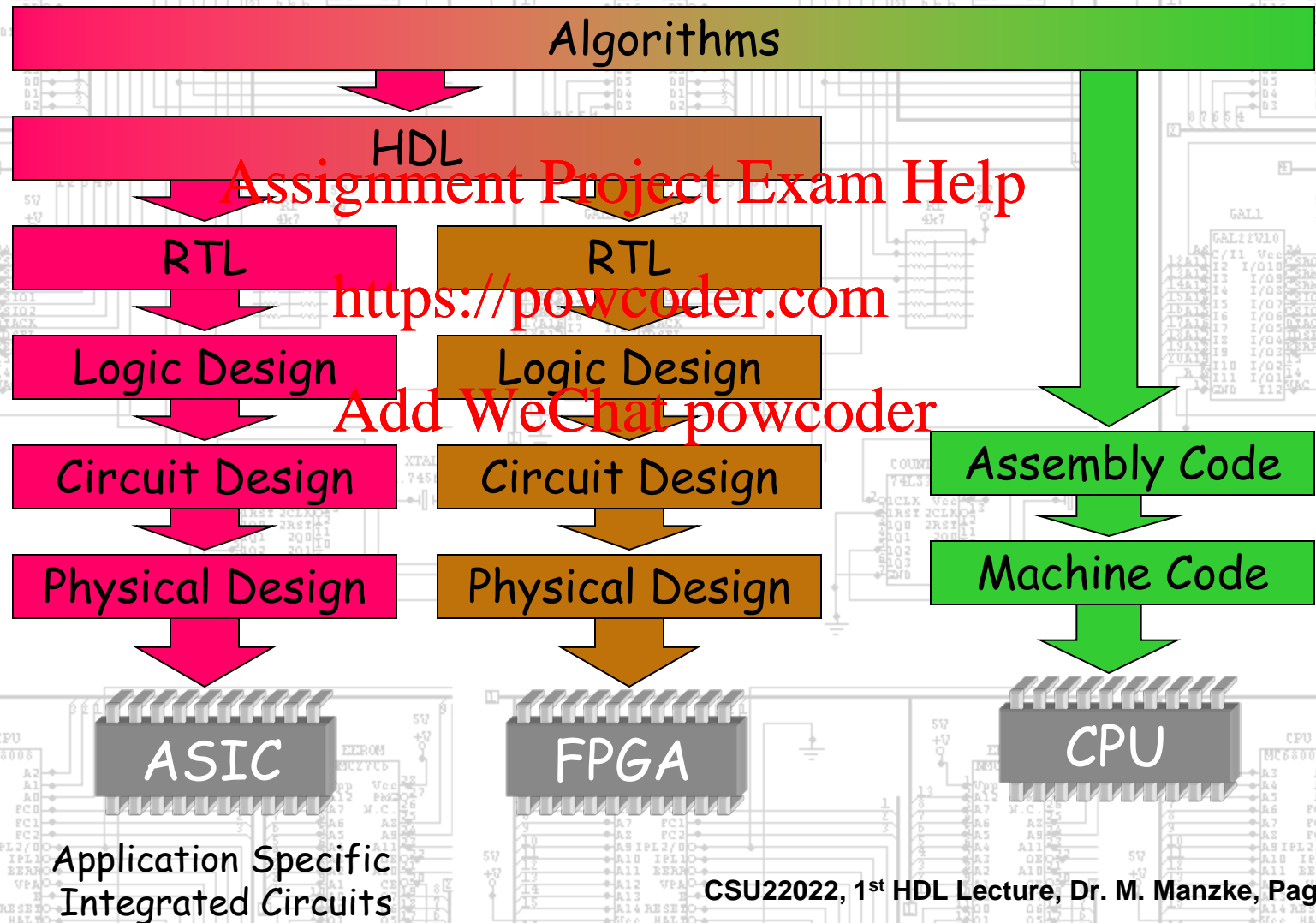
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Target Implementation

Design flow depends on target hardware



Design Views

Transistors

Register

Gates

Processor

Behavioural

Structural

Algorithms

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Cells

Modules

Register Transfers

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Boolean Expressions

Chips

Boards

Transfer Functions

Physical