

Microprogram Design

- ▶ Use ASM from Lecture 16 to design the Microprograms
 - ▶ See Symbolic/Binary Microprogram on next slide
- <https://powcoder.com>
- Add WeChat powcoder

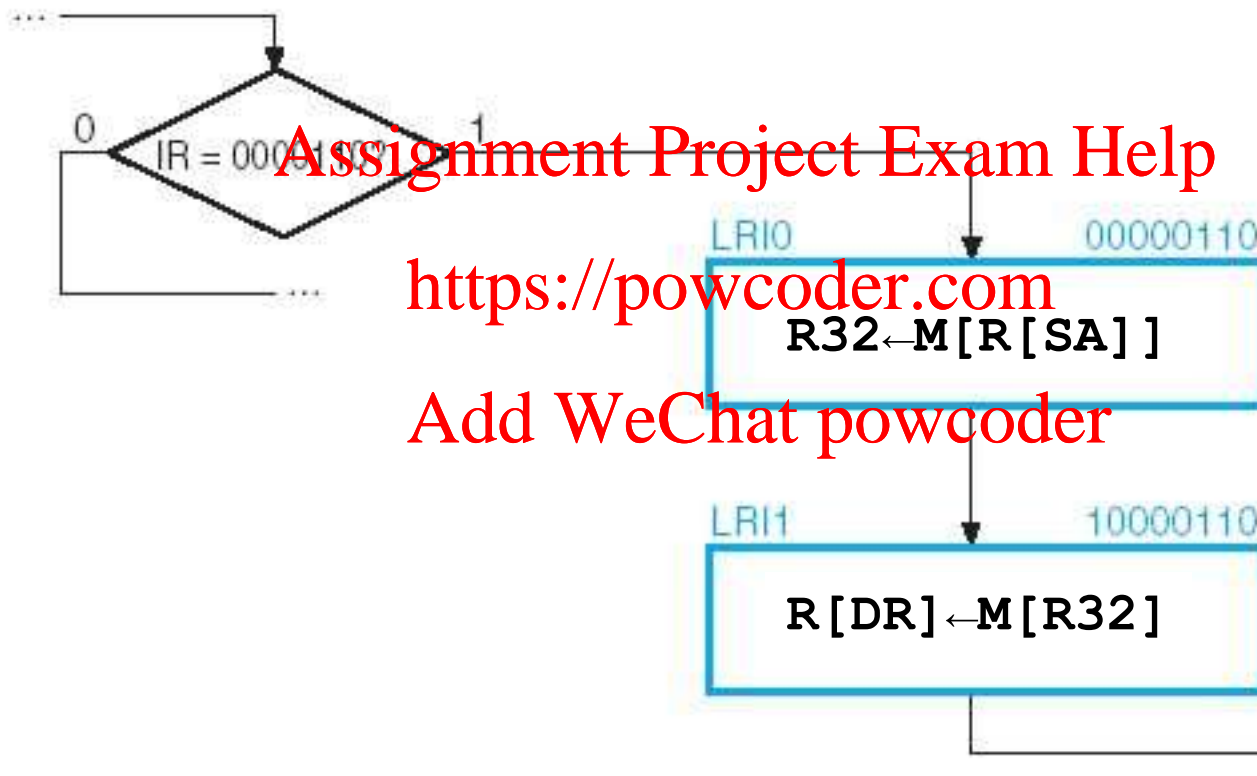
Symbolic/Binary Microprogram

Address	NXT ADD	MS	MC	IL	PI	PL	TD	TA	TB	MB	FS	MD	RW	MM	MW
IF	EX0	CNT	—	LDI	INP	NLP	—	—	—	—	—	—	NW	PC	NW
EXO	—	NXT	OPC	NLI	NLP	NLP	—	—	—	—	—	—	NW	—	NW
ADI	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	—	Constant $A = A + B$	—	FnUt	WR	—	NW
LD	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	—	—	—	Data	WR	MA	NW
ST	IF	NXT	NXA	NLI	NLP	NLP	—	SA	SB	Register	—	—	NW	MA	WR
INC	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	—	—	$F = A + 1$	FnUt	WR	—	NW
NOT	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	—	—	$F = \overline{A}$	FnUt	WR	—	NW
ADD	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	SB	Register	$F = A + B$	FnUt	WR	—	NW

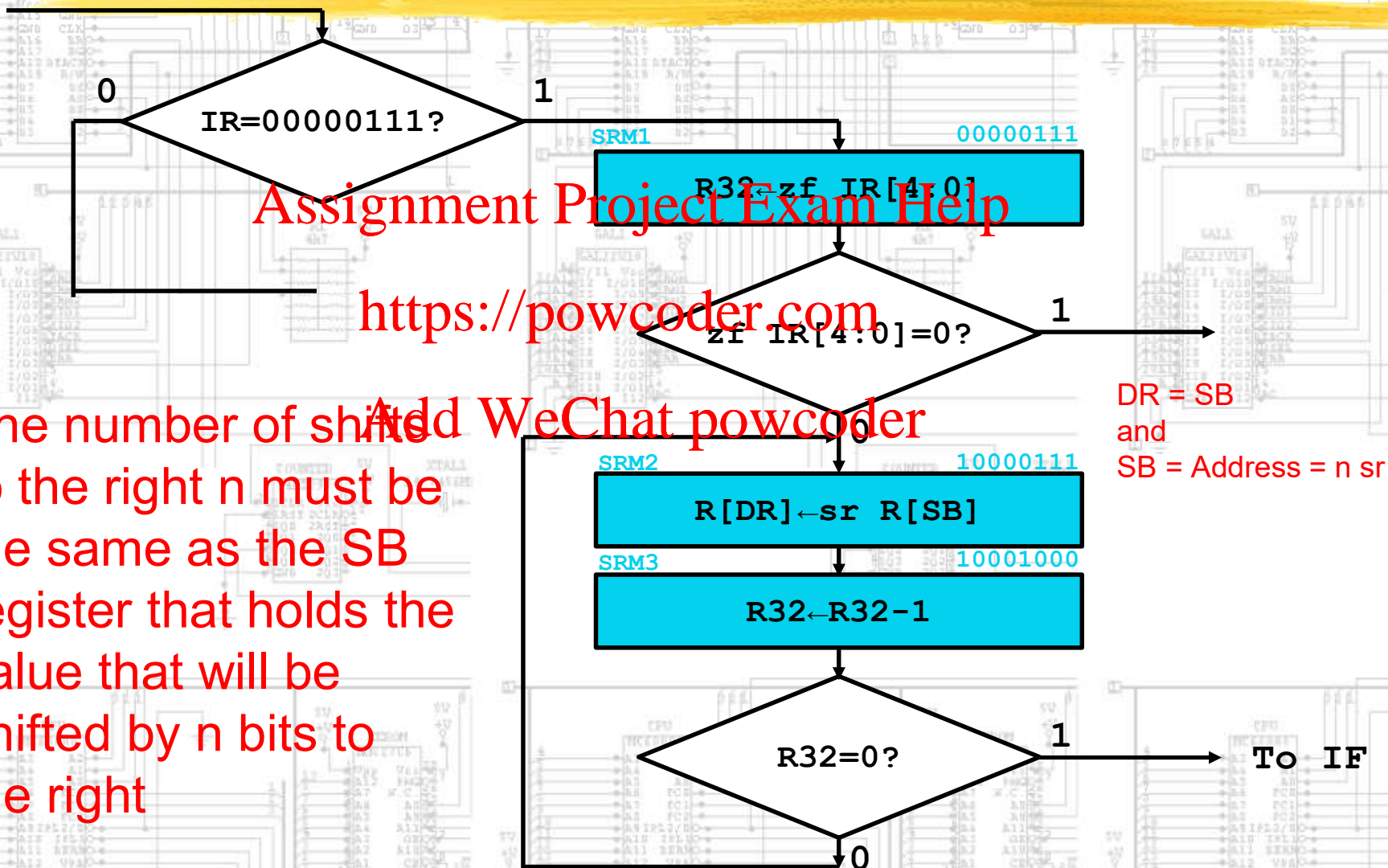
Address	NXT ADD	MS	MC	IL	PI	PL	TD	TA	TB	MB	FS	MD	RW	MM	MW
192	193	000	0	1	1	0	0	0	0	0	00000	0	0	1	0
193	000	001	1	0	0	0	0	0	0	0	00000	0	0	0	0
000	192	001	0	0	0	0	0	0	0	1	00010	0	1	0	0
001	192	001	0	0	0	0	0	0	0	0	00000	1	1	0	0
002	192	001	0	0	0	0	0	0	0	0	00000	0	0	0	1
003	192	001	0	0	0	0	0	0	0	0	00001	0	1	0	0
004	192	001	0	0	0	0	0	0	0	0	01110	0	1	0	0
005	192	001	0	0	0	0	0	0	0	0	00010	0	1	0	0

This is not our control memory but similar

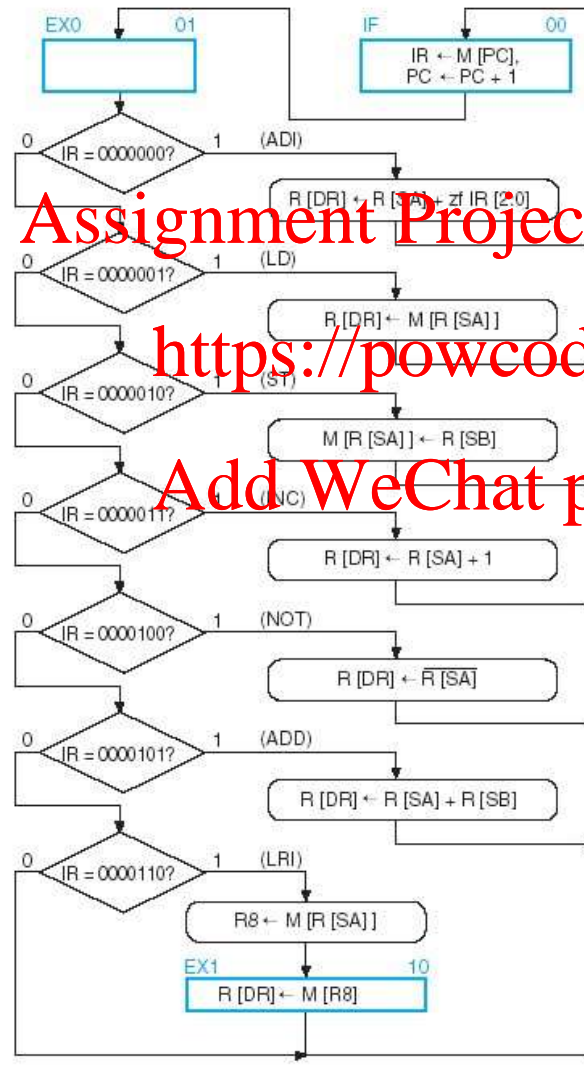
Indirect Instruction ASM



Right-Shift Instruction ASM



Hardwired Multiple-Cycle Control

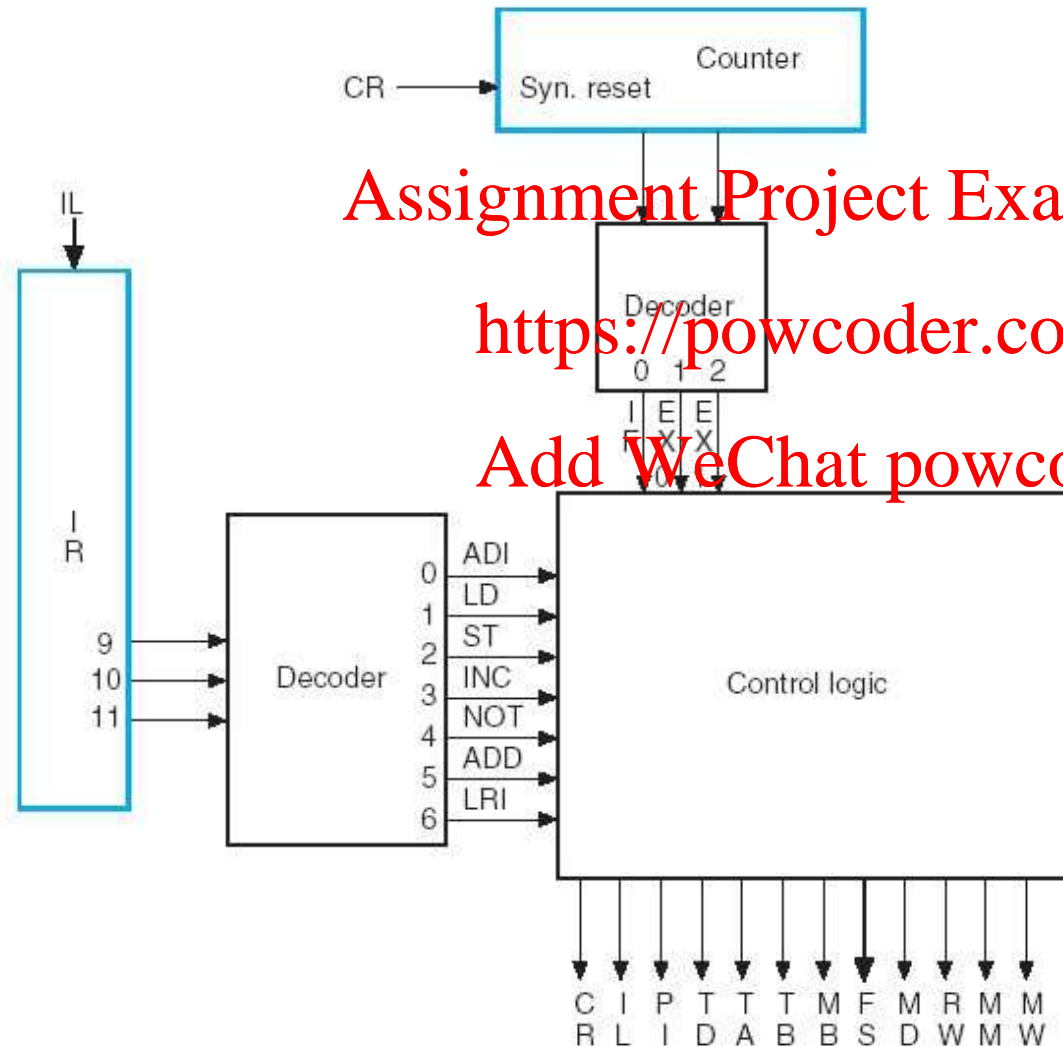


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Hardwired Control Unit



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Pipelined (based on single-cycle)

The diagram illustrates a 4-stage CPU pipeline. The stages are:

- Instruction Fetch (IF):** The instruction is fetched from instruction memory.
- Decode and Operand Fetch (DOF):** The instruction is decoded, and operands are fetched from the register file or memory.
- Execution (EX):** The instruction is executed by the function unit.
- Write-back (WB):** The result is written back to the register file.

The diagram also shows the control and datapath sections, including the instruction decoder, register file, function unit, and data memory.

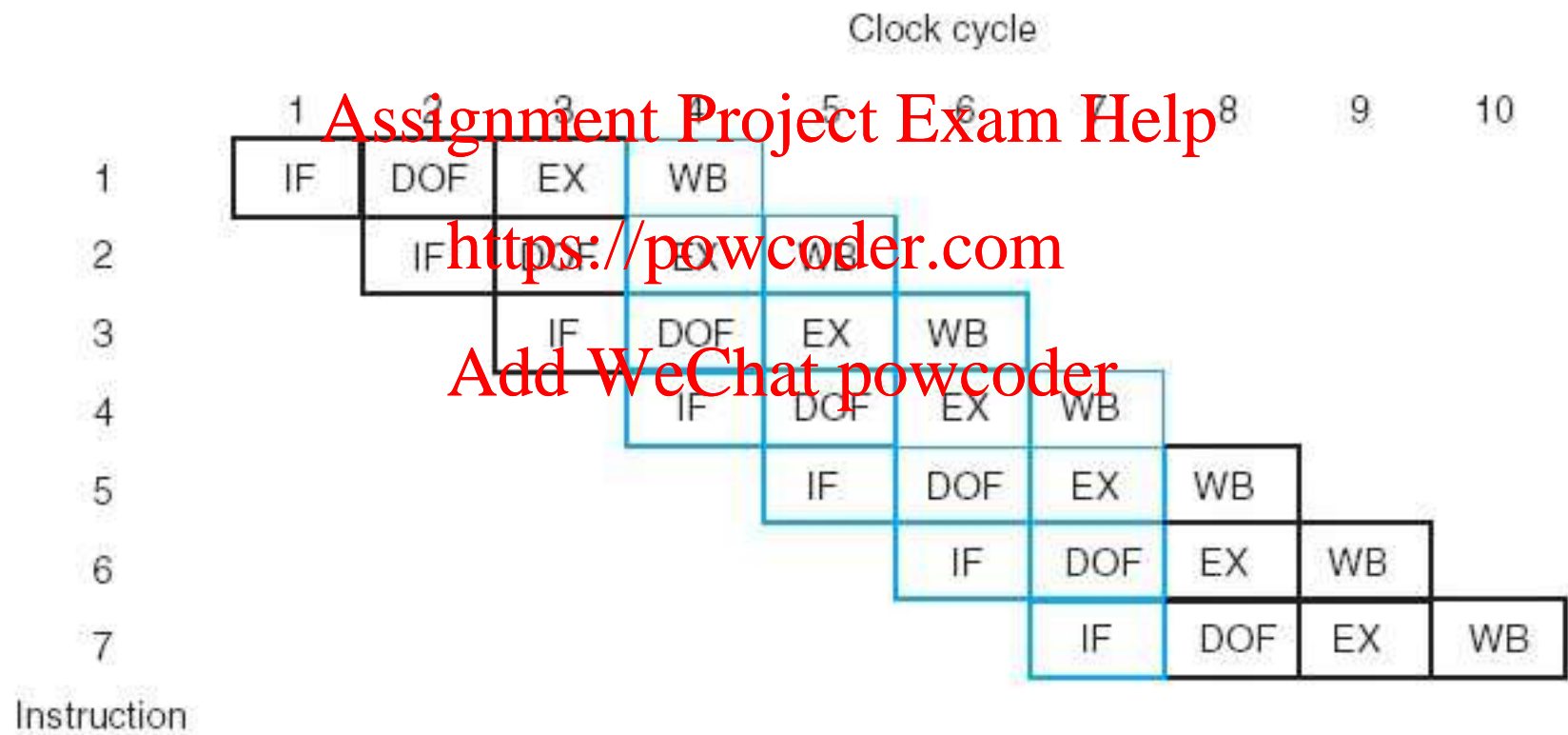
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Pipelined Execution Pattern



Computer Architecture and Microprocessor Systems

