CSU22022 Computer Architecture I

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Processor Assignment: Project Milestone Register File

Simulation Procedure

20th October 2022

Version 1.0

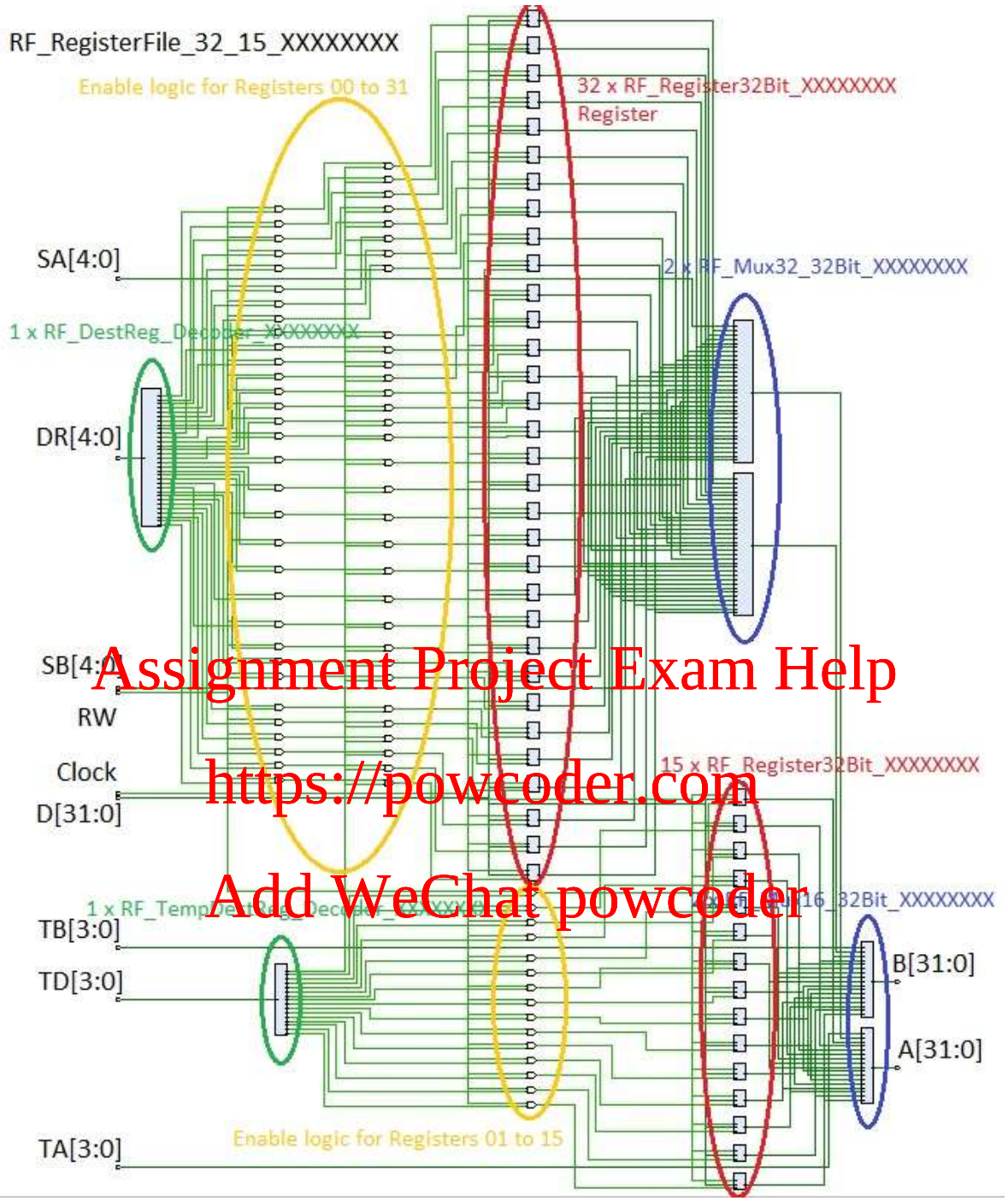
The Schematic 1 on the following page depicts the register file that you need to implement. You need to build a project in Vivado to run simulations and generate schematics for all entities of the assignment.

You Vivado project should be named “RegisterFile_32_15_XXXXXXXX”, with XXXXXXXX as your student number. The entity name follows the same convention, please see Table 1.

The project requires the following entities. Please see Table 1 below and Schematic 1 on the following page.

Number of Instantiations	Instantiation Name	Entity Name
1	TestRegFile	RF_TestRegisterFile_32_15_XXXXXXXX
1	RegFile	RF_RegisterFile_32_15_XXXXXXXX
1	DestReg_Decoder	RF_DestReg_Decoder_XXXXXXXX
1	DestTempReg_Decoder	RF_TempDestReg_Decoder_XXXXXXXX
32 15	RegisterXX, XX=00 to 31 TempRegXX, XX=01 to 15	RF_Register32Bit_XXXXXXXX
1 1	Mux32_A Mux32_B	RF_Mux32_32Bit_XXXXXXXX
1 1	Mux16_A Mux16_B	RF_Mux16_32Bit_XXXXXXXX
1	Mux3	RF_Mux3_32Bit_XXXXXXXX

Table 1



Schematic 1 depicts the register file with all entities and the enable logic for the Registers and Temp Registers

You must provide the following for every entity:

1. Design code e.g. RF_RegisterFile_32_15_XXXXXXXX.vhd
2. A test bench e.g. RF_RegisterFile_32_15_XXXXXXXX_TB.vhd
3. One or more schematics e.g. RF_RegisterFile_32_15_XXXXXXXX_SchematicXX.jpg
4. As many as needed annotated e.g. timing diagrams RF_RegisterFile_32_15_XXXXXXXX_TDXX.jpg
5. Simulation Procedure documentation RF_RegisterFile_32_15_XXXXXXXX_Doc.jpg

Simulation Procedure for the following entities:

RF_Mux3_32Bit_XXXXXXXX

Convert your student ID into binary and set:

IN00 = student ID
IN01 = student ID + 1
IN02 = student ID + 2

Demonstrate that the multiplexer functions correctly.

RF_Mux16_32Bit_XXXXXXXX

Convert your student ID into binary and set:

IN00 = student ID
IN01 = student ID + 1
IN02 = student ID + 2
continue for all inputs

Demonstrate that the multiplexer functions correctly.

RF_Mux32_32Bit_XXXXXXXX

Convert your student ID into binary and set:

IN00 = student ID
IN01 = student ID + 1
IN02 = student ID + 2
continue for all inputs

Demonstrate that the multiplexer functions correctly.

RF_Register32Bit_XXXXXXXX

Convert your student ID into binary.
Write and read the register with your ID.

Demonstrate that the register functions correctly.

RF_DestReg_Decoder_XXXXXXXX

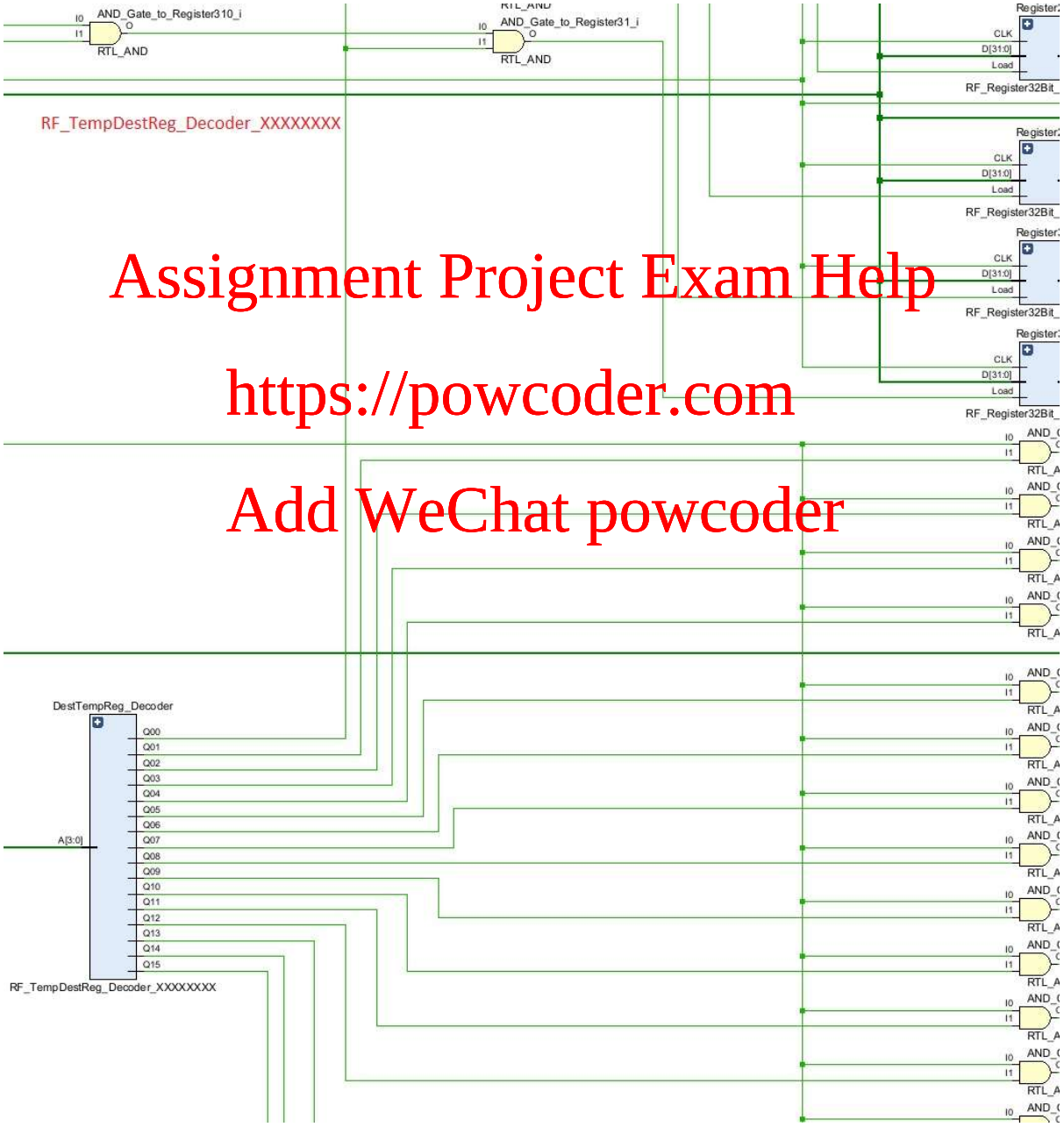
Demonstrate that the decoder functions correctly.

RF_TempDestReg_Decoder_XXXXXXXX

Demonstrate that the decoder functions correctly.

RF_RegisterFile_32_15_XXXXXXXX

In addition to an overview schematic, you must provide zoom in screenshots that allow me to read the entity names. The following screenshots is an example:



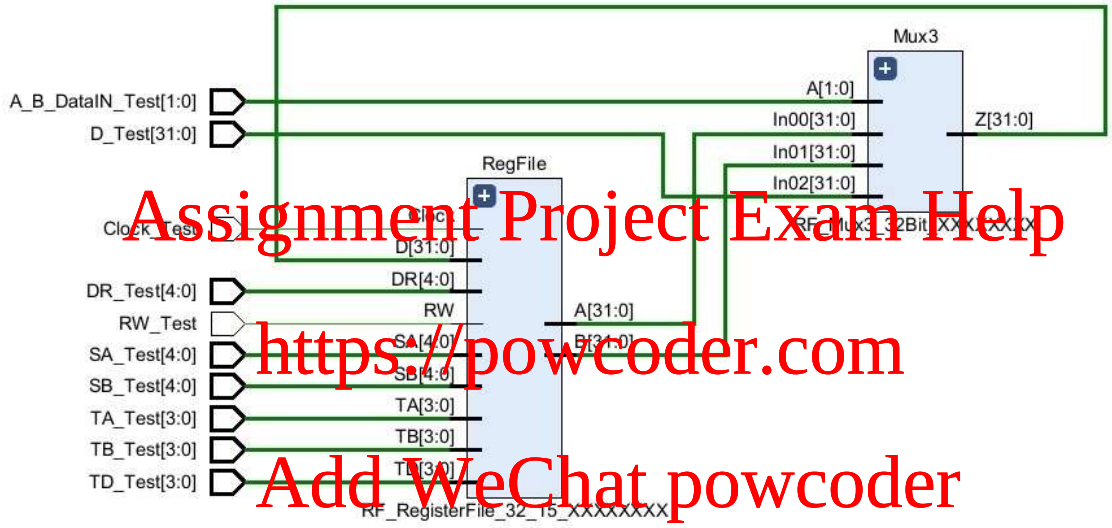
Convert your student ID into binary and set:

Load registers as follows:

Register00 = student ID
Register01 = student ID + 1
Register02 = student ID + 2
continue for all Registers (32+15) including the Temp Registers.

Read all registers and confirm that the functions correctly.

RF_Test_RegisterFile_32_15_XXXXXXXX



Load registers via RF_Mux3_32Bit_XXXXXXXX:

Register00 = student ID
Register01 = student ID + 1
Register02 = student ID + 2
continue for all Registers (32+15) including the Temp Registers.

Read all registers and confirm that the functions correctly.

Perform 4 register transfer operations on the Port A (A[31:1]) and 4 register transfer operations on the Port B (B[31:1]).

All files must be submitted to Blackboard as individual files, no zip files. Submit only entities that are working and are fully tested. You must follow the entity order on the checklist. You cannot skip entities. You must also submit the Checklist "CSU22022 Project Milestone Register File 2022-2023 Checklist V1.1"