Chapter 16

Solutions to Exercises within the Chapter

Ex: 16.1 Observe the two PMOS transistors in series with gates connected to inputs A and B, and the parallel path with three PMOS transistors in series with gates connected to inputs C, D, and E. Therefore, the PUN realizes the function $Y = \bar{A}\bar{B} + \bar{C}\bar{D}\bar{E}$.

Ex: 16.2

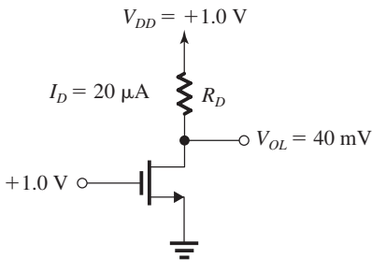


Figure 1

Refer to Fig. 1.

$$r_{DS} = \frac{V_{OL}}{I_D} = \frac{40 \text{ mV}}{20\ \mu\text{A}} = 2\ \text{k}\Omega$$

Substituting in the expression given for r_{DS}, we get

$$2 = \frac{1}{0.540 \times \left(\frac{W}{L}\right) \times (1.0 - 0.35)}$$

$$\Rightarrow \frac{W}{L} = 1.42$$

The value of R_D can be obtained from

$$R_D = \frac{V_{DD} - V_{OL}}{I_D}$$

$$= \frac{1.0 - 0.04}{0.02} = 48\ \text{k}\Omega$$

When the switch is open, $I_D = 0$ and

$$P_{D\text{rawn}} = V_{DD} I_D = 0$$

When the switch is closed, $I_D = 20\ \mu$A, and

$$P_{D\text{rawn}} = V_{DD} I_D = 1.0 \times 20 = 20\ \mu\text{W}$$

Ex: 16.3 If V_x remains unchanged at 0.0225 V, then

$$k_n R_D = \frac{1}{V_x} = \frac{1}{0.0225} = 44.44$$

For R_D to be 10 kΩ,

$$k_n = \frac{44.44}{10} = 4.444\ \text{mA/V}^2$$

Thus,

$$4.444 = 0.54 \times \frac{W}{L}$$

$$\Rightarrow \frac{W}{L} = 8.22$$

The parameters V_{OH}, V_{OL}, V_{IL}, V_{IH} and thus NM_L and NM_H do not depend on the value R (but on V_x) and thus their values will not change.

The current I_{DD} drawn from the power supply during the low-output interval becomes

$$I_{DD} = \frac{V_{DD} - V_{OL}}{R_D} = \frac{1.0 - 0.033}{10} = 96.7\ \mu\text{A}$$

and the power drawn from the supply during the low-output interval is

$$P_D = V_{DD} I_D = 1.0 \times 96.7 = 96.7\ \mu\text{W}$$

Since the inverter spends half of the time in this state, we have

$$P_{D\text{average}} = \frac{1}{2} P_D = 48\ \mu\text{W}$$

Ex: 16.4 $k_n R_D = \frac{1}{V_x}$

For $R_D = 10$ kΩ and

$$k_n = k'_n \left(\frac{W}{L}\right) = 0.54 \times 1.5 = 0.81\ \text{mA/V}^2$$

we obtain

$$V_x = \frac{1}{0.81 \times 10} = 0.12\ \text{V}$$

Now

$$V_{OH} = 1.0\ \text{V}$$

From Eq. (16.22) we get

$$V_M = \frac{1.0}{1 + \frac{1.0 - 0.35}{0.12}} = 0.16\ \text{V}$$

From Eq. (16.12) we obtain

$$V_{IL} = V_t + V_x = 0.35 + 0.12 = 0.47\ \text{V}$$

From Eq. (16.20) we have

$$V_{IH} = 0.35 + 1.63\sqrt{1.0 \times 0.12} - 0.12$$

$$= 0.80\ \text{V}$$

Thus,

$$NM_L = V_{IL} - V_{OL} = 0.47 - 0.16 = 0.31\ \text{V}$$

$$NM_H = V_{OH} - V_{IH} = 1.0 - 0.80 = 0.20\ \text{V}$$

During the output-low interval, we have

$$I_{DD} = \frac{V_{DD} - V_{OL}}{R_D}$$

$$= \frac{1.0 - 0.16}{10} = 84\ \mu\text{A}$$

and

$$P_D = 1.0 \times 84 = 84\ \mu\text{W}$$

Thus,

$$P_{D\text{average}} = \frac{1}{2} P_D = 42\ \mu\text{W}$$

Ex: 16.5 (a) For $V_M = 0.6\text{ V} = \frac{1}{2}\,V_{DD}$, the inverter must be matched, thus

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$$

$$\Rightarrow \frac{W_p}{0.13} = 4$$

$$\Rightarrow W_p = 0.52\ \mu\text{m}$$

(b) $V_{OH} = V_{DD} = 1.2\text{ V}$

$V_{OL} = 0\text{ V}$

To obtain V_{IH}, we use Eq. (16.35):

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$$

$$= \frac{1}{8}(5 \times 1.2 - 2 \times 0.4)$$

$$= 0.65\text{ V}$$

To obtain V_{IL}, we use Eq. (16.36):

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

$$= \frac{1}{8}(3 \times 1.2 + 2 \times 0.4)$$

$$= 0.55\text{ V}$$

The noise margins can now be found as

$$NM_H = V_{OH} - V_{IH}$$

$$= 1.2 - 0.65 = 0.55\text{ V}$$

$$NM_L = V_{IL} - V_{OL}$$

$$= 0.55 - 0 = 0.55\text{ V}$$

(c) With $v_I = V_{DD}$ and v_O low, the output resistance is r_{DSN}:

$$r_{DSN} = 1\Big/\left[\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{DD} - V_t)\right]$$

$$= \frac{1}{0.43 \times 1(1.2 - 0.4)} = 2.9\text{ k}\Omega$$

With $v_I = 0$ V and $v_O = V_{DD}$, the output resistance is r_{DSP}:

$$r_{DSP} = 1\Big/\left[\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{DD} - |V_t|)\right]$$

$$= \frac{1}{\frac{0.43}{4} \times 4(1.2 - 0.4)} = 2.9\text{ k}\Omega$$

The two output resistances are equal because the inverter is matched.

(d) Using Eq. (16.39), we obtain

$$V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{tn}}{r + 1}$$

where

$$|V_{tp}| = V_{tn} = 0.4\text{ V}$$

and

$$r = \sqrt{\frac{\mu_p W_p}{\mu_n W_n}} = \sqrt{\frac{1}{4} \times 1} = \frac{1}{2}$$

Thus,

$$V_M = \frac{0.5(1.2 - 0.4) + 0.4}{0.5 + 1} = 0.53\text{ V}$$

Ex: 16.6 To obtain $V_M = 2.5\text{ V} = \frac{1}{2}V_{DD}$, the inverter must be matched, thus

$$\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_p C_{ox}\left(\frac{W}{L}\right)_p$$

$$2\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_n C_{ox}\left(\frac{W}{L}\right)_p$$

$$\left(\frac{W}{L}\right)_p = 2\left(\frac{W}{L}\right)_n \qquad (1)$$

For $v_O = V_{OL} = 0.2$ V and $v_I = 0.2$ V, Q_N will be operating in the triode region. Thus,

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[(V_{DD} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$0.2 = 0.05 \times \left(\frac{W}{L}\right)_n \left[(5 - 1) \times 0.2 - \frac{1}{2} \times 0.2^2\right]$$

$$\Rightarrow \left(\frac{W}{L}\right)_n = 5.13 \simeq 5$$

$$\left(\frac{W}{L}\right)_p = 2 \times 5.13 = 10.26 \simeq 10$$

Solutions to End-of-Chapter Problems

16.1 (a) $R_{\text{on}} = r_{DSN}$

$$= \frac{1}{(\mu_n C_{ox})\left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})} \quad (1)$$

$$= \frac{1}{0.540 \times 1.5(1 - 0.35)} = 1.90\ \text{k}\Omega$$

(b) $R_{\text{on}} = r_{DSP}$

$$= \frac{1}{(\mu_p C_{ox})\left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)} \quad (2)$$

$$= \frac{1}{0.100 \times 1.5(1 - 0.35)} = 10.26\ \text{k}\Omega$$

(c) From (1) and (2) since $V_{tn} = -|V_{tp}|$, then if R_{on} are to be equal, then

$$(\mu_n C_{ox})\left(\frac{W}{L}\right)_n = (\mu_p C_{ox})\left(\frac{W}{L}\right)_p$$

$$\Rightarrow \left(\frac{W}{L}\right)_p = \frac{\mu_n C_{ox}}{\mu_p C_{ox}}\left(\frac{W}{L}\right)_n$$

$$= \frac{540}{100} \times 1.5 = 8.1$$

16.2 (a) For Q_N, we have

$$R_{\text{on}} = \frac{1}{(\mu_n C_{ox})\left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})}$$

For Q_P, we have

$$R_{\text{on}} = \frac{1}{(\mu_p C_{ox})\left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)}$$

Since $V_{tn} = |V_{tp}|$, then for R_{on} of Q_P to equal R_{on} of Q_N,

$$(\mu_p C_{ox})\left(\frac{W}{L}\right)_p = (\mu_n C_{ox})\left(\frac{W}{L}\right)_n$$

$$\Rightarrow \left(\frac{W}{L}\right)_p = \frac{\mu_n C_{ox}}{\mu_p C_{ox}}\left(\frac{W}{L}\right)_n$$

$$= \frac{500}{125} \times 1.5 = 6.0$$

(b) For both devices, we have

$$R_{\text{on}} = \frac{1}{0.5 \times 1.5 \times (1.2 - 0.4)} = 1.67\ \text{k}\Omega$$

16.3

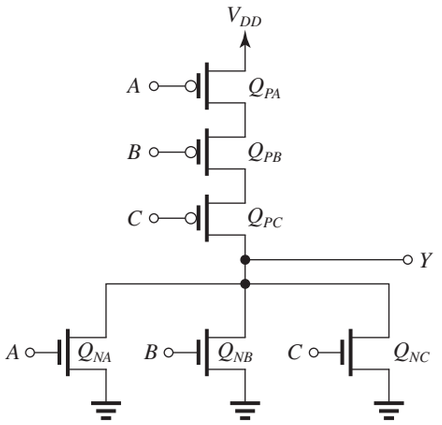


Figure 1

$Y = \overline{A + B + C}$

$\Rightarrow \overline{Y} = A + B + C \Rightarrow$ PDN

$Y = \overline{A}\,\overline{B}\,\overline{C} \Rightarrow$ PUN

The circuit realization is shown in Fig. 1.

16.4

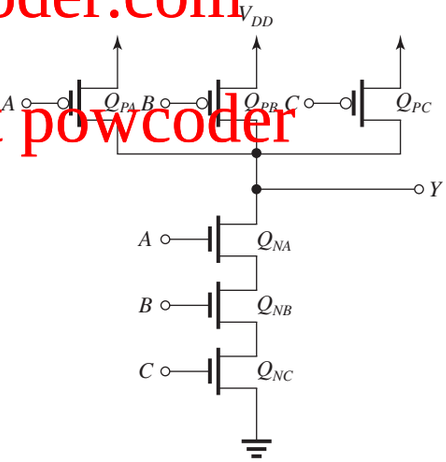


Figure 1

$Y = \overline{ABC}$

$\Rightarrow \overline{Y} = ABC \Rightarrow$ PDN

$Y = \overline{A} + \overline{B} + \overline{C} \Rightarrow$ PUN

Figure 1 shows the circuit realization.

16.5

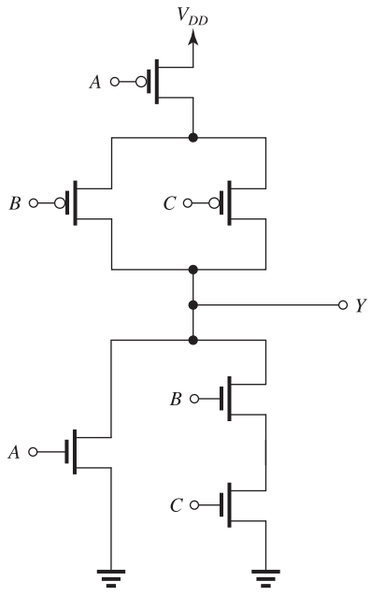


Figure 1

Figure 1 shows the complete CMOS logic gate where the PUN is obtained as the dual of the given PDN. The function realized can be found from the PDN as

$\overline{Y} = A + BC$

or

$Y = \overline{A + BC}$

16.6

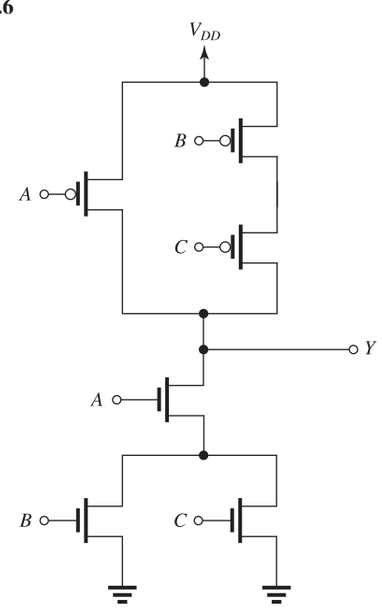


Figure 1

Figure 1 shows the complete CMOS circuit where the PUN is obtained as the dual network of the given PDN. The logic function realized can be written from the PDN as

$\overline{Y} = A(B + C)$

or equivalently

$Y = \overline{A(B + C)}$

16.7

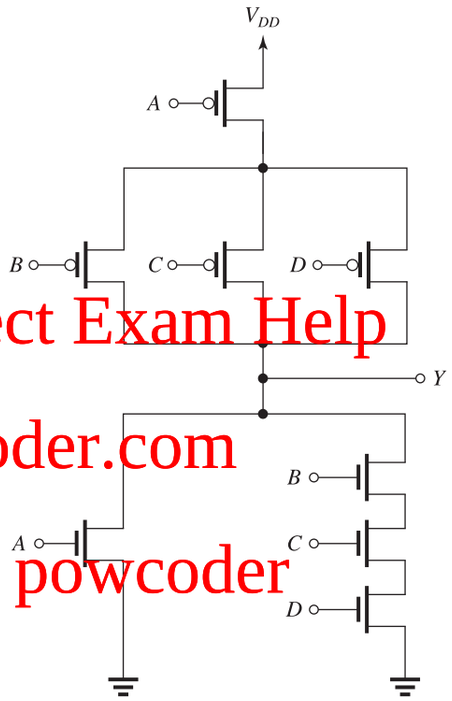


Figure 1

Figure 1 shows the complete CMOS logic circuit where we have obtained the PDN as the dual of the given PUN. The logic function can be written from the PDN as

$\overline{Y} = A + BCD$

or equivalently

$Y = \overline{A + BCD}$

16.8 The given Boolean expression can be written as

$\overline{Y} = AB + CDE$

from which the PDN of the circuit in Fig. 1 can be directly obtained.

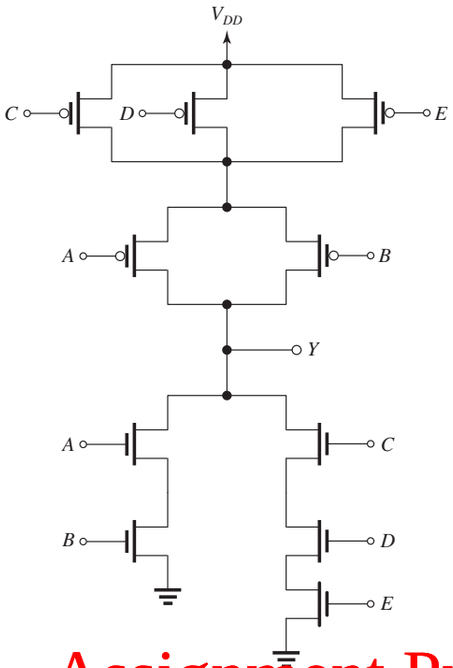


Figure 1

The PUN can then be found as the dual of the PDN. The complete circuit is shown in Fig. 1.

16.9

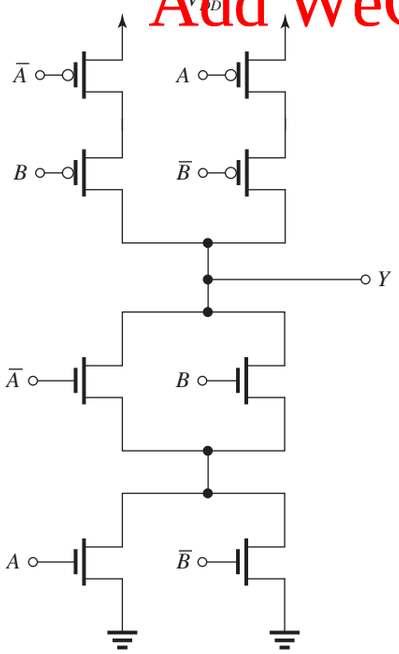


Figure 1

Figure 1 shows a CMOS realization of the Exclusive-OR function. This circuit is obtained by utilizing the PUN in Fig. 16.10(a) and then finding the dual PDN. Note that two additional inverters are needed to generate $\overline{A}$ and $\overline{B}$, for a total of 12 transistors.

16.10 $Y = \overline{A}BC + A\overline{B}C + AB\overline{C}$ (1)

Using this expression to directly synthesize the PUN we obtain the circuit shown in Fig. 1.

This PUN circuit requires 9 transistors plus three inverters for a total of 15 transistors.

This, of course, does not include the transistors required for the PDN which we shall consider shortly. Inspecting the PUN circuit reveals the potential for eliminating two transistors through what is known as "path merging." Specifically the two transistors in the top row that are controlled by $\overline{A}$ can be merged into a single transistor, and the two transistors in the bottom row that are controlled by $\overline{C}$ can be merged into a single transistor. The result is the 7-transistor PUN shown in Fig. 2.

We next consider the realization of the PDN. A straightforward realization can be obtained by finding the dual of the PUN in Fig. 1. This is shown in Fig. 3. It requires nine transistors

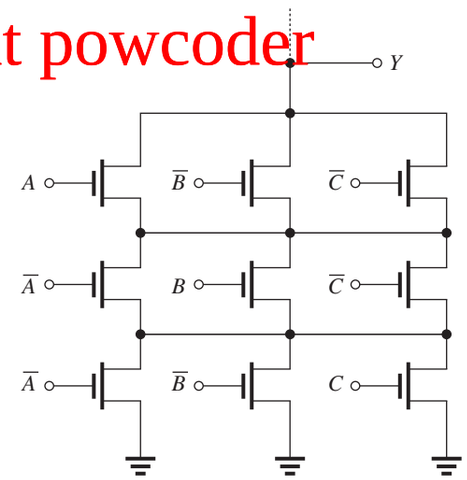


Figure 3

plus three inverters. The latter, of course are the same three inverters needed to obtain the complemented variables in PUN. The circuit in Fig. 3 does not lend itself to path merging, at least not in a straightforward way.

This figure belongs to Problem 16.10, part (a).

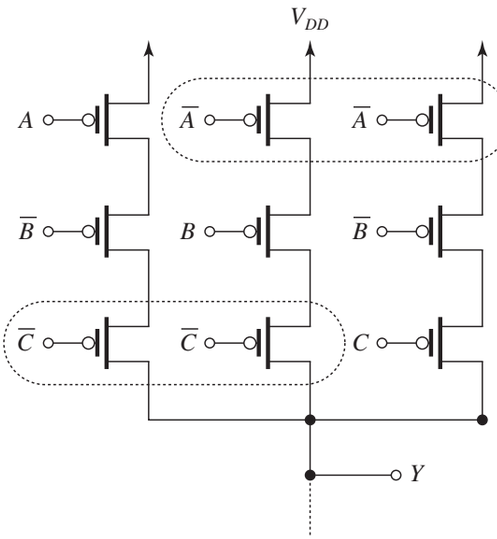


Figure 1

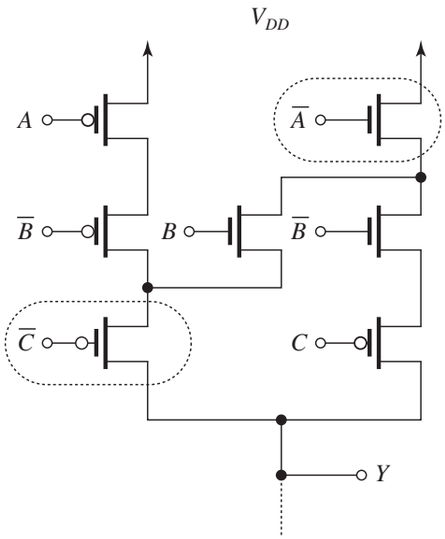


Figure 2

There is, however, an alternative way to synthesize a PDN with a lower number of transistors. We simply obtain $\overline{Y}$ from the expression in Eq. (1) using DeMorgan's law as follows:

$$\overline{Y} = \overline{\overline{A}BC}.\overline{A\overline{B}C}.\overline{AB\overline{C}}$$

$$= (A + \overline{B} + \overline{C})(\overline{A} + B + \overline{C})(\overline{A} + \overline{B} + C) \qquad (2)$$

Direct synthesis of Eq. (2) results in the circuit of Fig. 3. However, further manipulation of the expression in (2) results in a more economical realization, as follows:

$$\begin{aligned}\overline{Y} &= AB(\overline{A} + \overline{B} + C) + A\overline{C}(\overline{A} + \overline{B} + C) \\ &\quad + \overline{B}\,\overline{A}(\overline{A} + \overline{B} + C) + \overline{B}\,\overline{C}(\overline{A} + \overline{B} + C) \\ &\quad + \overline{C}\,\overline{A}(\overline{A} + \overline{B} + C) + \overline{C}B(\overline{A} + \overline{B} + C) \\ &\quad + \overline{C}(\overline{A} + \overline{B} + C) \\ &= ABC + \overline{B}\,\overline{C} + \overline{A}\,\overline{B} + \overline{A}\,\overline{C} \\ &= ABC + \overline{A}(\overline{B} + \overline{C}) + \overline{B}\,\overline{C} \qquad (3)\end{aligned}$$

A direct realization of this expression results in the PDN shown in Fig. 4. This circuit requires 8 transistors (not counting the inverters).

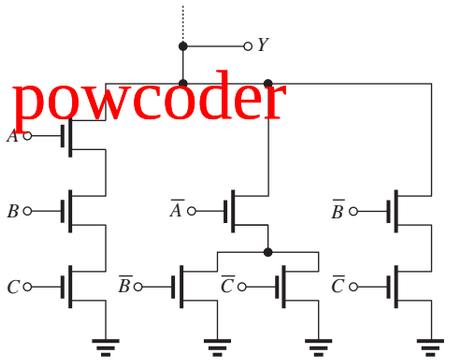


Figure 4

16.11 Direct realization of the given expression results in the PUN of the logic circuit shown in Fig. 1. The PDN shown is obtained as the dual of the PUN. Not shown are the two inverters needed to obtain $\overline{A}$ and $\overline{B}$.

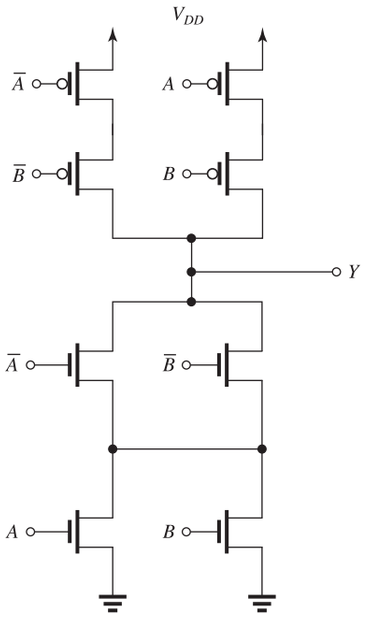


Figure 1

16.12 Direct realization of the given expression results in the PUN portion of the circuit shown in Fig. 1. The PDN is obtained as the dual of the PUN. Not shown are the three inverters needed to obtain $\overline{A}$, $\overline{B}$ and $\overline{C}$.

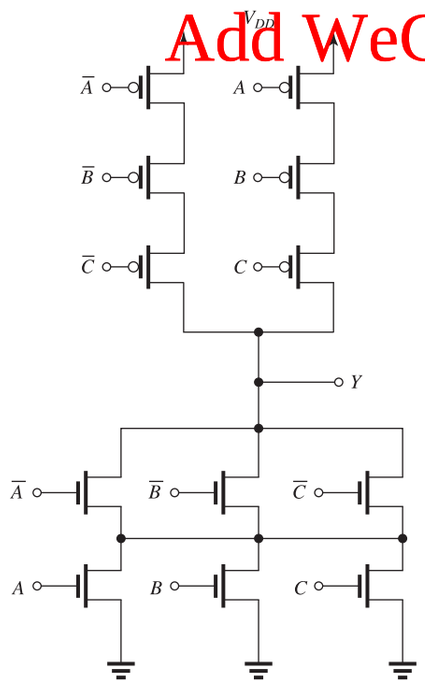


Figure 1

16.13 (a) Even-parity checker:

$$\overline{Y} = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}BC + A\overline{B}C + AB\overline{C}$$

See Fig. 1 on next page.

(b) This expression can be directly realized with the PDN shown in Fig. 1. Note that the circuit requires 12 transistors in addition to the three inverters needed to generate $\overline{A}$, $\overline{B}$, and $\overline{C}$.

(c) From inspection of the PDN in Fig. 1 we see that we can combine the two transistors controlled by $\overline{A}$ and the two transistors controlled by A. This results in the PDN realization shown in Fig. 2 which requires 10 transistors, not counting those in the inverters. See Fig. 2 on next page.

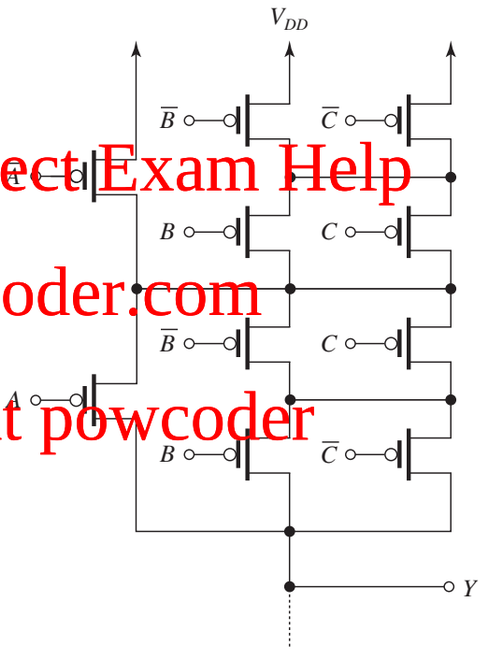


Figure 3

(d) The PUN in Fig. 3 can be obtained as the dual of the PDN in Fig. 2. Combining the PDN and the PUN gives the complete realization of the even-parity checker.

Note: The number of transistors in the PDN of Fig. 2 can be reduced by 2 by combining the two transistors in the bottom row that are controlled by C, and the two transistors that are controlled by $\overline{C}$. The resulting 8-transistor realization is shown in Fig. 4. However, it is not easy to obtain a PUN as a dual of this circuit. See Fig. 4 on next page.

This figure belongs to Problem 16.13, part (a).

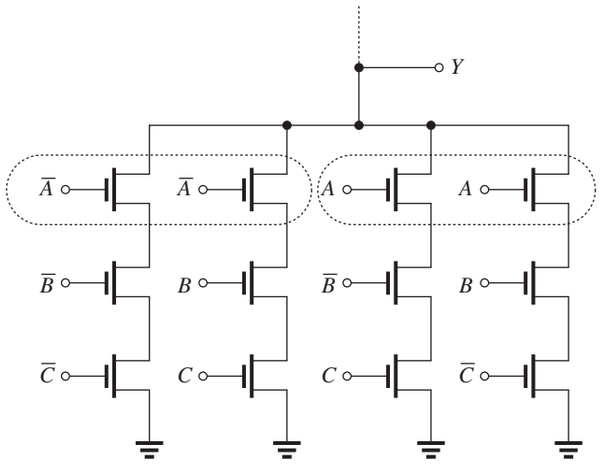


Figure 1

This figure belongs to Problem 16.13, part (c).

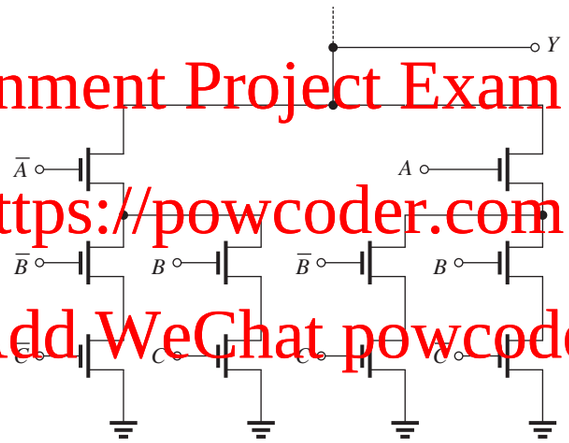


Figure 2

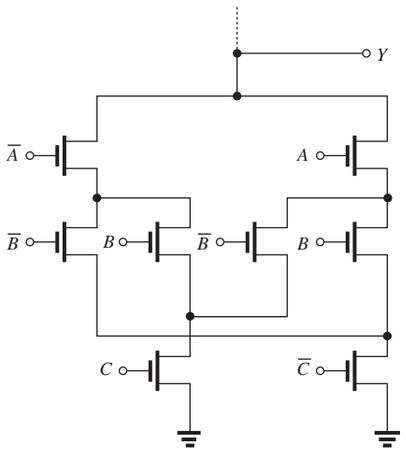


Figure 4

16.14 Odd-parity checker:

$$Y = AB\,\overline{C} + A\,\overline{B}C + \overline{A}\,BC + \overline{A}\,\overline{B}\,\overline{C}$$

$$= A(B\overline{C} + \overline{B}C) + \overline{A}(BC + \overline{B}\,\overline{C}) \qquad (1)$$

The Boolean expression in Eq. (1) can be directly realized by the PUN in Fig. 1. Recall that we use for the switch control variables the complements of the variables in the equation. It requires 10 transistors in addition to the three inverters needed to provide $\overline{A}$, $\overline{B}$ and $\overline{C}$. The dual of the PUN can be obtained and results in the PDN shown in Fig. 1.

This figure belongs to Problem 16.14.

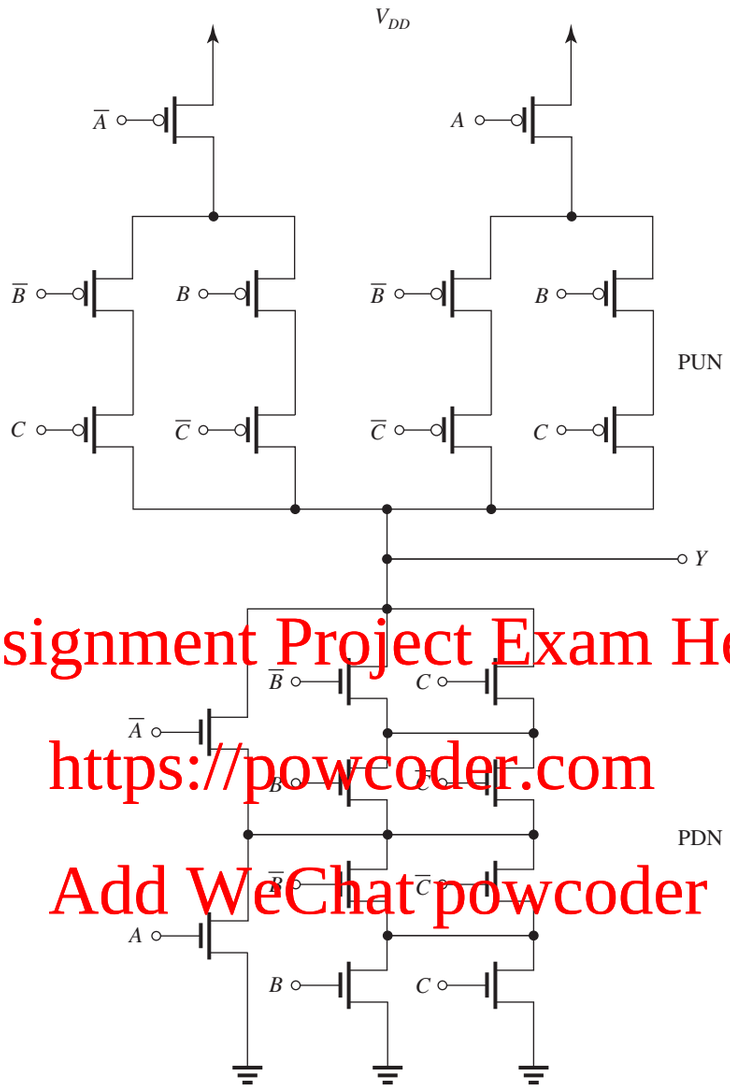


Figure 1

16.15 $S = \overline{A}B\,\overline{C} + \overline{A}\,\overline{B}C + A\overline{B}\,\overline{C} + ABC$

$= \overline{A}(B\overline{C} + \overline{B}C) + A(BC + \overline{B}\,\overline{C})$

This is the same function as that of the odd-parity checker in Problem 16.13. Thus the realization of the S function will be identical to that in Fig. 1 of Problem 16.13.

As for C_0 we write

$C_0 = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$

This expression can be minimized as follows:

$C_0 = (\overline{A} + A)BC + (\overline{B} + B)AC + (\overline{C} + C)AB$

$= BC + AC + AB = A(B + C) + BC$

which can be realized directly by the PUN of the circuit in Fig. 1 where the PDN is obtained as the dual network of the PUN. In addition to the 10 transistors, we need three inverters to generate $\overline{A}$, $\overline{B}$ and $\overline{C}$.

This figure belongs to Problem 16.15.

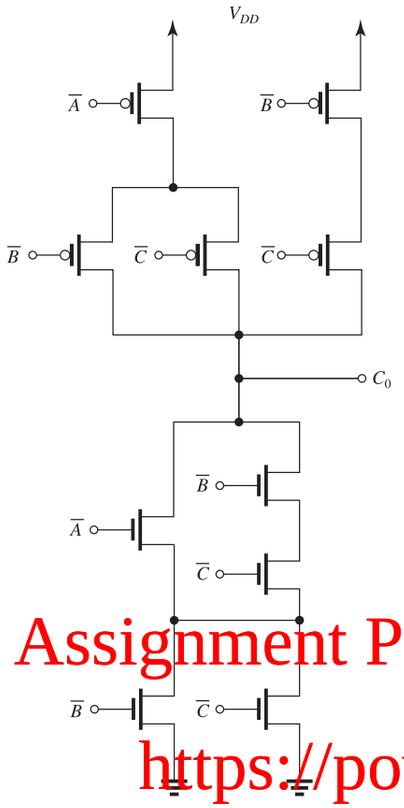


Figure 1

16.16 $NM_H = V_{OH} - V_{IH}$

$= 1.2 - 0.7 = 0.5$ V

$NM_L = V_{IL} - V_{OL}$

$= 0.5 - 0.1 = 0.4$ V

16.17 (a) $NM_H = V_{OH} - V_{IH}$

$= 1.5 - 1.2 = 0.3$ V

$NM_L = V_{IL} - V_{OL}$

$= 1.1 - 0.3 = 0.8$ V

(b)

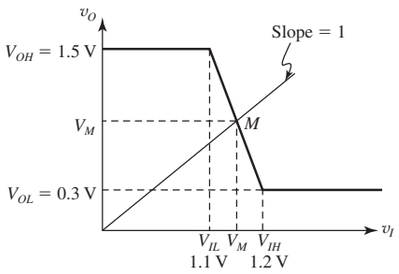


Figure 1

Refer to Fig. 1. Slope of the VTC in the transition region is:

$$\text{Slope} = \frac{V_{OH} - V_{OL}}{V_{IL} - V_{IH}}$$

$$= \frac{1.5 - 0.3}{1.1 - 1.2} = -12 \text{ V/V}$$

But the slope can also be expressed as

$$\text{Slope} = \frac{V_M - V_{OH}}{V_M - V_{IH}}$$

Thus,

$$\frac{V_M - 0.3}{V_M - 1.2} = -12$$

$\Rightarrow V_M = 1.13$ V

(c) The voltage gain in the transition region is equal to the slope found above, thus

Gain $= -12$ V/V

16.18 $NM_H = V_{OH} - V_{IH}$

$= 0.8V_{DD} - 0.6V_{DD} = 0.2V_{DD}$

$NM_L = V_{IL} - V_{OL}$

$= 0.4V_{DD} - 0.1V_{DD} = 0.3V_{DD}$

Width of transition region $= V_{IH} - V_{IL}$

$= 0.6V_{DD} - 0.4V_{DD} = 0.2V_{DD}$

For a minimum noise margin of 0.25 V, we have

$NM_H = 0.25$

$\Rightarrow 0.2V_{DD} = 0.25$

$\Rightarrow V_{DD} = 1.25$ V

16.19 (a) Refer to Fig. 16.17.

$$V_{OL} = V_{DD} \frac{R_{\text{on}}}{R + R_{\text{on}}}$$

$$= 1.8 \times \frac{0.1}{2 + 0.1} = 0.086 \text{ V}$$

$V_{OH} = V_{DD} = 1.8$ V

$NM_H = V_{OH} - V_{IH}$

$= 1.8 - 0.8 = 1$ V

$NM_L = V_{IL} - V_{OL}$

$= 0.6 - 0.086 = 0.514$ V

(b) Refer to Fig. 1.

$V_{OH} = V_{DD} - N \times 0.1 \times R$

$= 1.8 - N \times 0.1 \times 2$

$= 1.8 - 0.2N$

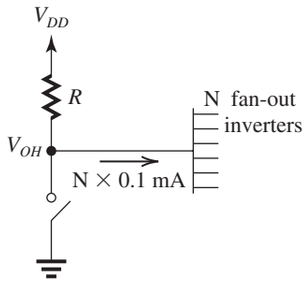


Figure 1

$NM_H = 1.8 - 0.2N - 0.8$

$= 1 - 0.2N$

For $NM_H \geqslant NM_L$, we have

$1 - 0.2N \geqslant 0.514$

$\Rightarrow N \leqslant 2.43$

which means

$N = 2$

(c) (i) When the inverter output is low,

$$P_D = \frac{V_{DD}^2}{R + R_{on}} = \frac{1.8^2}{2 + 0.1} \simeq 1.54 \text{ mW}$$

(ii) When the output is high and the inverter is driving two inverters, the current drawn from the supply is $2 \times 0.1 = 0.2$ mA, and thus the power dissipation is

$P_D = V_{DD} I_{DD} = 1.8 \times 0.2 = 0.36$ mW

16.20 For an ideal inverter:

$V_M = \frac{1}{2} V_{DD} = 0.9$ V

$V_{IL} = V_{IH} = V_M = 0.9$ V

$V_{OL} = 0$ V

$V_{OH} = V_{DD} = 1.8$ V

$NM_L = V_{IL} - V_{OL}$

$= 0.9 - 0 = 0.9$ V

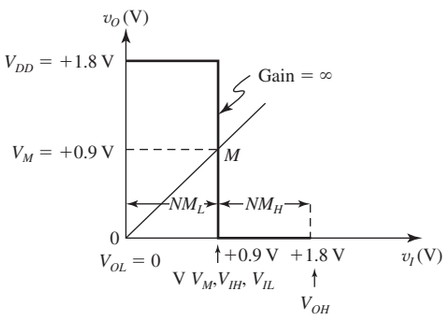


Figure 1

$NM_H = V_{OH} - V_{IH}$

$= 1.8 - 0.9 = 0.9$ V

The ideal transfer characteristic is shown in Fig. 1, from which we see that

Gain in transition region $= \infty$

16.21

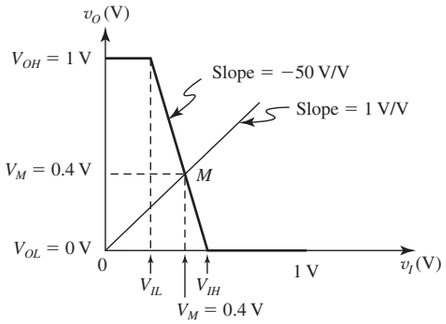


Figure 1

Figure 1 shows a sketch of the VTC where we have approximated the VTC in the transition region by a straight line with a slope equal to the maximum possible small-signal gain, namely 50 V/V. We can use the geometry of the VTC to determine V_{IH} and V_{IL} as follows:

$|\text{Slope}| = 50$

$= \frac{V_M}{V_{IH} - V_M}$

Thus,

$50 = \frac{0.4}{V_{IH} - 0.4}$

$\Rightarrow V_{IH} = 0.408$ V

Similarly,

$|\text{Slope}| = \frac{V_{OH}}{V_{IH} - V_{IL}}$

$50 = \frac{1}{0.408 - V_{IL}}$

$\Rightarrow V_{IL} = 0.388$ V

$NM_H = V_{OH} - V_{IH}$

$= 1 - 0.408 = 0.592$ V

$NM_L = V_{IL} - V_{OL}$

$= 0.388 - 0 = 0.388$ V

Since we approximated the VTC in the transition region by a straight line, the large-signal voltage gain will be equal to the small-signal voltage gain,

$= -50$ V/V

16.22 Here, $V_{OH} = 0.9$ V, and $V_{OL} = 0.0$ V

Also, $V_{IH} - V_{IL} \leq 0.9/3 = 0.3$ V (1)

Now, the noise margins are "within 30% of one other." Thus, $NM_H = (1 \pm 0.3)\, NM_L$ or $NM_L = (1 \pm 0.3)\, NM_H$. Thus, they remain "within" either $NM_H = 1.3NM_L$ or $NM_L = 1.3NM_H$, in which case either $NM_L = 0.769NM_H$ or $N_{MH} = 0.769NM_L$

For the former case:

$0.769\,(V_{OH} - V_{IH}) = (V_{IL} - V_{OL})$ or

$0.769\,(0.9 - V_{IH}) = V_{IL} - 0$, whence

$V_{IL} = 0.692 - 0.769V_{IH}$

Now, from (1), $V_{IH} = V_{IL} + 0.3$

Thus,

$V_{IL} = 0.692 - 0.769\,(V_{IL} + 0.3)$

$= 0.461 - 0.769V_{IL}$

and $V_{IL} = 0.461/1.769 = 0.26$ V

whence $V_{IH} = 0.3 + 0.26 = 0.56$ V

Alternatively, $NM_H = 0.769NM_L$ and

$(V_{OH} - V_{IH}) = 0.769\,(V_{IL} - V_{OL})$ or

$0.9 - V_{IH} = 0.769V_{IL} - 0$ and

$V_{IH} = 0.9 - 0.769V_{IL}$, with (1),

$V_{IL} + 0.3 = 0.9 - 0.769V_{IL}$, and

$1.769V_{IL} = 0.6$, whence $V_{IL} = 0.34$ V

and $V_{IH} = 0.3 + 0.34 = 0.64$

Thus, overall, $V_{OH} = 0.9$ V, $V_{OL} = 0.0$ V,

V_{IH} ranges from 0.56 V to 0.64 V, and

V_{IL} ranges from 0.26 V to 0.34 V, in

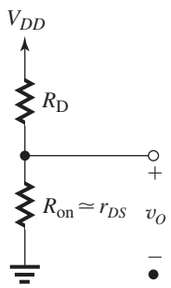
which case the margins can be as low as

$NM_L = V_{IL} - V_{OL} = 0.26$ V and

$NM_H = V_{OH} - V_{IH} = 0.9 - 0.64 = 0.26$ V

and as high as 0.34 V.

16.23



Equivalent circuit for output-low state

The output-high level for the simple inverter circuit shown in Fig. 16.12 of the text is

$V_{OH} = V_{DD} \Rightarrow V_{DD} = 1.0$ V.

When the output is low, the current drawn from the supply can be calculated as

$$I = \frac{V_{DD}}{R_D + R_{on}} = 30\ \mu\text{A}$$

Therefore: $R_D + r_{DS} = \dfrac{1.0}{30 \times 10^{-6}} = 33.3\ \text{k}\Omega$

Also:

$$V_{OL} = 0.05\ \text{V} = \frac{r_{DS}}{R_D + r_{DS}} \times V_{DD}$$

$$\Rightarrow r_{DS} = 33.3\ \text{k}\Omega \times \frac{0.05}{1.0} = 1.67\ \text{k}\Omega$$

Hence: $R_D = 33.3\ \text{K} - 1.67\ \text{K} = 31.6\ \text{k}\Omega$

$$r_{DS} = \frac{1}{\mu_n C_{ox} \dfrac{W}{L}(V_{GS} - V_t)}$$

$$= \frac{1}{540 \times 10^{-6} \times \dfrac{W}{L}(1.0 - 0.35)}$$

$$= 1.67\ \text{k}\Omega$$

$$\Rightarrow \frac{W}{L} = 1.7$$

When the output is low:

$P_D = V_{DD} I_{DD} = 1.0 \times 30\ \mu\text{A} = 30\ \mu\text{W}$

When the output is high, the transistor is off: $P_D = 0$ W

16.24 Refer to Example 16.2 from the text:

$V_{OH} = V_{DD} = 1.2$ V

The power drawn from the supply during the low-output state is

$P_{DD} = V_{DD} I_{DD} \Rightarrow 50\ \mu\text{W} = 1.2 \times I_{DD}$

$\Rightarrow I_{DD} = 41.7\ \mu\text{A}$

In this case:

$$I_{DD} = \frac{V_{DD} - V_{OL}}{R_D} \Rightarrow 41.7\ \mu\text{A} = \frac{1.2 - 0.05}{R_D}$$

$\Rightarrow R_D = 27.6\ \text{k}\Omega$

In order to determine $\dfrac{W}{L}$, we note that

$$k_n R_D = 1/V_X \text{ or } k'_n \frac{W}{L} R_D = \frac{1}{V_X}$$

Therefore, we need to first calculate V_X using Eq. (16.22) from the text.

$$V_{OL} = \frac{V_{DD}}{1 + \dfrac{V_{DD} - V_t}{V_X}} \text{ or equivalently}$$

$$0.05 \text{ V} = \frac{1.2}{1 + \dfrac{1.2 - 0.4}{V_X}}$$

$$\Rightarrow V_X = \frac{0.8}{23} = 0.035 \text{ V}$$

Hence, $k_n' \dfrac{W}{L} R_D = \dfrac{1}{V_x}$ gives

$$500 \times 10^{-6} \times \frac{W}{L} \times 27.6 \times 10^3 = \frac{1}{0.035} \Rightarrow$$

$$\frac{W}{L} = 2.1$$

Using Eq. (16.12), we obtain

$$V_{IL} = V_t + V_X = 0.4 + 0.035 = 0.435 \text{ V}$$

From Eq. (16.14) we obtain

$$V_M = V_t + \sqrt{2\,(V_{DD} - V_t)V_x + V^2{}_x} - V_x$$

$$= 0.4 + \sqrt{2\,(1.2 - 0.4)\,0.035 + 0.035^2} - 0.035$$

$$V_M = 0.8 \text{ V}$$

From Eq. (16.20) we get

$$V_{IH} = V_t + 1.63\sqrt{V_{DD}V_x} - V_x$$

$$= 0.4 + 1.63\sqrt{1.2 \times 0.035} - 0.035 = 0.7 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 1.2 - 0.7 = 0.5 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.435 - 0.05 = 0.385 \text{ V}$$

16.25 $V_t = 0.3V_{DD}$, $V_M = V_{DD}/2$

From Eq. (16.13), we obtain

$$V_x\big|_{V_M = \frac{V_{DD}}{2}} = \frac{\left(\dfrac{V_{DD}}{2} - V_t\right)^2}{V_{DD}}$$

$$= \frac{(0.5V_{DD} - 0.3V_{DD})^2}{V_{DD}}$$

$$\Rightarrow V_x = 0.04V_{DD}$$

$$V_{OH} = V_{DD}$$

From Eq. (16.12), we get

$$V_{IL} = V_t + V_x = 0.3V_{DD} + 0.04V_{DD}$$

$$= 0.34V_{DD}$$

From Eq. (16.20), we obtain

$$V_{IH} = V_t + 1.63\sqrt{V_{DD}V_x} - V_x$$

$$= 0.3V_{DD} + 1.63\sqrt{V_{DD} \times 0.04V_{DD}} - 0.04V_{DD}$$

$$= 0.586V_{DD}$$

From Eq. (16.22), we get

$$V_{OL} = \frac{V_{DD}}{1 + (V_{DD} - V_t)/V_x}$$

$$= \frac{V_{DD}}{1 + \dfrac{V_{DD} - 0.3V_{DD}}{0.04V_{DD}}} = 0.054V_{DD}$$

$$NM_H = V_{OH} - V_{IH}$$

$$= V_{DD} - 0.586V_{DD} = 0.414V_{DD}$$

$$NM_L = V_{IL} - V_{OL}$$

$$= 0.34V_{DD} - 0.054V_{DD} = 0.286V_{DD}$$

For $V_{DD} = 1.0$ V:

$V_x = 0.04$ V, $V_{OH} = 1.0$ V, $V_{IL} = 0.34$ V,

$V_{IH} = 0.586$ V, $V_{OL} = 0.054$ V,

$NM_H = 0.414$ V, $NM_L = 0.286$ V

$$P_D = V_{DD}I_D$$

$$= V_{DD} \times \frac{V_{DD} - V_{OL}}{R_D}$$

Substituting for R_D from

$$R_D = \frac{1}{k_n V_x}$$

we obtain

$$P_D = V_{DD}(V_{DD} - 0.054V_{DD}) \times k_n \times 0.04V_{DD}$$

$$P_D = 0.038V_{DD}^3 \times k_n \left(\frac{W}{L}\right)$$

$$= 0.038 \times 1.0^3 \times 0.54 \times 10^{-3}\left(\frac{W}{L}\right)$$

$$= 0.021\left(\frac{W}{L}\right), \text{ mW}$$

For $P_D = 100\ \mu\text{W} = 0.1$ mW, we obtain

$$0.1 = 0.021\left(\frac{W}{L}\right)$$

$$\Rightarrow \frac{W}{L} = 4.9$$

$$R_D = \frac{1}{k_n V_x}$$

$$= \frac{1}{0.54 \times 4.9 \times 0.04}$$

$$= 9.4 \text{ k}\Omega$$

16.26

(a) $v_I = 0$, so Q_N is off

Q_P is in the triode region but conducts zero current, so the output voltage is equal to V_{DD}
$V_{OH} = V_{DD} = 1.0$ V

(b) $v_I = V_{DD}$, and the output is likely lower than V_t, such that Q_P is in the saturation region and Q_N is in the triode region

$$i_{DP} = \frac{1}{2}k_p(V_{DD} - V_t)^2$$

$$i_{DN} = k_n\left[(V_{DD} - V_t)V_{OL} - \frac{V_{OL}^2}{2}\right]$$

Equating i_{DP} and i_{DN} yields a quadratic equation that can be solved to obtain

$$V_{OL} = (V_{DD} - V_t)(1 - \sqrt{1 - k_p/k_n})$$

(c) $V_{OL} = (1 - 0.35)(1 - \sqrt{1 - 1/5.4}) = 63$ mV

16.27

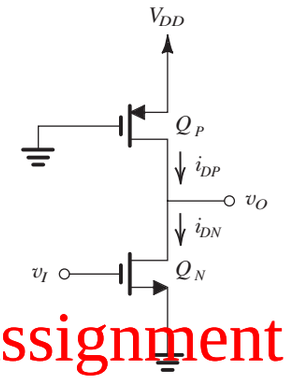


Figure 1

Referring to Fig. 1, we can assume that $V_M < V_t$ such that Q_P operates in the triode region. Q_N operates in the saturation region.

$$i_{DP} = k_p\left[(V_{DD} - V_t)(V_{DD} - V_M) - \frac{(V_{DD} - V_M)^2}{2}\right]$$

$$i_{DN} = \frac{k_n}{2}(V_M - V_t)^2$$

Equating i_{DP} and i_{DN}

$$\frac{1}{2}k_n(V_M - V_t)^2 = k_p\left[(V_{DD} - V_t)(V_{DD} - V_M) - \frac{(V_{DD} - V_M)^2}{2}\right]$$

$$\Rightarrow \frac{1}{2}r(V_M^2 - 2V_tV_M + V_t^2) = \frac{1}{2}V_{DD}^2 - V_{DD}V_t + V_MV_t - \frac{1}{2}V_M^2$$

$$\Rightarrow (r+1)V_M^2 - 2(r+1)V_tV_M + (r+1)V_t^2 = V_{DD}^2 - 2V_{DD}V_t + V_t^2$$

$$\Rightarrow (r+1)(V_M - V_t)^2 = (V_{DD} - V_t)^2$$

$$\Rightarrow V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{r+1}}$$

16.28 (a) To obtain $V_M = V_{DD}/2$, the inverter must be matched, thus

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} = 5.4$$

$$\Rightarrow W_p = 5.4W_n = 5.4 \times 1.5 \times 65 = 527 \text{ nm}$$

Silicon area $= W_nL_n + W_pL_p$

$= 1.5 \times 65 \times 65 + 5.4 \times 1.5 \times 65 \times 65$

$= 1.5 \times 65 \times 65(1 + 5.4)$

$= 40,560 \text{ nm}^2$

(b) $V_{OH} = V_{DD} = 1$ V

$V_{OL} = 0$ V

To obtain V_{IH}, we use Eq. (16.35):

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$$

$$= \frac{1}{8}(5 \times 1 - 2 \times 0.35)$$

$= 0.5375$ V

To obtain V_{IL}, we use Eq. (16.36):

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

$$= \frac{1}{8}(3 \times 1 + 2 \times 0.35)$$

$= 0.4625$ V

The noise margins can now be found as

$NM_H = V_{OH} - V_{IH}$

$= 1 - 0.5375 = 0.4625$ V

$NM_L = V_{IL} - V_{OL}$

$= 0.4625 - 0 = 0.4625$ V

The noise margins are equal at approximately 0.46 V; a result of the matched design of the inverter.

(c) Since the inverter is matched, the output resistances in the two states will be equal. Thus,

$$r_{DSP} = r_{DSN} = 1\Big/\left[(\mu_nC_{ox})\left(\frac{W}{L}\right)_n(V_{DD} - V_t)\right]$$

$$= \frac{1}{0.54 \times 1.5(1 - 0.35)} = 1.9 \text{ k}\Omega$$

16.29 $V_{OH} = 2.5$ V

$V_{OL} = 0$ V

(a) For the matched case we have

$W_p = 3.5W_n$

$V_M = \frac{1}{2}V_{DD} = 1.25$ V

Eq. (16.35): $V_{IH} = \frac{1}{8}(5\ V_{DD} - 2\ V_t)$

$$= \frac{1}{8}(5 \times 2.5 - 2 \times 0.5)$$

$= 1.4375$ V

Eq. (16.36): $V_{IL} = \frac{1}{8}(3\ V_{DD} + 2\ V_t)$

$= \frac{1}{8}(3 \times 2.5 + 2 \times 0.5)$

$= 1.0625$ V

$NM_H = NM_L = 1.0625$ V

Silicon area $= W_n L_n + W_p L_p$

$= 1.5 \times 0.25 \times 0.25 + 3.5 \times 1.5 \times 0.25 \times 0.25$

$= 4.5 \times 1.5 \times 0.25^2 = 0.42\ \mu\text{m}^2$

(b) $W_p = W_n$ (minimum-size design):

Eq. (16.40): $r = \sqrt{\frac{\mu_p}{\mu_n}\frac{W_p}{W_n}} = \sqrt{\frac{1}{3.5} \times 1} = 0.53$

Eq. (16.39): $V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{tn}}{r + 1}$

$= \frac{0.53(2.5 - 0.5) + 0.5}{0.53 + 1}$

$= 1.02$ V

Thus, V_M shifts to the left by 0.23 V. Assuming V_{IL} shifts by approximately the same amount, then

$V_{IL} \simeq 1.0625 - 0.23 \simeq 0.83$ V

Since $NM_L = V_{IL}$, NM_L will be reduced by approximately 22% (relative to the matched case).

Silicon area $= W_n L_n + W_p L_p$

$= 1.5 \times 0.25 \times 0.25 + 1.5 \times 0.25 \times 0.25$

$= 3 \times 0.25^2 = 0.19\ \mu\text{m}^2$

which is a reduction of 55% relative to the matched case.

(c) $W_p = 2W_n$ (a compromise design):

Eq. (16.40): $r = \sqrt{\frac{\mu_p}{\mu_n}\frac{W_p}{W_n}} = \sqrt{\frac{1}{3.5} \times \frac{2}{1}}$

$= 0.756$

Eq. (16.39): $V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{tn}}{r + 1}$

$= \frac{0.756(2.5 - 0.5) + 0.5}{0.756 + 1}$

$= 1.15$ V

Thus, relative to the matched case the switching point (V_M) is shifted left by $(1.25 - 1.15) = 0.1$ V. Assuming that V_{IL} is reduced by approximately the same amount, then

$V_{IL} = 1.0625 - 0.1 = 0.9625$ V

Thus, NM_L which equals V_{IL} is reduced by about 9% (relative to the matched case).

Silicon area $= W_n L_n + W_p L_p$

$= 1.5 \times 0.25 \times 0.25 + 2 \times 1.5 \times 0.25 \times 0.25$

$= 3 \times 1.5 \times 0.25^2$

$= 0.28\ \mu\text{m}^2$

Compared to the matched case, the silicon area is reduced by 33%.

16.30 Q_N will be operating in the triode region, thus

$$I_{Dn} = k_n'\left(\frac{W}{L}\right)_n\left[(V_{DD} - V_{tn})V_O - \frac{1}{2}V_O^2\right]$$

For $V_{tn} = 0.3V_{DD}$ and $V_O = 0.1V_{DD}$, we have

$$I_{Dn} = k_n'\left(\frac{W}{L}\right)_n \left[(V_{DD} - 0.3V_{DD}) \times 0.1V_{DD} - \frac{1}{2} \times 0.1^2 V_{DD}^2\right]$$

$= k_n'(W/L)_n(0.07V_{DD}^2 - 0.005V_{DD}^2)$

$= 0.065k_n'(W/L)_n V_{DD}^2$ Q.E.D.

For $V_{DD} = 1.2$ V, $k_n' = 0.5$ mA/V^2 and $I_{Dn} = 0.1$ mA, we have

$0.1 = 0.065 \times 0.5(W/L)_n \times 1.2^2$

$\Rightarrow \left(\frac{W}{L}\right)_n = 2.14$

16.31 For $v_I = +1.5$ V, Q_N will be conducting and operating in the triode region while Q_P will be off. Thus, the incremental resistance to the left of node A will be r_{DSN},

$$r_{DSN} = \frac{1}{k_n(V_I - V_{tn})}$$

$$= \frac{1}{0.25(1.5 - 0.4)} = 3.64\ \text{k}\Omega$$

Thus,

$$v_a = 100\left(\frac{3.64}{3.64 + 100}\right)$$

$= 3.5$ mV

For $v_I = -1.5$ V, Q_N will be off but Q_P will be operating in the triode region with a resistance r_{DSP},

$$r_{DSP} = \frac{1}{k_p(V_{SGP} - |V_{tp}|)}$$

$$= \frac{1}{0.05(1.5 - 0.4)} = 18.2\ \text{k}\Omega$$

Thus,

$$v_a = 100\left(\frac{18.2}{18.2 + 100}\right) = 15.4\ \text{mV}$$

16.32 From Eq. (16.39) we have

$$V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{tn}}{r + 1}$$

$$rV_M + V_M = r(V_{DD} - |V_{tp}|) + V_{tn}$$

$$r(V_{DD} - |V_{tp}| - V_M) = V_M - V_{tn}$$

$$\Rightarrow r = \frac{V_M - V_{tn}}{V_{DD} - |V_{tp}| - V_M} \qquad \text{Q.E.D.}$$

For $V_{DD} = 1.0$ V, $V_{tn} = |V_{tp}| = 0.35$ V, to obtain $V_M = 0.6V_{DD}$, we need

$$r = \frac{0.6 \times 1.0 - 0.35}{1.0 - 0.35 - 0.6 \times 1.0}$$

$$= 5$$

But,

$$r = \sqrt{\frac{\mu_p}{\mu_n}\frac{W_p}{W_n}}$$

$$5 = \sqrt{\frac{1}{5.4} \times \frac{W_p}{W_n}}$$

$$\frac{W_p}{W_n} = 5^2 \times 5.4 = 135$$

16.33 The current reaches its peak at $v_I = V_M = \frac{V_{DD}}{2}$. At this point, both Q_N and Q_P are operating in the saturation region and conducting a current

$$I_{DP} = I_{DN} = \frac{1}{2}k'_n\left(\frac{W}{L}\right)_n\left(\frac{V_{DD}}{2} - V_t\right)^2$$

$$= \frac{1}{2} \times 540 \times 1.5\left(\frac{1.0}{2} - 0.35\right)^2$$

$$= 9.1\ \mu\text{A}$$

16.34 Refer to Example 16.3 except here:

$V_{DD} = 1.3$ V, $V_{tn} = |V_{tp}| = 0.4$ V, $\mu_n = 4\ \mu_p$, and $\mu_n C_{ox} = 0.5$ mA/V^2. Also, Q_N and Q_P have $L = 0.13\ \mu$m and $(W/L)_n = 1.5$.

(a) For $V_M = V_{DD}/2 = 0.65$ V, the inverter must be matched, thus

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} = 4$$

Since $W_n/L = 1.5$,
$W_n = 1.5 \times 0.13 = 0.195\ \mu$m. Thus,

$$W_p = 4 \times 0.195 = 0.78\ \mu\text{m}$$

For this design, the silicon area is

$$A = W_nL + W_pL = L(W_n + W_p)$$

$$= 0.13(0.195 + 0.78) = 0.127\ \mu\text{m}^2$$

(b) $V_{OH} = V_{DD} = 1.3$ V

$V_{OL} = 0$ V

To obtain V_{IH}, we use Eq. (16.35):

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$$

$$= \frac{1}{8}(5 \times 1.3 - 2 \times 0.4)$$

$$= 0.7125 \text{ V}$$

To obtain V_{IL}, we use Eq. (16.36):

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

$$= \frac{1}{8}(3 \times 1.3 + 2 \times 0.4)$$

$$= 0.5875 \text{ V}$$

We can now compute the noise margins as

$$NM_H = V_{OH} - V_{IH} = 1.3 - 0.7125$$

$$= 0.5875 \text{ V} \simeq 0.59 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.5875 - 0$$

$$= 0.5875 \text{ V} \simeq 0.59 \text{ V}$$

For $v_I = V_{IH} = 0.7125$ V, we can obtain the corresponding value of v_O by substituting in Eq. (16.34):

$$v_O = V_{IH} - \frac{V_{DD}}{2} = 0.7125 - 0.65 = 0.0625 \text{ V}$$

Thus, the worst-case value of V_{OL} is $V_{O\max} = 0.0625 \simeq 0.06$ V, and the noise margin NM_L reduces to

$$NM_L = 0.5875 - 0.0625 = 0.5250 \text{ V}$$

or approximately 0.53 V.

From symmetry, we can obtain the value of v_O corresponding to $v_I = V_{IL}$ as

$$v_O = V_{DD} - 0.0625$$

$$= 1.3 - 0.0625 = 1.2375 \text{ V} \simeq 1.24 \text{ V}$$

Thus, the worst-case value of V_{OH} is $V_{OH\min} \simeq 1.24$ V, and the noise margin NM_H is reduced to

$$NM_H = V_{OH\min} - V_{IH}$$

$$= 1.2375 - 0.7125 = 0.5250 \text{ V}$$

or approximately 0.53 V.

Note that the reduction in the noise margin (about 0.06 V) is slight.

(c) The output resistance of the inverter in the low-output state is

$$r_{DSN} = \frac{1}{\mu_n C_{ox}(W/L)_n(V_{DD} - V_{tn})}$$

$$= \frac{1}{0.5 \times 1.5(1.3 - 0.4)} = 1.48 \text{ k}\Omega$$

Since Q_N and Q_P are matched, the output resistance in the high-output state will be equal, that is,

$$r_{DSP} = r_{DSN} = 1.48 \text{ k}\Omega$$

(d) If the inverter is biased to operate at $v_I = v_O = V_M = 0.65$ V, then each of Q_N and Q_P will be operating at an overdrive voltage $V_{OV} = V_M - V_t = 0.65 - 0.4 = 0.25$ V and will be conducting equal dc currents I_D of

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n V_{OV}^2$$

$$= \frac{1}{2} \times 500 \times 1.5 \times 0.25^2$$

$$= 23.4 \text{ μA}$$

Thus, Q_N and Q_P will have equal transconductances:

$$g_{mn} = g_{mp} = \frac{2I_D}{V_{OV}} = \frac{2 \times 23.4}{0.25} = 0.19 \text{ mA/V}$$

Transistors Q_N and Q_P will have output resistances r_{on} and r_{op} given by

$$r_{on} = \frac{V_{An}}{I_D}$$

$$r_{op} = \frac{|V_{Ap}|}{I_D}$$

Since no values are given for V_{An} and V_{Ap} we shall use the data in Table K.1, namely

$$V'_{An} = 5 \text{ V/μm and } |V'_{Ap}| = 6 \text{ V/μm}$$

Thus,

$$V_{An} = 5 \times 0.13 = 0.65 \text{ V}$$

$$|V_{Ap}| = 6 \times 0.13 = 0.78 \text{ V}$$

$$r_{on} = \frac{0.65 \text{ V}}{23.4 \text{ μA}} = 27.8 \text{ k}\Omega$$

$$r_{op} = \frac{0.78 \text{ V}}{23.4 \text{ μA}} = 33.3 \text{ k}\Omega$$

We can now compute the voltage gain at M as

$$A_v = -(g_{mn} + g_{mp})(r_{on} \parallel r_{op})$$

$$= -(0.19 + 0.19)(27.8 \parallel 33.3)$$

$$= -5.8 \text{ V/V}$$

When the straight line at M of slope -5.8 V/V is extrapolated, it intersects the line $v_O = 0$ at $\left[0.65 + \frac{0.65}{5.8}\right] = 0.762$ V and the line $v_O = V_{DD}$ at $\left[0.65 - \frac{0.65}{5.8}\right] = 0.538$ V. Thus the width of the transition region can be considered $(0.762 - 0.538) = 0.224$ V.

(e) For $W_p = W_n$, the parameter r can be found from Eq. (16.40):

$$r = \sqrt{\frac{\mu_p W_p}{\mu_n W_n}} = \sqrt{\frac{1}{4} \times 1} = 0.5$$

The corresponding value of V_M can be determined from Eq. (16.39) as

$$V_M = \frac{0.5(1.3 - 0.4) + 0.4}{0.5 + 1} = 0.57 \text{ V}$$

Thus, V_M shifts by only -0.08 V. We can estimate the reduction in NM_L to be approximately equal to the shift in V_M, that is, NM_L becomes

$$NM_L = 0.5875 - 0.08 \simeq 0.51 \text{ V}$$

The silicon area for this design can be computed as follows:

$$A = L(W_n + W_p)$$

$$= 0.13(1.5 \times 0.13 + 0.5 \times 0.13)$$

$$= 0.051 \text{ μm}^2$$

This represents a 60% reduction from the matched case!

(f) For $W_p = 2W_n$, we have

$$r = \sqrt{\frac{1}{4} \times 2} = \frac{1}{\sqrt{2}} = 0.707$$

$$V_M = \frac{0.707(1.3 - 0.4) + 0.4}{0.707 + 1} = 0.61 \text{ V}$$

Thus, relative to the matched case, V_M is reduced by only 0.04 V. Correspondingly, NM_L will be reduced by approximately an equal amount, thus NM_L becomes

$$NM_L \simeq 0.59 - 0.04 = 0.55 \text{ V}$$

In this case, the silicon area required is

$$A = L(W_n + W_p) = L \times 3W_n$$

$$= 0.13 \times 3 \times 1.5 \times 0.13$$

$$= 0.076 \text{ μm}^2$$

which represents a 40% reduction relative to the matched case.

16.35 (a) $W_p = 1.5 \times 2.0 \times 28 \text{ nm} = 84 \text{ nm}$

(b) $V_{OH} = 0.9 \text{ V}$

$V_{OL} = 0 \text{ V}$

$V_{IH} = \frac{1}{8}(5 \times 0.9 - 2 \times 0.3) = 0.49 \text{ V}$

$V_{IL} = \frac{1}{8}(3 \times 0.9 + 2 \times 0.3) = 0.41 \text{ V}$

$NM_H = 0.9 - 0.49 = 0.41 \text{ V}$

$NM_L = 0.41 - 0 = 0.41 \text{ V}$

(c) $r_{DSN} = \dfrac{1}{0.75 \times 2 \times (0.9 - 0.3)} = 1.11 \text{ k}\Omega$

$$r_{DSP} = \frac{1}{\dfrac{0.75}{1.5} \times 2 \times 1.5 \times (0.9 - 0.3)}$$

$= 1.11 \text{ k}\Omega$

(d) $r = \sqrt{\dfrac{1}{1.5} \times 1} = 0.816$

$V_M = \dfrac{0.816 \times (0.9 - 0.3) + 0.3}{1 + 0.816} = 0.43 \text{ V}$