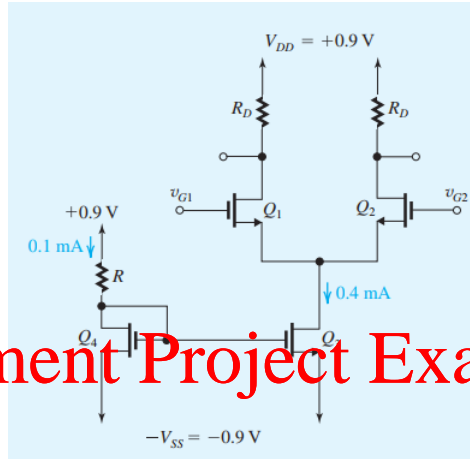


**6.1** Design the circuit in Fig. 1 to obtain a dc voltage of  $+0.1\text{V}$  at each of the drains of  $Q_1$  and  $Q_2$  when  $v_{G1} = v_{G2} = 0\text{V}$ . Operate all transistors at  $V_{ov} = 0.15\text{V}$  and assume that for the process technology in which the circuit is fabricated,  $V_{in} = 0.4\text{V}$  and  $\mu_n C_{ox} = 400 \mu\text{A}/\text{V}^2$ . Neglect channel-length modulation. Determine the values of  $R$ ,  $R_D$ , and  $W/L$  ratios of  $Q_1$ ,  $Q_2$ ,  $Q_3$ , and  $Q_4$ . What is the input common-mode voltage range for your design?

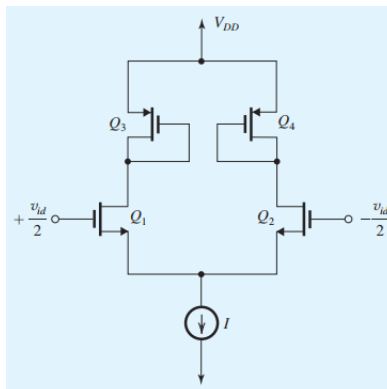


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**6.2** Figure 2 shows a MOS differential amplifier with the drain resistors  $R_D$  implemented using diode-connected PMOS transistors,  $Q_3$  and  $Q_4$ . Let  $Q_1$  and  $Q_2$  be matched, and  $Q_3$  and  $Q_4$  be matched.

- Find the differential half-circuit and use it to derive an expression for  $A_d$  in terms of  $g_{m1,2}$ ,  $g_{m3,4}$ ,  $r_{o1,2}$ , and  $r_{o3,4}$ .
- Neglecting the effect of the output resistances  $r_o$ , find  $A_d$  in terms of  $\mu_n$ ,  $\mu_p$ ,  $(\frac{W}{L})_{1,2}$ ,  $(\frac{W}{L})_{3,4}$ .
- if  $\mu_n = 4 \mu_p$  and all four transistors have the same channel length, find  $(W_{1,2}/W_{3,4})$  that results in  $A_d = 10 \text{ V/V}$ .



**6.3** Figure 3 shows a circuit for a differential amplifier with an active load. Here  $Q_1$  and  $Q_2$  form the differential pair, while the current source transistors  $Q_4$  and  $Q_5$  form the active loads for  $Q_1$  and  $Q_2$ , respectively. The dc bias circuit that establishes an appropriate dc voltage at the drains of  $Q_1$  and  $Q_2$  is not shown. It is required to design the circuit to meet the following specifications:

- (a) Differential gain  $A_d = 50$  V/V.
- (b)  $I_{REF} = I = 200 \mu A$
- (c) The dc voltage at the gates of  $Q_6$  and  $Q_3$  is  $+0.8V$ .
- (d) The dc voltage at the gates of  $Q_7$ ,  $Q_4$ , and  $Q_5$  is  $-0.8V$ .

The technology available is specified as follows:  $\mu_n C_{ox} = 2.5\mu_p C_{ox} = 250 \mu A/V^2$ ;  $V_{tn} = |V_{tp}| = 0.5V$ ,  $V_{An} = |V_{Ap}| = 10$  V. Specify the required value of  $R$  and the W/L ratios for transistors. Also specify  $L_D$  and  $|V_{GS}|$  at which each transistor is operating. For dc bias calculations you may neglect channel-length modulation.

