9.1

Solution:

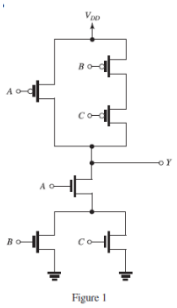


Figure 1

The logic function realized can be written from the PDN as:

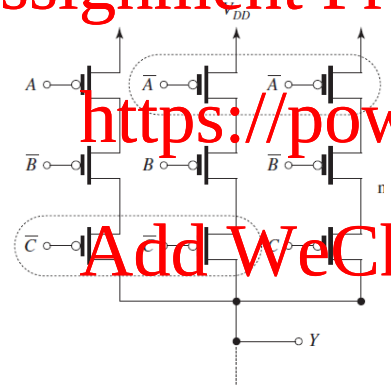
$\overline{Y} = A(B + C)$ or equivalently:

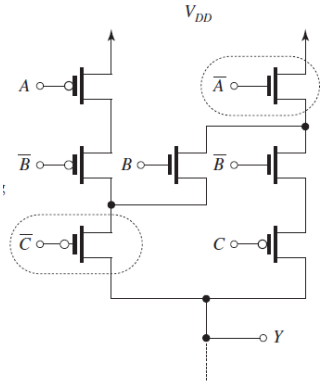
$Y = \overline{A(B + C)}$

9.2:

Solution:

Inspecting the PUN circuit reveal the potential for eliminating two transistors through what is known as path merging.





However, an alternative way to synthesize a PDN with a lower number of transistors. By using the DeMorgan's law:

$$\overline{Y} = \overline{\overline{A}BC}.\overline{A\overline{B}C}.\overline{AB\overline{C}} = (A + \overline{B} + \overline{C})(\overline{A} + B + \overline{C})(\overline{A} + \overline{B} + C)$$

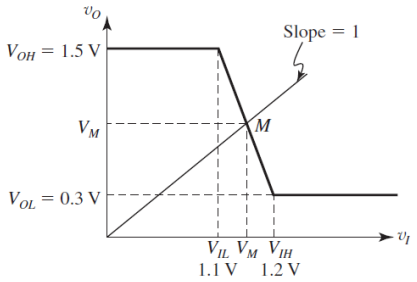
9.3:

Solution:

$$\mathrm{NM_H} = \mathrm{V_{OH}} - \mathrm{V_{IH}} = 1.5 - 1.2 = 0.3\ \mathrm{V}$$

$$\mathrm{NM_L} = \mathrm{V_{IL}} - \mathrm{V_{OL}} = 1.1 - 0.3 = 0.8\ \mathrm{V}$$

b)



Slope = $\frac{\mathrm{V_{OH}} - \mathrm{V_{OL}}}{\mathrm{V_{IL}} - \mathrm{V_{IH}}} = \frac{1.5-0.3}{1.1-1.2} = -12$

Thus,

$$\frac{\mathrm{V_M} - 0.3}{\mathrm{V_M} - 1.2} = -12 \rightarrow \mathrm{V_M} = 1.13\ \mathrm{V}$$

C) The voltage gain in the transition region is equal to the slope found above, thus Gain=-12