Chapter 17

Solutions to Exercises within the Chapter

Ex: 17.1 $I t_{PLH} = C\dfrac{V_{DD}}{2}$

$\Rightarrow t_{PLH} = CV_{DD}/2I$

To obtain $t_{PLH} = 10$ ps with $C = 10$ fF and $V_{DD} = 1.2$ V, we need a current I obtained as follows:

$$10 \times 10^{-12} = \frac{10 \times 10^{-15} \times 1.2}{2I}$$

$$\Rightarrow I = \frac{1.2 \times 10^{-14}}{2 \times 10^{-11}} = 0.6 \text{ mA}$$

Ex: 17.2

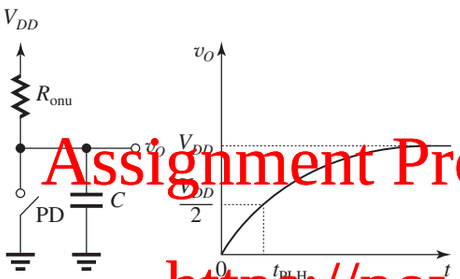


Figure 1(a)

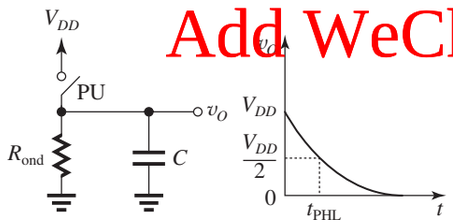


Figure 1(b)

To obtain t_{PLH}, consider the situation in Fig. 1(a). Here, PD has just opened (at $t = 0$) leaving $v_O = 0$ V at $t = 0+$. Capacitor C then charges through the on resistance of the pull-up switch, R_{onu}, toward V_{DD}, thus

$$v_O(t) = V_\infty - (V_\infty - V_{0+})e^{-t/\tau}$$

$$= V_{DD} - (V_{DD} - 0)e^{-t/\tau}$$

$$= V_{DD}(1 - e^{-t/\tau})$$

At $t = t_{PLH}$, $v_O = V_{DD}/2$, thus

$$\frac{V_{DD}}{2} = V_{DD}(1 - e^{-t_{PLH}/\tau})$$

$$\Rightarrow e^{-t_{PLH}/\tau} = 0.5$$

$$\Rightarrow t_{PLH} = \tau \ln 2 = 0.69\tau$$

For $C = 10$ fF and $R_{onu} = 20$ kΩ, then

$$\tau = 10 \times 10^{-15} \times 20 \times 10^3 = 200 \text{ ps}$$

and

$$t_{PLH} = 0.69 \times 200 = 138 \text{ ps}$$

Next we determine t_{PHL} by considering the situation depicted in Fig. 1(b). Here, PU has just opened, leaving $v_O(0+) = V_{DD}$. Capacitor C then discharges through the on resistance of the pull-down switch, R_{ond}, toward 0 V, thus $v_O(\infty) = 0$, thus

$$v_O = 0 - (0 - V_{DD})e^{-t/\tau}$$

$$= V_{DD}e^{-t/\tau}$$

At $t = t_{PHL}$, $v_O = V_{DD}/2$ and we get

$$\frac{V_{DD}}{2} = V_{DD}e^{-t_{PHL}/\tau}$$

$$\Rightarrow t_{PHL} = \tau \ln 2 = 0.69\tau$$

Here

$$\tau = CR_{ond}$$

$$= 10 \times 10^{-15} \times 10 \times 10^3 = 100 \text{ ps}$$

Thus,

$$t_{PHL} = 69 \text{ ps}$$

The propagation delay t_P can now be obtained as

$$t_P = \frac{1}{2}(t_{PLH} + t_{PHL})$$

$$= \frac{1}{2}(138 + 69) = 104 \text{ ps}$$

Ex: 17.3

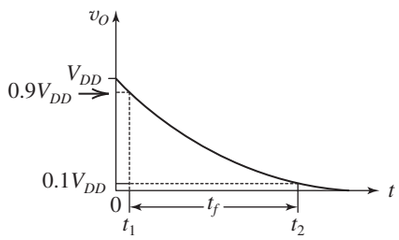


Figure 1

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

Figure 1 shows the exponential discharge curve and the two points that define the extent of the fall time, t_f. Here,

$$v_O(t) = V_{DD}e^{-t/\tau}$$

$$v_O(t_1) = 0.9V_{DD} = e^{-t_1/\tau} \quad (1)$$

$$v_O(t_2) = 0.1V_{DD} = e^{-t_2/\tau} \quad (2)$$

Dividing (1) by (2) gives

$$9 = e^{-(t_1-t_2)/\tau}$$

$$9 = e^{t_f/\tau}$$

$$\Rightarrow t_f = \tau \ln 9 = 2.2\tau$$

For $C = 100$ fF and $R = 2$ kΩ,

$$\tau = 100 \times 10^{-15} \times 2 \times 10^3 = 200 \text{ ps}$$

and

$$t_f = 2.2 \times 200 = 440 \text{ ps} = 0.44 \text{ ns}$$

Ex: 17.4 $\alpha_n = 2\Big/\left[\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2\right]$

$$= 2\Big/\left[\frac{7}{4} - \frac{3 \times 0.5}{1.8} + \left(\frac{0.5}{1.8}\right)^2\right] = 2.01$$

$$t_{PHL} = \frac{\alpha_n C}{k'_n(W/L)_n V_{DD}}$$

$$= \frac{2.01 \times 10 \times 10^{-15}}{300 \times 10^{-6} \times 1.5 \times 1.8}$$

$$= 24.8 \text{ ps}$$

$$\alpha_p = 2\Big/\left[\frac{7}{4} - \frac{3|V_{tp}|}{V_{DD}} + \left(\frac{V_{tp}}{V_{DD}}\right)^2\right]$$

$$= 2.01$$

$$t_{PLH} = \frac{\alpha_p C}{k'_p(W/L)_p V_{DD}}$$

$$= \frac{2.01 \times 10 \times 10^{-15}}{75 \times 10^{-6} \times 3 \times 1.8}$$

$$= 49.6 \text{ ps}$$

$$t_P = \frac{1}{2}(t_{PHL} + t_{PLH})$$

$$= \frac{1}{2}(24.8 + 49.6)$$

$$= 37.2 \text{ ps}$$

Ex: 17.5 $t_{PHL} = 0.69R_N C$

$$50 \times 10^{-12} = 0.69 \times \frac{12.5 \times 1}{(W/L)_n} \times 10^3 \times 20 \times 10^{-15}$$

$$\Rightarrow (W/L)_n = 3.5$$

$$t_{PLH} = 0.69R_P C$$

$$50 \times 10^{-12} = 0.69 \times \frac{30 \times 1}{(W/L)_p} \times 10^3 \times 20 \times 10^{-15}$$

$$\Rightarrow (W/L)_p = 8.3$$

Note: If the 0.69 factor is replaced by 1 to account for the fact that the pulse edges are not ideal, then

$$(W/L)_n = 5$$

$$(W/L)_p = 12$$

Ex: 17.6 With an additional 0.1 pF, C becomes

$$C = 0.866 \text{ fF} + 10 \text{ fF} = 10.866 \text{ fF}$$

Thus,

$$t_{PHL} = 4.18 \times \frac{10.866}{0.866}$$

$$= 52.4 \text{ ps}$$

$$t_{PLH} = 5.58 \times \frac{10.866}{0.866}$$

$$= 70.0 \text{ ps}$$

Thus,

$$t_P = \frac{1}{2}(52.4 + 70.0)$$

$$= 61.2 \text{ ps}$$

Ex: 17.7 $C = 2 \times 0.024 + 2 \times 0.024 + 0.03 + 0.03 + 4 \times 0.105 + 4 \times 0.105 + 0.5 = 1.496$ fF

$$t_P = (4.88 \text{ ps})\left(\frac{1.496}{0.866}\right) = 8.43 \text{ ps}$$

Ex: 17.8 Refer to Example 17.3.

(a) $C_{\text{int}} = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2}$

$$= 2 \times 0.024 + 2 \times 0.024 + 0.03 + 0.03$$

$$= 0.156 \text{ fF}$$

$$C_{\text{ext}} = C_{g3} + C_{g4} + C_w$$

$$= 0.105 + 0.105 + 0.5$$

$$= 0.71 \text{ fF}$$

(b) To reduce the extrinsic component of t_P by a factor of 2, we need to scale $(W/L)_n$ and $(W/L)_p$ by a factor

$$S = 2$$

(c) The original value of $t_P = 4.88$ ps is composed of an intrinsic component

$$t_{P,\text{int}} = t_P \times \frac{C_{\text{int}}}{C}$$

$$= 4.88 \times \frac{0.156}{0.866} = 0.88 \text{ ps}$$

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

This component remains unchanged. The extrinsic component

$t_{P,\text{ext}} = 4.88 - 0.88 = 4$

is reduced by a factor of 2. Thus, t_P becomes

$t_P = 0.88 + \frac{4}{2} = 2.88$ ps

(d) Area $= W_n L + W_p L$

$= L(W_n + W_p)$

By scaling W_n and W_p by a factor of 2, the area increases by a factor of 2.

Ex: 17.9 $L = 0.18$ μm, $n = 1.5$, $p = 3$

(a) Four-input NOR gate: Refer to Fig. 17.8.

For NMOS transistors: $W/L = n = 1.5 = \frac{0.27}{0.18}$

For PMOS transistors: $W/L = 4p = 12 = \frac{2.16}{0.18}$

(b) Four-input NAND gate: Refer to Fig. 17.9.

For NMOS transistors: $W/L = 4n = 6 = \frac{1.08}{0.18}$

For PMOS transistors: $W/L = p = 3 = \frac{0.54}{0.18}$

Area of NOR gate

$= 4 \times 0.18 \times 0.27 + 4 \times 0.18 \times 2.16 = 1.7496\ \mu\text{m}^2$

Area of NAND gate

$= 4 \times 0.18 \times 1.08 + 4 \times 0.18 \times 0.54 = 1.1664$

Thus,

$$\frac{\text{NOR area}}{\text{NAND area}} = \frac{1.7496}{1.1664} = 1.5$$

Ex: 17.10 Refer to Fig. 17.9.

(a) Maximum charging current is the current supplied by the four identical PMOS transistors. Minimum charging current is the current supplied by one of the PMOS transistors. Thus, the ratio of maximum to minimum currents is 4.

(b) There is only one possible configuration for discharging a load capacitance, namely, when all 4 NMOS transistors are conducting. So, as far as capacitor discharge is concerned, the ratio is one.

Ex: 17.11 $P_{\text{dyn}} = fCV_{DD}^2$

$= 1 \times 10^9 \times 0.866 \times 10^{-15} \times 0.9^2$

$= 0.70\ \mu\text{W}$

Ex: 17.12 $P_{\text{dyn}} = fCV_{DD}^2$

$= 250 \times 10^6 \times 80 \times 10^{-15} \times 1.2^2$

$= 28.8\ \mu\text{W}$

Ex: 17.13 $P_{\text{dyn}} = fCV_{DD}^2$

C decreases by a factor (0.13/0.5) and V_{DD} decreases from 5 V to 1.2 V; thus for the same f, the power dissipation will decrease by a factor

$$= \frac{0.5}{0.13} \times \frac{5}{1.2} = 66.8$$

Ex: 17.14 $PDP = fCV_{DD}^2 t_P$

When $f = f_{\max} = 1/2t_P$,

$PDP = \frac{1}{2}CV_{DD}^2 = \frac{1}{2} \times 0.866 \times 10^{-15} \times 0.9^2$

$= 0.35$ fJ

$EDP = \frac{1}{2}CV_{DD}^2 t_P = 0.35 \times 10^{-15} \times 4.88 \times 10^{-12}$

$= 1.7 \times 10^{-27}$ Js

Ex: 17.15 Since dynamic power dissipation is scaled by $\frac{1}{S^2}$ and propagation delay is scaled by $\frac{1}{S}$, hence, PDP is scaled by $\frac{1}{S^2} \times \frac{1}{S} = \frac{1}{S^3} = \frac{1}{8}$. Thus, PDP decreases by a factor of 8.

Ex: 17.16 If W_{DD} and V_t are kept constant, the entries in Table 17.1 that change are as follows:

Obviously, V_{DD} and V_t do not scale by $\frac{1}{S}$ anymore. They are kept constant!

$t_P \propto \frac{\alpha C}{k' V_{DD}}$: since α is a function of $\frac{V_t}{V_{DD}}$, then α remains unchanged, while C is scaled by $\frac{1}{S}$, and k' is scaled by S, therefore t_P is scaled by

$$\frac{1/S}{S} = \frac{1}{S^2}$$

Energy/Switching cycle, i.e., CV_{DD}^2, is scaled by $\frac{1}{S}$

$P_{dyn} \propto \frac{CV_{DD}^2}{2t_P}$ and thus is scaled by $\frac{1/S}{1/S^2} = S$ thus P_{dyn} increases.

The power density, i.e., $\frac{P_{dyn}}{\text{device area}}$, is scaled by $\frac{S}{1/S^2} = S^3$

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

Solutions to End-of-Chapter Problems

17.1 (a) Switch opens at time $t = 0$, thus $v_O(0+) = 0$ V. The capacitor then charges by a constant current I, thus

$$It = Cv_O(t)$$

$$\Rightarrow v_O(t) = \frac{I}{C}t$$

(b) For $I = 1$ mA and $C = 10$ pF the time t for v_O to reach 1 V can be found as

$$1 = \frac{1 \times 10^{-3}}{10 \times 10^{-12}}\, t$$

$$\Rightarrow t = 10^{-8} \text{ s} = 10 \text{ ns}$$

17.2 (a) Capacitor C is charged to 10 V and the switch closes at $t = 0$, thus

$$v_O(0+) = 10 \text{ V}$$

Capacitor C then discharges through R exponentially with $v_O(\infty) = 0$

$$v_O(t) = 0 - (0 - 10)\, e^{-t/\tau}$$

$$\Rightarrow v_O(t) = 10e^{-t/\tau}$$

(b) For $C = 100$ pF and $R = 1$ kΩ, we have

$$\tau = 100 \times 10^{-12} \times 1 \times 10^{3} = 100 \text{ ns}$$

$$t_{PHL} = 0.69\tau = 0.69 \times 100 = 69 \text{ ns}$$

$$t_f = 2.22\tau = 2.2 \times 100 = 220 \text{ ns}$$

17.3 $V_{OH} = V_{DD}$

At $t = 0$, v_I goes low and the transistor turns off instantly, thus

$$v_O(0+) = V_{OL}$$

Now capacitor C charges through R toward $v_O(\infty) = V_{DD}$, thus

$$v_O(t) = V_{DD} - (V_{DD} - V_{OL})\, e^{-t/\tau}$$

At $t = t_{PLH}$,

$$v_O = \frac{1}{2}(V_{OL} + V_{OH}) = \frac{1}{2}(V_{OL} + V_{DD}), \text{ thus}$$

$$\frac{1}{2}(V_{OL} + V_{DD}) = V_{DD} - (V_{DD} - V_{OL})e^{-t/\tau}$$

$$\Rightarrow t_{PLH} = 0.69\tau$$

For $R = 10$ kΩ and we wish to limit τ_{PLH} to 100 ps then the maximum value that C can have is found from

$$0.69 \times C \times 10 \times 10^{3} = 100 \times 10^{-12}$$

$$\Rightarrow C = 1.45 \times 10^{-14} \text{ F}$$

$$= 14.5 \text{ fF}$$

17.4

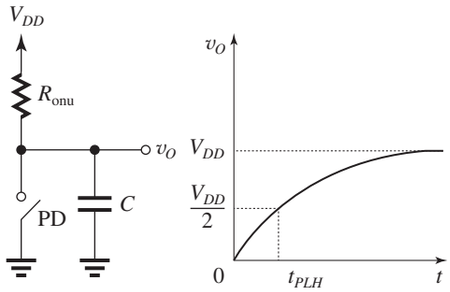


Figure 1(a)

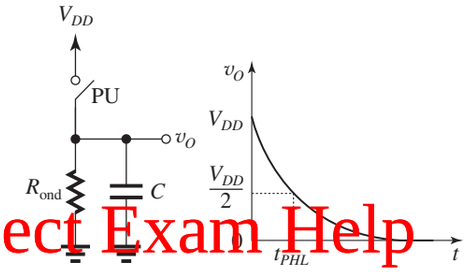


Figure 1(b)

To obtain t_{PLH}, consider the situation in Fig. 1(a). Here, PD has just opened (at $t = 0$), leaving $v_O = 0$ V at $t = 0+$. Capacitor C then charges through the "on" resistance of the pull-up switch, R_{onu}, toward V_{DD}, thus

$$v_O(t) = V_\infty - (V_\infty - V_{0+})e^{-t/\tau}$$

$$= V_{DD} - (V_{DD} - 0)e^{-t/\tau}$$

$$= V_{DD}(1 - e^{-t/\tau})$$

At $t = t_{PLH}$, $v_O = V_{DD}/2$, thus

$$\frac{V_{DD}}{2} = V_{DD}(1 - e^{-t_{PLH}/\tau})$$

$$\Rightarrow e^{-t_{PLH}/\tau} = 0.5$$

$$\Rightarrow t_{PLH} = \tau \ln 2 = 0.69\tau$$

For $C = 20$ fF, $R_{onu} = 2$ kΩ, then

$$t_{PLH} = 0.69 \times 20 \times 10^{-15} \times 2 \times 10^{3}$$

$$= 27.6 \text{ ps}$$

Next we determine t_{PHL} by considering the situation depicted in Fig. 1(b). Here, PU has just opened, leaving $v_O(0+) = V_{DD}$. Capacitor C then discharges through the on resistance of the pull-down switch, R_{ond}, toward 0 V, thus $v_O(\infty) = 0$, thus

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

$$v_O = 0 - (0 - V_{DD})\, e^{-t/\tau}$$

$$= V_{DD} e^{-t/\tau}$$

At $t = t_{PHL}$, $v_O = V_{DD}/2$ and we get

$$\frac{V_{DD}}{2} = V_{DD} e^{-t_{PHL}/\tau}$$

$$\Rightarrow t_{PHL} = 0.69\tau$$

Here,

$$\tau = C R_{\text{ond}}$$

$$= 20 \times 10^{-15} \times 1 \times 10^{3} = 20 \text{ ps}$$

Thus,

$$t_{PHL} = 0.69 \times 20 \simeq 13.8 \text{ ps}$$

The propagation delay t_P can now be obtained as

$$t_P = \frac{1}{2}(t_{PLH} + t_{PHL})$$

$$= \frac{1}{2}(27.6 + 13.8) = 20.7 \text{ ps}$$

Assignment Project Exam Help

17.5 (a) $V_{OL} = 0$ V

$V_{OH} = V_{DD} = 1.2$ V

https://powcoder.com

$$NM_L = V_{IL} - V_{OL} = \frac{V_{DD}}{2} - 0$$

$$= 0.6 \text{ V}$$

Add WeChat powcoder

$$NM_H = V_{OH} - V_{IH} = V_{DD} - \frac{V_{DD}}{2}$$

$$= 0.6 \text{ V}$$

(b) Capacitor C discharges through R_{on} of P_D,

$v_O(0+) = V_{DD} = 1.2$ V

$v_O(\infty) = 0$ V

Thus,

$$v_O(t) = V_{DD} e^{-t/\tau}$$

$$\Rightarrow t_{PHL} = 0.69\tau$$

$$= 0.69 \times 0.1 \times 10^{-12} \times 2 \times 10^{3}$$

$$= 138 \text{ ps}$$

(c) Here the capacitor charges through R_{on} of PU toward V_{DD}. Thus,

$v_O(0+) = 0$, $v_O(\infty) = V_{DD}$,

$v_O(t) = V_{DD}(1 - e^{-t/\tau})$

At $t = t_{PLH}$, $v_O(t) = V_{DD}/2$, thus

$$t_{PLH} = 0.69\tau$$

$$= 0.69 \times 0.1 \times 10^{-12} \times 2 \times 10^{3}$$

$$= 138 \text{ ps}$$

Finally, we obtain τ_P as

$$\tau_P = \frac{1}{2}(t_{PLH} + t_{PHL})$$

$$= \frac{1}{2}(138 + 138) = 138 \text{ ps}$$

17.6 (a) $t_P = \frac{1}{2}(t_{PLH} + t_{PHL})$

Since $t_P = 45$ ps, then

$$t_{PLH} + t_{PHL} = 90 \text{ ps} \quad (1)$$

Now, since I_{charge} is half $I_{\text{discharge}}$, then

$$t_{PLH} = 2t_{PHL} \quad (2)$$

Using (1) together with (2) yields

$t_{PLH} = 60$ ps

$t_{PHL} = 30$ ps

(b) Since the propagation delay is directly proportional to C, then the increase in propagation delay by 50%, when the capacitance is increased by 0.1 pF, indicates that the original total capacitance is 0.2 pF.

(c) The reduction of propagation delays by 40% when the load inverter is removed indicates that the load inverter was contributing 40% of the total capacitance found in (b), that is,

$C_{\text{out}} = 0.12$ pF

$C_{\text{load}} = 0.08$ pF

17.7 See figure on next page.

(a) For a rising input, time to the full change of output of second gate is

$$150 + 200 + \frac{250}{2} = 475 \text{ ps}$$

(b) For a falling input, time to the full change of output of the second gate is

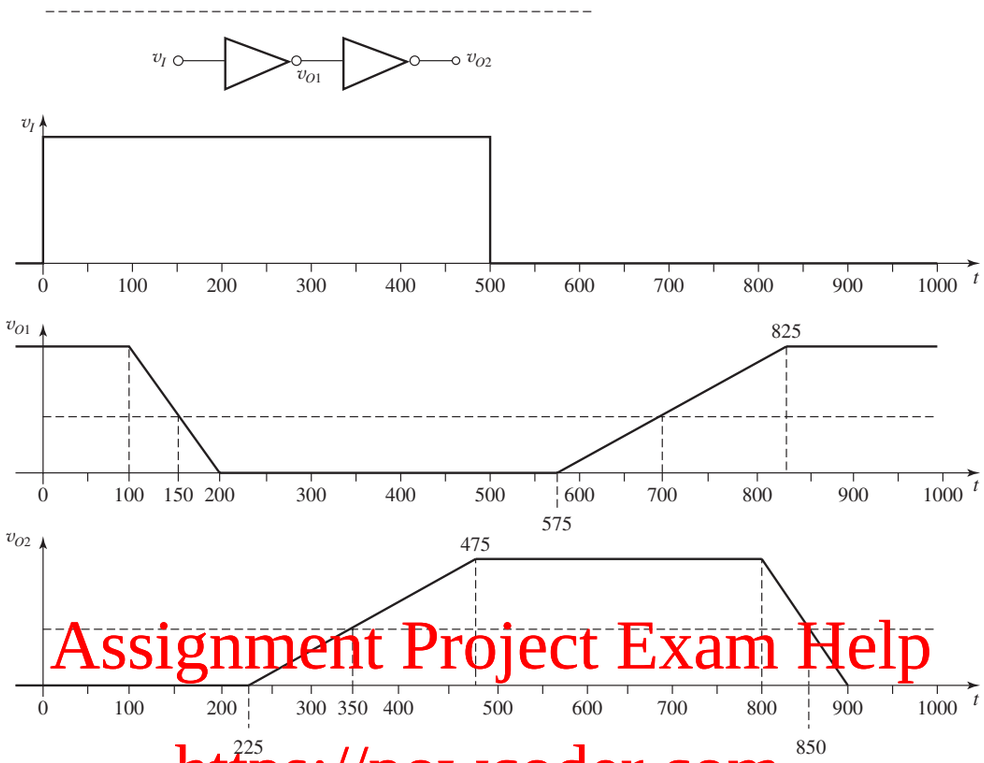
$$200 + 150 + \frac{100}{2} = 400 \text{ ps}$$

The propagation delay is

$$t_P = \frac{1}{2}(t_{PLH} + t_{PHL})$$

$$= \frac{1}{2}(200 + 150) = 175 \text{ ps}$$

This figure belongs to Problem 17.7.



Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

17.8 $\alpha_n = 2\Big/\left[\frac{7}{4} - \frac{3\,V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2\right]$

$= 2\Big/\left[\frac{7}{4} - \frac{3 \times 0.35}{1.0} + \left(\frac{0.35}{1.0}\right)^2\right]$

$= 2.44$

$t_{PHL} = \dfrac{\alpha_n C}{k'_n (W/L)_n V_{DD}}$

$= \dfrac{2.44 \times 4 \times 10^{-15}}{500 \times 10^{-6} \times 2 \times 1.0}$

$= 9.8$ ps

$\alpha_p = \alpha_n = 2.44$

$t_{PLH} = \dfrac{\alpha_p C}{k'_p (W/L)_p V_{DD}}$

$= \dfrac{2.44 \times 4 \times 10^{-15}}{\left(\frac{500}{4}\right) \times 10^{-6} \times 4 \times 1.0}$

$= 19.5$ ps

$t_P = \dfrac{1}{2}(t_{PHL} + t_{PLH})$

$= \dfrac{1}{2}(9.8 + 19.5) = 14.7$ ps

17.9 $\alpha_n = 2\Big/\left[\frac{7}{4} - \frac{3\,V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2\right]$

$= 2\Big/\left[\frac{7}{4} - \frac{3 \times 0.35}{1.0} + \left(\frac{0.35}{1.0}\right)^2\right]$

$= 2.44$

For a matched inverter, we have

$t_{PHL} = t_{PLH} = t_P$

For $t_P \leq 25$ ps,

$t_{PHL} \leq 25$ ps

But,

$t_{PHL} = \dfrac{\alpha_n C}{k'_n (W/L)_n V_{DD}}$

$\dfrac{2.44 \times 10 \times 10^{-15}}{500 \times 10^{-6} (W/L)_n \times 1.0} \leq 25 \times 10^{-12}$

$(W/L)_n \geq 1.95$

$(W/L)_p \geq 7.8$

17.10 $R_N = \dfrac{12.5 \times 1}{(W/L)_n} = \dfrac{12.5}{1.5} = 8.33\ \text{k}\Omega$

$t_{PHL} = 0.69 C R_N$

$$= 0.69 \times 10 \times 10^{-15} \times 8.33 \times 10^{3}$$

$$= 57.5 \text{ ps}$$

$$R_P = \frac{30 \times 1}{(W/L)_p} = \frac{30}{3} = 10 \text{ k}\Omega$$

$$t_{PLH} = 0.69 C R_P$$

$$= 0.69 \times 10 \times 10^{-15} \times 10 \times 10^{3}$$

$$= 69 \text{ ps}$$

$$t_P = \frac{1}{2}(57.5 + 69) = 63.3 \text{ ps}$$

17.11 $R_N = \dfrac{12.5 \times 1}{1} = 12.5 \text{ k}\Omega$

$$R_P = \frac{30 \times 1}{1} = 30 \text{ k}\Omega$$

$$t_{PHL} = 0.69 C R_N$$

$$= 0.69 \times 20 \times 10^{-15} \times 12.5 \times 10^{3}$$

$$= 172.5 \text{ ps}$$

$$t_{PLH} = 0.69 C R_P$$

$$= 0.69 \times 20 \times 10^{-15} \times 30 \times 10^{3}$$

$$= 414 \text{ ps}$$

$$t_P = \frac{1}{2}(172.5 + 414)$$

$$= 293.3 \text{ ps}$$

17.12 For

$$t_{PHL} = t_{PLH} = t_P \leq 15 \text{ ps}$$

we use

$$t_{PHL} = 0.69 C R_N$$

$$= 0.69 C \times \frac{8 \times 1.5}{(W/L)_n} \times 10^{3}$$

and thus obtain

$$0.69 \times 5 \times 10^{-15} \times \frac{12}{(W/L)_n} \times 10^{3} \leq 15 \times 10^{-12}$$

$$\Rightarrow \left(\frac{W}{L}\right)_n \geq 2.76$$

Similarly,

$$t_{PLH} = 0.69 \ C \ R_P$$

$$= 0.69 \ C \times \frac{24 \times 1.5}{(W/L)_p} \times 10^{3}$$

Thus,

$$0.69 \times 5 \times 10^{-15} \times \frac{36}{(W/L)_p} \times 10^{3} \leq 15 \times 10^{-12}$$

$$\Rightarrow (W/L)_p \geq 8.28$$

17.13 Refer to Example 17.2.

The method of average currents yields

$$t_{PHL} = 15.0 \text{ ps}$$

The method of equivalent resistance yields

$$t_{PHL} = 27.6 \text{ ps}$$

If the discrepancy is entirely due to the reduction in current due to velocity saturation in the NMOS transistor, then the factor by which the current decreases is 15.0/27.6 = 0.54.

The value of t_{PLH} does not change (in fact there is a slight decrease due to various approximations). We may therefore conclude that the effect of velocity saturation is minimal in the PMOS transistor.

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

17.14 $\alpha_n = 2 \Big/ \left[\dfrac{7}{4} - \dfrac{3\, V_{tn}}{V_{DD}} + \left(\dfrac{V_{tn}}{V_{DD}}\right)^2\right]$

$$= 2 \Big/ \left[\frac{7}{4} - \frac{3 \times 0.35}{1} + \left(\frac{0.35}{1}\right)^2\right]$$

$$= 2.43$$

$$t_{PHL} = \frac{\alpha_n C}{k_n'(W/L)_n V_{DD}}$$

$$= \frac{2.43 \times 10 \times 10^{-15}}{470 \times 10^{-6} \times 1.5 \times 1}$$

$$= 34.4 \text{ ps}$$

$$t_{PLH} = \frac{\alpha_p C}{k_p'(W/L)_p V_{DD}}$$

Since $|V_{tp}| = V_{tn}$, we have

$$\alpha_p = \alpha_n = 2.43$$

Thus,

$$t_{PLH} = \frac{2.43 \times 10 \times 10^{-15}}{190 \times 10^{-6} \times 3 \times 1}$$

$$= 42.6 \text{ ps}$$

$$t_P = \frac{1}{2}(34.4 + 42.6) = 38.5 \text{ ps}$$

The theoretical maximum switching frequency is

$$f_{\max} = \frac{1}{2t_P} = \frac{1}{2 \times 38.5 \times 10^{-12}} \simeq 13 \text{ GHz}$$

17.15 $C = 2.5 \times 0.13 + 2.5 \times 0.13 + 2$

$= 2.65$ fF

$$\alpha_n = 2\Big/\left[\frac{7}{4} - \frac{3\ V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2\right]$$

$$= 2\Big/\left[\frac{7}{4} - \frac{3 \times 0.35}{1.0} + \left(\frac{0.35}{1.0}\right)^2\right]$$

$= 2.44$

$$t_{PHL} = \frac{\alpha_n C}{k'_n\left(\frac{W}{L}\right)_n V_{DD}}$$

$$= \frac{2.44 \times 2.65 \times 10^{-15}}{500 \times 10^{-6} \times \frac{130}{65} \times 1.0}$$

$= 6.5$ ps

$\alpha_p = \alpha_n = 2.44$

$$t_{PLH} = \frac{\alpha_p C}{k'_p\left(\frac{W}{L}\right)_p V_{DD}}$$

$$= \frac{2.44 \times 2.65 \times 10^{-15}}{\frac{500}{4} \times 10^{-6} \times \frac{130}{65} \times 1.0}$$

$= 25.9$ ps

$$t_P = \frac{1}{2}(6.5 + 25.9) = 16.2 \text{ ps}$$

If the design is changed to a matched one, then

$W_p = 4W_n = 4 \times 130 = 520$ nm

$C = 2.5 \times 0.13 + 2.5 \times 0.52 + 2$

$= 3.625$ fF

$\alpha_n = \alpha_p = 2.44$

$$t_{PHL} = \frac{2.44 \times 3.625 \times 10^{-15}}{500 \times 10^{-6} \times \frac{130}{65} \times 1.0}$$

$= 8.8$ ps

$$t_{PLH} = \frac{2.44 \times 3.625 \times 10^{-15}}{\frac{500}{4} \times 10^{-6} \times \frac{520}{65} \times 1.0}$$

$= 8.8$ ps

$$t_P = \frac{1}{2}(8.8 + 8.8) = 8.8 \text{ ps}$$

17.16 $W_n = 260$ nm

$$W_p = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} \times W_n$$

$$= \frac{500}{125} \times 260 = 1040 \text{ nm}$$

$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$$

where

$C_{gd1} = 0.3 \times W_n = 0.3 \times 0.26 = 0.078$ fF

$C_{gd2} = 0.3 \times W_p = 0.3 \times 1.04 = 0.312$ fF

$C_{db1} = 0.5 \times W_n = 0.5 \times 0.26 = 0.13$ fF

$C_{db2} = 0.5 \times W_p = 0.5 \times 1.04 = 0.52$ fF

$C_{g3} = 0.26 \times 0.065 \times 25 + 2 \times 0.3 \times 0.26 = 0.5785$ fF

$C_{g4} = 1.04 \times 0.065 \times 25 + 2 \times 0.3 \times 1.04 = 2.314$ fF

Thus,

$C = 2 \times 0.078 + 2 \times 0.312 + 0.13 + 0.52 + 0.5785 + 2.314 + 2$

$= 6.32$ fF

$$\alpha_n = 2\Big/\left[\frac{7}{4} - \frac{3\ V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2\right]$$

$$= 2\Big/\left[\frac{7}{4} - \frac{3 \times 0.35}{1.0} + \left(\frac{0.35}{1.0}\right)^2\right]$$

$= 2.44$

$$t_{PHL} = \frac{\alpha_n C}{k'_n\left(\frac{W}{L}\right)_n V_{DD}}$$

$$= \frac{2.44 \times 6.32 \times 10^{-15}}{500 \times 10^{-6} \times \left(\frac{260}{65}\right) \times 1.0}$$

$= 7.7$ ps

Since the inverter is matched,

$t_{PLH} = t_{PHL} = 7.7$ ps

and

$t_P = 7.7$ ps

The propagation delay increases by 50% if C is increased by 50%, that is, by $6.32/2 = 3.16$ fF.

17.17 To reduce t_P by 15 ps, we need to reduce the extrinsic part by 15 ps. Now the original value of the extrinsic part is

$$t_P = 30 \times \frac{30}{30 + 10} = 22.5 \text{ ps}$$

A reduction by 15 ps requires the use of a scale factor S,

$S = 3$

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

This is the factor by which $(W/L)_n$ and $(W/L)_p$ must be scaled. The inverter area will be increased by the same ratio, that is, 3.

17.18 (a) Examination of Eq. (17.19) reveals that the NMOS transistors Q_1 and Q_3 contribute

$$C_n = 2\,C_{gd1} + C_{db1} + C_{g3} \tag{1}$$

and the PMOS transistors Q_2 and Q_4 contribute

$$C_p = 2\,C_{gd2} + C_{db2} + C_{g4} \tag{2}$$

The only difference in determining the corresponding capacitances in Eqs. (1) and (2) is the transistor width W. Thus each of the components in Eq. (2) can be written as the corresponding component in Eq. (1) multiplied by (W_p/W_n). Overall, we can write

$$C_p = C_n \frac{W_p}{W_n}$$

and the total capacitance C can be expressed as

$$C = C_n + C_p + C_w$$

$$= C_n + C_n \frac{W_p}{W_n} + C_w$$

Thus,

$$C = C_n\left(1 + \frac{W_p}{W_n}\right) + C_w \qquad \text{Q.E.D.}$$

(b) $R_N = \dfrac{12.5 \times 1}{(W/L)_n}\ \text{k}\Omega$

For $(W/L)_n = 1$, we have

$$R_N = 12.5\ \text{k}\Omega$$

Thus,

$$t_{PHL} = 0.69 C R_N$$

$$= 0.69 \times 12.5 \times 10^3 C$$

$$= 8.625 \times 10^3 C \qquad \text{Q.E.D.}$$

$$R_P = \frac{30 \times 1}{(W/L)_p}\ \text{k}\Omega$$

$$= \frac{30}{(W_p/W_n)(W/L)_n}\ \text{k}\Omega$$

For $(W/L)_n = 1$, we have

$$R_P = \frac{30}{W_p/W_n}\ \text{k}\Omega$$

and

$$t_{PLH} = 0.69 C R_P$$

$$= 0.69 \times \frac{30}{W_p/W_n} \times \times 10^3 C$$

$$= \frac{20.7 \times 10^3}{W_p/W_n} C \qquad \text{Q.E.D.}$$

(c) $t_P = \dfrac{1}{2}(t_{PHL} + t_{PLH})$

$$= \frac{1}{2}\left[8.625 \times 10^3 C + \frac{20.7 \times 10^3}{W_p/W_n} C\right]$$

For $W_p = W_n$, we have

$$t_P = 14.66 \times 10^3 C$$

$$t_P = 14.66 \times 10^3 \left[C_n\left(1 + \frac{W_p}{W_n}\right) + C_w\right]$$

$$= 14.66 \times 10^3 (2C_n + C_w) \tag{3}$$

(d) In the matched case, we have

$$t_{PLH} = t_{PHL}$$

From the results in (b), the required ratio (W_p/W_n) can be determined as

$$\frac{20.7}{W_p/W_n} = 8.625$$

$$\Rightarrow \frac{W_p}{W_n} = 2.4$$

In this case, we have

$$C = C_n(1 + 2.4) + C_w = 3.4\,C_n + C_w$$

and

$$t_P = t_{PLH} = 8.625 \times 10^3 (3.4\,C_n + C_w) \tag{4}$$

(e) (i) For $C_w = 0$, we have

$$W_p = W_n \qquad t_P = 29.32 \times 10^3 C_n$$

$$W_p = 2.4\,W_n \; t_P = 29.32 \times 10^3 C_n$$

Thus, in the case where C is entirely intrinsic, scaling does not affect t_P. This is what we found in Eq. (17.26).

(ii) For $C_w \gg C_n$, we have

$$W_p = W_n \qquad t_P = 14.66 \times 10^3 C_w$$

$$W_p = 2.4\,W_n \; t_P = 8.625 \times 10^3 C_w$$

Here C is entirely extrinsic, thus scaling the PMOS transistors has resulted in a decrease in t_P.

We conclude that using a matched design reduces t_P only when C is dominated by external capacitances. The matched design, of course, has the drawback of increased area.

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

17.19

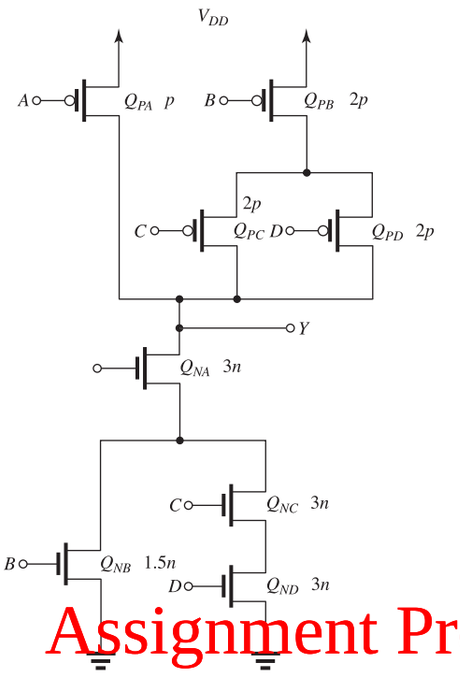


Figure 1

Figure 1 shows the CMOS logic gate with the (W/L) ratios selected so that the worst-case t_{PLH} and t_{PHL} are equal to the corresponding values of the basic inverter with $(W/L)_n = n$ and $(W/L)_p = p$. Observe that the worst-case for discharging a capacitor occurs through the three series transistors Q_{NA}, Q_{NC}, and Q_{ND}. To make the equivalent W/L for these three series transistors equal to n, we select each of their (W/L) ratios to be equal to $3n$. Finally, for the discharge path (Q_{NA}, Q_{NB}) to have an equivalent W/L equal to n, we selected W/L of Q_{NB} equal to $1.5n$.

For the PUN, the worst-case charging path is that through Q_{PB} and one of Q_{PC} or Q_{PD}. Thus we select each of these three transistors to have $W/L = 2p$. Finally, we selected W/L of Q_{PA} equal to p.

17.20

$$n = \frac{56}{28}, \quad p = \frac{84}{28}$$

Figure 1 shows the circuit with the W/L ratio of each of the eight transistors indicated. Observe that the worst-case situation for both charging and discharging is two transistors in series. To achieve an equivalent W/L ratio for each path

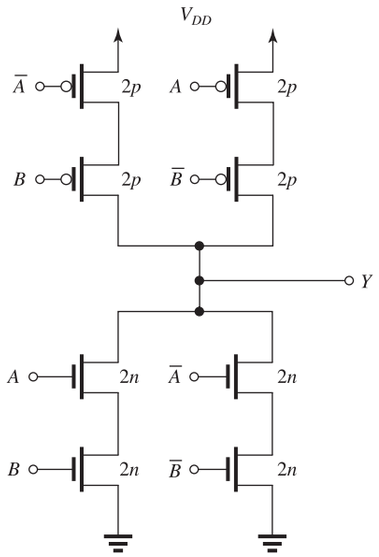


Figure 1

equal to that of the corresponding transistor in the basic inverter, each transistor is sized at twice that of the inverter including the two inverters required to obtain the complemented variable, the area is

$$A = 2W_nL + 2W_pL + 4 \times 2W_nL + 4 \times 2W_pL$$
$$= 10L(W_n + W_p)$$
$$= 10 \times 28(56 + 84)$$
$$= 39200$$

17.21 When the devices are sized as in Fig. 17.9, t_{PLH} that results when one PMOS transistor is conducting (worst case) is

$$t_{PLH} = 0.69 R_p C$$
$$= 0.69 \times \frac{R_{eff,P} \times (W/L)_p}{p} \times C$$

and t_{PHL} is obtained by noting that the equivalent W/L of the discharge path is $4n/4 = n$ and thus

$$t_{PHL} = 0.69\ R_N C$$
$$= 0.69 \times \frac{R_{eff,N} \times (W/L)_n}{n} \times C$$

For the case in which all p-channel devices have $W/L = p$ and all n-channel devices have $W/L = n$, we have

$$t_{PLH} = 0.69 \times \frac{R_{eff,P} \times (W/L)_p}{p} \times C$$

which is the same as in the first case. However,

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

$$t_{PHL} = 0.69 \times \frac{R_{eff,N} \times (W/L)_n}{n/4} \times C$$

$$= 0.69 \times \frac{4 \times R_{eff,N} \times (W/L)_n}{n} \times C$$

which is four times the value obtained in the first case.

17.22

$L = 0.90$ nm, $W_n = 180$ nm, $W_p = 360$ nm,

$n = 180/90$, $p = 360/90$

(a) Circuit (a) uses a six-input NOR gate and one inverter.

The six-input NOR requires:

6 NMOS transistors each with $W/L = n$

and

6 PMOS transistors each with $W/L = 6p$

The inverter requires

1 NMOS transistor with $W/L = n$

and

1 PMOS transistor with $W/L = p$

Thus,

$$\text{Area} = 6W_nL + 6 \times 6W_pL + W_nL + W_pL$$

$$= L(7\ W_n + 37\ W_p)$$

$$= 90(7 \times 180 + 37 \times 360)$$

$$= 90 \times 14,510 = 1{,}305{,}900\ \text{nm}^2$$

(b) Circuit (b) uses two three-input NOR gates and one two-input NAND gate.

Each three-input NOR gate requires

3 NMOS transistors, each with $W/L = n$

3 PMOS transistors, each with $W/L = 3p$

The two-input NAND gate requires

2 NMOS transistors, each with $W/L = 2n$

2 PMOS transistors, each with $W/L = p$

Thus,

$$\text{Area} = 2 \times 3 \times W_nL + 2 \times 3 \times 3 \times W_pL$$

$$+ 2 \times 2 \times W_nL + 2 \times W_pL$$

$$= L(10\ W_n + 20\ W_p)$$

$$= 90(10 \times 180 + 20 \times 360)$$

$$= 90 \times 9000$$

$$= 810{,}000\ \text{nm}^2$$

Thus circuit (a) required 1305900/810000 = 1.61 times the area of circuit (b).

17.23

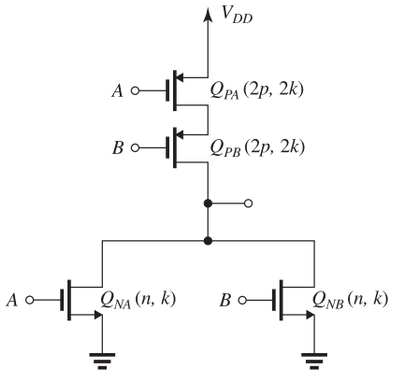


Figure 1

Refer to the circuit in Fig. 1. For Q_{NA} and Q_{NB}, (W/L) is equal to that of the NMOS transistor in the basic matched inverter. Thus,

$$k_{NA} = k_{NB} = k$$

For Q_{PA} and Q_{PB}, (W/L) is equal to twice the value of the PMOS transistor of the basic matched inverter. Since for the matched inverter $k = k_n = k_p$, here we have

$$k_{PA} = k_{PB} = 2k$$

(a)

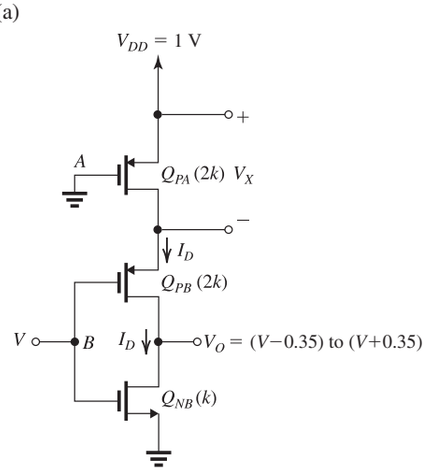


Figure 2

Figure 2 shows the circuit for the case input A is grounded. Note that Q_{NA} will be cut-off and has

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

been eliminated. Switching will occur at $v_I = V$ which will be near $V_{DD}/2$. At this point, Q_{NB} and Q_{PB} will be in saturation and Q_{PA} will be in the triode region with a very small voltage V_X across it. All transistors will be conducting the same current I_D. For Q_{PA} we can write

$$I_D = 2k\left[(1 - 0.35)V_X - \frac{1}{2}V_X^2\right]$$

or

$$I_D = k(1.3\ V_X - V_X^2) \tag{1}$$

For Q_{PB} we can write

$$I_D = \frac{1}{2} \times 2k(1 - V_X - V - 0.35)^2$$

or

$$I_D = k(0.65 - V_X - V)^2 \tag{2}$$

Finally, for Q_{NB} we can write

$$I_D = \frac{1}{2}k(V - 0.35)^2 \tag{3}$$

Next, we solve Eqs. (2) and (3) together to obtain V_X in terms of V. Equating Eqs. (2) and (3) gives

$$\pm\frac{1}{\sqrt{2}}(V - 0.35) = 0.65 - V_X - V$$

$$\pm 0.707(V - 0.35) = 0.65 - V_X - V \tag{4}$$

First try the solution corresponding to the + sign on the left-hand side of (4):

$$0.707(V - 0.35) = 0.65 - V_X - V$$

$$\Rightarrow V_X = 0.897 - 1.707\ \text{V} \tag{5}$$

Since $V_X \simeq 0$, this equation gives

$$V = 0.53\ \text{V}$$

which is reasonable. The other solution gives

$$-0.707(V - 0.35) = 0.65 - V_X - V$$

$$\Rightarrow V_X = 0.403 - 0.293\ \text{V}$$

For $V_X \simeq 0$, this equation gives

$$V = 1.37\ \text{V}$$

which is obviously impossible! Thus Eq. (5) is the solution that is physically meaningful. Next we substitute for V_X. From Eq. (5) into Eq. (1) to obtain

$$I_D = k\ 1.3(0.897 - 1.707\ \text{V}) - k(0.897 - 1.707\ \text{V})^2$$

$$= k(0.361 + 0.843\ \text{V} - 2.914\ \text{V}^2) \tag{6}$$

Equating this value of I_D to that in Eq. (3) gives

$$(V - 0.35)^2 = 2(0.361 + 0.843\ \text{V} - 2.914\ \text{V}^2)$$

$$\Rightarrow 6.83\ \text{V}^2 - 2.39\ \text{V} - 0.6 = 0$$

$$\Rightarrow V = 0.54\ \text{V}$$

This is a reasonable value: It is greater than $(V_{DD}/2)$, which is required since Q_{NB} has a conductance parameter k while Q_{PB} has a parameter $2k$. Of course, V_{SG} of Q_{PB} is smaller than that of Q_{NB} because of V_X. The latter, however, is small. It can be found by substituting for $V = 0.54$ in Eq. (5),

$$V_X = 0.89 - 1.707 \times 0.54 \approx 0\ \text{V}$$

(b) Figure 3 shows the circuit when the corresponding input terminals are connected

This figure belongs to Problem 17.23, part (b).

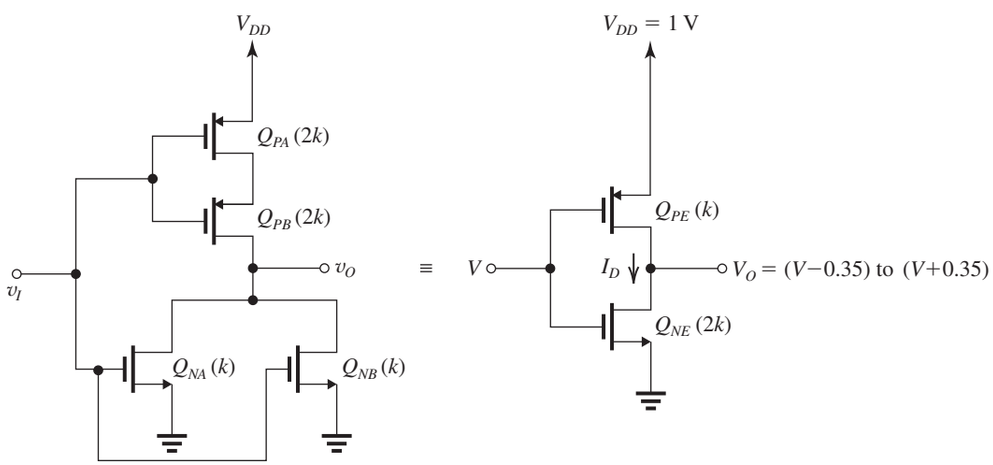


Figure 3

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

together. The two parallel NMOS transistors can be replaced by an equivalent NMOS transistor Q_{NE} having a $W/L = 2n$ and thus a transconductance parameter $2k$. The two series PMOS transistors can be replaced by an equivalent PMOS transistor Q_{PE} having a $W/L = (2p/2) = p$ and thus a transconductance parameter k. We are now ready to determine the threshold voltage, denoted V as before. Here, both Q_{NE} and Q_{PE} will be operating in saturation and conducting a current I_D. Thus, for Q_{PE} we can write

$$I_D = \frac{1}{2}k(V_{DD} - V - 0.35)^2$$

or

$$I_D = \frac{1}{2}k(0.65 - V)^2 \qquad (7)$$

and for Q_{NE}, we can write

$$I_D = \frac{1}{2} \times 2k(V - 0.35)^2$$

or

$$I_D = k(V - 0.35)^2 \qquad (8)$$

The value of V can be obtained by solving (7) and (8) together. Equating (7) and (8) gives

$$\frac{1}{2}(0.65 - V)^2 = (V - 0.35)^2$$

One solution is

$$\Rightarrow \frac{1}{\sqrt{2}}(0.65 - V) = V - 0.35$$

$$\Rightarrow V = 0.47 \text{ V}$$

This is a reasonable, physically meaningful answer and thus there is no need to find the other solution. As expected, V is lower than $(V_{DD}/2)$, which is a result of the fact that Q_{NE} has a larger (twice as large) transconductance parameter than Q_{PE}. Thus, Q_{NE} needs a smaller V_{GS} that V_{SG} of Q_{PE} to provide an equal I_D.

17.24 (a) $n = 4$

Minimum delay is obtained when the scaling factor x is given by

$$x^n = \frac{C_L}{C}$$

Here,

$$x^4 = \frac{1600C}{C} = 1600$$

$$\Rightarrow x = 6.32$$

$$t_P = 4xCR$$

$$= 4 \times 6.32CR = 25.3CR$$

(b) Let the number of the inverters be n. Optimum performance is obtained when

$$x^n = \frac{C_L}{C} = 1600$$

and

$$x = e = 2.718$$

$$n = \frac{\ln 1600}{\ln e} = 7.4 \simeq 7$$

Thus, we use 7 inverters. The actual scaling factor required can be found from

$$x^7 = 1600$$

$$\Rightarrow x = (1600)^{1/7} = 2.87$$

The value of t_P realized will be

$$t_P = 7 \times 2.87CR$$

$$= 20.1CR$$

which represents a reduction in t_P by about 20.6%. Thus adding three inverters reduces the delay by 20.6%.

17.25 (a) Refer to Fig. 17.11(c). By inspection we see that

$$t_P = \tau_1 + \tau_2 + \ldots + \tau_{n-1} + \tau_n$$

But

$$\tau_1 = \tau_2 = \ldots = \tau_{n-1} = xCR$$

and

$$\tau_n = \frac{R}{x^{n-1}}C_L$$

Thus,

$$t_P = (n-1)xRC + \frac{1}{x^{n-1}}RC_L \qquad \text{Q.E.D.} \quad (1)$$

(b) Differenting t_P in Eq. (1) relative to x gives

$$\frac{\partial t_P}{\partial x} = (n-1)RC - \frac{(n-1)}{x^n}RC_L$$

Equating $\frac{\partial t_P}{\partial x}$ to zero gives

$$x^n = \frac{C_L}{C} \qquad \text{Q.E.D.} \qquad (2)$$

(c) Differenting t_P in Eq. (1) relative to n gives

$$\frac{\partial t_P}{\partial n} = xRC - \frac{1}{x^{n-1}}(\ln x)RC_L$$

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

Equating $\frac{\partial t_P}{\partial n}$ to zero gives

$$x^n \left(\frac{C}{C_L}\right) = \ln x \qquad \text{Q.E.D.} \qquad (3)$$

To obtain the value of x for optimum performance, we combine the two optimality conditions in (2) and (3). Thus

$$\ln x = 1$$

$$\Rightarrow x = e \qquad \text{Q.E.D.}$$

17.26 $E = CV_{DD}^2$

$$= 3 \times 10^{-15} \times 1.2^2 = 4.32 \text{ fJ}$$

For 5×10^6 inverters switched at $f = 2.5$ GHz,

$$P_D = 5 \times 10^6 \times 2.5 \times 10^9 \times 4.32 \times 10^{-15}$$

$$= 54 \text{ W}$$

$$I_{DD} = \frac{P_D}{V_{DD}} = \frac{54}{1.2} = 45 \text{ A}$$

Assignment Project Exam Help

17.27 $P_{\text{dyn}} = fCV_{DD}^2$

$$= 2.5 \times 10^9 \times 5 \times 10^{-15} \times 1$$

$$= 12.5 \ \mu\text{W}$$

https://powcoder.com

$$I_{DD} = \frac{12.5 \times 10^{-6}}{1} = 12.5 \ \mu\text{A}$$

Add WeChat powcoder

17.28 Each cycle, the inverter draws an average current of

$$I_{\text{av}} = \frac{15 + 0}{2} = 7.5 \ \mu\text{A}$$

Since $I_{\text{av}} = 60 \ \mu$A, then the average current corresponding to the dynamic power dissipation is 52.5 μA. Thus,

$$P_{\text{dyn}} = 1.2 \times 52.5 \times 10^{-6} = 63 \ \mu\text{W}$$

But,

$$P_{\text{dyn}} = fCV_{DD}^2$$

Thus,

$$63 \times 10^{-6} = 250 \times 10^6 \times 1.2^2 \times C$$

$$\Rightarrow C = 0.175 \text{ pF}$$

17.29 Since P_{dyn} is proportional to V_{DD}^2, reducing the power supply from 1.2 V to 1.0 V reduces the power dissipation by a factor of $\left(\frac{1.0}{1.2}\right)^2 = 0.694$. The power dissipation now becomes $0.694 \times 10 = 6.94$ mW. Since P_{dyn} is proportional to f, reducing f by the same factor as the supply voltage (0.83) results in reducing the power dissipation *further* by a factor of 0.83, i.e.,

Additional savings in power $= (1 - 0.83) \times 6.94$

$$= 1.16 \text{ mW}$$

17.30 $t_{PLH} = 1.3$ ns, $t_{PHL} = 1.2$ ns

$$t_P = \frac{1}{2}(1.3 + 1.2) = 1.25 \text{ ns}$$

$$P_{D\text{av}} = \frac{1}{2}(0.1 + 0.2) = 0.15 \text{ mW}$$

$$PDP = 0.15 \times 10^{-3} \times 1.25 \times 10^{-9} = 0.188 \text{ pJ}$$

17.31 (a)

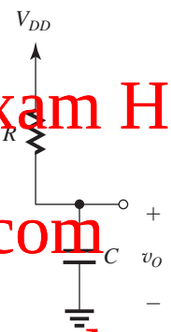


Figure 1

Figure 1 shows the circuit as the switch is opened ($t = 0+$). Capacitor C will charge through R, and its voltage will increase from the initial value of V_{OL} to the high value V_{OH},

$$v_O = v_O(\infty) - v_O(\infty) - v_O(0+)e^{-t/\tau}$$

$$= V_{OH} - (V_{OH} - V_{OL})e^{-t/\tau_1} \qquad \text{Q.E.D.}$$

where

$$\tau_1 = CR$$

To reach the 50% point, $\frac{1}{2}(V_{OH} + V_{OL})$ the time required, t_{PLH}, can be found as follows:

$$\frac{1}{2}(V_{OH} + V_{OL}) = V_{OH} - (V_{OH} - V_{OL})e^{-t_{PLH}/\tau_1}$$

$$(V_{OH} - V_{OL})\, e^{-t_{PLH}/\tau_1} = \frac{1}{2}(V_{OH} - V_{OL})$$

$$\Rightarrow t_{PLH} = \tau_1 \ln 2$$

$$= 0.69\tau_1 = 0.69CR \qquad \text{Q.E.D.}$$

(b) Figure 2(a) shows the circuit after the switch closes ($t = 0+$). At this instant the capacitor voltage in V_{OH}. The capacitor then discharges and eventually reaches the low level V_{OL}. To determine τ_{PHL}, we simplify the circuit to that in Fig. 2(b). Using this circuit, we can express v_O as

$$v_O(t) = v_O(\infty) - v_O(\infty) - v_O(0)e^{-t/\tau_1}$$

$$= V_{OL} - (V_{OL} - V_{OH})e^{-t/\tau_2}$$

when

$$\tau_2 = C(R_{\text{on}} \parallel R) \simeq CR_{\text{on}}$$

The value of t_{PHL} can be found from

$$v_O(t_{PHL}) = \frac{1}{2}(V_{OH} + V_{OL})$$

$$= V_{OL} - (V_{OL} - V_{OH})e^{-t_{PLH}/\tau_2}$$

$$\Rightarrow t_{PHL} = \tau_2 \ln 2$$

$$= 0.69\tau_2$$

$$= 0.69CR_{\text{on}} \qquad \text{Q.E.D.}$$

(c) $t_P = \frac{1}{2}(t_{PLH} + t_{PHL})$

$$= \frac{1}{2}(0.69CR + 0.69CR_{\text{on}})$$

$$t_P = \frac{1}{2} \times 0.69C(R + R_{\text{on}})$$

Since $R_{\text{on}} \ll R$,

$$t_P \simeq 0.35CR \qquad \text{Q.E.D.}$$

(d) During the low-input state, the switch is open, the current is zero, and the power dissipation is zero.

During the high-input state, the switch is closed and a current

$$I_{DD} = \frac{V_{DD}}{R + R_{\text{on}}} \simeq \frac{V_{DD}}{R}$$

flows, and the power dissipation is

$$P_D = V_{DD}I_{DD} = \frac{V_{DD}^2}{R}$$

Now, if the inverter spends half the time in each state, the average power dissipation will be

$$P = \frac{1}{2}\frac{V_{DD}^2}{R} \qquad \text{Q.E.D.}$$

(e) For $V_{DD} = 1.8$ V and $C = 2$ pF, we have

$$t_P = 0.35 \times 2 \times 10^{-12}\ R$$

If t_P is to be smaller or equal to 1.4 ns, we must have

$$0.35 \times 2 \times 10^{-12} R \leq 1.4 \times 10^{-9}$$

$$\Rightarrow R \leq 2.03\ \text{k}\Omega$$

If P is to be smaller or equal to 2 mW, we must have

$$\frac{1}{2} \times \frac{1.8^2}{R} \leq 2 \times$$

where R is in kΩ, thus

$$R \geq 1.23\ \text{k}\Omega$$

Thus, to satisfy both constraints, R must lie in the range

$$1.23\ \text{k}\Omega \leq R \leq 2.03\ \text{k}\Omega$$

Selecting $R = 1.5$ kΩ yields

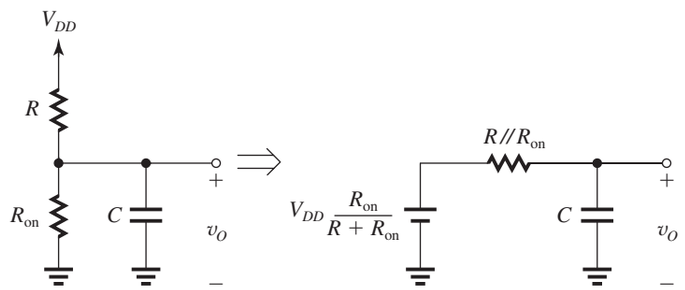
$$t_P = 0.35 \times 2 \times 10^{-12} \times 1.5 \times 10^3$$

$$= 1.04\ \text{ns}$$

and

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

This figure belongs to Problem 17.31, part (b).



(a) (b)

Figure 2

$$P = \frac{1}{2}\,\frac{1.8^2}{1.5} = 1.08 \text{ mW}$$

Both values are within the design specifications.

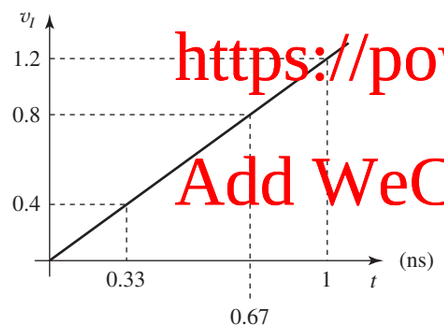
17.32 (a) The currents decrease by a factor of $\frac{1.2}{1.8} = 0.67$; that is, the new current values are 0.67 of the old current values. However, the voltage swing is also reduced by the same factor. The result is that t_P remains unchanged. The PDP will be reduced by a factor of 0.44.

Since the maximum operating frequency is proportional to $1/t_P$, it also will remain unchanged.

(b) If current is proportional to V_{DD}^2, the currents become 0.67^2 of their old values. This together with the reduction of voltage swing by a factor of 0.67 will result in t_P increasing by a factor of (1/0.67) and the maximum operating frequency being reduced by a factor of 0.67. The PDP decreases by a factor of 0.67.

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder

17.33



From Eq. (17.40), we have

$$I_{\text{peak}} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left(\frac{V_{DD}}{2} - V_{tn}\right)^2$$

$$I_{\text{peak}} = \frac{1}{2} \times 500\ \frac{\mu\text{A}}{\text{V}^2}\left(\frac{1.2}{2} - 0.4\right)^2 = 10\ \mu\text{A}$$

The time when the input reaches V_t is

$$\frac{0.4}{1.2} \times 1 = 0.33 \text{ ns}$$

The time when the input reaches $V_{DD} - V_t$ is

$$\frac{1.2 - 0.4}{1.2} \times 1 = 0.67 \text{ ns}$$

So the base of the triangle is

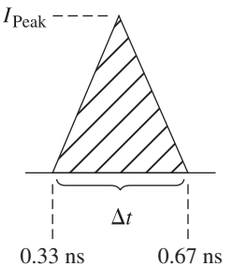
$$\Delta t = 0.67 - 0.33 = 0.34 \text{ ns}$$

$$E = \frac{1}{2} I_{\text{peak}} \times V_{DD} \times \Delta t$$

$$= \frac{1}{2} \times 10\ \mu\text{A} \times 1.2 \times 0.34 \text{ ns}$$

$$= 2 \text{ fJ}$$

$$P = f \times E = 100 \times 10^6 \times 2 \times 10^{-15} = 0.2\ \mu\text{W}.$$



17.34 (a) $t_P \propto \frac{\alpha C}{k' V_{DD}}$, and k' is scaled by S, and C and V_{DD} are scaled by $\frac{1}{S}$; thus t_P is scaled by

$$\frac{\frac{1}{S}}{S \times \frac{1}{S}} = \frac{1}{S}$$

$S = 2 \Rightarrow t_P$ is scaled by $\frac{1}{2}$ (t_P decreases)

The maximum operating speed is $\frac{1}{2t_p}$ and therefore is scaled by $\frac{1}{S}$.

$P_{\text{dyn}} = f_{\max} C V^2{}_{DD}$ and thus is scaled by

$$S \times \frac{1}{S} \times \frac{1}{S^2} = \frac{1}{S^2} = \frac{1}{4}\ (P_{\text{dyn}} \text{ decreases}).$$

Power density $= \frac{P_{\text{dyn}}}{\text{area}}$ and thus is scaled by

$$\frac{\frac{1}{S^2}}{\frac{1}{S^2}} = 1, \text{ i.e., remains unchanged.}$$

PDP is scaled by $\frac{1}{S^3}$ $\left(\text{power is scaled by } \frac{1}{S^2} \text{ and delay by } \frac{1}{S}\right)$ and thus it is scaled by $\frac{1}{8}$ (PDP decreases).

(b) If V_{DD} and V_{tn} remain unchanged while $S = 2$, we have

$$t_p = \frac{\alpha C}{k' V_{DD}} \text{ and } \alpha = \frac{2}{\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2} \text{ so } \alpha$$

remains unchanged and t_P is scaled by

$$\frac{\frac{1}{S}}{S} = \frac{1}{S^2} = \frac{1}{4}$$

The maximum operating speed is $\frac{1}{2t_P}$ and therefore is scaled by 4.

$P_{\text{dyn}} = f_{\max} C V^2{}_{DD}$ and thus is scaled by

$$4 \times \frac{1}{2} \times 1 = 2$$

Power density $= \frac{P_{\text{dyn}}}{\text{area}}$ is thus scaled by

$$\frac{2}{\frac{1}{S^2}} = \frac{2}{\frac{1}{4}} = 8$$

PDP is scaled by $2 \times \frac{1}{4} = \frac{1}{2}$

17.35 $I_D = \frac{1}{2} k_n (V_{GS} - V_{tn})^2$

$0.2 = \frac{1}{2} \times 0.4(V_{GS} - 0.4)^2$

$\Rightarrow V_{GS} = 1.4\text{V}$

(a) For $V_{tn} = 0.4 + 10\% = 0.44$ V, we have

$$I_D = \frac{1}{2} \times 0.4(1.4 - 0.44)^2 = 0.184 \text{ mA}$$

For $V_{tn} = 0.4 - 10\% = 0.36$ V, we have

$$I_D = \frac{1}{2} \times 0.4(1.4 - 0.36)^2$$

$$= 0.216 \text{ mA}$$

Thus, I_D will range from 0.184 mA to 0.216 mA (i.e., $0.2 \pm 8\%$, mA).

(b) If the time for a 0.1-V change of the capacitor voltage is denoted T, then

$$I_D T = C \triangle V$$

$$T = \frac{C \triangle V}{I_D}$$

For $I_D = 0.184$ mA, we have

$$T = \frac{100 \times 10^{-15} \times 0.1}{0.184 \times 10^{-3}} = 54.3 \text{ ps}$$

For $I_D = 0.216$ mA, we have

$$T = \frac{100 \times 10^{-15} \times 0.1}{0.216 \times 10^{-3}} = 46.3 \text{ ps}$$

Thus, the discharge time ranges from 46.3 ps to 54.3 ps.

Assignment Project Exam Help
https://powcoder.com
Add WeChat powcoder