

# Assignment Project Exam Help

Computers and computer architecture  
Code-generation (2): register-machines

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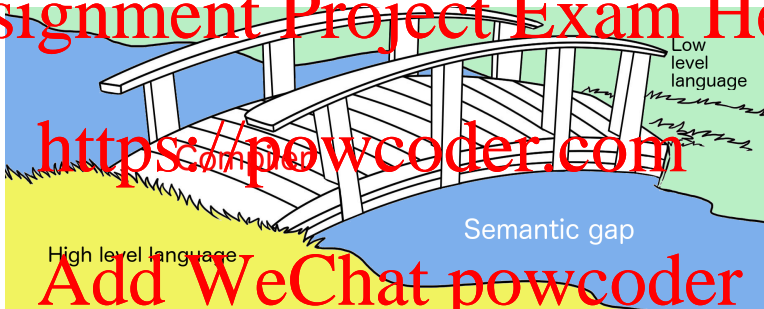
Martin Berger

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November 2017

Recall the function of compilers

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Plan for this week

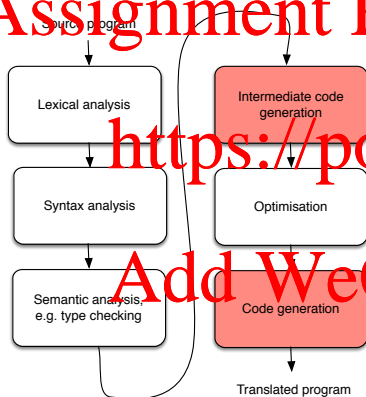
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## Plan for this week

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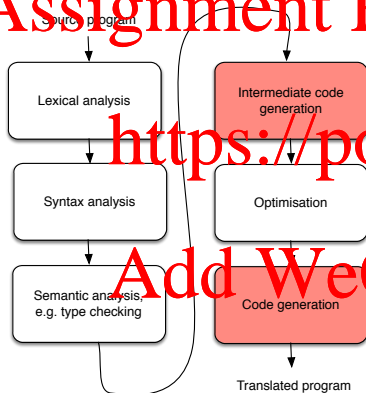
In the previous section we introduced the stack machine architecture, and then investigated a simple syntax-directed code generator for this architecture.

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# Plan for this week

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In the previous section we introduced the stack machine architecture, and then investigated a simple syntax-directed code generator for this architecture.

This week we continue looking at code generation, but for register machines, a faster CPU architecture. If time permits, we'll also look at accumulator machines.

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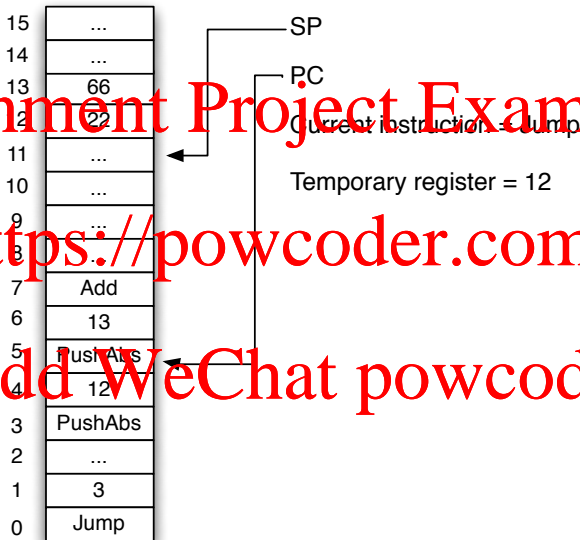
Recall: stack machine architecture

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## Recall: stack machine architecture



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Recall: stack machine language

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Recall: stack machine language

Nop	Pop x
PushAbs x	PushImm n
CompGreater Than	CompEq
Jump l	JumpTrue l
Plus	Minus
Times	Divide
Negate	

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## Recall: stack machine language

Nop	Pop x
PushAbs x	PushImm n
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Jump l	JumpTrue l
Plus	Minus
Times	Divide
Negate	

Important: arguments (e.g. to Plus) are always on top of the stack and are 'removed' (by rearranging the stack pointer (SP)). The result of the command is placed on the top of the stack.

Register machines

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## Register machines

The problem with the stack machine is that memory access (on modern CPUs) is **very slow** in comparison with CPU operations, approx. 20-100 times slower.

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## Register machines

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The stack machine forces us constantly to access memory, even for the simplest operations. It would be nice if the CPU let us store access and manipulate data directly, rather than only work on the top elements of the stack.

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Registers are **fast** (in comparison with memory), temporary, addressable storage in the CPU, that let us do this, whence register machines.

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Registers are **fast** (in comparison with memory), temporary, addressable storage in the CPU, that let us do this, whence register machines.

But compilation for register machines is more complicated than compilation for stack machines. Can you guess why?

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## Compilation for register machines

Each CPU has only a small finite number of registers (e.g. 16, 32, 128). That can be a problem. Why?

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Each CPU has only a small finite number of registers (e.g. 16, 32, 128). That can be a problem. Why?

Because for small expressions, we can fit all the relevant parameters into the registers, but for the execution of larger expressions this is no longer the case. Moreover, what registers are available at each point in the computation depends on what other code is being executed. Hence a compiler must be able to do the following things.

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- ▶ Generate code that has some (or most) parameters in main memory.

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- ▶ Detect which of the above is the case, and be able seamlessly to switch between the two.

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All of this makes compilers more difficult. Let's look at register machines.

A simple register machine

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# A simple register machine

15	...
14	...
13	66
12	22
11	...
10	...
9	...
8	...
7	Add
6	13
5	PushAbs
4	12
3	PushAbs
2	...
1	3
0	Jump

SP

PC

Cur. instr. = Jump

R0 = 2

R1 = 4

R2 = 33

R3 = 12

R4 = 20

R5 = 25

R6 = 116

R7 = 123

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Quite similar to the stack machine, but we have additional registers.

**Important:** operations like add, multiply operate on registers, no longer on the top of the stack

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15	...
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How to generate code for register machines?

Dealing with registers by 'divide-and-conquer'

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## Dealing with registers by 'divide-and-conquer'

In order to explain the difficult problem of generating efficient code for register machines, we split the problem into three simpler sub-problems.

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## Dealing with registers by 'divide-and-conquer'

In order to explain the difficult problem of generating efficient code for register machines, we split the problem into three simpler sub-problems.

- Generate code assuming an unlimited supply of registers.

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## Dealing with registers by 'divide-and-conquer'

In order to explain the difficult problem of generating efficient code for register machines, we split the problem into three simpler sub-problems.

- ▶ Generate code assuming an unlimited supply of registers.
- ▶ Modify the translator to evaluate expressions in the order which minimises the number of registers needed, while still generating efficient code.

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## Dealing with registers by 'divide-and-conquer'

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- ▶ Invent a scheme to handle cases where we run out of registers.



## Dealing with registers by 'divide-and-conquer'

In order to explain the difficult problem of generating efficient code for register machines, we split the problem into three simpler sub-problems.

- ▶ Generate code assuming an unlimited supply of registers.
- ▶ Modify the translator to evaluate expressions in the order which minimises the number of registers needed, while still generating efficient code.
- ▶ Invent a scheme to handle cases where we run out of registers.

Let's start by looking at register machines with an **unlimited** number of registers.

Commands for register machines

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## Commands for register machines

We assume an **unlimited** supply of registers  $R0, R1, R2, \dots$  ranged over by  $r, r'$  We call these general purpose registers (as distinct from PC, SP).

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## Commands for register machines

We assume an **unlimited** supply of registers R0, R1, R2, ... ranged over by  $r, r'$ . We call these general purpose registers (as distinct from PC, SP).

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Nop	Does nothing
Pop r	removes the top of the stack and stores it in register r

Push r	Pushes the content of the register r on stack
--------	---

Load r x	Loads the content of memory location x into register r
----------	--

LoadImm r n	Loads integer n into register r
-------------	---------------------------------

Store r x	Stores the content of register r in memory location x
-----------	---

CompGreater r r'	Compares the content of register r with the content of register r'. Stores 1 in r if former is bigger than latter, otherwise stores 0
------------------	---

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## Commands for register machines

CompEq r r'	Compares the content of register r with the content of register r'. Stores 1 in r if both are equal, otherwise stores 0
Jump l	Jumps to l
JumpTrue r l	Jumps to address/label l if the content of register r is not 0
JumpFalse r l	Jumps to address/label l if the content of register r is 0
Plus r r'	Adds the content of r and r', leaving the result in r
...	Remaining arithmetic operations are similar

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## Commands for register machines

CompEq r r'      Compares the content of register r with the content of register r'. Stores 1 in r if both are equal, otherwise stores 0

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...      Remaining arithmetic operations are similar

Some commands have arguments (called operands). They take two (if the command has one operand) or three units of storage, the others only one. These operands need to be specified in the op-code, unlike with the stack machine. (Why?)

Commands for register machines

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Commands for register machines

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Question: Why do we bother with stack operations at all?

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Question: Why do we bother with stack operations at all?

Important for e.g. procedure/method invocation. We'll talk about that later.

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Source language

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Source language

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Our source language is unchanged: a really simple imperative language.

$$\begin{array}{l} M ::= M; M \mid \text{for } x = E \text{ to } E \{ M \} \mid x := E \\ E ::= n \mid x \mid E + E \mid E - E \mid E * E \mid E / E \mid -E \end{array}$$

Everything that's difficult to compile, e.g. procedures, objects, is left out. We come to that later.

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Code generation for register machines

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## Code generation for register machines

```
def codegen ( s : AST, target : Register )  
    : List [ Instruction ]
```

```
def codegenExpr ( exp : Expr, target : Register )  
    : List [ Instruction ]
```

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Important convention 1:

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Important convention 1: The code generated by  
`codegenExpr( e, i )` can use registers `Ri, Ri+1, ..`  
**upwards**, but must leave the other registers `R0 ... Ri-1`  
**unchanged!**

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is returned in register `target`.

One way of thinking about this `target` is that it is used to track  
where the stack pointer would point.

# Code generation for register machines

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```

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    : List [ Instruction ]
```

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Important convention 1: The code generated by `codegenExpr( e, r )` can use registers `Ri, Ri+1, .. upwards`, but must leave the other registers `R0 ... Ri-1 unchanged`!

Important convention 2: The result of evaluating the expression is returned in register `target`.

One way of thinking about this `target` is that it is used to track where the stack pointer would point.

Similar conventions for `codegen` for statements.

Code generation for constants

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# Assignment Project Exam Help

```
def codegenExpr ( exp : Expr, target : Register ) = {  
  if exp is of shape  
  :.  
  Const ( n ) then  
    List ( I_LoadImm ( target, n ) ) } }
```

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Code generation for variables

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# Assignment Project Exam Help

```
def codegenExpr ( exp : Expr, target : Register ) = {  
  if exp is of shape  
    Ident ( x ) then  
    List ( I_Load ( target, x ) )
```

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Code generation for binary expressions

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## Code generation for binary expressions

```
def codegenExpr ( exp : Expr, target : Register ) = {  
  if exp is of shape
```

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```
    Binop ( lhs, op, rhs ) then {  
      codegenExpr ( rhs, target ) ++  
      codegenExpr ( lhs, target+1 ) ++  
      codegenBinop ( op, target, target+1 ) }  
  }
```

where

```
def codegenBinop ( op : Op, r1 : Register,  
                  r2 : Register ) = {  
  if op is of shape  
    Plus then List ( I_Plus ( r1, r2 ) )  
    Minus then List ( I_Minus ( r1, r2 ) )  
    Times then List ( I_Times ( r1, r2 ) )  
    Divide then List ( I_Divide ( r1, r2 ) ) } }
```

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Code generation for binary expressions

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## Code generation for binary expressions

Note that the call `codegenExpr (lhs, target+1)` in

```
Binop ( lhs, op, rhs ) then {  
    codegenExpr ( rhs, target ) ++  
    codegenExpr ( lhs, target+1 ) ++  
    codegenBinop ( op, target, target+1 ) }
```

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leaves the result of the first call `codegenExpr (rhs, target)` in the register `target` unchanged by our assumptions that `codegenExpr` never modifies registers below its second argument.

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```

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leaves the result of the first call `codegenExpr (rhs, target)` in the register `target` unchanged by our assumptions that `codegenExpr` never modifies registers below its second argument.

Please convince yourself that each clause of `codegenExpr` really implements this guarantee!

Example  $(x*3)+4$

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Example  $(x*3)+4$

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Compiling the expression  $(x*3)+4$  (to target register r17, say) gives:

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Example  $(x*3)+4$

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Compiling the expression  $(x*3)+4$  (to target register r17, say) gives:

```
LoadImm r17 4
```

```
LoadImm r18 3
```

```
Load r19 x
```

```
Times r18 r19
```

```
Plus r17 r18
```

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How can this be improved (1)?

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How can this be improved (1)?

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Let's use commutativity of addition ( $a+b = b+a$ ) and compile  $4+(x*3)$ ! When we compile it, we obtain:

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How can this be improved (1)?

# Assignment Project Exam Help

Let's use commutativity of addition ( $a+b = b+a$ ) and compile  $4+(x*3)$ ! When we compile it, we obtain:

```
LoadImm r17 3
```

```
Load r18 x
```

```
Times r17 r18
```

```
LoadImm r18 4
```

```
Plus r17 r18
```

How is this better?

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Side by side

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Side by side

Compilation of  $(x*3)+4$

```
LoadImm r17 4  
LoadImm r18 3  
Load r19 x  
Times r18 r19  
Plus r17 r18
```

Compilation of  $4+(x*3)$

```
LoadImm r17 3  
Load r18 x  
Times r17 r18  
LoadImm r18 4  
Plus r17 r18
```

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## Side by side

Compilation of  $(x*3)+4$

```
LoadImm r17 4
LoadImm r18 3
Load r19 x
Times r18 r19
Plus r17 r18
```

Compilation of  $4+(x*3)$

```
LoadImm r17 3
Load r18 x
Times r17 r18
LoadImm r18 4
Plus r17 r18
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The translation on the left uses 3 registers, while the right only two. We are currently assuming an unbounded number of registers, so who cares...

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## Side by side

Compilation of  $(x*3)+4$

```
LoadImm r17 4  
LoadImm r18 3  
Load r19 x  
Times r18 r19  
Plus r17 r18
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Compilation of  $4+(x*3)$

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LoadImm r17 3  
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Times r17 r18  
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Plus r17 r18
```

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The translation on the left uses 3 registers, while the right only two. We are currently assuming an unbounded number of registers, so who cares... For realistic CPUs the number of registers is small, so smart translation strategies that save registers are better. More on this later!

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How can this be improved (2)?

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How can this be improved (2)?

We used two registers – can we get away with fewer?

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## How can this be improved (2)?

We used two registers – can we get away with fewer?

Probably not with this machine architecture. But some widely used CPUs can use constants directly in arithmetic operations,

e.g.

```
MulImm r 3
```

Multiplies the content of register r with 3, storing the result in r

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## How can this be improved (2)?

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`MulImm r 3`

Multiplies the content of register `r` with 3, storing the result in `r`

`AddImm r 4`

Adds the content of register `r` with 3, storing the result in `r`

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## How can this be improved (2)?

We used two registers – can we get away with fewer?

Probably not with this machine architecture. But some widely used CPUs can use constants directly in arithmetic operations.

e.g.

```
MulImm r 3
```

Multiplies the content of register r with 3, storing the result in r

```
AddImm r 4
```

Adds the content of register r with 3, storing the result in r

Then  $(x \times 3) + 4$  translates to

```
Load r17 x
```

```
TimesImm r17 3
```

```
PlusImm r17 4
```

This is a different **address(ing) mode**. We may see more about this later.

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Translation of statements

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Now we do something more interesting.



Bounded register numbers

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## Bounded register numbers

It's easy to compile to register machine code, when the number of registers is unlimited. Now we look at compilation to register machines with a fixed number of registers.

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Let's go to the other extreme. just one register called **accumulator**. Operations take one of their arguments from the accumulator, and store the result in the accumulator. Additional arguments are taken from the top of the stack.

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The effect is that most expressions get the full benefit of registers, while unusually large expressions are handled correctly.