

Operating Systems

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Lecture 10a

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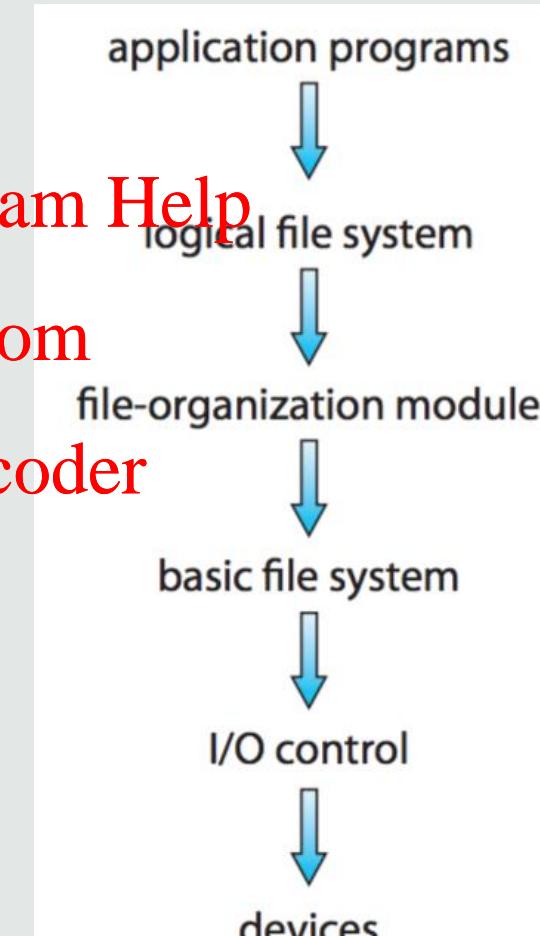
Previously

- Logical file system
 - Provides file interface (e.g., system calls)
- File organisation module
 - Manages block allocation of files
E.g. i-nodes in UNIX
- Basic file system
 - Block-based storage format
E.g. FAT-32, NTFS, ext4
- I/O device drivers
 - Physical access to storage media
E.g. HD, DVD, USB

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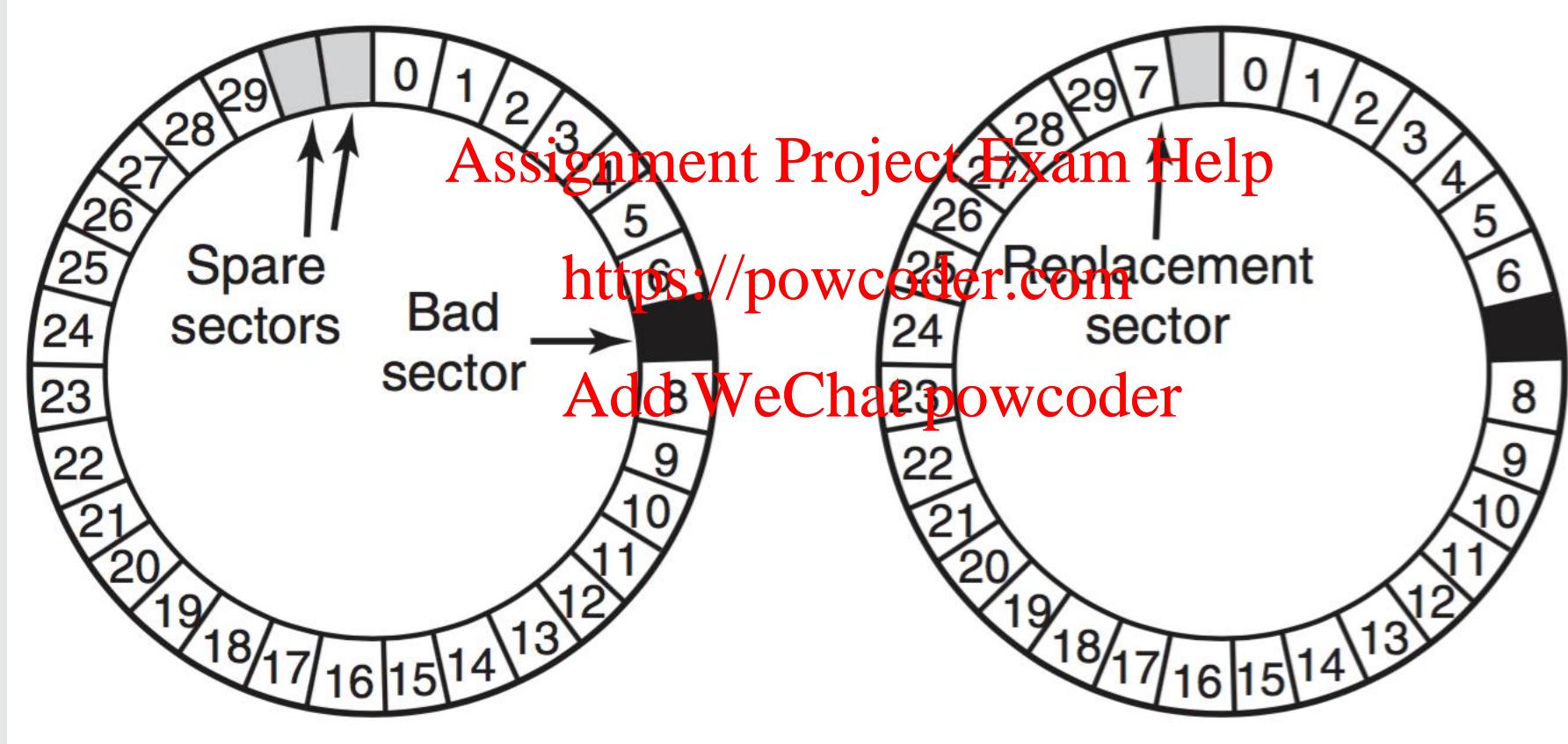
Recap: Questions

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Recap questions

1. Which factors have an impact on maximum volume storage capacity?
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2. Which factors have an impact on the maximum file size?
3. What are the effects of different block sizes?
4. How can we detect or prevent inconsistencies in a file system?
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5. What is journaling?
6. What are the advantages/disadvantages of a write-through cache?

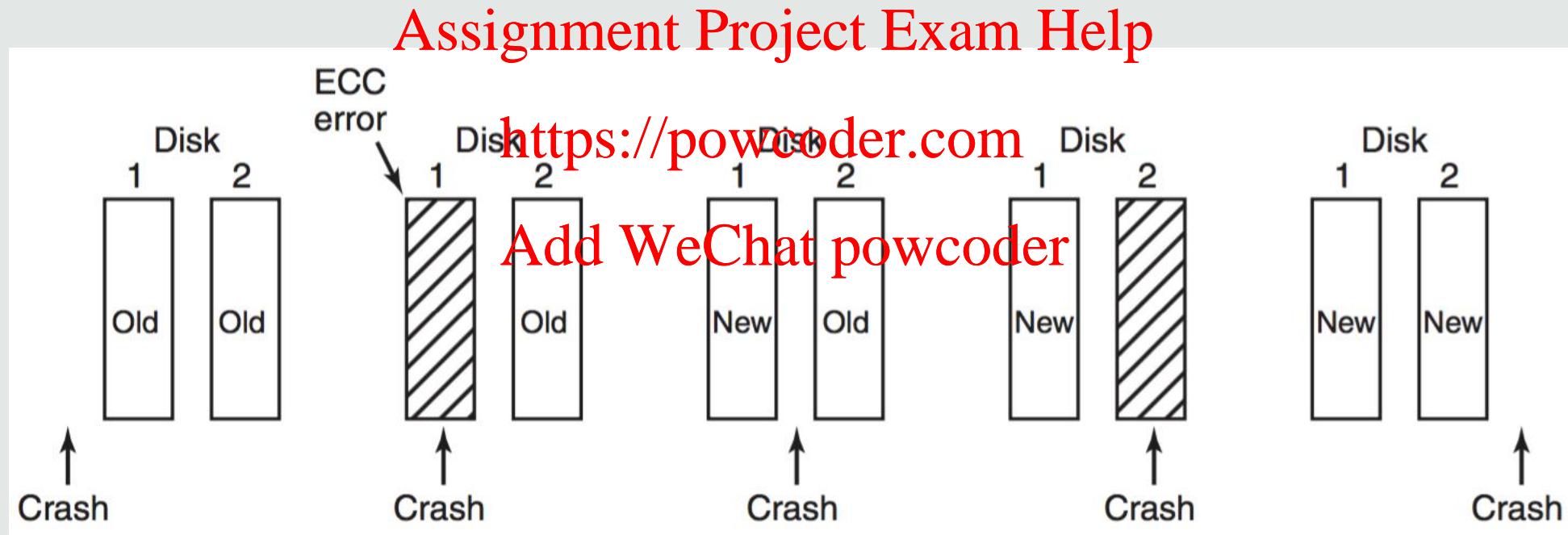
Bad blocks



Stable storage

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- Guaranteed consistent data on disk?
- E.g. two disks, write same data to each sequentially:

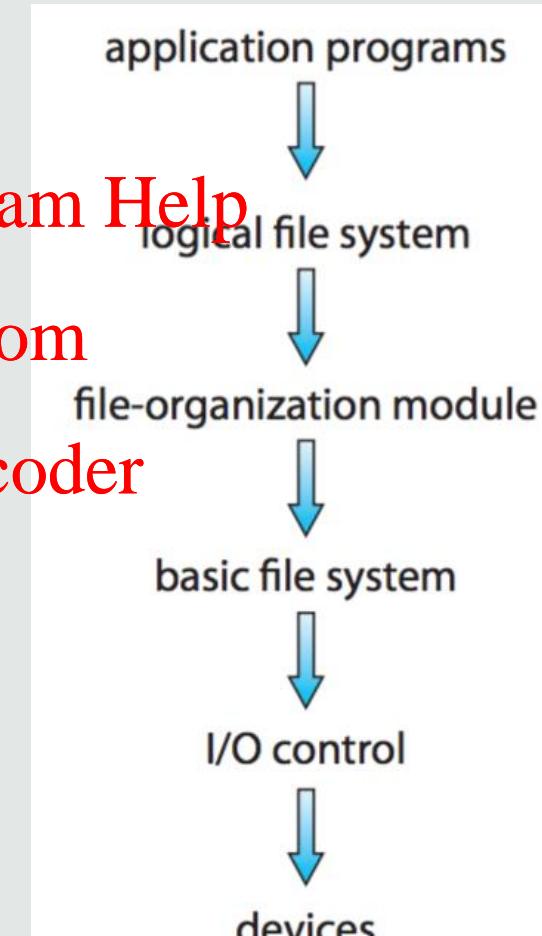


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I/O System

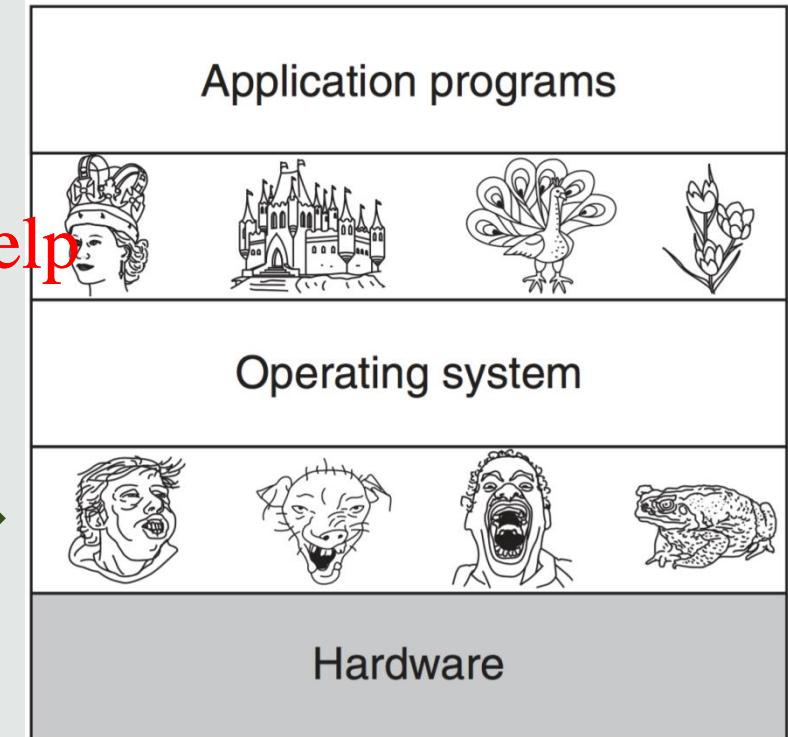
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- Probably the most complex part of an OS (and the “ugliest” – remember lecture 1a?)
- Numerous devices with different needs and properties
- Continuously optimised and updated to support new devices
- Device drivers interact with hardware (without abstraction)
- Parts written in assembly language, error-prone

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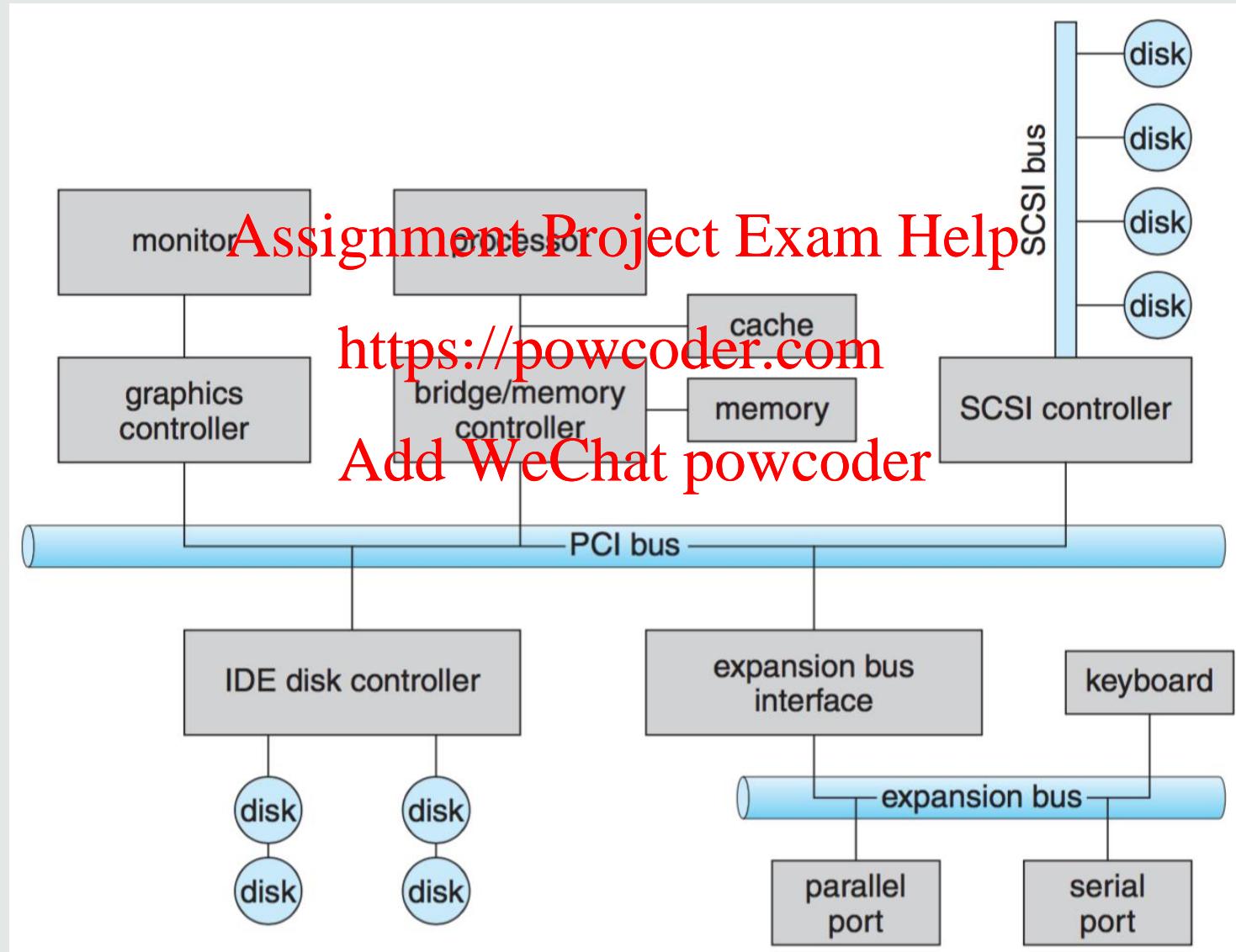
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I/O Devices

- Human-machine interface: display, keyboard, audio, video, . . .
- Sensors, actuators, storage, network communication, printers, . . .

Bus architecture



I/O device properties

aspect	variation	example
data-transfer mode	character block	terminal disk
access method	sequential random	modem CD-ROM
transfer schedule	synchronous asynchronous	tape keyboard
sharing	dedicated sharable	tape keyboard
device speed	latency seek time transfer rate delay between operations	
I/O direction	read only write only read-write	CD-ROM graphics controller disk

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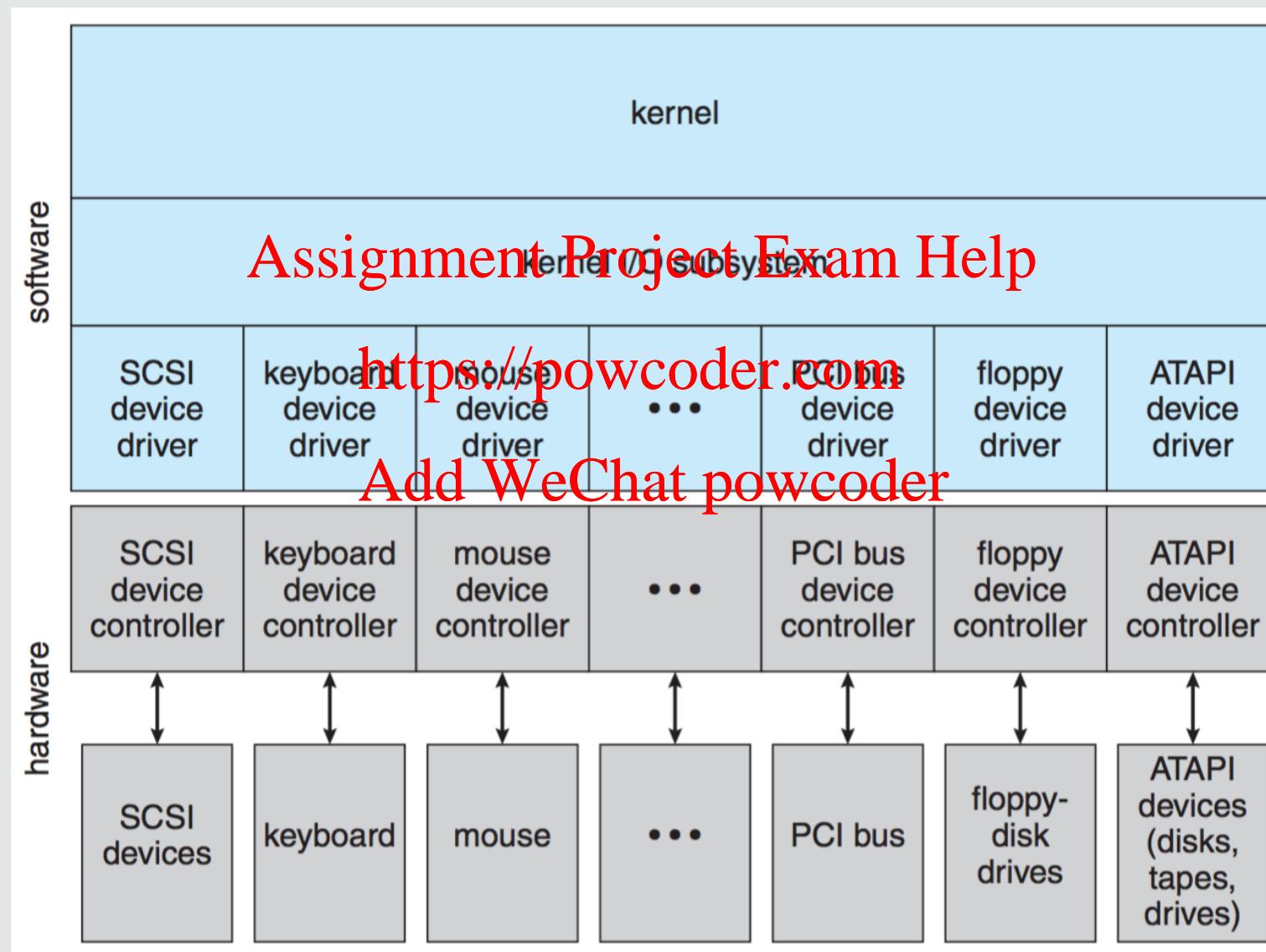
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Data rates

Device	Data rate
Keyboard	10 bytes/sec
Mouse	100 bytes/sec
56K modem	7 KB/sec
Scanning at 200 dpi	1 MB/sec
Digital camcorder	3.5 MB/sec
4x Blu-ray disc	13 MB/sec
802.11n Wireless	37.5 MB/sec
USB 2.0	60 MB/sec
FireWire 800	100 MB/sec
Gigabit Ethernet	125 MB/sec
SATA 3 disk drive	600 MB/sec
USB 3.0	625 MB/sec
SCSI Ultra 5 bus	640 MB/sec
Single-lane PCIe 3.0 bus	985 MB/sec
Thunderbolt 2 bus	2.5 GB/sec
SONET OC-768 network	5 GB/sec

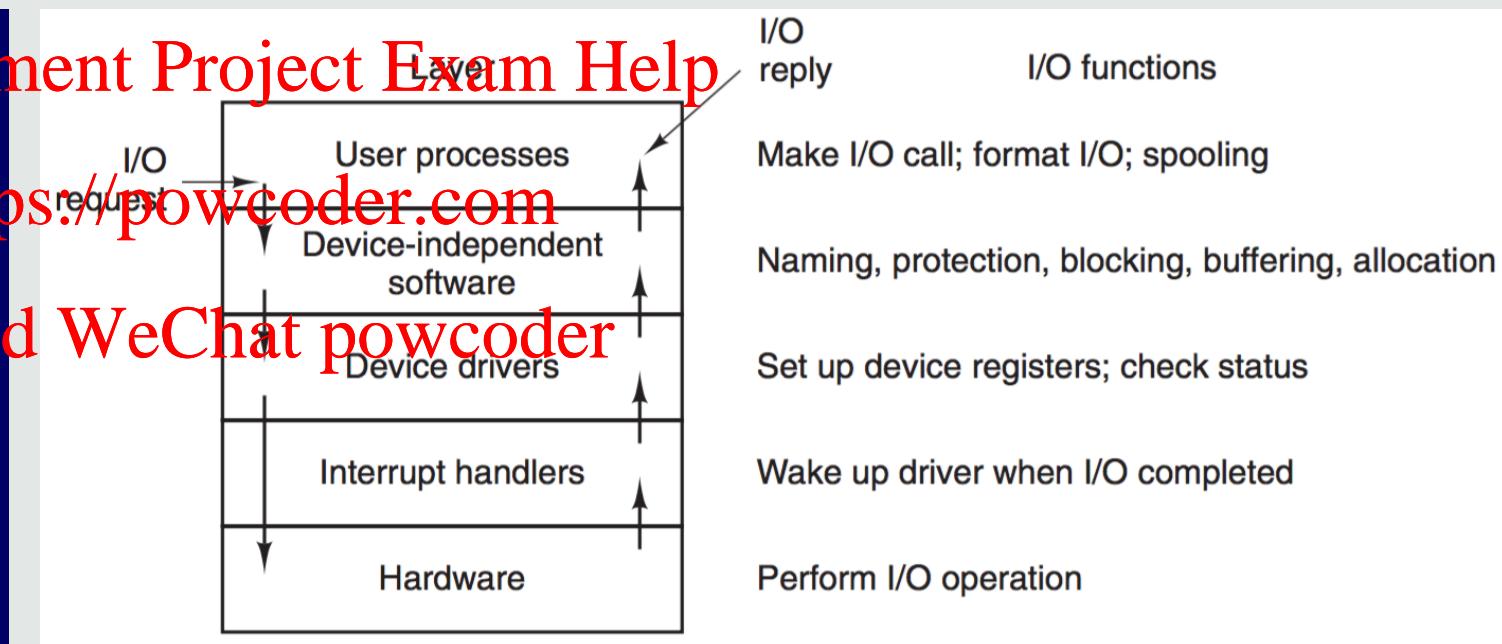
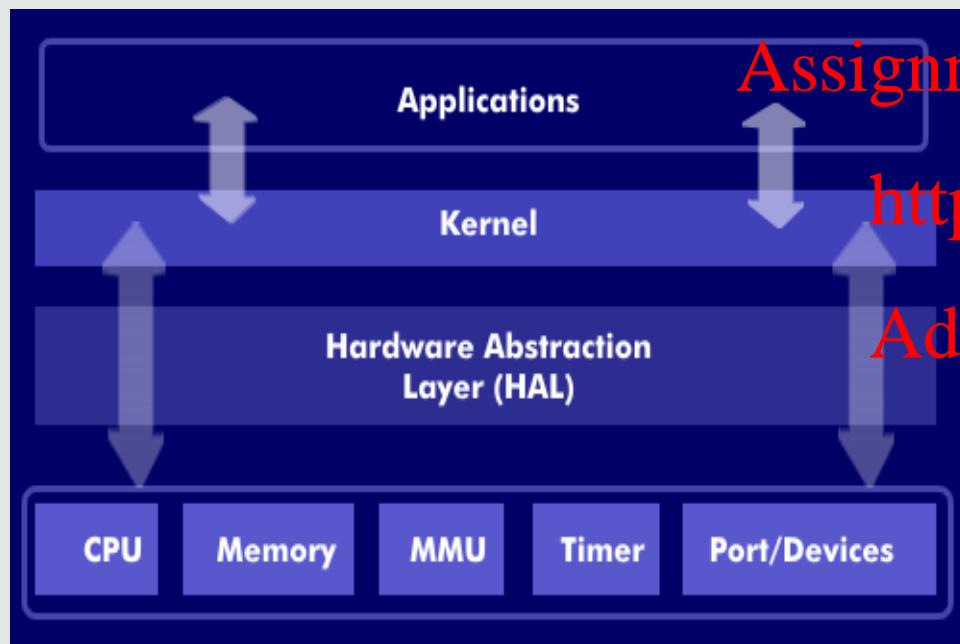
I/O Subsystem

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Layered I/O Structure

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Interface for communication between device driver and device

Registers:

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- Data-in: data read by device driver
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- Data-out: data written by device driver
- Status: read by device driver
 - e.g. command completion, byte available to read, error
- Control: written by device driver
 - e.g. command, communication and device configuration

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Simple example of lower-level operations

1602 LCD display / HD44780 MCU

- Small display with an integrated controller
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- 2 lines, 16 characters each
- 80 bytes of RAM
- 8 bits for data, 3 bits for control
- Simple instruction set (init, cursor, clear screen, etc.)
- RS (register-select) control bit determines if what is sent is an instruction (RS=0) or data (RS=1)
- R/W mode (wait for not-busy / send instruction or data) – (R/W=0 for writing)
- Supports 2x4-bit or 1x8-bit data transfers



Simple example of lower-level operations

1602 LCD display / HD44780 MCU



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Pin number	Pin name	Function
1	V _{SS}	Power supply (GND)
2	V _{DD}	Power supply (5 V)
3	V _E	Contrast adjust
4	R/S	Register select signal
5	R/W	Data read / write
6	E	Enable signal
7	D _{B0}	Data bus line bit 0
8	D _{B1}	Data bus line bit 1
9	D _{B2}	Data bus line bit 2
10	D _{B3}	Data bus line bit 3
11	D _{B4}	Data bus line bit 4
12	D _{B5}	Data bus line bit 5
13	D _{B6}	Data bus line bit 6
14	D _{B7}	Data bus line bit 7
15	A	Power supply for LED backlight (5 V)
16	K	Power supply for LED backlight (GND)

Simple example of lower-level operations

1602 LCD display / HD44780 MCU – Essential initialization procedure

- Set RS & E pins to 0

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- Configure function mode

- Width of data packets (4 or 8 bits)

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- Number of display lines used (1 or 2)

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- Symbol size (5x8 or 5x10 pixels)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	BW	N	F	X	X

BW = 0 → 4 bit mode

N = 0 → 1 line mode

F = 0 → 5×8 pixels

BW = 1 → 8 bit mode

N = 1 → 2 line mode

F = 1 → 5×10 pixels

X = Don't care bits (can be 0 or 1)

- Configure display mode

- Display on/off

- Cursor on/off

- Cursor blinking

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	P	C	B

P = 0 → display off

C = 0 → cursor off

B = 0 → cursor no blink

P = 1 → display on

C = 1 → cursor on

B = 1 → cursor blinking

I/O Controller Example: UART 16550

TABLE II. Summary of Registers

Bit No.	Register Address											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)	
RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM	
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Carrier Detect (DCFS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	XMIT FIFO Reset	Number of Stop Bit (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 2)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 2)	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: These bits are always 0 in the 16450 Mode.

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Programmed I/O

1. Transfer data from main memory into I/O registers
2. Send I/O command <https://powcoder.com>
3. Wait for completion by busy waiting
4. Transfer results from I/O registers into main memory

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Interrupt-driven I/O

1. Setup interrupt and interrupt service routine (ISR)
2. Transfer data from main memory into I/O registers
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3. Send I/O command
4. On completion, ISR transfers results from I/O registers into main memory

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Direct Memory Access I/O (DMA)

1. Send I/O command to DMA controller
2. DMA controller handles data transfer from/to main memory
3. DMA controller interrupts to signal completion

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Programmed I/O - Example

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Also known as polling.

Example: Output data transfer:

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1. Device driver repeatedly reads busy bit until clear.
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2. Device driver writes data into data-out register and sets the write command bit, and continues busy waiting
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3. Controller notices the write command bit set and sets the busy bit.
4. Controller reads data-out register and sends data to device.
5. Controller clears write command bit, clears error bit in status register if transfer succeeded, and clears busy bit to indicate that it is finished.
6. Device driver detects that the transfer is complete.

Polling example: UART 16550

TABLE II. Summary of Registers

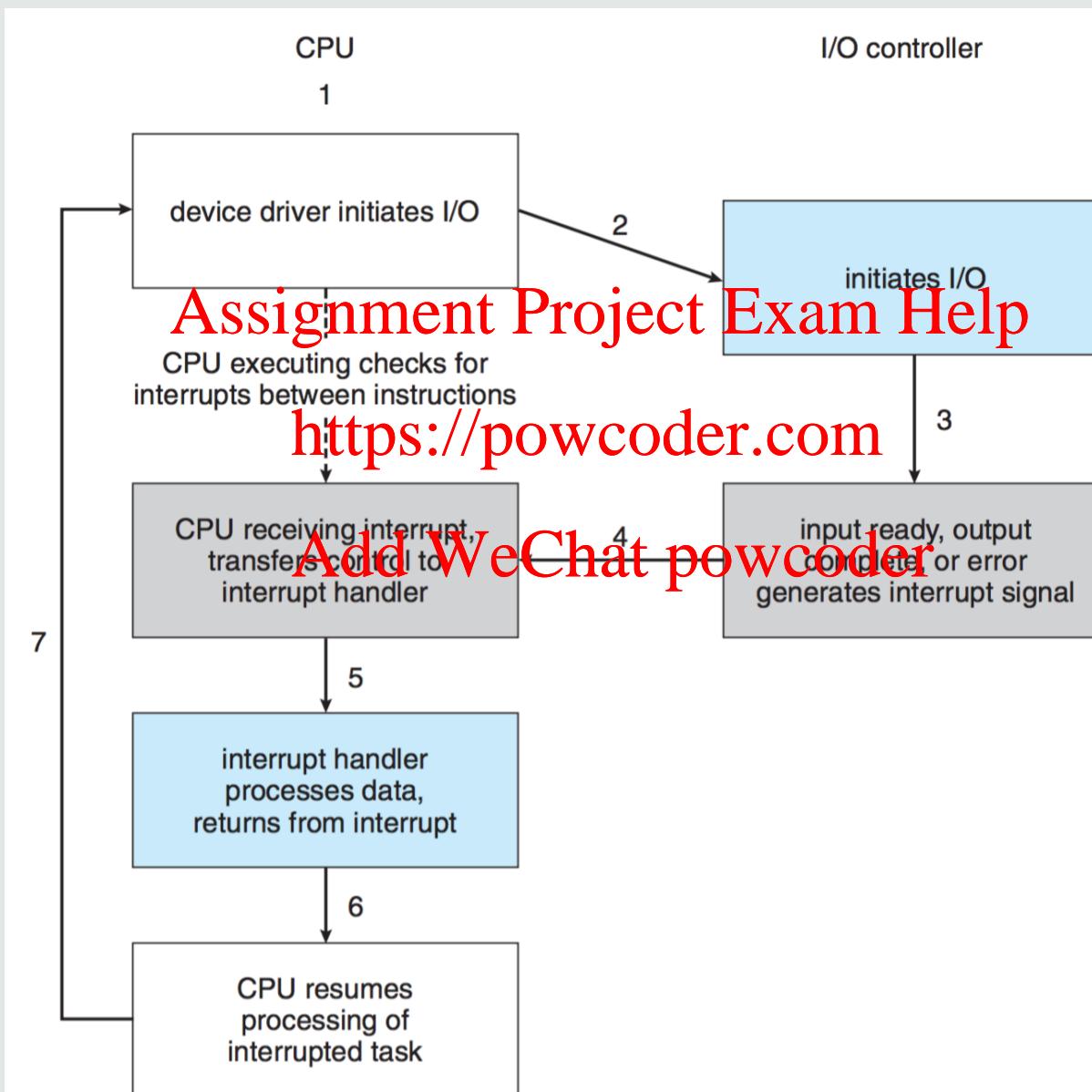
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Interrupt-driven I/O - Example

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Interrupt Example: UART 16550

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Controlling Interrupts

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- HW-provided mechanisms
 - Global disabling
 - Selective disabling (masking)
 - Priorities
- Interrupt „scheduling“?
- Some OS execute ISRs as kernel threads.

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vector number	description
0	divide error
1	debug exception
2	null interrupt
3	breakpoint
4	INTO-detected overflow
5	bound range exception
6	invalid opcode
7	device not available
8	double fault
9	coprocessor segment overrun (reserved)
10	invalid task state segment
11	segment not present
12	stack fault
13	general protection
14	page fault
15	(Intel reserved, do not use)
16	floating-point error
17	alignment check
18	machine check
19–31	(Intel reserved, do not use)
32–255	maskable interrupts

Direct Memory Access (DMA) I/O

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Programmed I/O and low-level interrupt-driven I/O

- Waste a lot of CPU cycles

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Better handled by specialised hardware: DMA Controller

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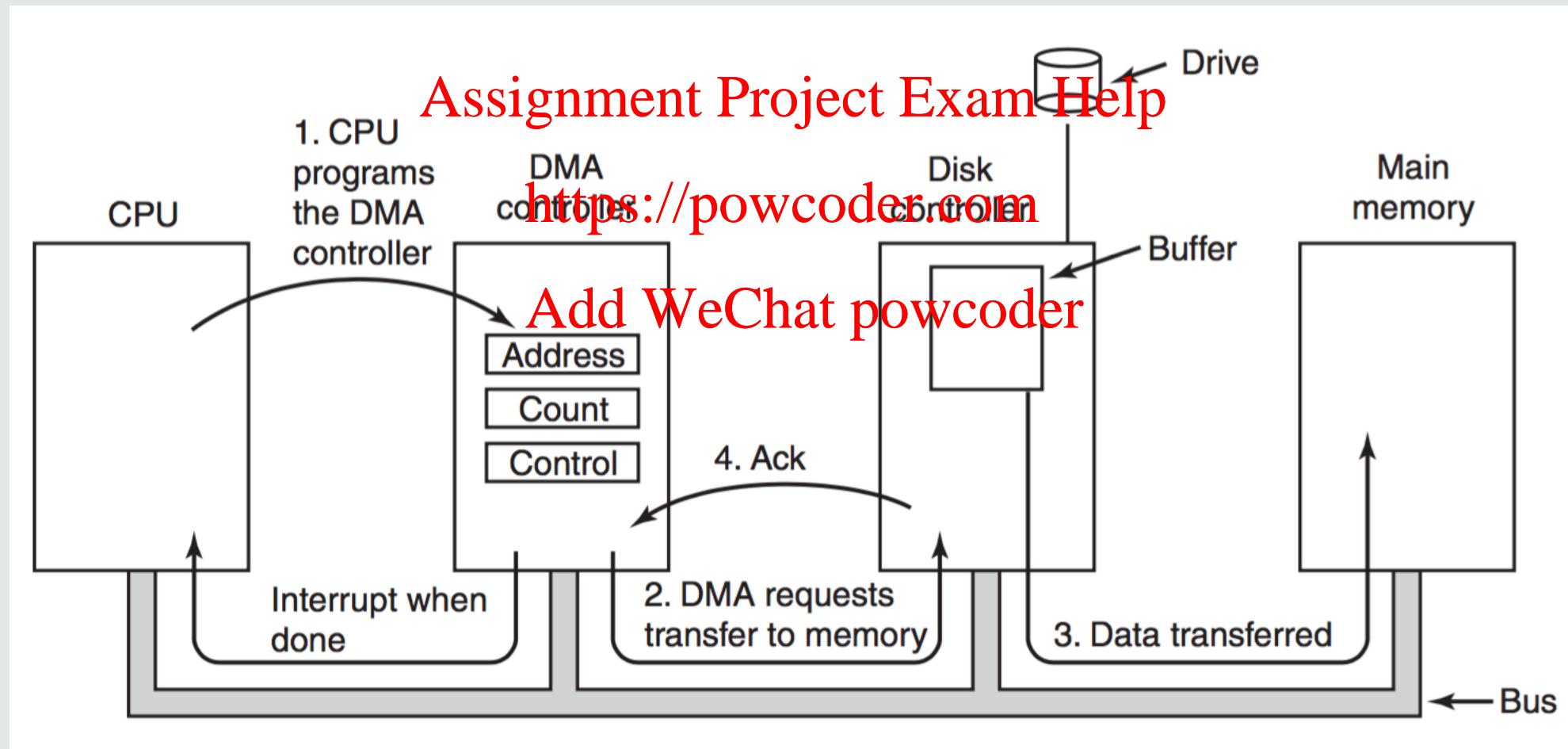
- Handles transfer autonomously
- Bottleneck: bus
 - “Steals” bus cycles from CPU
- Device must support DMA

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Direct Memory Access (DMA) I/O

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Example: Reading data from a hard disk drive



Non-blocking I/O

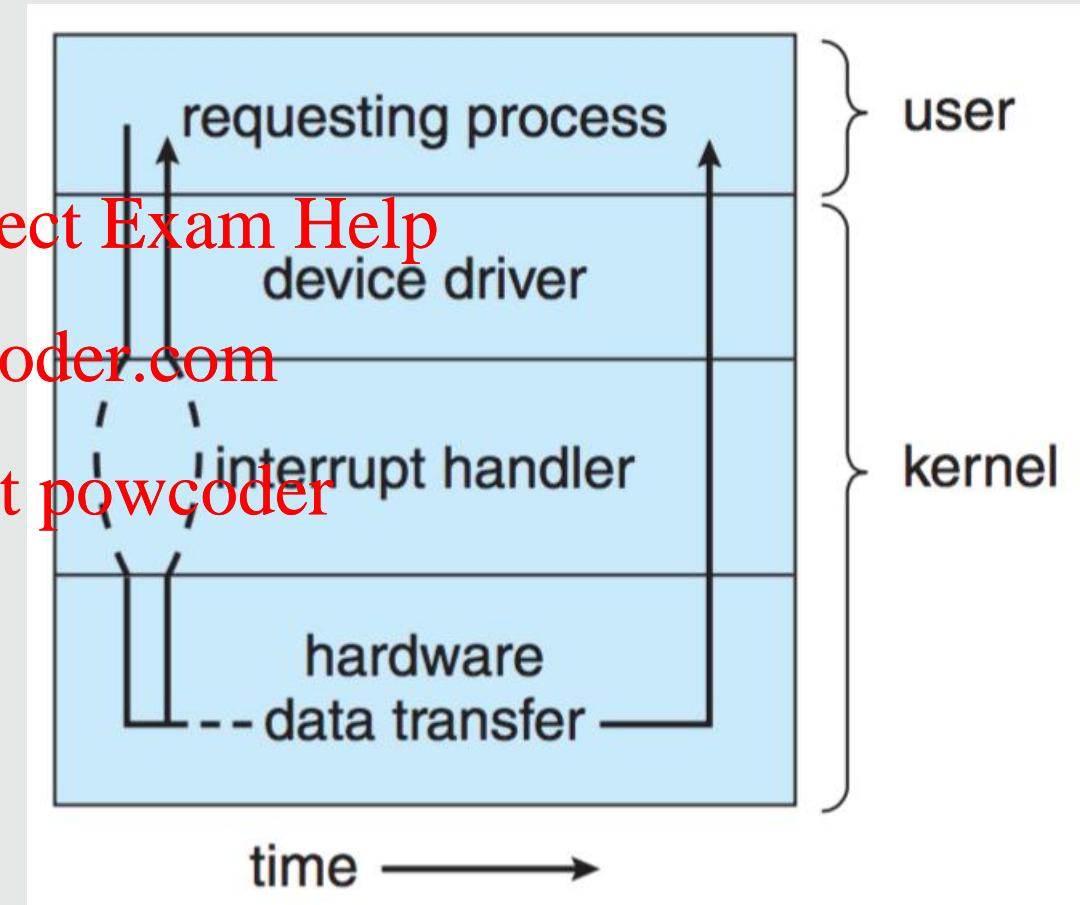
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1. Process initiates I/O
2. Process continues execution
3. Notification by callback in a separate thread item
“Asynchronous”

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Blocking I/O

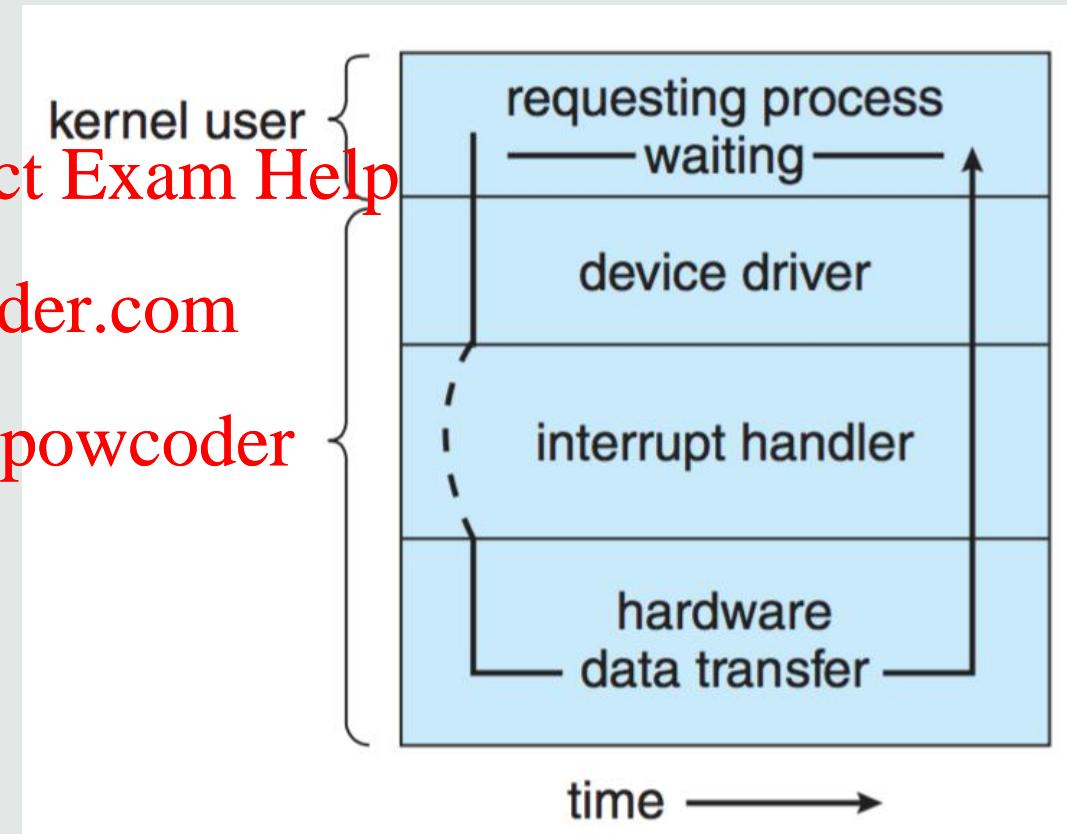
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1. Process initiates I/O
2. Process blocks
3. OS unblocks process when I/O finished
4. "Synchronous"

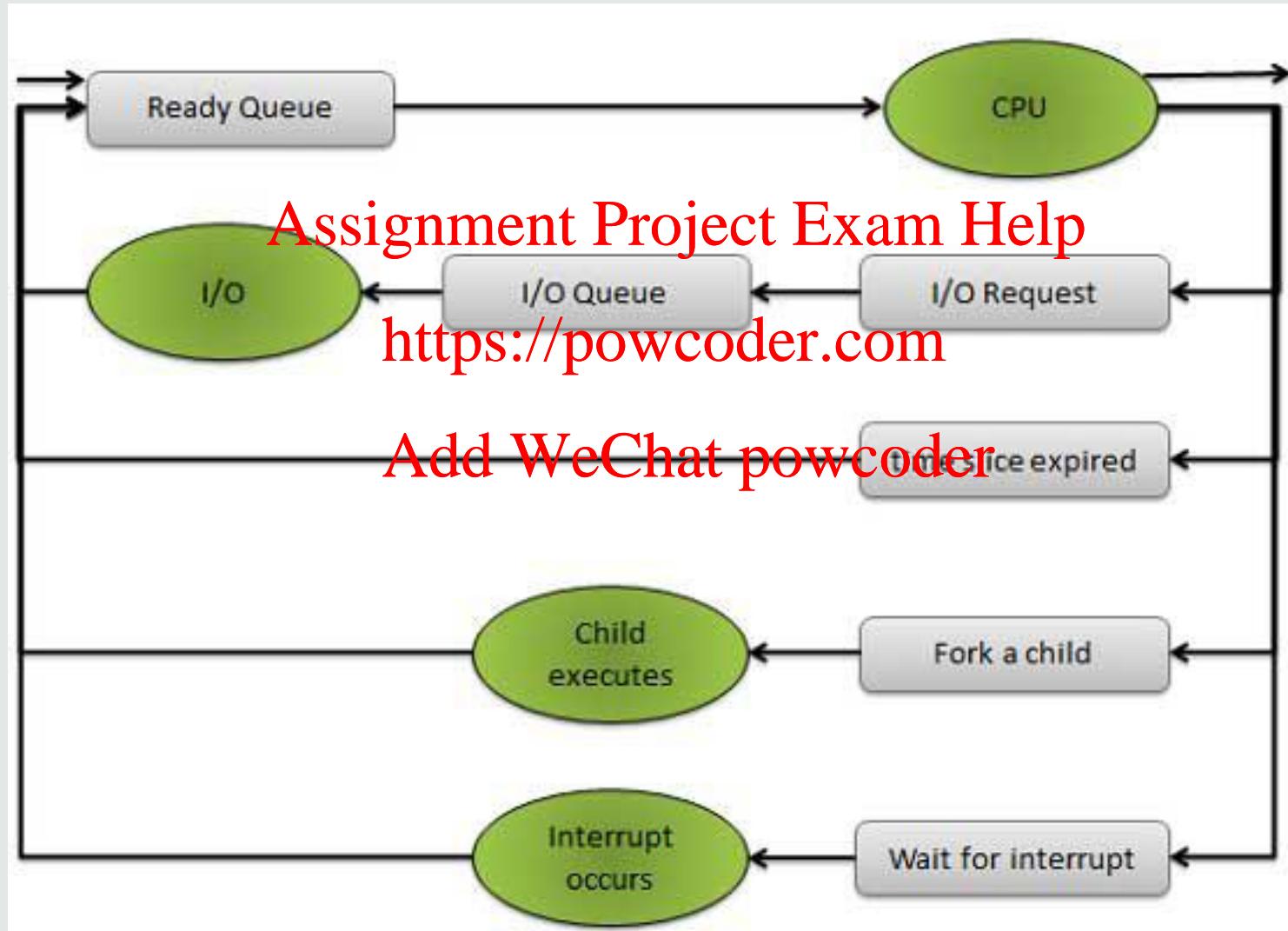
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I/O Queue



I/O System

- I/O device properties
- Layered structure
- I/O controller
- Device driver

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Interaction protocols

- Polling
- Interrupts
- Direct memory access (DMA)

Blocking vs non-blocking I/O

- Tanenbaum & Bos., Modern Operating Systems

- Chapter 5

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- Silberschatz et al., Operating System Concepts

- Chapter 13

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- Introduction
 - Operating System Architectures
 - Processes
 - Threads - Programming
 - Process Scheduling - Evaluation
 - Process Synchronisation
 - Deadlocks
 - Memory Management
 - File Systems
 - Input / Output (continued)
 - Security and Virtualisation
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