UCCD1133
Introduction to Computer Organisation and Architecture

Chapter 3
Basic Concept of Logic

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Chapter 3-6

Memory element and register

Outline

- Delay flip-flops (DFF)
- Registers

Memory Elements

- Memory elements are the most primitive sequential circuits for storing a bit value.

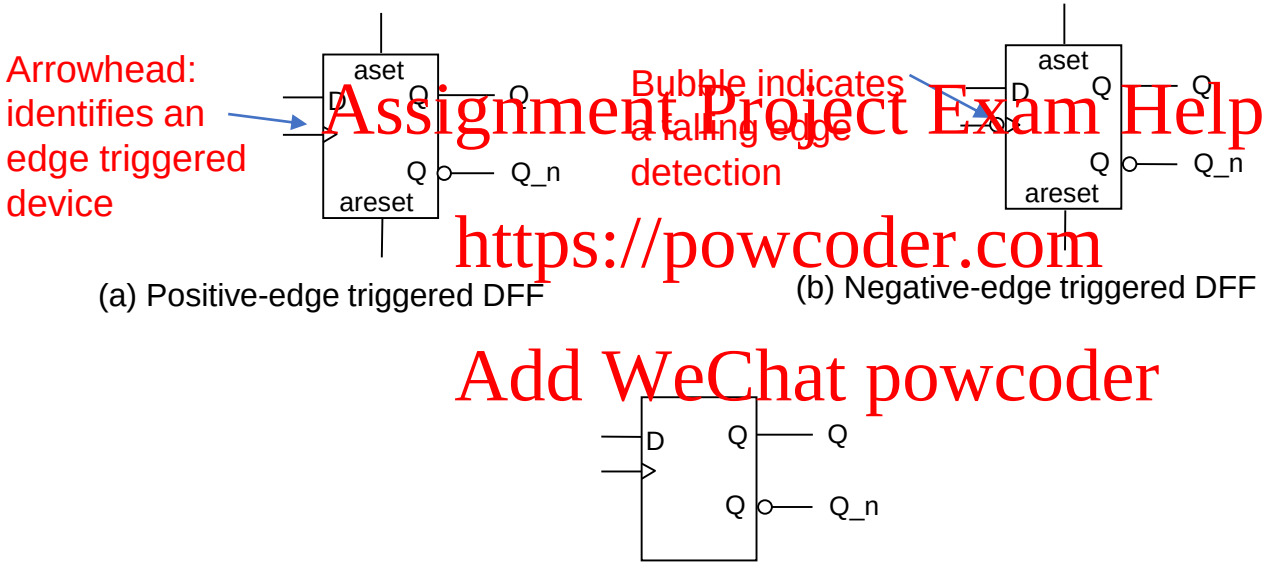
- 2 types of memory elements
  - Latch (clockless)
  - **Flip-flop (clock based)** ✓

- Common types of flip-flop:
  - Set-Reset flip-flop (SRFF).
  - JK flip-flop (JKFF).
  - **Delay flip-flop (DFF)**
  - Toggle flip-flop (TFF).

Delay Flip-Flop (DFF)

- A flip-flop has edge sensitive behavior.
  - The output responds to the input data only during the active edge of the clock.

- Logic symbols of DFF:



(a) Positive-edge triggered DFF

(b) Negative-edge triggered DFF

(c) No aset and areset input

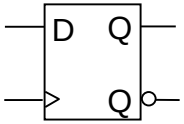
- The arrowhead pin: usually apply periodic signal – e.g. **clock signal**
- One FF -> one clock pin

- Aset: output become 1; areset: output become 0. (asynchronous inputs – regardless of clock).
- When not used, aset and areset inputs no need to show. Its only logic symbol.
- But in actual hardware implementation, need to Connect them to values that de-activate them.

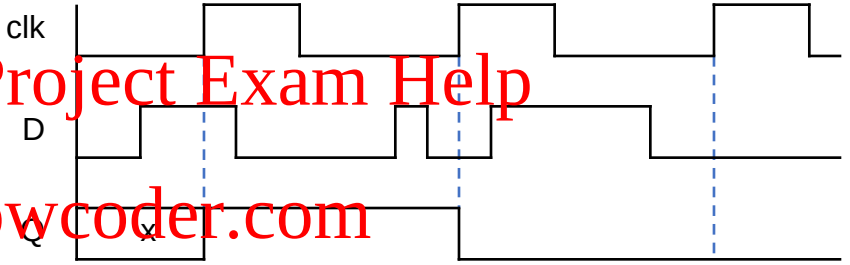
Delay Flip-Flop (DFF)

- A DFF copies input value at D (from one cycle) to output Q (in the next cycle) when **active clock edge** occurs.
  - At other times, not copied.

D flip-flop copies D to Q on the rising edge of the clock, and remembers its state at all other times



(a) DFF logic symbol



(c) Timing diagram (rising/positive edge triggered)

Inputs	Output	Function
D	Q*	
0	0	Copy
1	1	Copy

(b) Function table

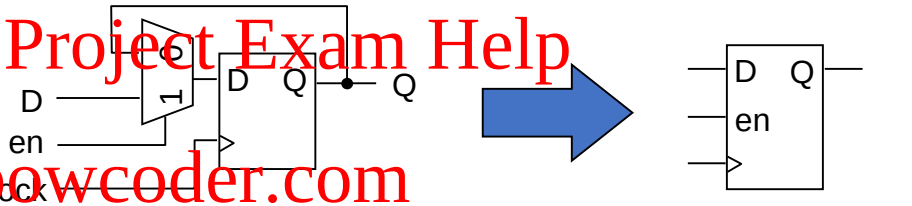
- 3 basic functionalities
  - To synchronise a signal to clock
    - How? Copy value at D to Q only during the active edge of the clock.
  - To delay a signal at D by one cycle.
    - The value should appear at Q in the next cycle (relative to the time at D).
  - To filter glitches that appears in a signal

DFF with Enable

- However, the previous DFF cannot store or hold a signal value.
- To hold a value, need to add a hold function into DFF
  → A DFF with enable

Inputs		Outputs	
Enable input E	**D**	**Q***	**Function**
0	d	Q	Hold
1	0	0	Copy
1	1	1	Copy

Function table for DFF with enable



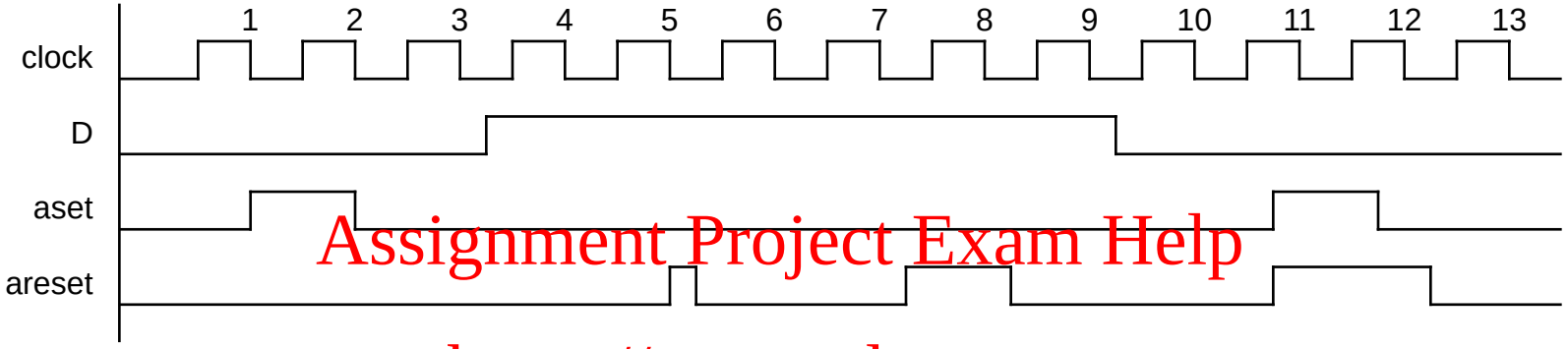
(a) Creating a storage effect by adding a Hold function into a DFF

(b) DFF with enable

Example

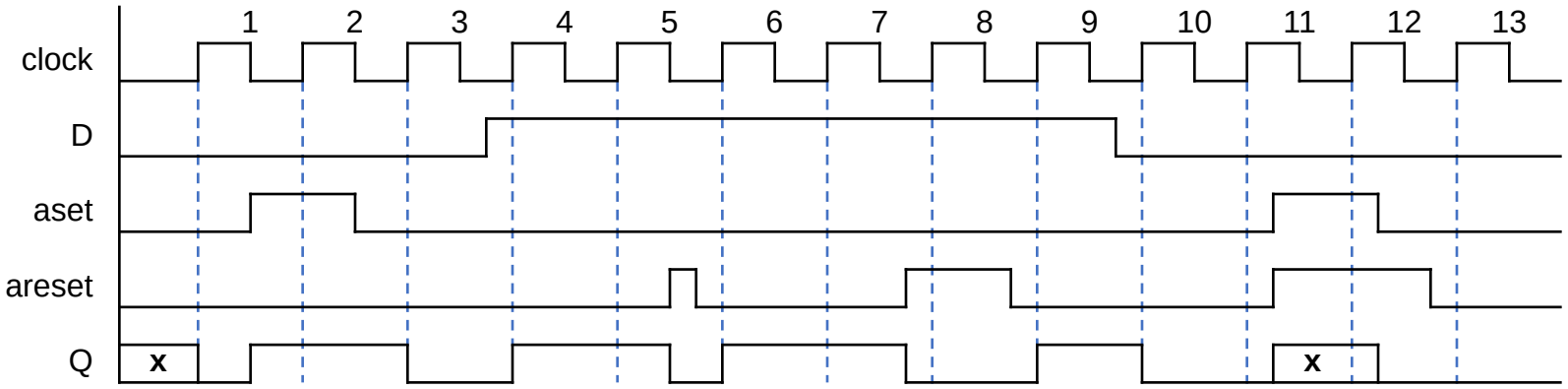
- Example 1

  Draw the output waveform of the positive-edge DFF given the input signals as below.



Solution 1

- To draw the output waveform, the output is computed one cycle by one cycle during the clock transition of LOW-to-HIGH (positive edge).



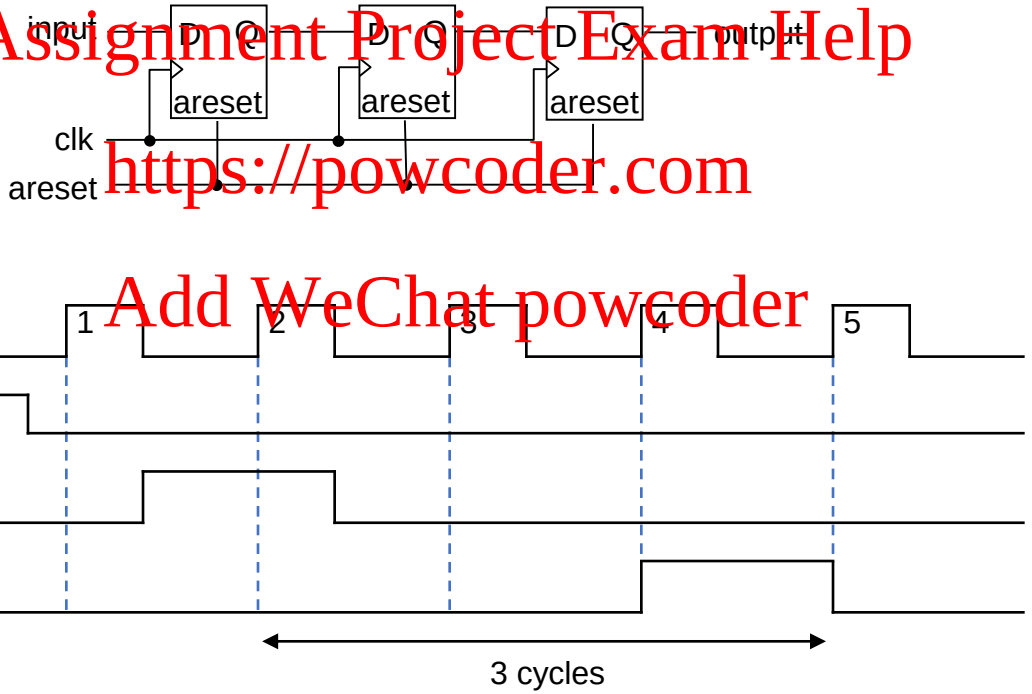
Depends on whether set or reset has the higher priority

Example

- Example 2

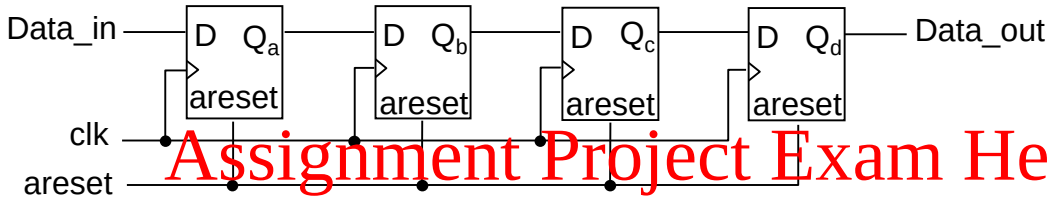
  Show how DFFs can be used to delay a signal by 3 clock cycles. Draw a timing diagram to illustrate the delay.

- Solution 2



Registers

- Register consists of a set of N flip-flops with a common clock input.
  - N is typically an integral power of 2
  - It is mainly build from D-type flip-flops



(a) A four bit serial-in/serial out shift register

- Registers can be replicated to build larger memory units. It is typically used as a fast temporary storage in a central processing unit (CPU).

- Each flip-flop can store one bit of information; therefore, the number of stages (flip-flops) in a register determines its storage capacity.

- A typical CPUs either store 32 or 64 bits in registers.

Register File

- A **register file** is a collection of registers.
  - Each of it is individually addressed.
  - By specifying the register number to be accessed, the register file can be read and written.

- Registers are grouped in array to form **M x N register file**
  - M registers, each N-bit wide
  - E.g.4 x 32 dual-port
    - Four 32-bit registers

- The interface of a register file should at least has:
  - A clock signal (CLK)
  - An input to specify the register number (address) (A)
  - An output read port (RD)
  - An input write port (WD)
  - A control bit(s) to enable/disable write operation (WE)