CHIP DESIGN AND USE
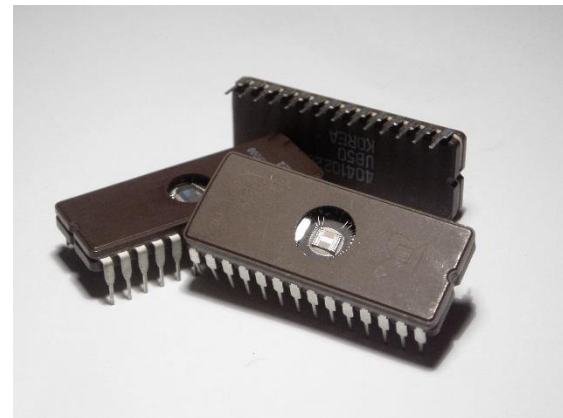
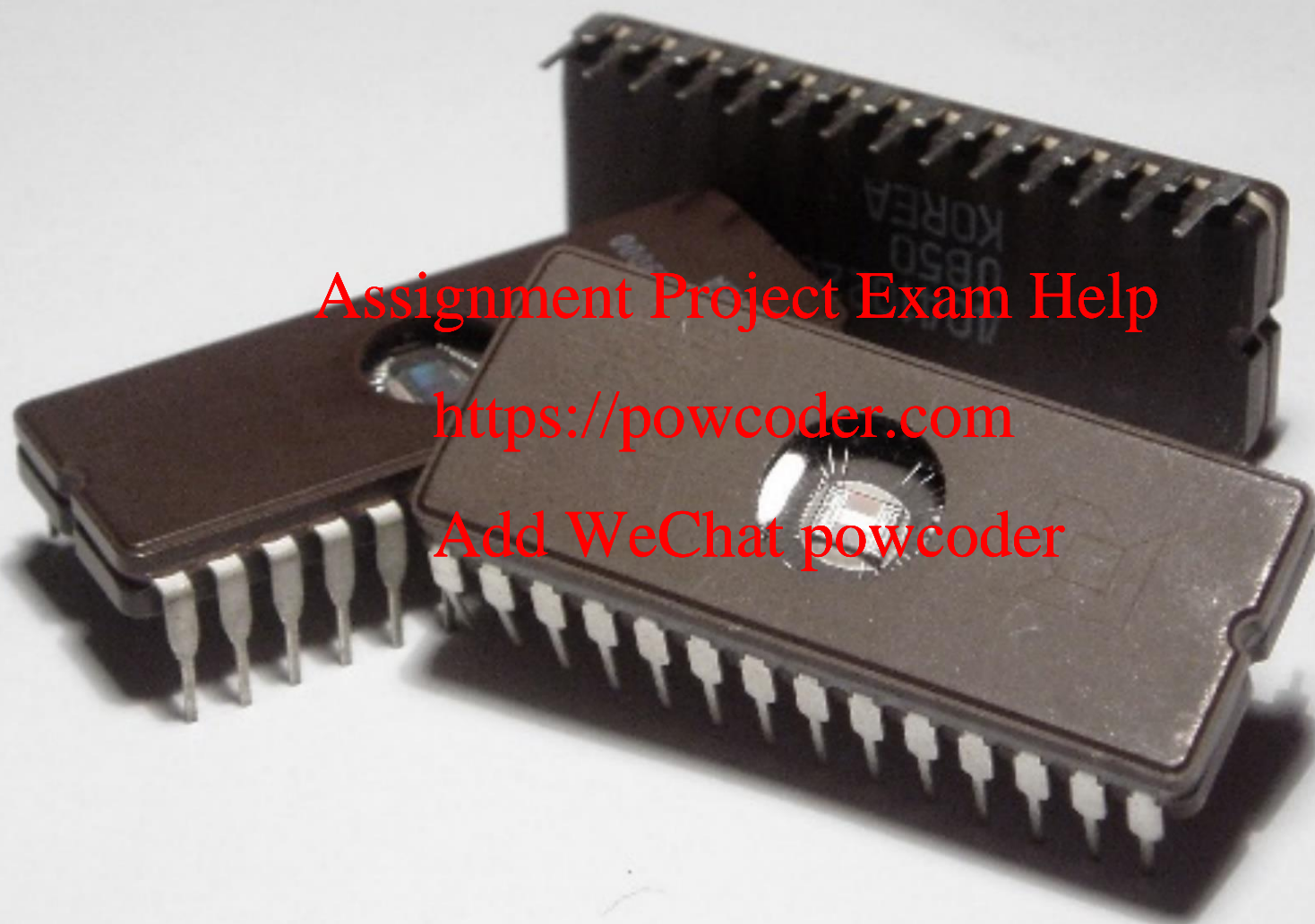**Bernhard Kainz** (with thanks to **A. Gopalan, N. Dulay** and **E. Edwards**)

b.kainz@imperial.ac.uk

Integrated Circuits

- All ICs (chips) are made up of logic gates

- ICs are square pieces of silicon onto which logic gates have been deposited

- Generally rows of pins are able to be mounted onto a larger circuit

wikipedia

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IC – Sizes

Name	Abbreviation	Number of Gates
Small Scale Integrated	SSI	1-10
Medium Scale Integrated	MSI	10-100
Large Scale Integrated	LSI	100-100,000
Very Large Scale Integrated	VLSI	>100,000

Example SSI Chips
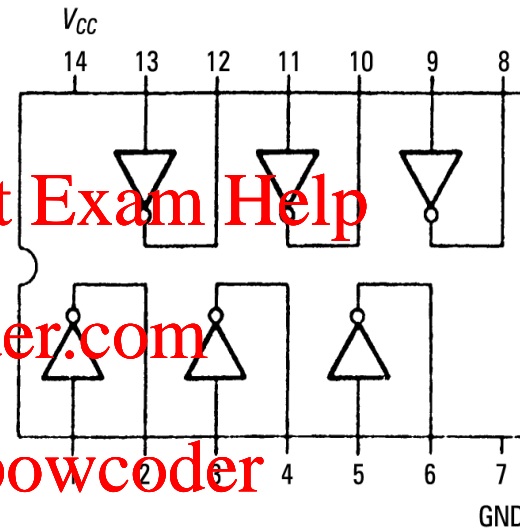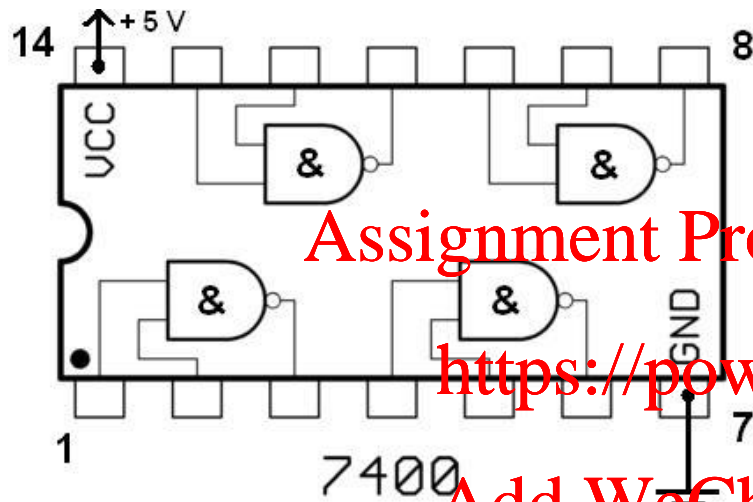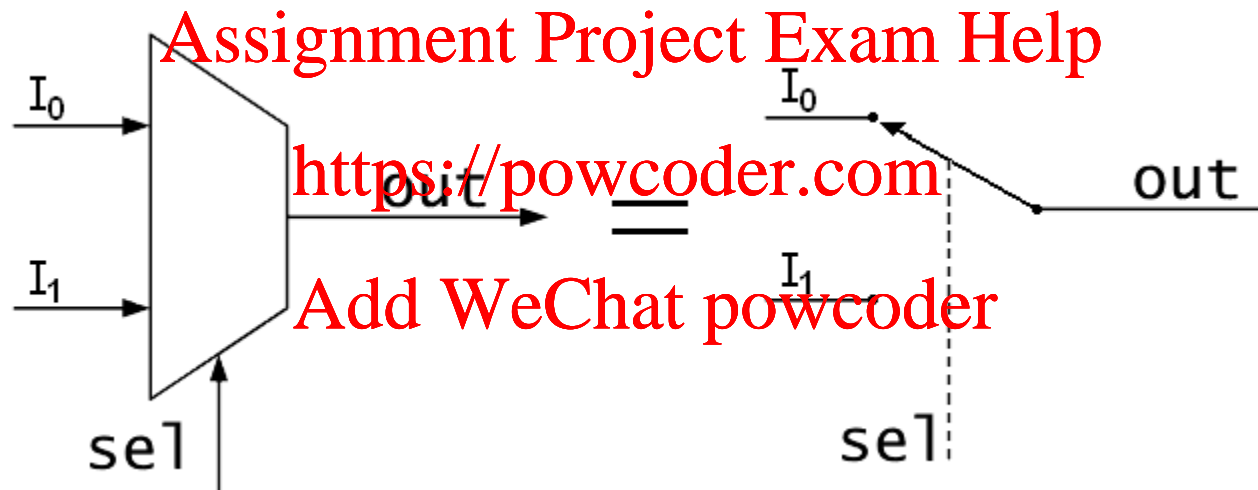
7404 – hex inverter

7400 - Nand Gates

The 7400 TTL series

Example Circuit with SSI/MSI Chips

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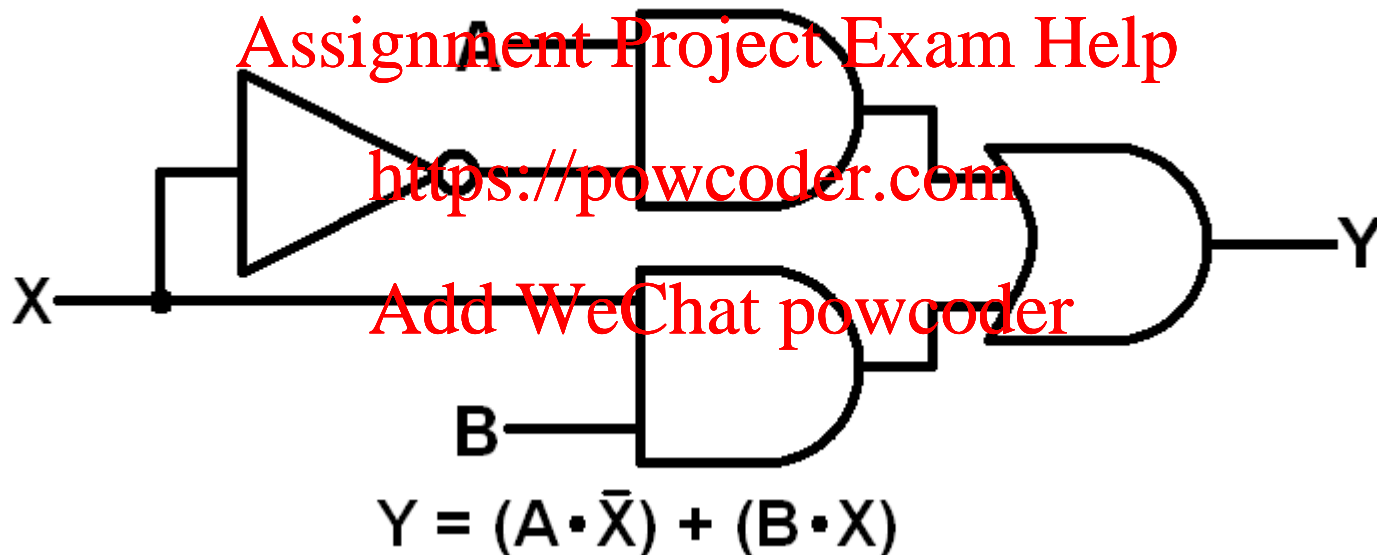
MSI Chips – Multiplexer

- A multiple-input, single-output switch
- Also called MUX for short ☺

- **sel** selects which of I_0 or I_1 is mapped to the output
- For example, **sel** = 0 selects I_0 and **sel** = 1 selects I_1
- Example is called a 2-to-1 MUX
- With n *selects*/control lines, we can have 2^n input lines
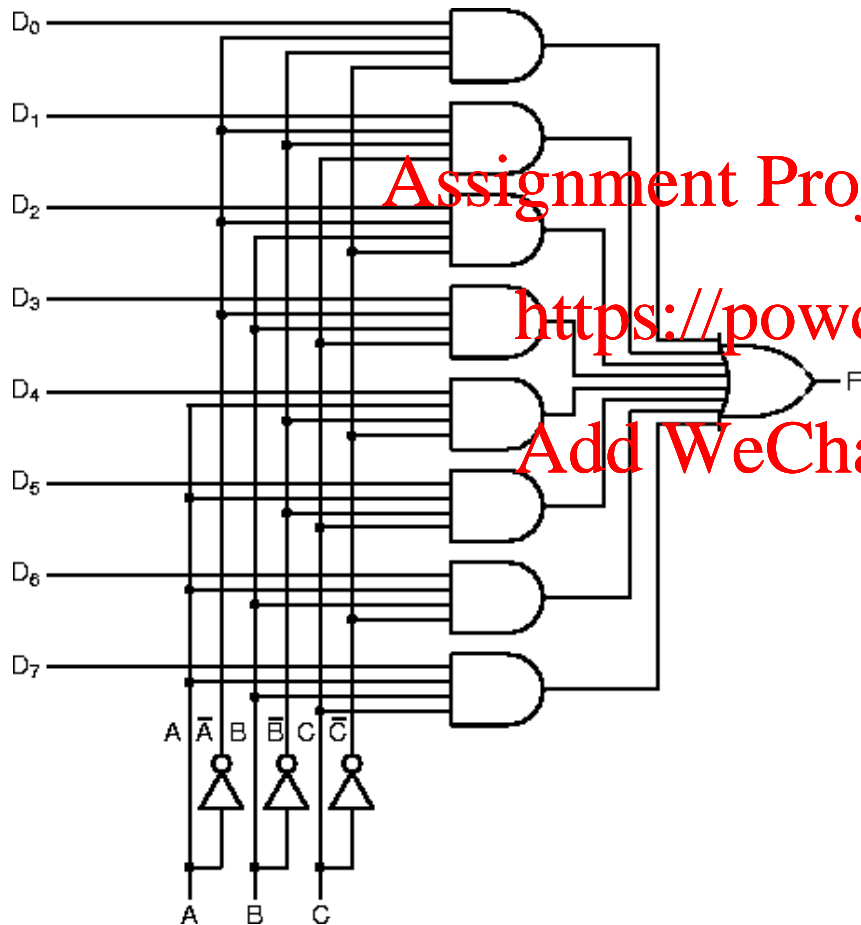
MSI Chips – Multiplexer

- 2-to-1 Multiplexer

$$Y = (A \cdot \bar{X}) + (B \cdot X)$$

Source: http://www.sparkfun.com/tutorials/371

MSI Chips – Multiplexer

- Truth Table

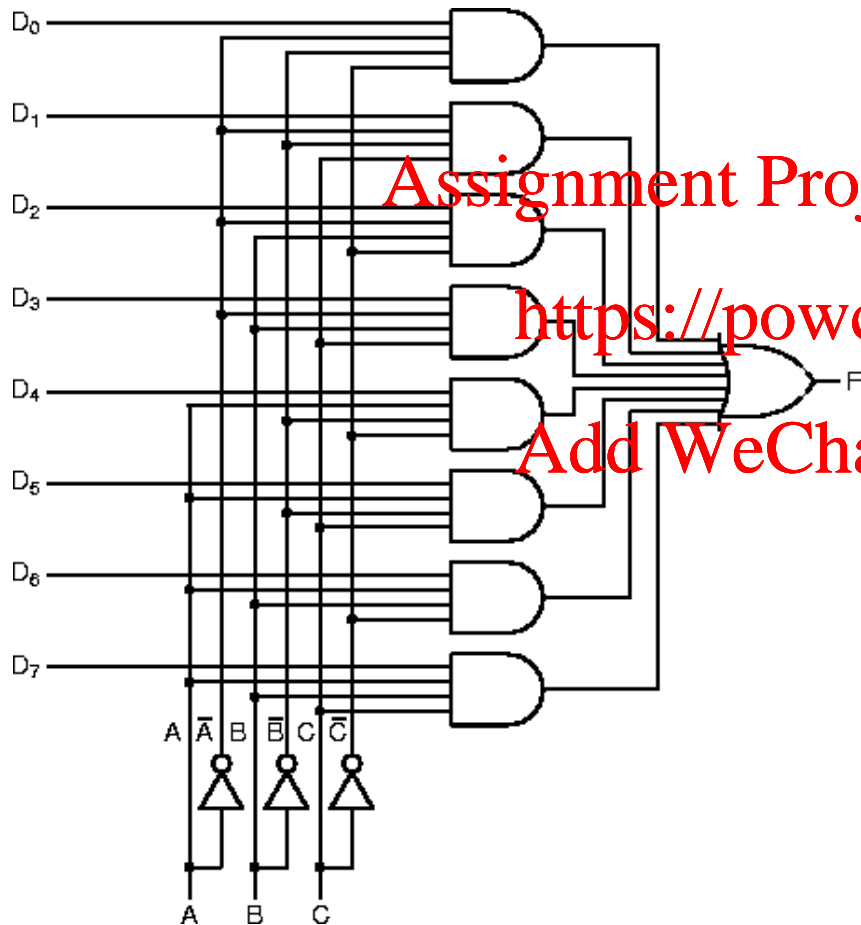| A	B	X	C	E	Y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	1	0	1
1	1	1	0	1	1

MSI Chips – Multiplexer

- The 3 inputs **A**, **B**, **C** select which of the input lines (D_0-D_7) is copied through to the output **F**

- In general, a multiplexer has 2^n inputs and n control lines and one output

MSI Chips – Multiplexer
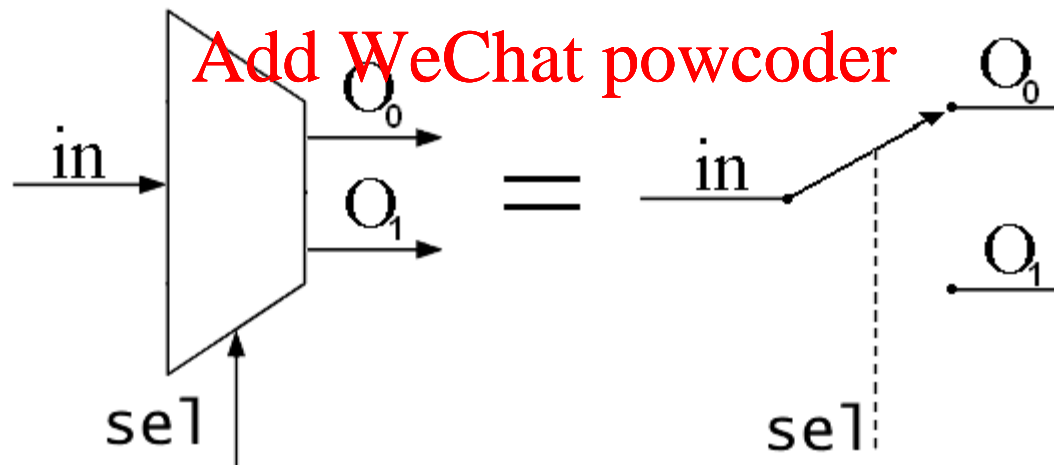

- Fits nicely into a 14-pin package (with ground and +5V)

MSI Chips – Demultiplexer

- A single-input, multiple-output switch
  - Opposite of a MUX
- Also called DEMUX ☺
- Usually used in conjunction with a MUX

MSI Chips – Decoder
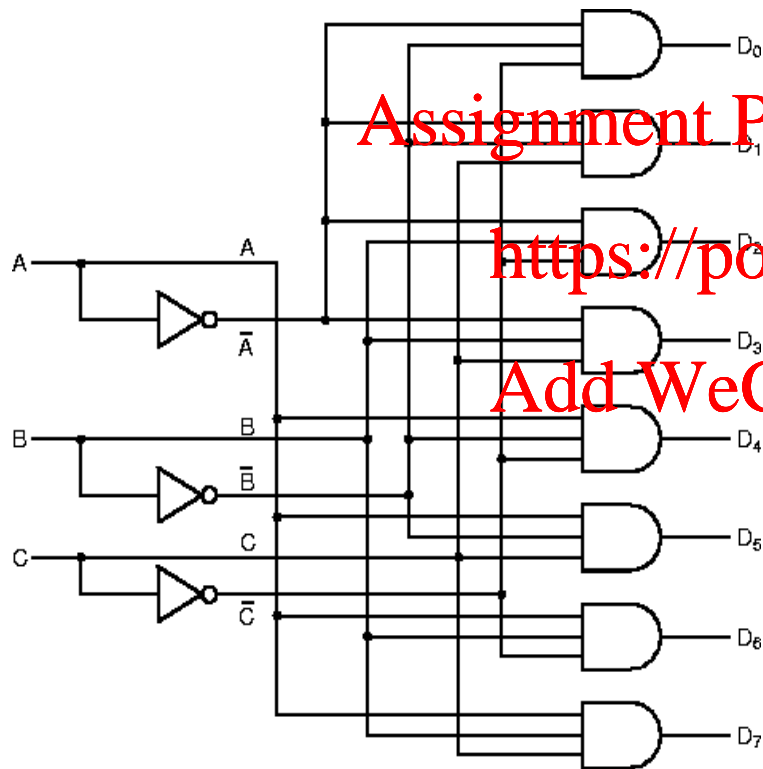
- A multiple-input, multiple-output logic circuit

  - Converts coded inputs into coded outputs

  - Binary Decoder has n inputs and 2^n outputs

  - Necessary in applications such as data multiplexing and memory address decoding

MSI Chips – Decoder

- Only one output is 1 – the one selected by the n-bit binary input number – the rest are zero

- Useful in transmitting line selection with fewer wires (e.g. selecting a memory chip)

MSI Chips – Decoder

- Truth Table

A	B	C	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

MSI Chips – Calculations – Comparator

- To compare two numbers

- Example: 1-bit comparison

  - Which gate ~~Assig~~? ~~ment Project Exam Help~~
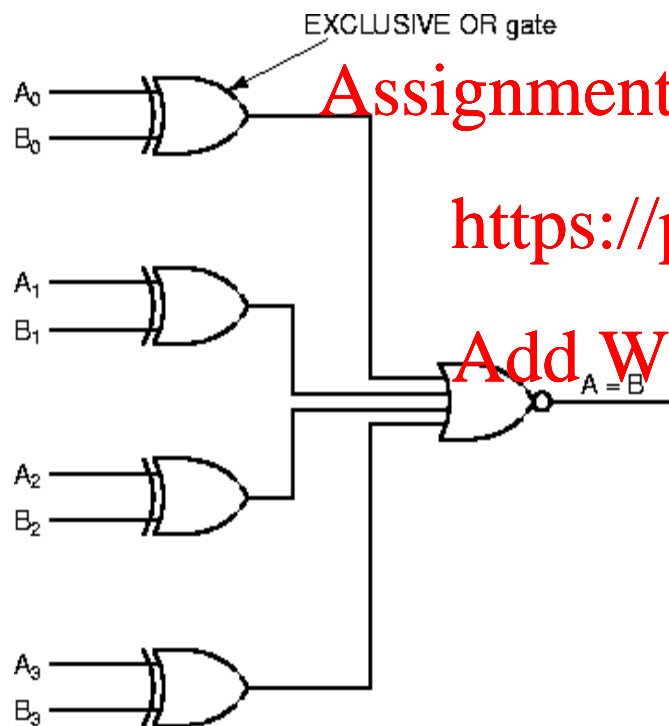
  - Recall: ~~https://powcoder.com~~

~~Add WeChat powcoder~~

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

MSI Chips – Calculations – Comparator

EXCLUSIVE OR gate

A_0
B_0

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A_1
B_1

https://powcoder.com

- The comparator returns 1
  if the two len-bit inputs A and
  B are equal, 0 otherwise

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$A = B$

A_2
B_2

A_3
B_3

MSI Chips – Calculations – Bit-shifter

- Faster calculations for powers of 2
- Shift left and right (multiply and divide)
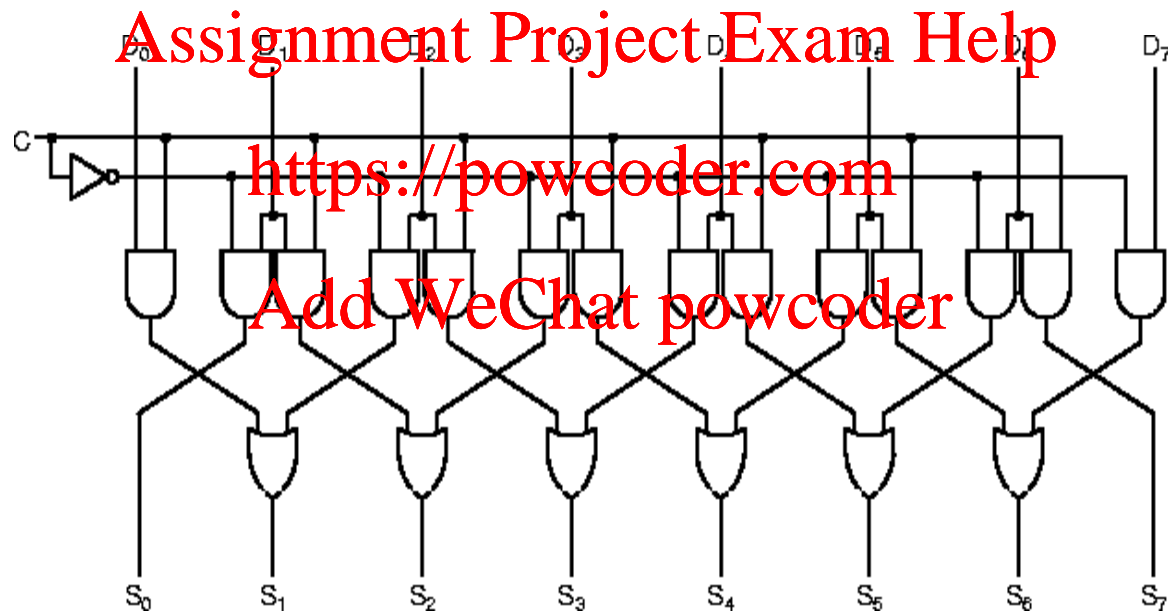
- c = 0 → shift left
- c = 1 → shift right

The Arithmetic Logic Unit (ALU)

- Digital circuit that performs arithmetic and logical operations

- Fundamental building block of the central processing unit (CPU) of a computer
  - Even the simplest microprocessors contain one for purposes such as maintaining timers
  - Processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs

- Concept proposed in 1945 by Mathematician John von Neumann

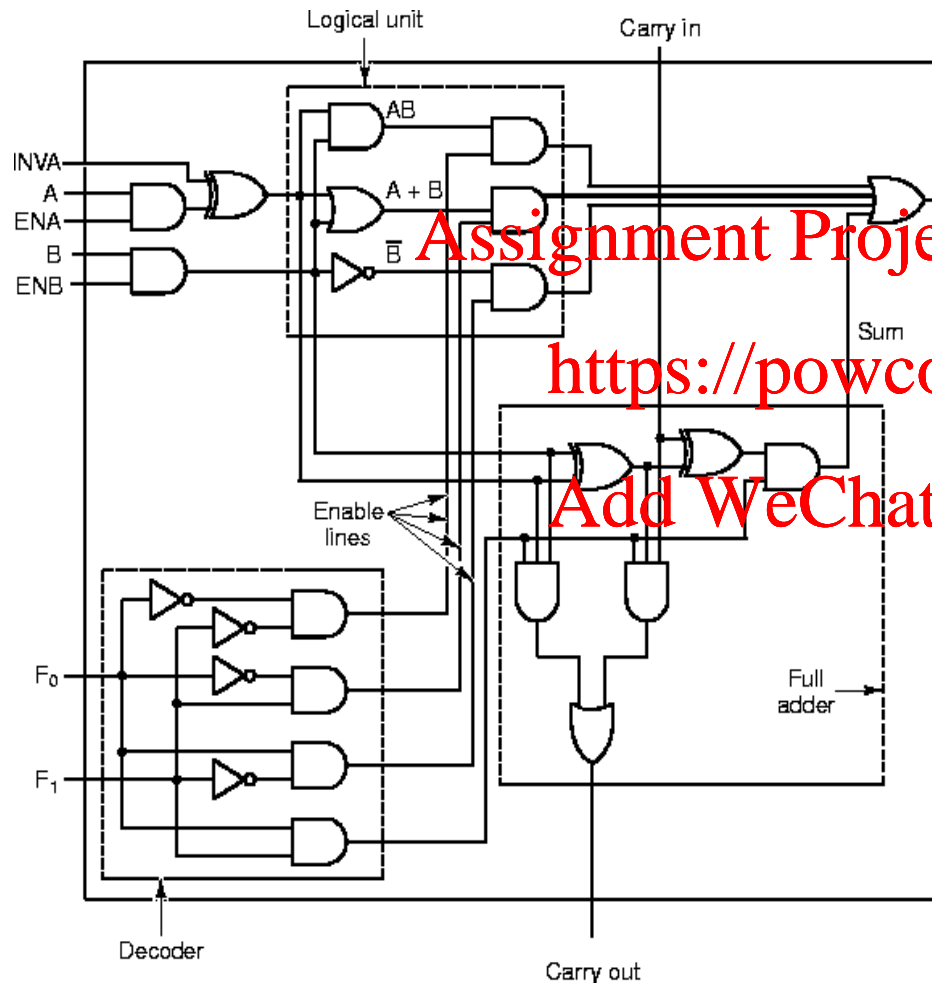- Research into ALUs remains an important part of computer science

ALU

• Recall: Full Adder

A	B	Carry In	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
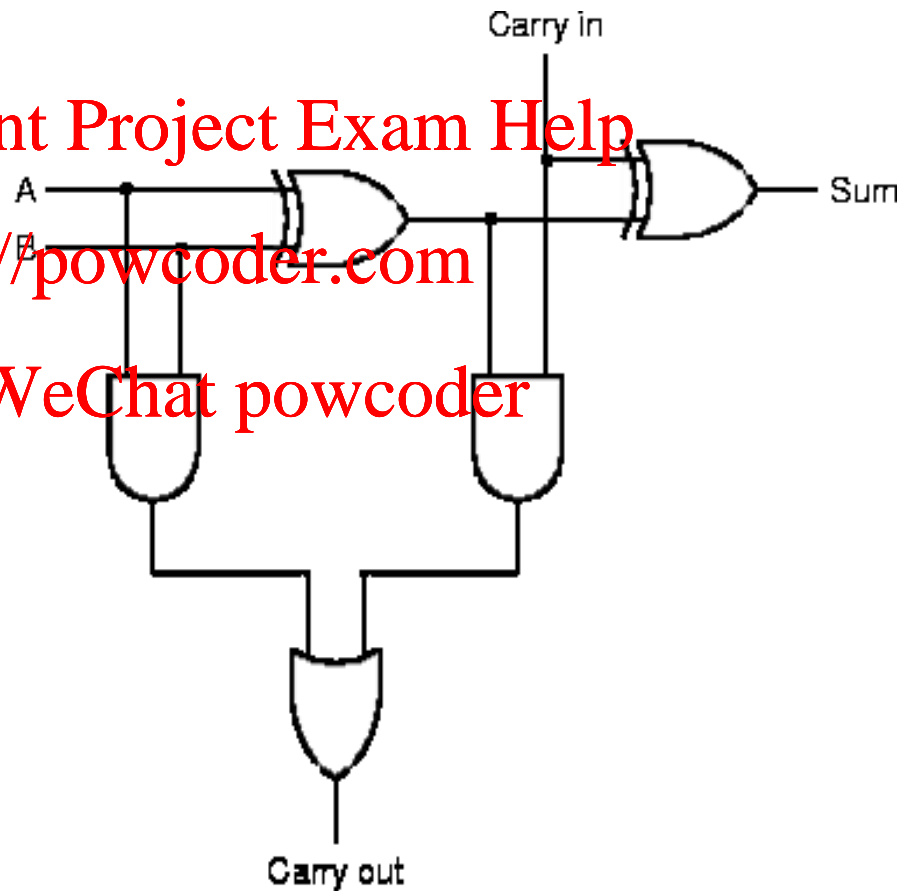
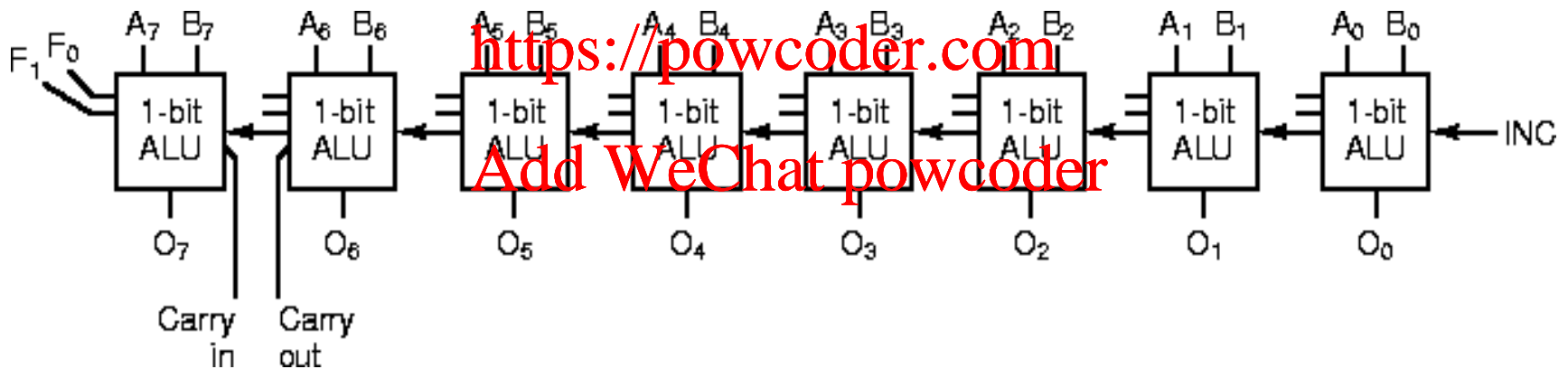# The Arithmetic Logic Unit (ALU)

- The ALU is able to perform multiple functions

  - Depending on the input to the decoder (F_0,F_1) one of four functions is selected – A and B, A or B, not B, arithmetic A+B
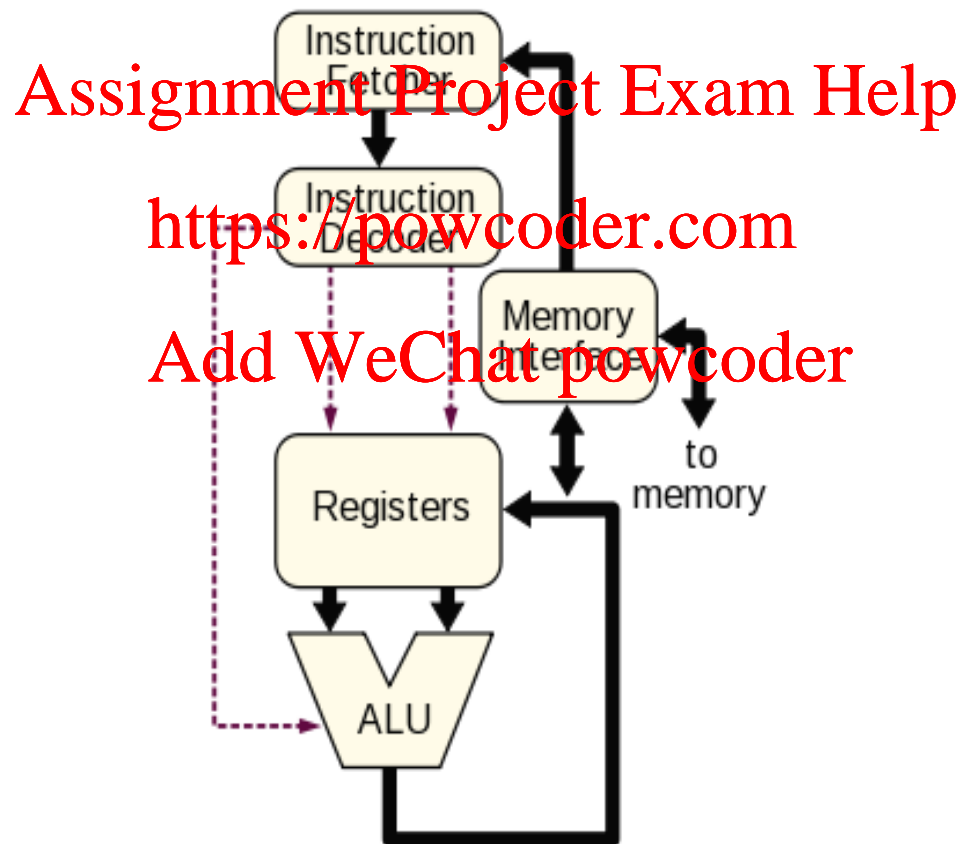
8-bit ALU

- Can link together 1-bit ALUs to form a multi-bit ALU
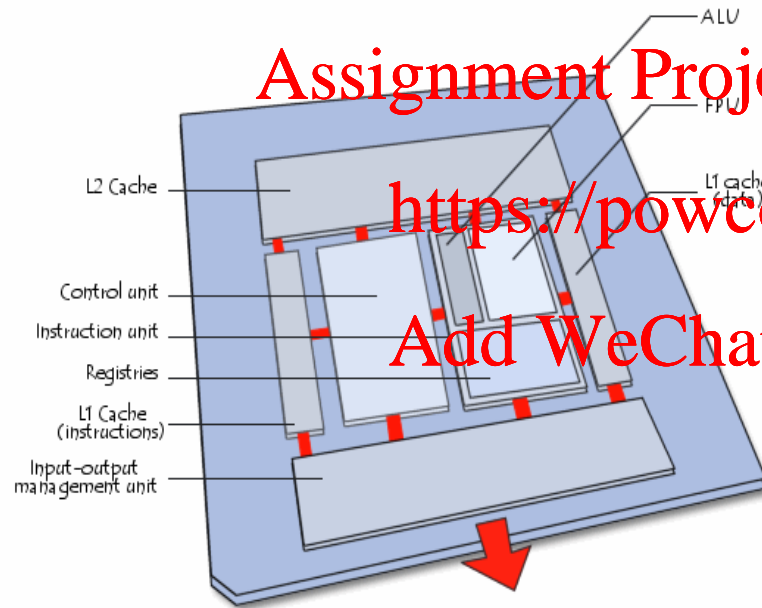 - Sometimes known as bit-slice circuits

CPU Design – VLSI

- Contains millions of gates – same structure as below

CPU Design – VLSI

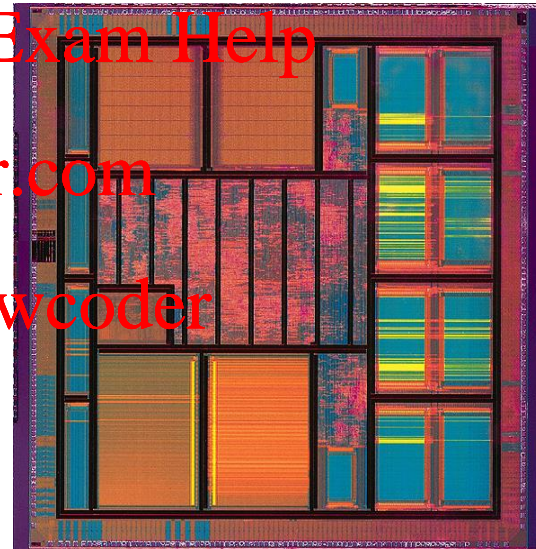
L2 Cache

Control unit

Instruction unit

Registries

L1 Cache
(instructions)

Input-output
management unit

ALU

FPU

L1 cache
(data)

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Production

- Good video:
https://www.youtube.com/watch?v=vK-geBYygXo

- Bad video: Assignment Project Exam Help
https://www.youtube.com/watch?v=YIkMaQJSyP8
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