MOTOROLA MICROPROCESSOR & MEMORY TECHNOLOGY GROUP M68000 Hi-Performance Microprocessor Division M68060 Software Package Production Release P1.00 -- October 10, 1994

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# 68060 FLOATING-POINT ACCEPTATE POWICO DET

The file fplsp.sa contains the "Library version" of the 68060SP Floating-Point Software Package. The routines included in this module can be used to emulate the FP instructions not implemented in 68060 hardware. These instructions normally take exception vector #11 "FP Unimplemented Instruction".

By re-compiling a program that uses these instructions, and making subroutine calls in place of the unimplemented instructions, a program can avoid the overhead associated with taking the exception.

### Release file format:

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The file fplsp.sa is essentially a hexadecimal image of the release package. This is the ONLY format which will be supported. The hex image was created by assembling the source code and then converting the resulting binary output image into an ASCII text file. The hexadecimal numbers are listed using the Motorola Assembly Syntax assembler directive "dc.l" (define constant longword). The file can be converted to other assembly syntaxes by using any word processor with a global search and replace function.

To assist in assembling and linking this module with other modules,

the installer should add a symbolic label to the top of the file. This will allow calling routines to access the entry points of this package.

The source code fplsp.s has also been included but only for documentation purposes.

### Release file structure:

The file fplsp.sa contains an "Entry-Point" section and a code section. The FPLSP has no "Call-Out" section. The first section is the "Entry-Point" section. In order to access a function in the package, a program must "bsr" or "jsr" to the location listed below in "68060FPLSP entry points" that corresponds to the desired function. A branch instruction located at the selected entry point within the package will then enter the correct emulation code routine.

The entry point addresses at the beginning of the package will remain fixed so that a program calling the routines will not have to be re-compiled with every new 68060FPLSP release.

There are 3 entry-points for each instruction type: single precision, double precision, and extended precision.

As an example, the "fsin" library instruction can be passed an extended precision operand if program executes:

## # fsin.x fp Assignment Project Exam Help

# pass operand on stack fmovm.x &0x01, -(%sp) bsr.l \_060FPLSP\_TOP+0x1a8, # branch to fsin routine add.l &0xc, %shttps://poww.cogtex.com

Upon return, fp0 holds the correct result. The FPSR is

set correctly. The FPCR is unchanged. The FPIAR is undefined.

Another example. This did, Wyell peratipowcoder

# frem.s %fp1,%fp0

fmov.s %fp1, -(%sp) # pass src operand fmov.s %fp0,-(%sp) # pass dst operand bsr.l \_060FPLSP\_TOP+0x168 # branch to frem routine &0x8,%sp # clear operands from stack

Again, the result is returned in fp0. Note that BOTH operands are passed in single precision format.

### Exception reporting:

The package takes exceptions according to the FPCR value upon subroutine entry. If an exception should be reported, then the package forces this exception using implemented floating-point instructions. For example, if the instruction being emulated should cause a floating-point Operand Error exception, then the library routine executes an FMUL of a zero and an infinity to force the OPERR exception. Although the FPIAR will be undefined for the enabled Operand Error exception handler, the user will at least be able to record that the event occurred.

#### Miscellaneous:

The package does not attempt to correctly emulate instructions with Signalling NAN inputs. Use of SNANs should be avoided with this package.

68060FPLSP entry points:

The fabs/fadd/fdiv/fint/fintrz/fmul/fneg/fsqrt/fsub entry points are provided for the convenience of older compilers that make subroutine calls for all fp instructions. The code does NOT emulate the instruction but rather simply executes it.

```
_060FPLSP_T0P:
            _060LSP__facoss_
0x000:
0x008:
            _060LSP__facosd_
            _060LSP__facosx_
0x010:
0x018:
            _060LSP__fasins_
0x020:
             _060LSP___fasind_
0x028:
             _060LSP___fasinx_
0x030:
             _060LSP___fatans_
0x038:
             _060LSP___fatand_
0x040:
             _060LSP___fatanx__
0x048:
             _060LSP___fatanhs__
0x050:
             _060LSP___fatanhd_
             _060LSP___fatanhx__
0x058:
0x060:
             060LSP
                    _fcoss_
0x068:
             060LSP
                    _fcosd_
0x070:
             060LSP
                    _fcosx_
0x078:
             060LSP
                    fcoshs
            Project Exam Help
0x080:
0x088:
             060LSP fetoxs
0x090:
             060LSP
                    fetoxd
0x098:
             060LSP
                     fetoxx
0x0a0:
             060LSP_fetbxm1d_/powcoder.com
0x0a8:
0x0b0:
            _060LSP
                     _fetoxm1x_
0x0b8:
            _060LSP
                     _fgetexps
0x0c0:
            _060LSP_fgetexpx
                               VeChat powcoder
0x0c8:
0x0d0:
            _060LSP_
0x0d8:
                     _fgetmans_
            _060LSP_
0x0e0:
                     _fgetmand_
            _060LSP_
0x0e8:
                     _fgetmanx_
            _060LSP_
0x0f0:
                     _flog10s_
            _060LSP_
0x0f8:
                     _flog10d_
            _060LSP_
0x100:
                     _flog10x_
            _060LSP_
0x108:
                     _flog2s_
             _060LSP_
0x110:
                     flog2d_
            _060LSP_
0x118:
                     _flog2x_
            _060LSP_
0x120:
                     _flogns_
            _060LSP_
0x128:
                     _flognd_
            _060LSP_
0x130:
                     _flognx_
            _060LSP_
0x138:
                     _flognp1s_
0x140:
            _060LSP_
                     flognp1d_
0x148:
            _060LSP_
                     flognp1x_
0x150:
            _060LSP_
                     _fmods_
0x158:
            _060LSP__
                     _fmodd_
0x160:
                     _fmodx_
            _060LSP__
0x168:
            _060LSP__frems_
0x170:
            _060LSP__fremd_
            _060LSP__fremx_
0x178:
             _060LSP___fscales_
0x180:
             _060LSP__fscaled_
0x188:
0x190:
            _060LSP__fscalex_
0x198:
            _060LSP__fsins_
0x1a0:
            _060LSP__fsind_
0x1a8:
            _060LSP__fsinx_
```

```
_060LSP__fsincoss_
0x1b0:
            _060LSP
0x1b8:
                      fsincosd_
0x1c0:
             _060LSP_
                      fsincosx_
            _060LSP_
0x1c8:
                      fsinhs_
            _060LSP_
                      fsinhd_
0x1d0:
            _060LSP_
0x1d8:
                      fsinhx_
            _060LSP_
                      _ftans_
0x1e0:
                      ftand_
0x1e8:
             060LSP
                      ftanx_
0x1f0:
             060LSP
0x1f8:
             _060LSP_
                      _ftanhs_
0x200:
             _060LSP___ftanhd_
0x208:
            _060LSP__ftanhx_
            _060LSP__ftentoxs_
0x210:
            _060LSP__ftentoxd_
0x218:
0x220:
             _060LSP___ftentoxx_
0x228:
             _060LSP___ftwotoxs_
0x230:
             _060LSP___ftwotoxd_
0x238:
             _060LSP___ftwotoxx_
0x240:
            _060LSP__fabss_
0x248:
            _060LSP_
                     __fabsd_
0x250:
             060LSP
                      _fabsx_
0x258:
             060LSP
                      _fadds_
0x260:
             060LSP
                      _faddd_
                      faddx_
0x268:
             060LSP
0x270:
             060LSP
                      _fdivs_
0x278:
             060LSP
                      fdivd
                      fiment Project Exam Help
            100005P
0x280:
             060LSP fints
0x288:
             060LSP
                     _{	t fintd}
0x290:
             060LSP
                      fintx_
0x298:
             060LSP_finerzd_//powcoder.com
0x2a0:
0x2a8:
0x2b0:
             _060LSP_
                      _fintrzx_
0x2b8:
            _060LSP
                      _fmuls
            _060LSP__fmld_
_060LSP__fmld_
                              WeChat powcoder
0x2c0:
0x2c8:
0x2d0:
            _060LSP_
                      _fnegs_
            _060LSP_
0x2d8:
                      _fnegd_
            _060LSP_
0x2e0:
                      _fnegx_
            _060LSP_
0x2e8:
                     _fsqrts_
            _060LSP__fsqrtd_
0x2f0:
            _060LSP__fsqrtx_
0x2f8:
             _060LSP__fsubs_
_060LSP__fsubd_
0x300:
0x308:
            __060LSP__fsubx_
0x310:
```