Summary of RISC-V workshop

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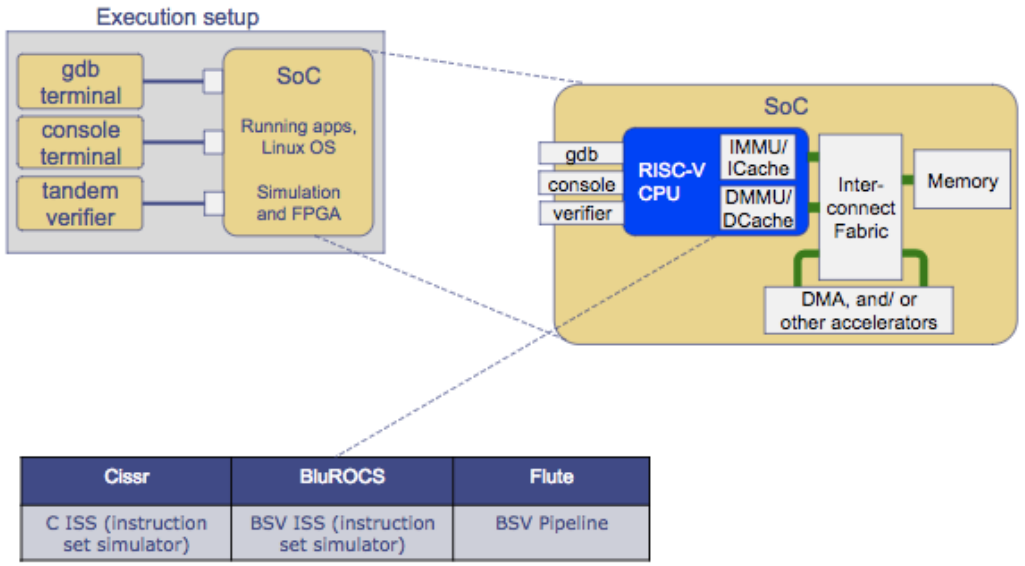
04.07.2017

1st workshop (Jan 2015 at CA)

- Focus on fundamentals:
  - Processors from Berkeley, Bluspec, India
  - Lowrisc SoC
  - Software toolchain
  - Debugging on RISC-V(Spike)
  - EDA:Chisel

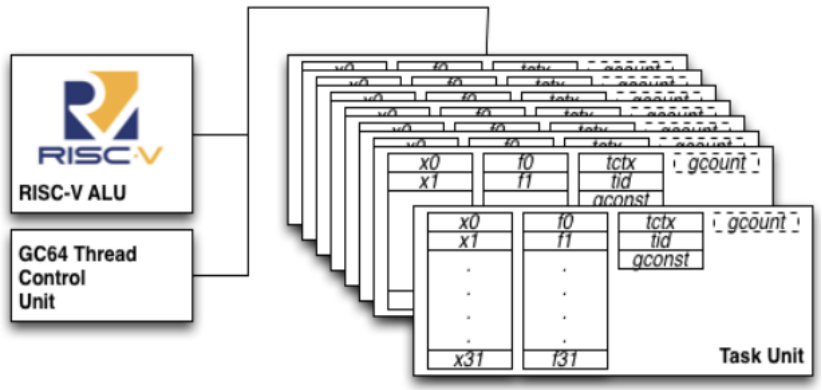


2nd workshop (June 2015 at CA)

- More processor
  - BOOM (OoO)
  - Z-scale (3 stage MCU)
  - Superscalar CPU generator (FabScalar from NCSU, 2011)
  - Pulpino
- Parallel cpu
  - CAVA : 96 threads, 384KB (No update and result now)
- Data intensive computing
  - GC64: (Texas Tech)
  - Keep going now

GC64

- Data intensive algorithms & applications
  - Sparse data structure
  - Sparse Matrix

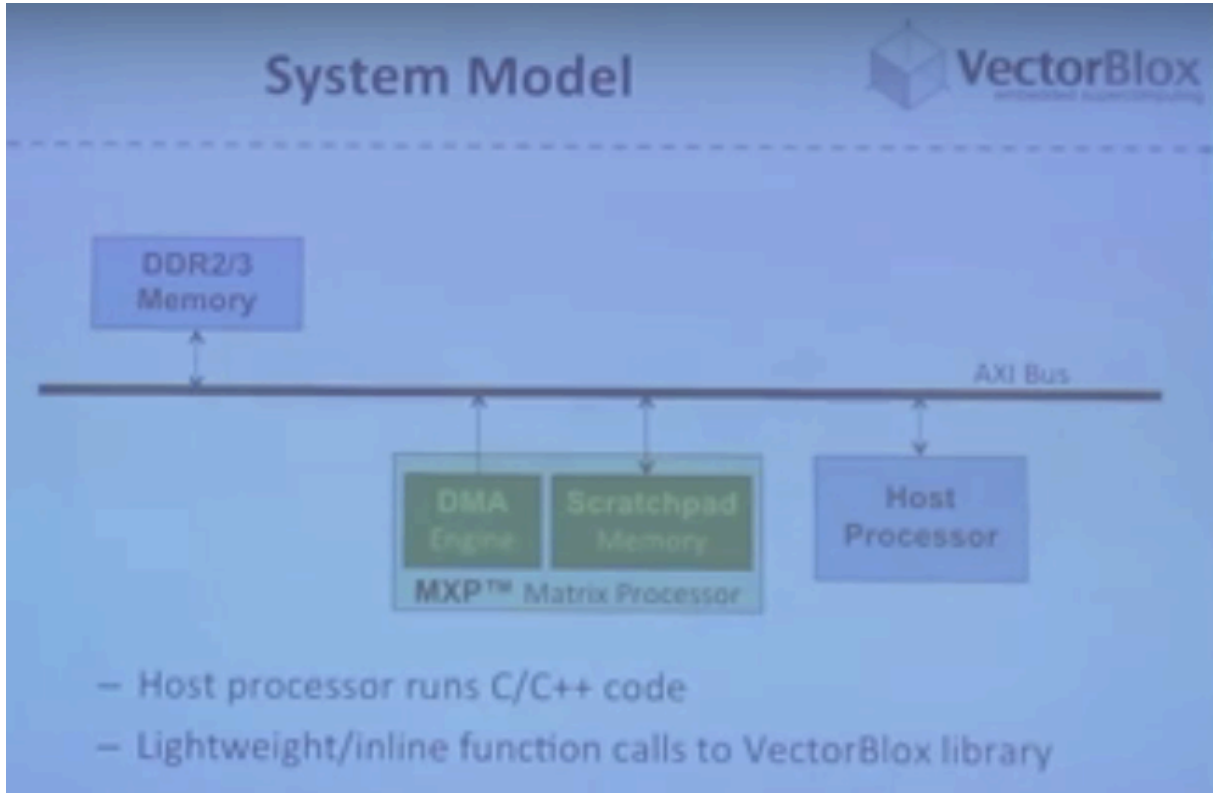


Architectural Goals

- Simple architectural components
  - Scaling the degree concurrency within an SoC is a manufacturing problem, not a design problem
- Simple ISA extensions conducive to compiler optimizations for concurrent applications
  - NOT writing the world's latest parallel compiler
- Provide low-level hardware support for mutable concurrency
  - A task lives in HARDWARE
- Provide hardware mechanisms to minimize hardware context switch latency
- Provide well-defined mechanisms on *when* and *how* context switch events occur
  - Provide a well-defined mechanism for USER SPACE code to induce a context switch

2nd workshop (June 2015 at berkeley)

- Formal verification (SRI lab, CA)
- Clockless CPU- Aristotle (RMIT, Australia)
- Vector Processor from Berkeley
- Lowrisc SoC with tagged memory
- Matrix processor from VectorBlox



2nd workshop (June 2015 at CA)

- C,V, Privileged proposal
- Collaboration
  - RapidIO

3rd Workshop (oracle CA, January 5th, 2016)

- Integration
  - SoC for a Satellite Navigation Unit based on the RISC-V single-core Rocket chip
  - Open Source Camera using RISC-V in FPGA
- Parallelism
  - Emulating future HPC SoC Architectures Using RISC-V
  - GRVI-Phalanx: A Massively Parallel RISC-V FPGA Accelerator Accelerator
- Security
  - A Metadata--Extended RISC-V by Draper Lab

3rd Workshop (oracle CA, January 5th, 2016)

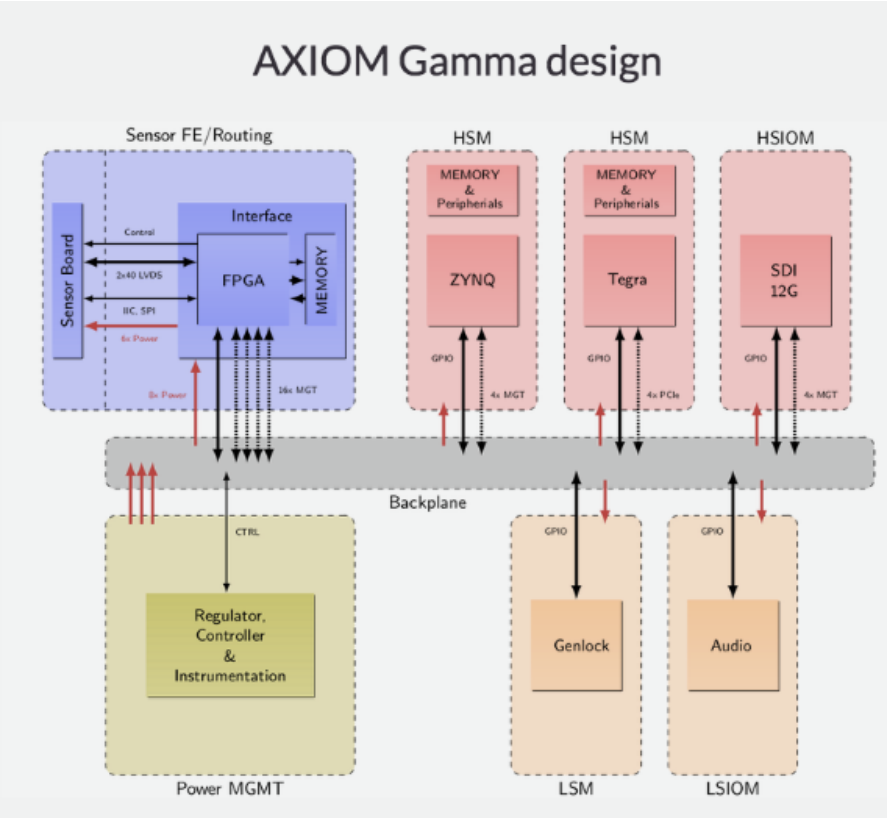
- Circuit and Process
  - RISC-V Photonic Processor
  - RISC-V microcontroller with SAR ADC
- Simulator
  - Pydgin: An Extensible Instruction-Set Simulator for RISC-V
- Formal, memory model
  - MIT Arvind
- More CPU & Soc update:
  - Bluespec Factory
  - ROALogic
  - ORCA
  - Krestel
  - PicoRV showed up? (ORCA use it to analyze)

3rd Workshop (January 5th, 2016)

- Fundamental
  - Coreboot, UEFI, FreeBSD on RISC-V
  - External Debug support
  - RISC-V torture
- More:
  - https://www.youtube.com/watch?v=6gelvReEQQU&feature=youtu.be
  - https://riscv.org/2016/01/3rd-risc-v-workshop/

3rd Workshop (January 5th, 2016)

- Open Source Camera using RISC-V in FPGA



4th workshop (MIT, July 25, 2016)

- Fundamental
  - RISC-V Interrupts
  - ISA comparison
  - Trace Debugging
  - FPGArduino
- More open source CPU
  - Riscy from MIT
- More formal
  - Kami for HW verification
  - Arvind for uniprocessor consistency

4th workshop (MIT, July 25, 2016)

- ISA extensions
  - DSP from ETH
  - Lightweight Vector extension from ORCA
  - RISC-V as basis for ASIP Design – an IoT Security Example
- Accelerator:
  - RISC-V + Neural network (XFILES & 中科院）
  - RISC-V + FFT for Radio from Berkeley

X-FILES/DANA: RISC-V Hardware/Software for Neural Networks

Schuyler Eldridge, Han Dong, Thomas Unger, Marcia Sahaya Louis, Leila Delshad Tehrani, Jonathan Appavoo, and Ajay Joshi

Hardware and Software

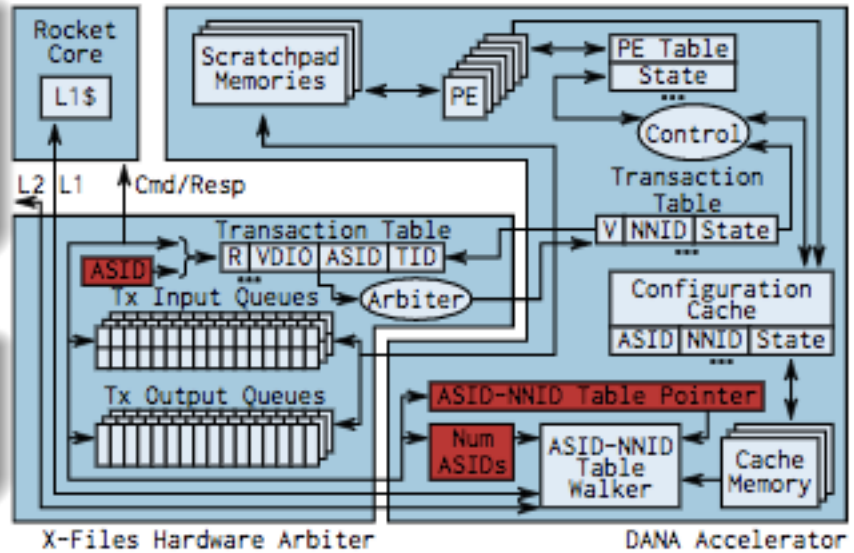
- **X-FILES:** Hardware/software for neural network management
- **DANA:** An X-FILES backend for neural network acceleration

Operating System Support

- RISC-V Proxy Kernel systemcalls
- RISC-V Linux Port (ongoing)

Open Source Availability

- Chisel hardware, C libraries [2]



[1] Eldridge, S., Waterland, A., Seltzer, M., Appavoo, J., and Joshi, A. (2015). Towards general-purpose neural network computing. In *Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (PACT)*.

[2] Boston University Integrated Circuits and Systems Group (2016). X-files/dana github repository. Online: `https://github.com/bu-icsg/xfiles-dana`.

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4th workshop (MIT, July 25, 2016)

- HLS
  - SW Programmable FPGA IoT Platform: RISC-V Processor with Auto-Generated HW Accelerators
- Multicore SoC
  - Heterogeneous Multicore RISC-V Processors in FD-SOI Silicon
- EDA tool:
  - Improving The Performance Per Area Factor of RISC-V Based Multi-Core Systems
  - Power model
- Company's adoption
  - Nvidia

4th workshop (MIT, July 25, 2016)

- SW
  - Apache Mynewt
  - Debian
- Others:
  - NVM talks from WD- > hardware coherence is needed.
  - Interconnect
    - RISC-V I/O Scale Out Architecture for Distributed Data Analytics

5th workshop at Google, CA,Nov,2016

- Fundamental
  - Memory model from MIT and Princeton
  - Vector extension
- EDA tool
  - Extending RISC-V for Application-Specific Requirements (Instruction design)
- SoC tool
  - Joined up debugging and analysis in the RISC-V world
  - OpenSoC System Architect: An Open Toolkit for Building High Performance SoCs

5th workshop at Google, CA,Nov,2016

- Multicore
  - UCSD Taylor
  - Thousand core from MIT
- Security
  - 128-bit addressing in RISC-V and security from Micron
  - The Challenges of Securing and Authenticating Embedded Devices and a Suggested Approach for RISC-V (SecureRF on SiFive)
- Hardware for software Isolation
  - Sanctum: Minimal Hardware Extensions for Strong Software Isolation
- HW-SW codesign
  - LLVM from Alex, Cambridge

5th workshop at Google, CA,Nov,2016

- SW:
  - Go
  - JVM
  - Low power GUI
- Simulator
  - Fast instruction simulator from Esperanto (Dave Ditzel)
- VM:
  - VM model
- More core:
  - Syntacore from Russia

5th workshop at Google, CA,Nov,2016

- Peripheral
  - RISC-V Community needs Peripheral Cores
- Low power:
  - Sub-microsecond Adaptive Voltage Scaling in a 28nm RISC-V SoC
  - Reprogrammable Redundancy for Cache Vmin Reduction in a 28nm RISC-V Processor
- Fault tolerant:
  - Software-Defined ECC
- Open board
  - YoPuzzle

Reflection

- ISA extension design tool
- ISA extension of ML
  - LSTM, MLP
  - Matrix

Appendix

Poster on 1st Workshop

- Datacenter Extension (with no detail)
- Sodor and BOOM
- RISC-V poky & Gentoo
- Fast functional simulation for SW development for many-processor NoC-connected systems
- FlexPRET: A Predictable Processor
- Practical RISC-V Random Test Generation using Constraint programming
- Hardware Acceleration of Key-Value Stores
- Eve: An Event-Driven Architecture For Asynchronous Programming Models
- More: https://docs.google.com/presentation/d/1I1XzlG6VmgsHgBVmEnbS-oQJgVaEVmroxgWsklP8UYw/edit#slide=id.g606c475db_00

Poster on 2nd Workshop

- Krestel
- Image processing application on RISC-V
- FIRRTL
- More:
- https://www.youtube.com/watch?v=KlegdDacIQE&feature=youtu.be