High Speed VCO for PLL system in 0.13μm CMOS technology

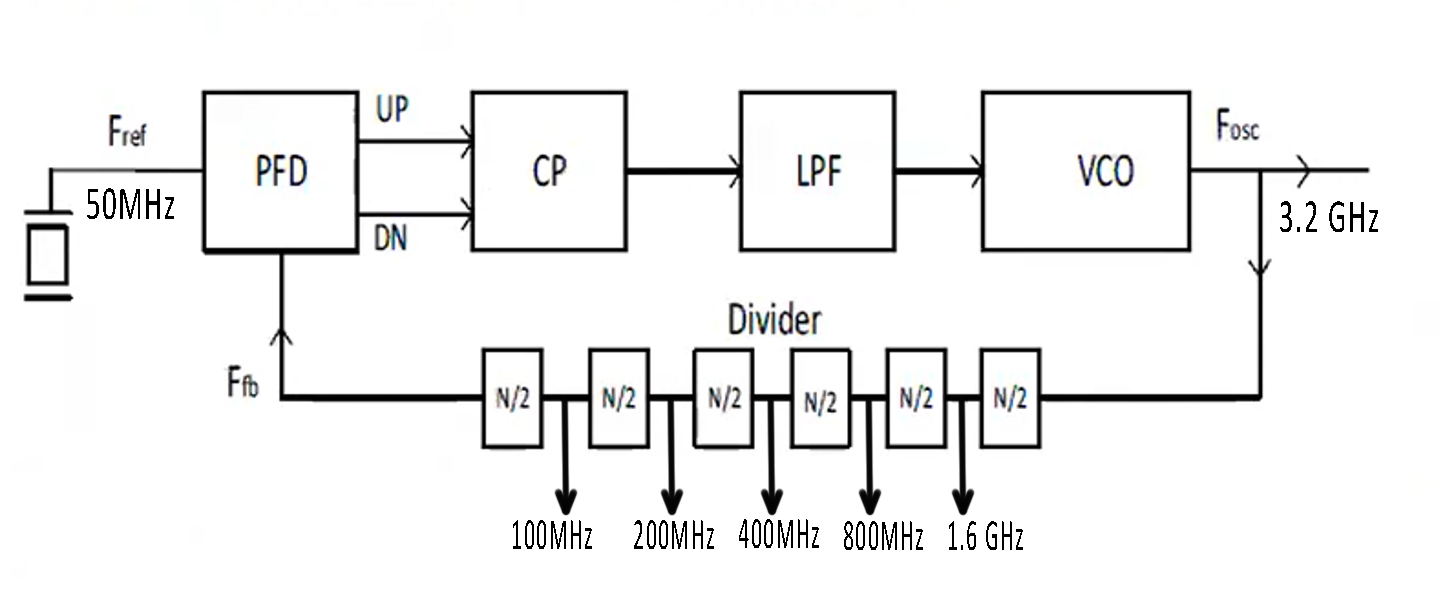
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*Abstract*—The scope of the work is to design a high speed VCO that can run in the GHz range (1.6 – 3.2GHz) with relatively low power consumption and low area. A Phase Locked Loop (PLL) using this VCO in combination with appropriate frequency divider ratios can generate a range of output frequencies up to 3.2GHz. The design is to be implemented in 130nm CMOS technology. (*Abstract*)

Keywords—VCO, PLL, high speed, CMOS (key words)

# Introduction (*Heading 1*)

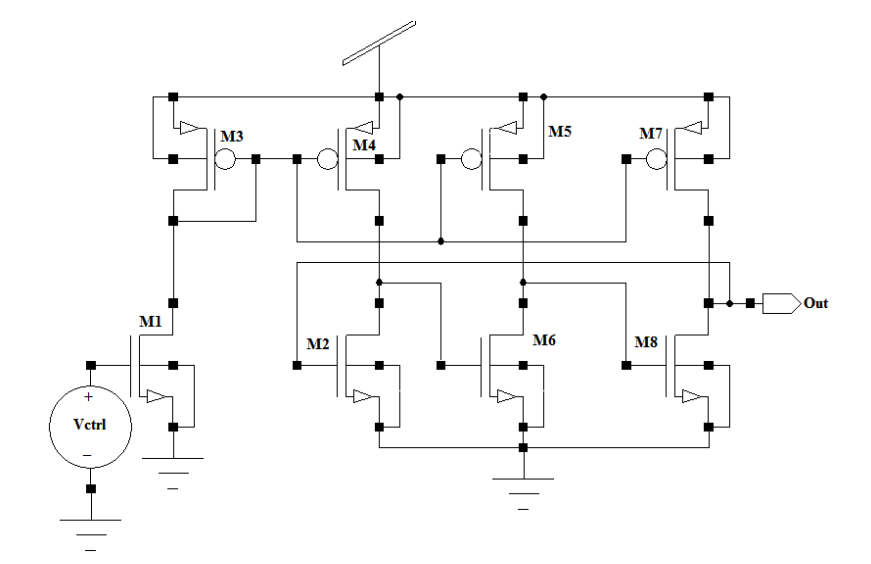
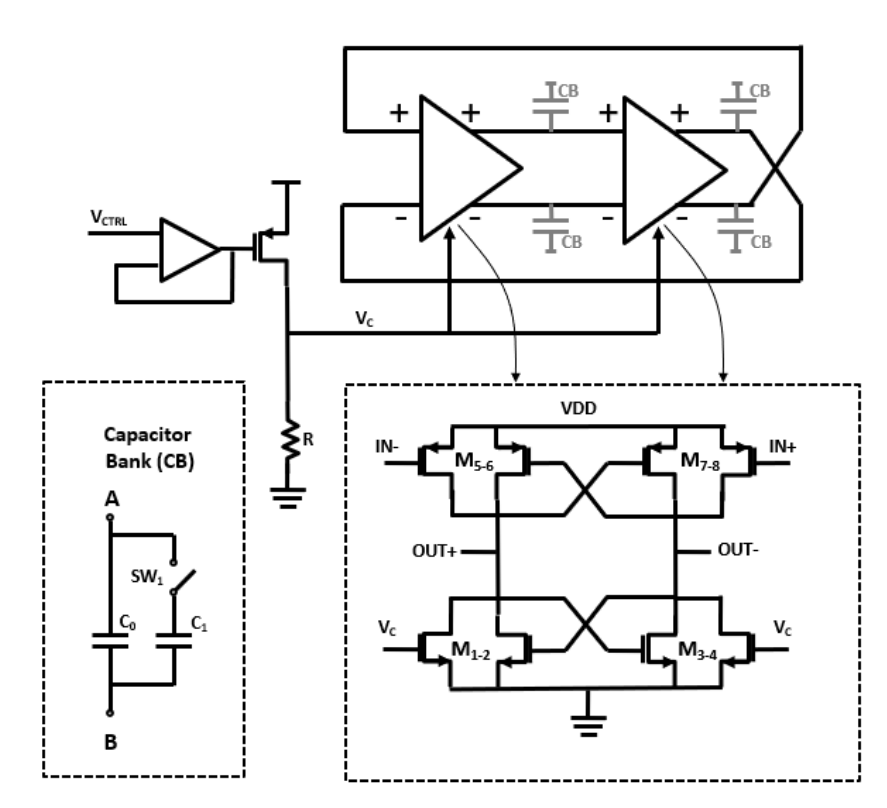
PLLs are a critical block in applications requiring frequency synthesis, frequency or phase demodulation, clock/carrier recovery, etc. Hence they are widely used in integrated circuits for wireless communications for IoT, biomedical, automotive/aerospace, consumer applications, etc.

The Voltage Controller Oscillator (VCO) is a key building block in phase-locked loops (PLL) as it has to operate at the highest frequency and its votage sensitivity, linearity and noise affect directly the PLL performance. Additionally, the VCO must have a wide enough tuning range to be able to compensate for PVT variations and to cover the PLL system required output frequencies.

# Vco Circuit Design

Two of the main topologies used for VCO design are LC-VCO and Ring Oscillators. LC-VCOs tend to have low noise/jitter performance, but usually require more area due to the passive integrated inductors, and they have a narrower tuning range. Ring oscillators usually require less area, less power and have a wider tuning range at the expense of worse phase noise and jitter. [1]

For this design we choose to implement a ring VCO. Delay stages can be either current starved inverters [2], differential to single ended [3] or differential cross-coupled delay stages [5].

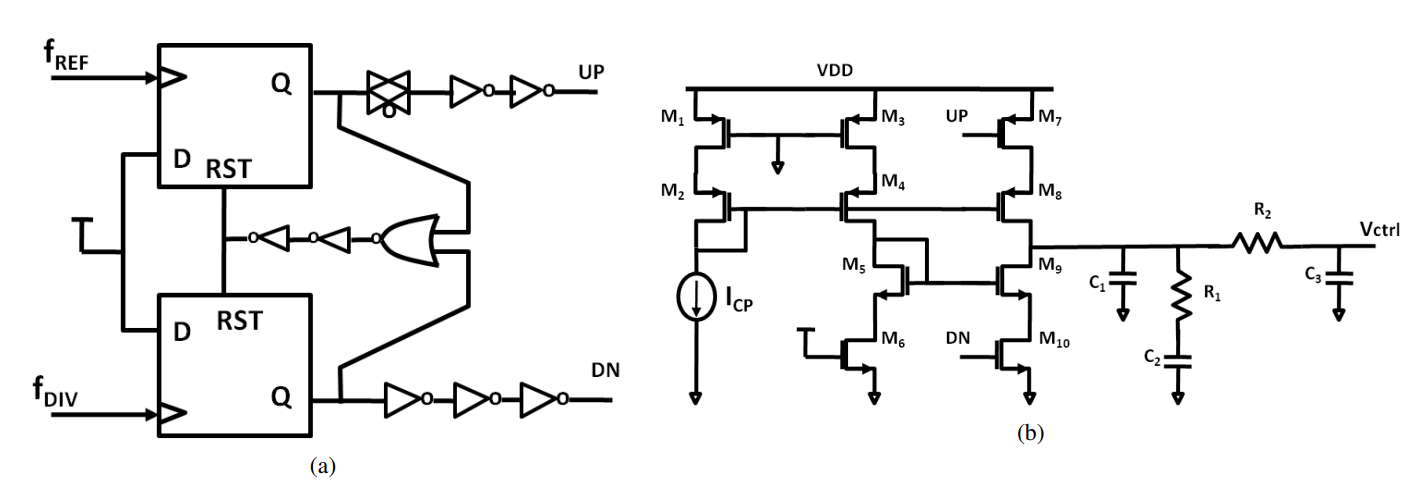


Differential topology can provide a full voltage swing on the VCO outputs which may benefit high speed operation as the near rail-to-rail voltage can charge the capacitive load on the VCO provided by subsequent stages like the frequency divider in the PLL feedback loop, possibly at the expense of a higher power consumption.

# PFD, Charge Pump and Loop Filter

Phase Frequency Difference Detector (PFD) compares the phase of the input reference clock and the VCO output clock, hence locking the PLL output the desired multiple of the input frequency. The Charge Pump and Low Pass Filter translate this phase difference into a control voltage to regulate the VCO frequency.

The PFD, CP and LPF topology that we plan to use is shown below, from [4]:

The PFD consists of D flip-flops (DFFs) with matched delays on the UP and DN signals and the reset path being designed to eliminate the dead-zone caused by the time it takes to turn on the charge pump.

The CP circuit mitigates the effects of current mismatch between the UP and DN pulses, thus avoiding the effects of charge sharing and charge injection mismatch.

# Testing Plan

The results verification strategy will consist of pre-layout simulations, followed by RC or RCC extracted post-layout simulations. For this high speed VCO design, post-layout simulations are important due to the high sensitivity to device and routing parasitics on the VCO frequency performance.

##### References

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