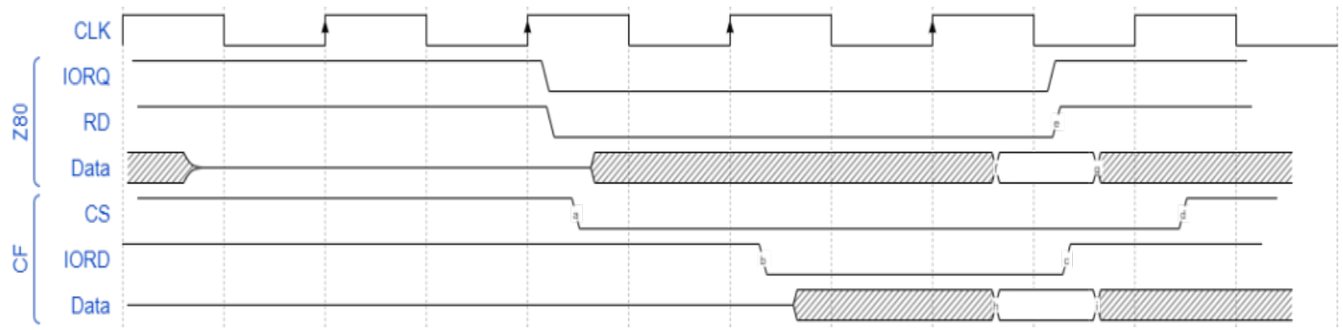
Electronics designed by Tadeusz Pycio
and reproduced with his permission

U3.2 generates an extended /IORQ
for I/O addresses with A4 high

U1 decodes the I/O address range
0x10 to 0x17 (binary 0001 0XXX)

U2.1 and U2.2 delay the Write signal

U2.3, U2.4 and U3.1 delay the Read signal



Design by Tadeusz Pycio

For full details see: http://www.vtsys.pl/

Address decoding

/DIO = address XXX1 XXXX

Default I/O address = 0x10 to 0x17 (binary 0001 0xxx)

/SEL = address 0001 0XXX

Title:	SC715 RCBus Compact Flash module		Schematic: v1.0.0
Date:	2023-04-27	Created: 2023-04-25	Sheet: 1 of 1
Designer:	Stephen C Cousins, Small Computer Central, www.scc.me.uk		