YHM4001A/4002A

Voltage Modulation Communication Over Smart Power Switch

Features

- Input voltage range: 2.5V ~ 5.5V
- Any of VIN, VOUTL, VOUTR and VDD may supply the chip
- Min Power Path On-resistance: typical 60mΩ each
- Max 1.5A continuous current capability
- Max 12.5K bps for physical signal traffic for VMC (Voltage Modulation Communication)
- Power Path On/Off and discharge control
- Optional active low (YHM4001A default reg bit on after POR) or high (YHM4002A default reg bit off after POR) for power switch
- 10-bits ADC for current sensing through each power path，additional impedance & passive load short and VIN/VOUTL/VOUTR voltage detection
- Cable impedance and contact quality detection
- Active Short protection or high accuracy OCP
- Reverse current detection and protection
- Watch dog time-out to turn off power path and Reset MCU or AP as well
- Direct Single Wire Communication Support such as support 1.2Mbps Half Duplex UART Traffic
- Simple VIN Command Detection for direct RSTB logic control and UART path on/off control
- OTP (Over Temperature Protection)
- Robust ESD capability
- >2kV HBM & >1kV CDM
- 15kV air discharge & 8kV contact discharge under IEC 61000-4-2 with TVS

Applications

- Mobile Phone, AR/VR Device, TWS Charging Box/Earbuds, Wearable Watch/Band and Smart IOT devices etc.

General Description

The YHM4001A and YHM4002A handle special bidirectional on-power line data traffic based on YHMICROS' Voltage Modulation Communication protocol with Smart Capacitance Hysteresis Capture technology.

YHM4001A active low default on to typically work in tiny portable device such as earbud side. YHM4002A active high default off to typically work in power output side such as TWS charging box side.

YHM4001A/4002A adopt special technology to measure the current through power path with high accuracy.

The chips integrate high side current source and ADC for VIN, VOUTL, VOUTR pins' passive impedance and active voltages.

The low side current source, power path on/off and through current comparison and VMC Implement Unit will help data traffic between master and slave sides.

These chips also support watch dog function, once MCU or AP crash, the power path will be forced off, even may use RSTB pin to reset MCU or AP as well.

I^2C Interruption INTB may bypass to VIN, VOUTL or VOUTR for direct single wire communication between Master and Slave MCU/SOC.

The YHM4001A/4002A as master may do slave presence and in-existent detection and interruption.

The YHM4001A/YHM4002A come in a 3x3 array, 9-bump, 0.4mm pitch, 1.205mmx1.25mm wafer-level package (WLP) and a 2mmx3mm, 8-PIN，0.5mm pitch DFN package.

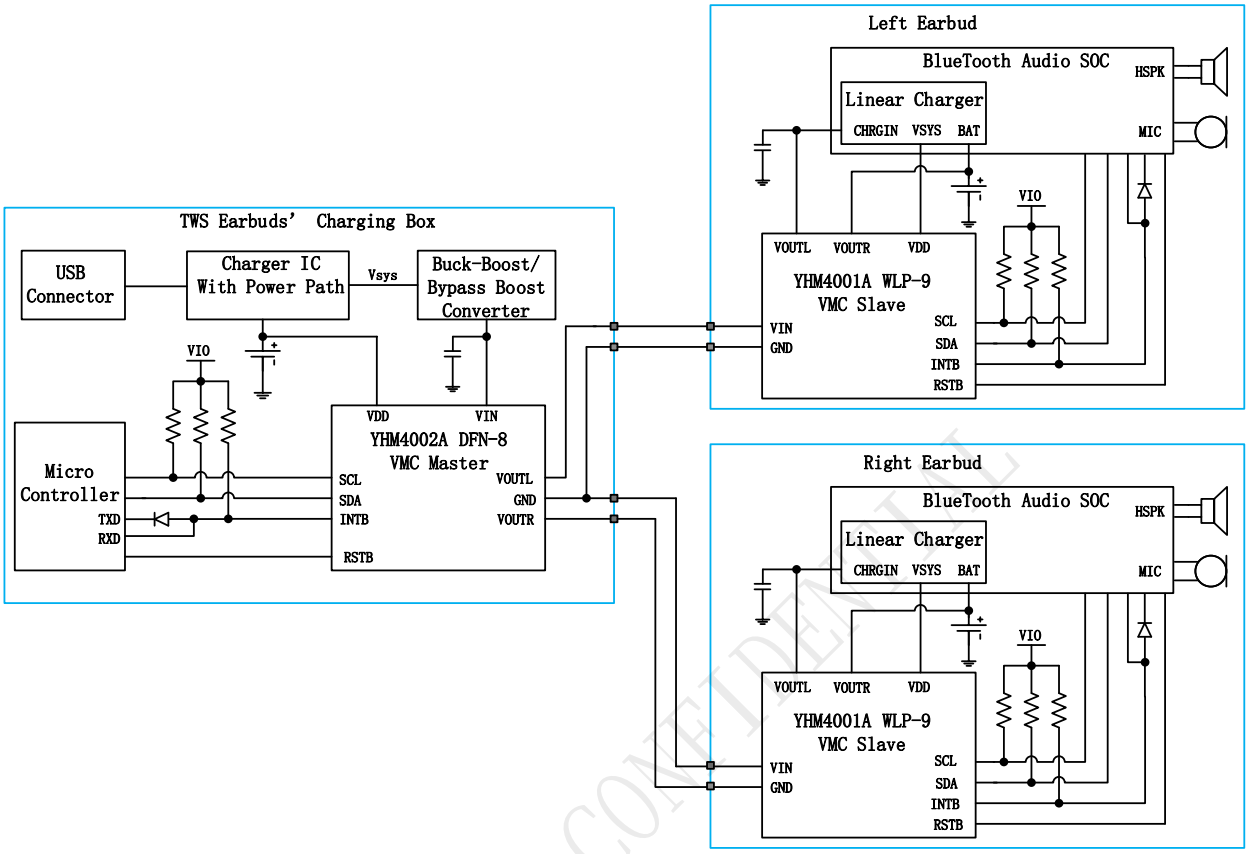


Fig 1. YHM4001A/2 Typical Application in TWS Charging Box and Ear Buds

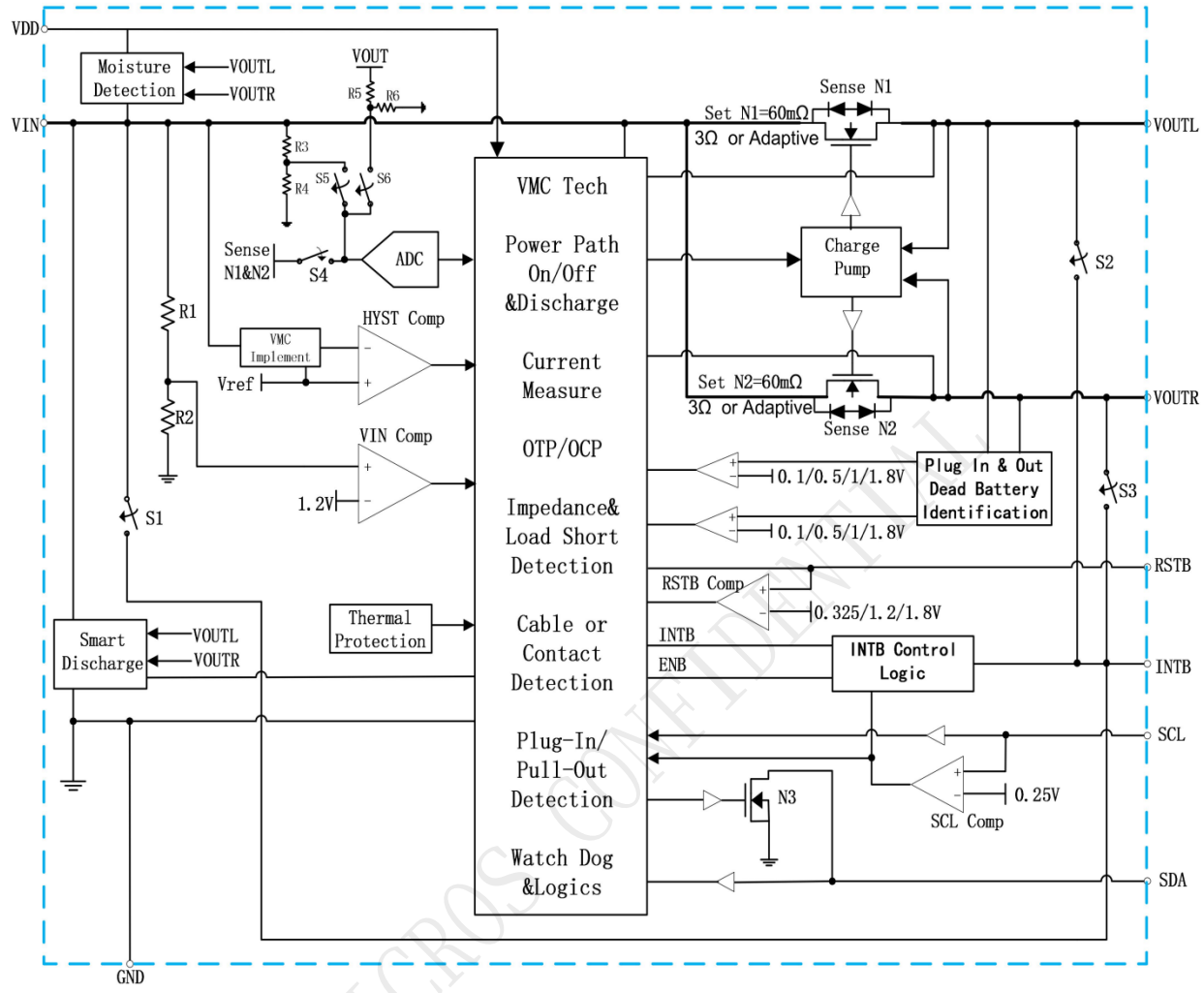


Fig 2. YHM4001A/YHM4002A Internal Block Diagram

YHM4001A/YHM4002A Pin Configurations

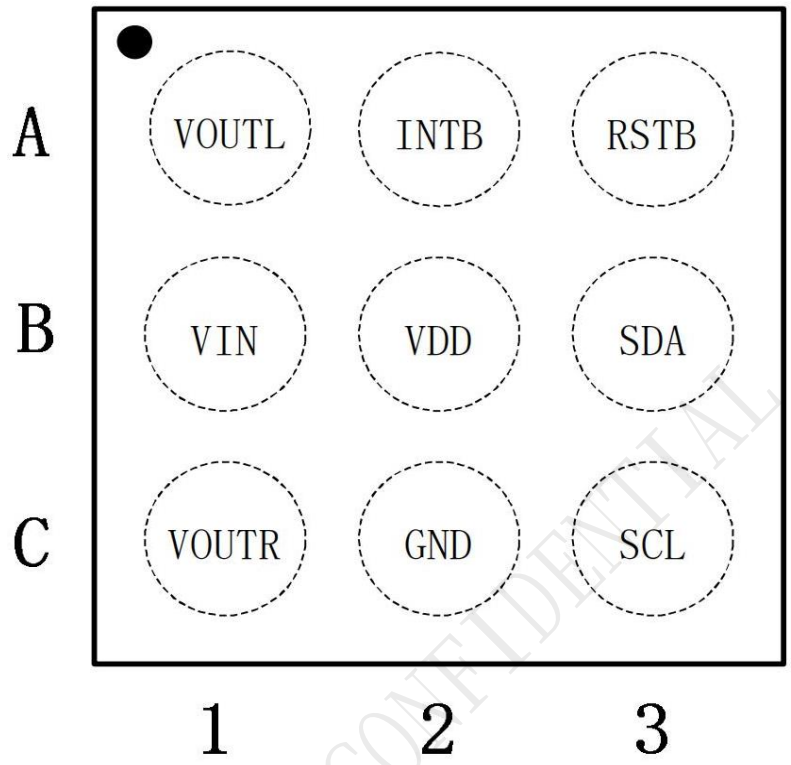


Fig 3. YHM4001A/4002A WLP-9 Pin Assignment (Top Through View）

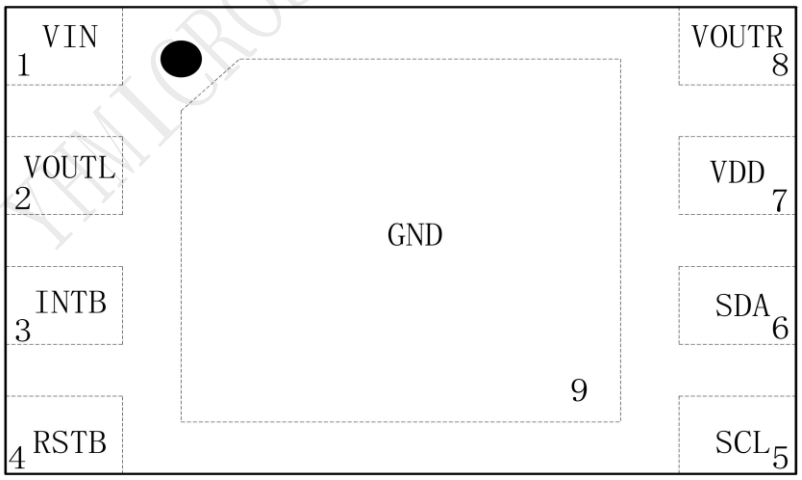


Fig 4. YHM4001A/YHM4002A DFN-8 Pin Assignment (Top Through View)

YHM4001A/YHM4002A DFN and WLP Pin Descriptions

DFN	WLP	Name	Description
1	B1	VIN	**Power Input**: Power Path Input and Chip Supply
2	A1	VOUTL	**Power Output**: Power Path Output to Left Load
3	A2	INTB	**Interruption** viz Open-drain output Pull down to ground when any FLG register alarms. Act as ENB function while SCL tied to GND. Way to VIN or VOUTL or VOUTR for Direct Single Wire Communication
4	A3	RSTB	**Signal Output:** Support Open drain output，Push-Pull output, Weak pull up and pull down output based on VIN command detection, Watch dog or I^2C command
5	C3	SCL	**Serial Clock Input:** Be used to synchronize data movement on the I2C serial interface. Tied GND for ENB function by INTB pin. Open-drain output and requires an external pull-up resistor
6	B3	SDA	**Serial Data Input/Output:** Input / Output pin for the 2-wire serial interface. Open-drain output and requires an external pull-up resistor
7	B2	VDD	Chip Supply while VIN less than VDD
8	C1	VOUTR	**Power Output**: Power Path Output to Right Load
9	C2	GND	Ground

1 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may no function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters		Min.	Max.	Unit
VIN	VIN to GND		-0.3	6.0	V
VOUTL, VOUTR	VOUT to GND		-0.3	VIN+0.3	V
INTB	INTB to GND		-0.3	VIN+0.3	V
VDD	VDD to GND		-0.3	6.0	V
V_{IO}	Maximum DC Voltage Allowed on RSTB, SCL, SDA		-0.3	6.0	V
I_{IN}	Switch I/O Current (Continuous) each path			1.5	A
t_{PD}	Total Power Dissipation at T_A=25°C			900	mW
T_{STG}	Storage Junction Temperature		-65	+150	°C
T_J	Operating Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient (100mm^2 pad of 1 oz. copper)			80(1)	°C/W
VIN, VOUTL and VOUTR	Electrostatic Discharge Capability	Human Body Model, EIA/JESD22-A114	2		kV
		Charged Device Model, JESD22-C101	1		
	IEC61000-4-2 System Level	Air Discharge	12		
		Contact Discharge	8		
All Other Pins		Human Body Model, EIA/JESD22-A114	2		

Note 1. Refer to JEDEC JESD51-7, use a 4-layerboard

2 Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance.

Parameters	Min.	Max.	Unit
Supply Voltage: VIN	2.8	5.5	V
Supply Voltage: VDD	2.8	5.5	V
V_{MAX}=Highest one of VIN, VDD, VOUTL and VOUTR	2.8	5.5	V
I^2C: SDA and SCL	1.5	5.5	V
I/O pins: RSTB, INTB, SDA, SCL	0	5.5	V
Ambient Operating Temperature, T_A	-40	85	°C
VOUT Load Capacitor (Slave)	0.01	0.1	μF

3 Detailed Electrical Characteristics

Unless otherwise noted, VIN = 2.5 to 5.5V, T_A = -40 to 85°C; Typical values are at VIN = 5.0V, I_{IN} ≤ 0.75A, C_{IN} = 0.1µF and T_A = 25ºC.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Basic Operation (Refer to active low version YHM4001A)						
I_Q	Input Quiescent Current on VIN	VIN = 5V, Chip Enable, Power Path On		52		µA
		VIN = 2.4V, Chip default enable, default Power Path On		50		
	Input Quiescent Current on VDD	VDD = 3.3V, Chip enable, power path Off, detection mode, 0A, single pulse			10	
		VDD = 3.3V, Chip enable, VIN = 0V, Power Path On		48		
I_{ADC}	VDD Current consumption of ADC	VDD = 3.3V, Chip Enable, Power Path Off			1	mA
I_{SHDN}	Device shutdown current	VIN = 5 V, ENB = 3.3 V, VOUTL/R=0V		2	3	µA
I_{DSLP}	Device deep sleep	VIN = 0V, VDD = 3.3V, VOUTL/R = 0V			1	uA
I_{LEAK}	VIN Leakage current during detection (2)	VIN = 2.1 V, VOUT = 0 V, T_A = 65°C, DET_EN = 1, I_{SRC} = 0A;		30	100	nA
$V_{MAX\_UV\_R}$	Under-Voltage Rising Trip Level	V_{MAX} rising, T_A= -40 to 85°C	2.2	2.3	2.5	V
$V_{MAX\_UV\_F}$	Under-Voltage Falling Trip Level			2.2		V
$V_{VIN\_UV\_F}$	Voltage Compare Falling Trip Level for VIN	VIN falling, T_A= -40 to 85°C	2.3	2.5	2.7	V
V_{HYS_VIN}	Change Hysteresis for VIN			100		mV
R_{ON}	Resistance from VIN to VOUT Via I^2C setting	VIN= 5V, I_{OUT} = 300mA, T_A = 25°C		60		mΩ
		For VMC over Power Path		3.2		Ω
I_{OCP}	Default Over Current Protection threshold (2)	VIN = 5V, T_A= 0 to 65°C		1.5		A
V_{HD_SHT}	Hard Short threshold	VIN = 5V		0.5		V
T_{SD}	Thermal Shutdown (2)			130		°C
T_{SH}	Thermal Shutdown Hysteresis (2)			20		
R_{PD}	Pull-down resistor on ENB			2		MΩ
I/O and Interface						

V_{OL_INTB} and RSTB	INTB/RSTB Output Low Voltage	$I_{INTB/RSTB}$ = 2mA, Interrupt Asserted or RESET claimed			0.3	V
V_{OH_RSTB}	RSTB Output High Voltage	I_{RSTB} = 1mA (RSTB driving load current	2.5			V
V_{IH_INTB}	INTB HIGH Voltage	V_{IN} = 2.8V to V_{IN_OVLO}	1.2			V
V_{IL_INTB}	INTB LOW Voltage	V_{IN} = 2.8V to V_{IN_OVLO}			0.55	V
I_{OUT_LEAK}	Leakage Current of INTB and RSTB	$V_{INTB/RSTB}$ = 3V, Interrupt De-asserted or RSTB floating setting			0.1	μA
I²C Interface						
V_{IH_I2C}	HIGH voltage of I²C input		1.2			V
V_{IL_I2C}	LOW voltage of I²C input				0.55	V
V_{OL_SDA}	LOW voltage of SDA	I_{OL}=2mA			0.3	V
f_{SCL}	SCL clock frequency	Fast Mode		400		kHz
t_{BUF}	Bus Free Time Between STOP and START conditions (2)	Fast Mode		1.3		μs
$t_{HD;STA}$	START or Repeated START Hold Time (2)	Fast Mode		600		ns
t_{LOW}	LOW Period of SCL Clock (2)	Fast Mode		1.3		μs
t_{HIGH}	HIGH Period of SCL Clock (2)	Fast Mode		600		ns
$t_{SU;STA}$	Repeated START Setup Time (2)	Fast Mode		600		ns
$t_{SU;DAT}$	Data Setup Time (2)	Fast Mode		100		ns
$t_{HD;DAT}$	Data Hold Time (2)	Fast Mode	0		900	ns
t_{RSCL}	SCL Rising Time (2)	Fast Mode	20+0.1Cb		300	ns
t_{RSDA}	SDA Rising Time (2)	Fast Mode	20+0.1Cb		300	ns
t_{FSDA}	SDA Falling Time (2)	Fast Mode	20+0.1Cb		300	ns
$t_{SU;STO}$	Stop Condition Setup Time (2)	Fast Mode		600		ns
Cb	Capacitive Load for SDA and SCL				400	pF
t_{SP}	Pulse width of spikes which must be suppressed by input filter (2)		0		50	ns
Moisture Detection and Output Short Detection						
I_{SRC}	Current source applied on VIN for moisture detection and on VOUTL/VOUTR for short detection	Set by register	0.001		11	mA

V_{SRC}	Clamping voltage on VIN in detection mode (ISRC=10mA, always ON)	VDD = 3.3V, Chip Enable, Detection Mode	1.8	1.9	2.0	V
I_{OD}	Current needed to over-drive VIN	VDD = 3.3V, Chip enable, Detection mode, use I_{SINK} VIA I^2C setting	40		160	mA
t_{SET}	Settle time for I_{SRC} and ADC (2)			40	60	µs
VMC Over Power Path						
t_{UNIT}	Time Unit	I^2C Programmable		80		us
				320		us
				640		us
I_{SINK}	Sink current in VIN/VOUTL/VOUTR	I^2C Programmable (default 120mA)		60		mA
				80		mA
				100		mA
				120		mA
Timing Characteristics						
t_{OCP_QUAL}	OCP qualification time	From I_{SW} > I_{OCP} to turning off action		500		µs
t_{OCP_RST}	OCP switch auto-restart time	Time from power switch turned off (OCP) to being turned on		200		ms
t_{INTB}	Interrupt maximum duration			1000		ms
tcmp_de	De-bounce time on VOUTL/VOUTR/RSTB linked with Comp Input			0.1(2)		us
t_{SW_DEB}	De-bounce Time of Power Switch turned on	Time from 2.5V < V_{IN} < V_{IN_OVLO} to VOUT = 0.1 × V_{IN}	15	22	30	ms
t_{TAG_DEB}	De-bounce Time of register TAG_STS	Time from V_{IN} > V_{TH_VIN} to V_{INTB} = 0.1V		100		µs
t_{UV_DEB}	De-bounce Time of Under Voltage Release (2)	VDD = 3.3V, ENB = 0V, 0x01 = 8'hC0		9		µs
t_{SS}	Soft-Start Time (2)(3)	Time from de-bounce time finished to Power Switch fully turn on		15		ms
t_{HS_BLK}	Hard short blank time during soft-start period	Time before power switch turned off with VOUT short to GND		3		ms
t_R	Switch Turn-On rising Time	VIN = 5V, R_L = 100Ω, C_L = 22µF, VOUT from 0.1 × VIN to 0.9 × VIN		2		ms

Note 2. This parameter is guaranteed by design and characterization; not production tested.
Note 3. Over Current Protection will be screened during this period.

4 Function description

4.1 Key Working Flow

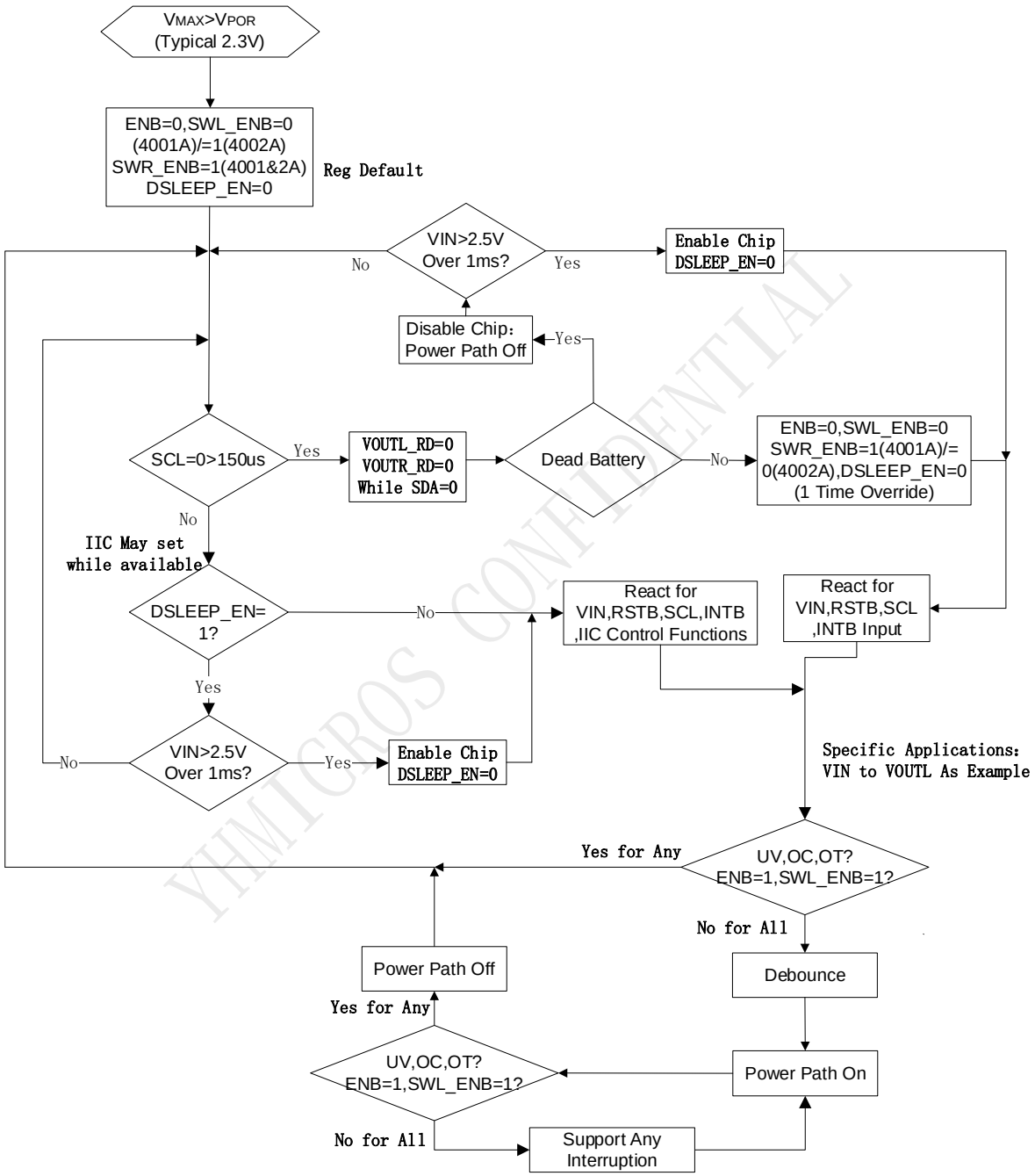


Fig 5. YHM4001A/YHM4002A Key working Flow

4.2 Power ON Reset

VMAX is the power to supply detection mode I_{SRC} and ADC. The I2C interface will keep working even if there is under disable stage.

The internal V_{VDD_UV} is used to reset all the detection related internal registers to the initial state. When VMAX voltage rises above $V_{VDD\_UV\_R}$, chip starts work and all related registers bits will be reset to default value.

When all of VDD, VIN, VOUTL and VOUTR drop below $V_{VDD\_UV\_F}$, the entire chip will stop working.

4.3 Working Modes

YHM4001A/YHM4002A defined as Master or Slave by system design, YHM4001A/YHM4002A in Charge Box or Charger Adapter side running as Master, the chip in Ear bud or wearable device side running as slave, The YHM4001A/YHM4002A have some main modes which refer to registers details to configure: Master, Slave, Detection, VMC, Simple VIN Toggle, Switch modes and so on. Refer to Fig 6 as well.

4.3.1 Voltage Modulation Communication (VMC)

For Master to Slave VMC initiated by Master, Master side power path(VIN to VOUTL or VIN to VOUTR) set On resistance as 3.2Ω，Turn on or off ISINK for VOUTL to GND or VOUTR to GND，then VOUTL or VOUTR voltage will be changed because ISINK On/Off to make VOUTL or VOUTR drop or not .

The slave side has Smart Capacitance Hysteresis Capture circuits, the circuits will get VIN (slave's VIN pin) up edge or down edge for digital communication.

For slave to master VMC, Slave will control the ISINK On/Off on Slave VIN pin, then Master side current through power path(VIN to VOUTL or VIN to VOUTR of Master) to make VOUTL or VOUTR voltage big drop or not（for example drop over 200mV), so Master will get digital signal from Slave.

Finally we may have logic to physical to logic process as: Master logic 0 --> 3Ω Power Path, Turn on ISINK on VOUTL/R-->Master VOUTL/R Drop more-->Hysteresis Capture in Slave VIN-->logic 0, and Master logic 1 --> 3Ω Power Path, Turn off ISINK -->Master VOUTL/R no more drop-->Hysteresis Capture in Slave VIN-->logic 1 , or Slave logic 0--> Turn on Slave ISINK on VIN-->more current through Master power path-->Master side Hysteresis Capture-->Master logic 0 and Slave logic 1--> Turn off Slave ISINK on VIN-->less current through Master power path-->Master side Hysteresis Capture-->Master logic 1.

Master to Slave and Slave to Master signaling with smart capacitance hysteresis capture technology to immunize system noise impact, the communication logic pattern is same no matter bytes from Master to Slave or bytes from Slave to Master.

Before voltage modulation communication between master and slave, the default internal logic is high (such as no enable sink current on Master VOUTL/R or Slave VIN), then initiate the VMC based on pulse short or long for logic identification, then construct byte with parity check.

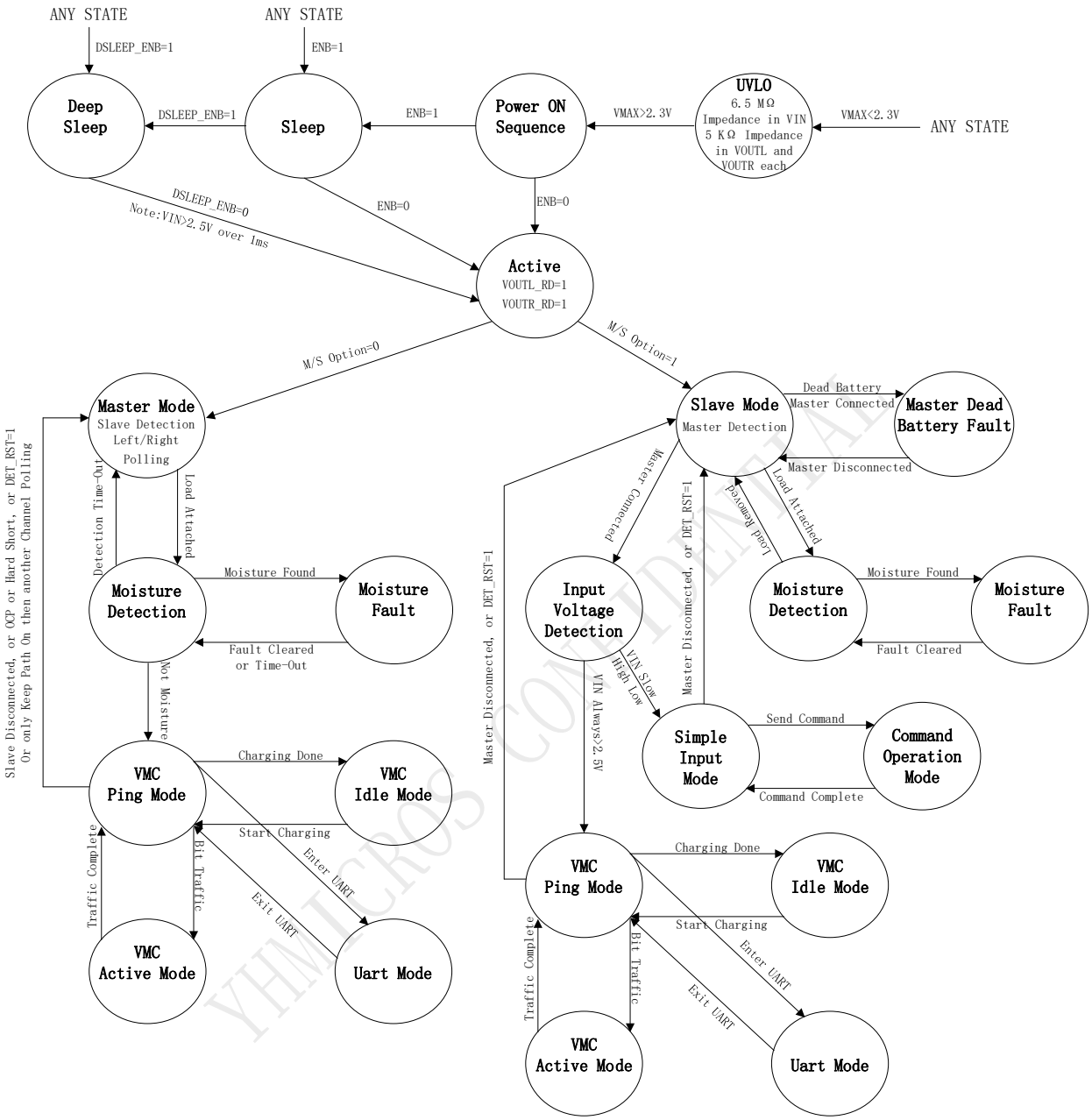


Fig 6. YHM4001A/YHM4002A Work Modes and System Control Flow

4.3.2 Simple VIN Toggle Command

The VIN of YHM4001A or YHM4002A can accept external logic signal as Command N to take some control action. For example Command 1 will clear 2Bh Reg CMD_TOG_REG[7:2].

Command 2 will force RSTB pin to Ground (for example Reset Ear bud SOC), Command 3 will force RSTB pin to logic high(>2.5V), Command 3 priority is higher than Command 2, Command 4 will turn on VIN to INTB switch with level shift capability for UART communication or other one wire communication, Command 5 will turn on VIN to VOUTL switch even in Dsleep mode, Send Command 2 or Command 3 or Command 4 or Command 5 second time, the previous action of Command 2 or Command 3 or Command 4 or Command 5 is canceled. BTW I^2C can read 2Bh to know which Command N ongoing. Refer to Fig 7, detailed simple VIN Toggle Command N described as following:

Externally force VIN to Ground with 1ms, then keep VIN high logic (>1.1 V) with 15ms, follow 16-N waveform (each waveform is 7ms Ground and 7ms High logic), then keep VIN high logic with 15ms and then to release VIN and end the Command N.

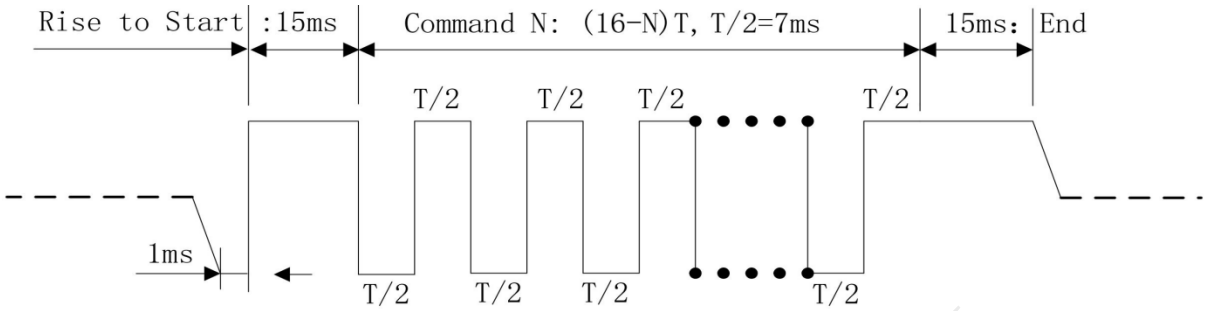


Fig 7. Simple VIN Toggle Command

4.3.3 Power Path On

Enabled by writing or resetting register SWL_ENB or SWR_ENB to 0. In this mode, the power path will be turned on when there is no UV, OC or OT event. Impedance (Moisture) Detection related function of registers will not be activated in this mode.

4.3.4 Impedance Detection Mode

Enabled by writing register DET_EN to 1. In this mode, I_{SRC} and ADC will be activated periodically and VIN to VOUTL and VOUTR Power Path off according to related registers' value for measuring VIN to GND impedance. Under power path off, the I_{SRC} and ADC may support to measure the impedance between VOUTL or VOUTR and GND as well.

4.3.5 Current Measurement Mode

Under Power Path on status, Enable ADC with right configuration, make current-to-voltage into ADC.

4.3.6 VIN Voltage measurement Mode

No matter Power Path on or off, disable I_{SRC}, May active ADC to test.

4.3.7 Deep Sleep Mode

I^2C may set 0Eh DSLEEP_EN bit=1 to make the chip into deep sleep mode with below 1uA current consumption. Force SCL GND over 150us and INTB=0(YHM4001A) or INTB=1(YHM4002A) would force switches ON but would not clear DSLEEP_EN bit. The only way to clear DSLEEP_EN bit is by I2C configuration. In this mode, the chip can accept simple command control.

4.3.8 Watch Dog Mode

The watchdog default disable, after enable watchdog and by I^2C to feed, once time-out the 02h reg WD_TO bit=1, The watchdog time-out may output through RSTB pin by I^2C configuration with continuous high logic or low logic, high pulse or low pulse on RSTB pin. For example, 1. Reg 18h=8'b01010100, Reg 19h=8'b10111111, Watchdog timer 16s, once time-out, output continuous high logic on RSTB pin. 2. Reg 18h=8'b01010100, Reg 19h=8'b10011111, Watchdog timer 16s, once time-out, output continuous low logic on RSTB pin.3. Reg18h=8'b01010100, Reg19h=8'b10111011, Watchdog timer 16s, once time-out, output 200ms high pulse on RSTB pin. 4. Reg18h=8'b01010100, Reg19h=8'b10011011, Watch dog timer 16s, once time-out, output 200ms low pulse on RSTB pin. The watch dog output circuit architecture supports open drain or push-pull, default open drain output by RSTB.

4.4 Soft-start

YHM4001A/YHM4002A power switch's start-up includes two stages:

- When all the power switch's on-conditions are all met, there is t_{DEB} = 22ms de-bounce time before the power switch start being turned on. The on-conditions include:
  - SWL_ENB = 0 or SWR_ENB=0, ENB=0, DSLEEP_EN=0
  - $V_{IN\_UVLO\_F}$ < VIN
  - Device junction temperature < T_{SD}.
- After t_{DEB}, the power switch is turned on but there is another t_{SS} = 15ms before the switch be fully turned on. During this period, the OCP function will be disabled temporally unless there is hard short on VOUT. Refer to 3.7 section for OCP and hard short feature.

4.5 Under Voltage Lockout

YHM4001A/YHM4002A power switch will be turned off when the voltage on VMAX is lower than the UVLO threshold $V_{IN\_UVLO\_F}$.

Whenever VMAX voltage ramps up to higher than $V_{IN\_UVLO\_R}$, the related register bits will be reset to default value and the power path switch will be turned on automatically after t_{DEB} de-bounce time if there is no OT.

4.6 Over Current Protection and Hard-Short Protection

When the current through the device exceeds the threshold I_{OCP} for t_{OCP_QUAL} = 0.5ms, or VOUTL or VOUTR drop below V_{HD_SHT} = 0.5 V as hard short, the related power switch will be turned off. INTB pin will be triggered to ground. At the meantime, L_OCP or R_OCP will be set to 1 and latched. The related switch will be turned on again after t_{OCP_RST} = 200ms.

The Over Current Protection will be screened during soft-start t_{SS} = 15ms.

The Hard-Short Protection will be screened during a blank time t_{HS_BLK} = 3ms. During this period, the output current will be limited to no larger than 1.5A. If VOUT does not rise above V_{HD_SHT} = 0.5 V in t_{HS_BLK}, the switch will be turned off as hard short and re-try again after t_{OCP_RST}.

4.7 Typical Status Bits

TMO and TAG etc. are status bits. Interruption registers will latch high once triggered until the register is read or the device is reset by power down or INTB pulled up(YHM4001A)/down(YHM4002A) while SCL=0 over 150us. But the value could be set to 1 again after read if the condition triggered it still exist. Status registers will change its value any time according to the condition define it changes.

- **TMO:** When the device is in detection mode, the register bit TMO will be set by YHM400X to 1 in t_{BLNK} and to 0 in t_{DET}. Every time TMO is set from 0 to 1, INTB will be pulled down as interrupt. Unless interrupt time out t_{INTB} reached, or Interruption register byte is read, or the device withdraws from detection mode, INTB will not be de-asserted until t_{DET} start.
- **TAG:** When the device is in detection mode, DET_EN = 1, the value in register VIN[9:0] will be compared with the value in register TH_VIN[9:0]. When VIN < TH_VIN, TAG will be set to 0. When VIN ≥ TH_VIN, TAG will be set to 1. Every time TAG is set from 0 to 1, INTB will be pulled down as interrupt. Unless interrupt time out t_{INTB} reached, or Flag register byte is read, INTB will not be de-asserted.

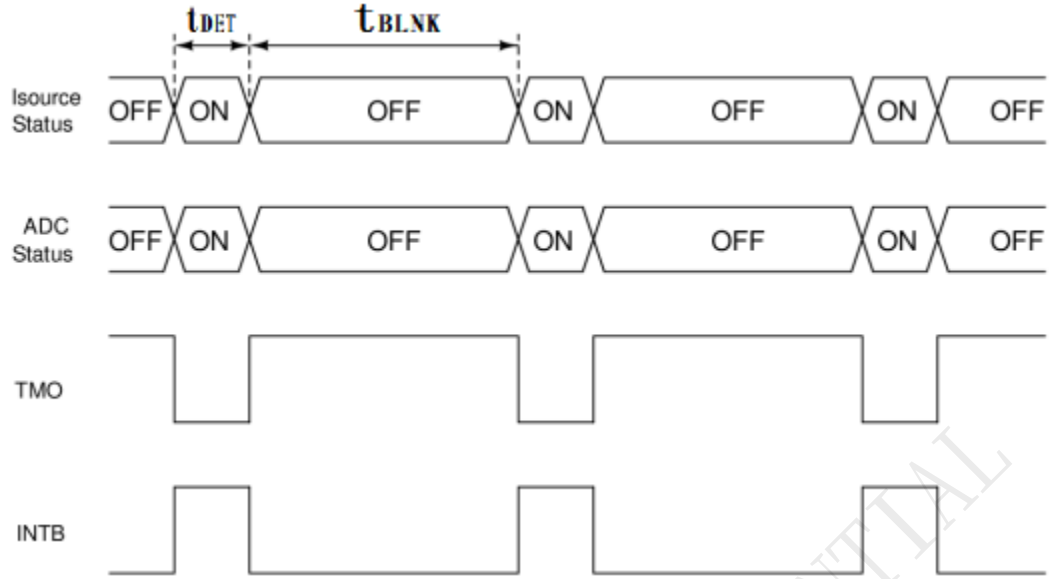


Fig.8 Timing for TMO and related interrupt (tBLNK < tINTB)

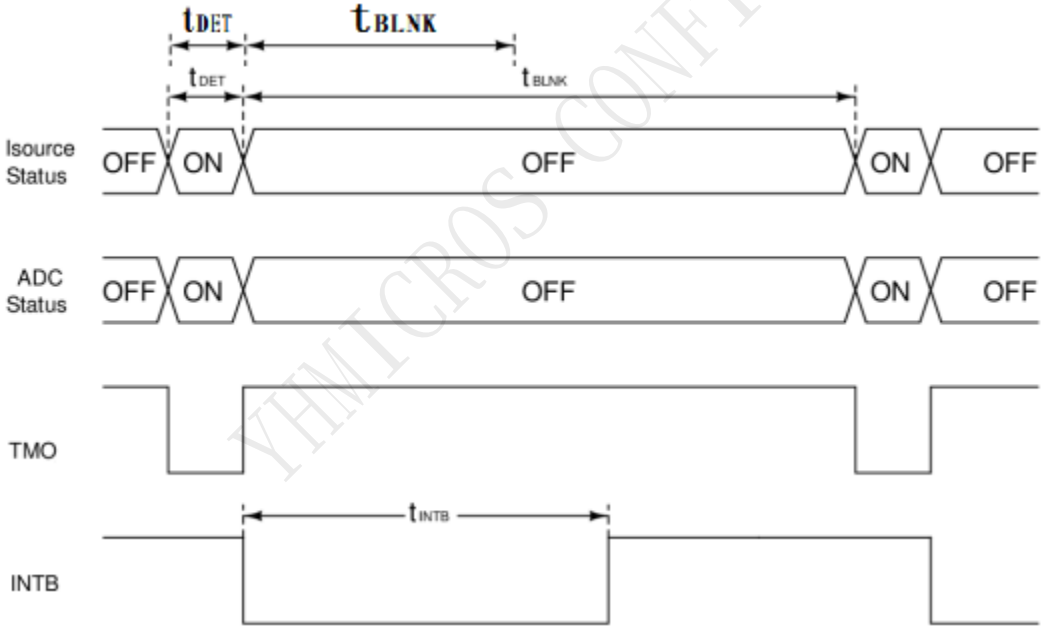


Fig 9. Timing for TMO and related interrupt (tBLNK > tINTB)

4.8 Thermal shutdown

When the part is in switch mode, to protect the chip from over temperature, the power path will be turned off when the junction temperature exceeds TSND = 130°C. INTB will be triggered to ground. At the meantime, OT_I will be set to 1 and latched. The related power path switch will be turned on again when temperature drop below 110°C. The device power dissipation capability is dependent on board design and layout. Mounting pad configuration on the PCB, the board material and the ambient temperature affect the rate of junction temperature rise for the part. When YHM4001A/YHM4002A has good thermal conductivity through the PCB, the junction temperature will be relatively low

under high power through applications. Refer to section 1 spec, the maximum dissipation the YHM4001A/YHM4002A can handle is given by:

$$P_{D(MAX)}=[T_{J(MAX)}-T_A]/R_{\theta JA}$$

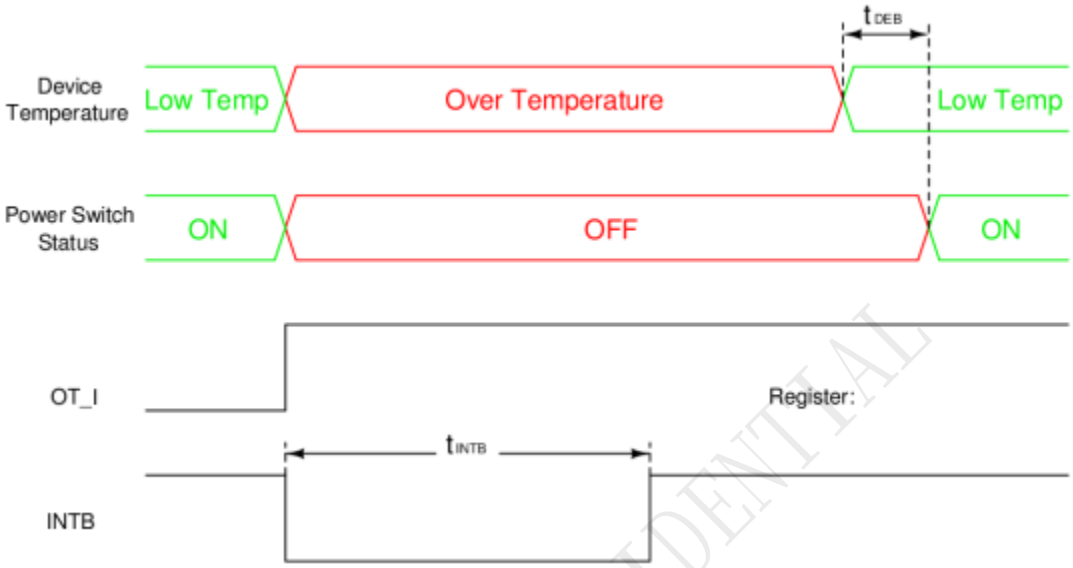


Fig.10 Timing for power switch thermal shutdown

4.9 Power path leakage

The leakage on the power switches is important because it could cause big inaccuracy on moisture or input and output impedance detection. Make sure the turn off leakage is smaller than 100nA especially when I_{SRC} = 1uA.

4.10 Input discharge

There is a discharging path on VIN. The discharge path on VIN be enabled by I^2C setting. The device uses high accuracy sink current source to do VIN discharge function.
The default discharge current 120mA lasting 10ms to discharge while some of power path turned off if I^2C setting .The high accuracy sink current also may help to do input cable impedance or connector contact quality measurement by below actions: turn off power path switches, then measure VIN to get VIN1, enable such as 120mA ISINK discharge current and measure VIN again to get VIN2, the power supply to VIN cable resistance is (VIN1-VIN2)/ISINK, If the resistance is unreasonable, it means cable isn't qualified or connector contact mismatch.

4.11 Hints

The YHM4001A/YHM4002A are stable component and don't require a minimum ESR for the capacitor connected to VIN or VOUT. Higher capacitance and lower ESR will improve the overall line and load transient response but negatively impact VMC communication data rate. On master YHM4002A VOUT and slaver YHM4001A VIN, the capacitor is not allowed. On slaver side, if must add a ceramic to YHM4001A VOUT, the maximum output decoupling value is 0.1uF.

VIN and VOUT printed circuit board traces should be as wide as possible. Place external components, especially the input capacitor and TVS, as close as possible to the YHM4001A/YHM4002A, and make traces short as possible.

5 I2C interface

YHM4001A and YHM4002A allows I²C communication to program the registers. Registers will control I_{SRC} and ADC for moisture detection, and will control the power switches, I_{SRC}, I_{SINK} and ADC for Input power external path or contact impedance detection. I²C communication is only valid when VMAX supply is higher than 1.5V. The I²C of YHM4001A and YHM4002A supports 400Kbps fast speed mode.

5.1 Overview of I2C

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

5.2 Starting and Stopping I2C Bus Communications

- START condition: SDA level changes from high to low while SCL is at high level
- STOP condition: SDA level changes from low to high while SCL is at high level
- Repeated START condition (RESTART condition)

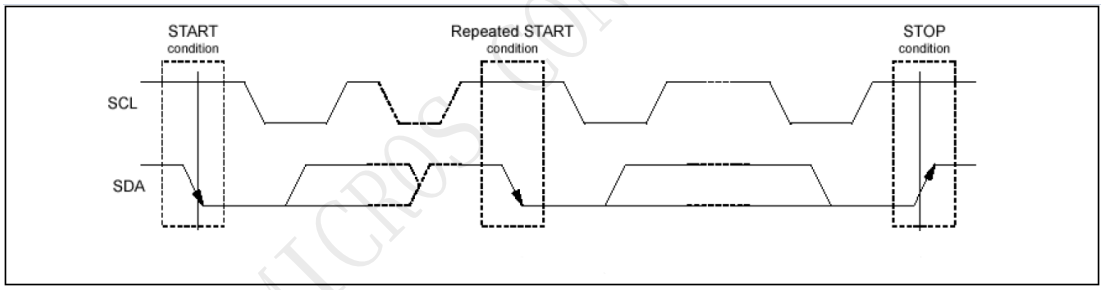


Fig.11 Start and Stop condition on I2C bus

5.3 Data Transfer and Acknowledge Responses during I2C communication

5.3.1 Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition. The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) captures data while the SCL line is at high level.

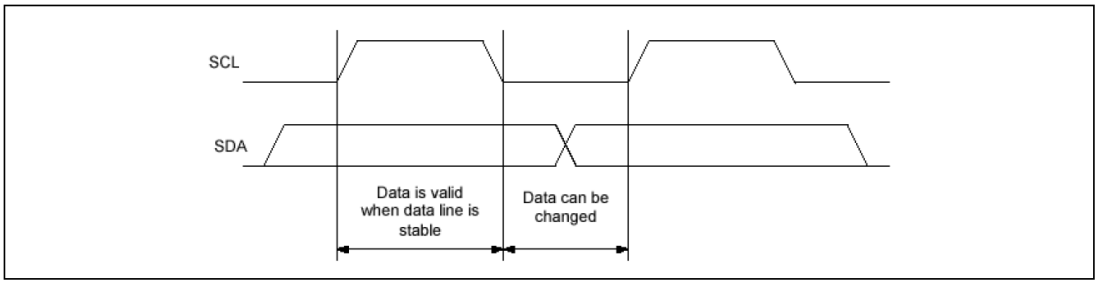


Fig.12 I²C data transmitting

5.3.2 Data acknowledge response

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.

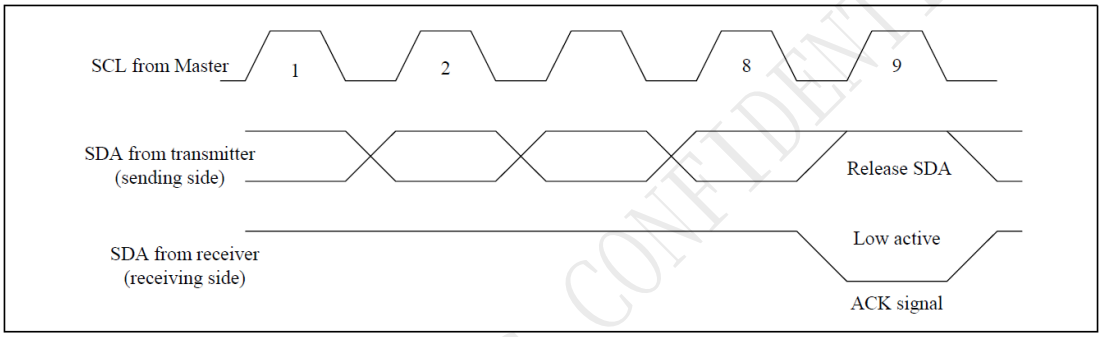


Fig.13 I²C to Acknowledge

After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, it indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

5.4 Slave Address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.

All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address. Slave addresses have a fixed length of 7-bits (7'b1100100 in YHM4001A/YHM4002A default case. Fuse (rom bit) to set 7'b1100101/1100110/1100111 as another slave address). See table for the details. An R/W bit is added to each 7-bits slave address during 8-bits transfers.

Operation	Transfer data	**Slave Address**							R/W bit
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	C9h	1	1	0	0	1	OTP (0)	OTP (0)	1(=Read)
Write	C8h								0(=Write)

6 Registers mapping

Register Table

Addr	Description	Def Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00H	Device ID R	80H	Vendor		Version			Revision		
01H	ISNS TRIM R	xxH	ISRC_TRIM[3:0]				ISNS_TRIM[3:0]			
02H	DET Status1 R	00H	VIN_DET	L_DET	R_DET	OT	TAG	TMO	ADC	WD_TO
03H	SW Status2 R	00H	L_RCB	L_UV	L_SHT	L_OCP	R_RCB	R_UV	R_SHT	R_OCP
04H	CMP Status3 R	00H	ADC_CMP	VMAX_UV	VIN_UV	LR_CMP	RSTB_CMP	VIN_CMP	L_CMP	R_CMP
05H	VMC Status4 R	00H	VMC_EXP	VMC_FAIL	VMC_DONE	ISNK_ON	L_IMIN	R_IMIN	L_ON	R_ON
06H	Det Int R/C	00H	VIN_DET_I	L_DET_I	R_DET_I	OT_I	TAG_INT	TMO_I	ADC_I	WD_TO_I
07H	SW Int R/C	00H	L_RCB_I	L_UV_I	L_SHT_I	L_OCP_I	R_RCB_I	R_UV_I	R_SHT_I	R_OCP_I
08H	CMP Int，R/C	00H	Reserved	VMAX_UV_I	VIN_UV_I	LR_CMP_I	RSTB_CMP_I	VIN_CMP_I	L_CMP_I	R_CMP_I
09H	VMC Int R/C	00H	VMC_EXP_I	VMC_FAIL_I	VMC_DONE_I	ISNK_ON_I	L_IMIN_I	R_IMIN_I	L_ON_I	R_ON_I
0AH	DET Mask R/W	00H	VIN_DET_M	L_DET_M	R_DET_M	OT_M	TAG_M	TMO_M	ADC_M	WD_TO_M
0BH	SW Mask R/W	00H	L_RCB_M	L_UV_M	L_SHT_M	L_OCP_M	R_RCB_M	R_UV_M	R_SHT_M	R_OCP_M
0CH	CMP Mask R/W	00H	Reserved	VMAX_UV_M	VIN_UV_M	LR_CMP_M	RSTB_CMP_M	VIN_CMP_M	L_CMP_M	R_CMP_M
0DH	VMC MASK R/W	00H	VMC_EXP_M	VMC_FAIL_M	VMC_DONE_M	ISNK_ON_M	L_IMIN_M	R_IMIN_M	L_ON_M	R_ON_M
0EH	Enable R/W	00H	Reserved	VMC_MODE	INTB_ENB	DSLEEP_EN	CG_EN	ENB	FSM_RST	DET_EN
0FH	IO_CONFIG R/W	40H	Reserved	N_UART	INTB_VIN	INTB_VL	INTB_VR	INTB_IO[1:0]		RSTB_WD
10H	L_ISNS_OCP R/W	6CH	Reserved	L_OCP_SEL[1:0]		L_ISNS_AUTO	L_ISNS_SCALE[3:0]			
11H	R_ISNS_OCP R/W	6CH	Reserved	R_OCP_SEL[1:0]		R_ISNS_AUTO	R_ISNS_SCALE[3:0]			
12H	SW OPTION R/W	8'b00_01 xx00	ISNS_CMP_SEL[1:0]		VMC_SW_OFF	INT_EXP	HIGH_SW_ON	LOW_SW_ON	RCB_SW_OFF	WD_SW_OFF
13H	SW Ctrl R/W		L_EN_SW	L_EN_ISNS	L_GND_SW	L_VIN_HIGH	R_EN_SW	R_EN_ISNS	R_GND_SW	R_VIN_HIGH
14H	DET Ctrl R/W	00H	EN_UV	EN_SHT	VIN_EN_DETI	VIN_EN_DETR	L_EN_DETI	L_EN_DETR	R_EN_DETI	R_EN_DETR
15H	CMP Vth R/W	3FH	RSTB_SEL[1:0]		VIN_SEL[1:0]		VOUTL_SEL[1:0]		VOUTR_SEL[1:0]	
16H	CMP En R/W	00H	EN_ICMP	EN_VMAX_UV	EN_VIN_UV	EN_CMP_LR	EN_CMP_RSTB	EN_CMP_VIN	EN_CMP_VL	EN_CMP_VR
17H	DISCHG R/W	6'b01_11_00			DISC_TIME[1:0]		DISC_ISEL[1:0]		DISC_RES	ISINK_CTRL
18H	Watch Dog Timer R/W	14H	Reserved	Post Pulse	Pulse Time[1:0]		WDI Wait Time[3:0]			
19H	Watch Dog Control R/W	C6H	WD CLK En	WDO OD	WDO DEF	WDO_EN	WD Post Pulse[1:0]		WD Mode	WD RST (W/C)
1AH	ISRC Time R/W	00H	ISRC_TDET[3:0]				ISRC_TBLK[3:0]			
1BH	ISRC DAC R/W	00H	ISRC_SEL[1:0]		ISRC_UNIT[1:0]		ISRC_DAC_CODE[3:0]			

Addr	Description	Def Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
1CH	Tag of DET H R/W	FFH	TAG_DET[9:2]							
1DH	Tag of DET L R/W	03H	Reserved						TAG_DET[1:0]	
1EH	ADC OPTION R/W	02H		TAG_DIR	ADC_RATIO	ADC_SEL[2:0]			ADC CLKDIV[1:0]	
1FH	ADC Control R/W	6EH	ADC_TRACK	ADC_DONE	ADC_AUTO	EN_ADC	DEB_MASK[1:0]		DEB_NUM[1:0]	
20H	ADC CodeH R	00H	ADC_CODE[9:2]							
21H	ADC CodeL R	00H	Reserved						ADC_CODE[1:0]	
22H	L_SW_STS				li_cmp_1p8	li_cmp_0p6	l_scale[3:0]			
23H	R_SW_STS				ri_cmp_1p8	ri_cmp_0p6	r_scale[3:0]			
2AH	FUSE R	00H	Reserved	SLV_ADDR[1:0]		H or L SW	ADC_OFFSET			
2BH	CMD_TOG R	00H	CMD_TOG[7:2]						Reserved	
2CH	VMC FSM R		Reserved	I_BYTE[2:0]			VMC_PAUSE (RW)	VMC_CS[2:0]		
2DH	VMC BYTE R		Reserved	I_BYTE[2:0]			Reserved	RX_BYTE[3:0]		
2EH	VMC OPTION R/W	8'b00_01000x	VMC_PIN[1:0]		TWAIT_TMR[1:0]		TX_FREQ[1:0]		ACK_RST	M/S
2FH	VMC CTRL R/W	04H	Reserved	TX_BYTES[2:0]			IGNORE_ERR	AUTO_PAUSE	RX_EN	TX_EN
30-33H	TX/RX Data R/W									

ID Register

Address: 00h, Bit[7:0]

Type: Read Only

Bits	Name	Defaults	Description
7:6	Vendor	2'b10	Vendor ID for customer recognition
5:3	Version	0	Version ID
2:0	Revision	0	Revision ID

ISNS TRIM Register

Address: 01h, Bit[7:0]

Type: Read/Write

<table>
<tr><th>Bits</th><th>Name</th><th>Defaults</th><th>Description</th></tr>
<tr><td>7:4</td><td>ISRC_TRIM[3:0]</td><td>0000</td><td>ISRC_TRIM is for silicon R trimming to get ideal R0=25k ohms, below is the trim ratio table.
<table>
<tr><td>Isrc_trim I_{src}</td><td>0000</td><td>0001</td><td>0010</td><td>0011</td></tr>
<tr><td>R0/R=$f_{src}(I_{src})$</td><td>30/30</td><td>29/30</td><td>28/30</td><td>27/30</td></tr>
<tr><td>Isrc_trim I_{src}</td><td>0100</td><td>0101</td><td>0110</td><td>0111</td></tr>
<tr><td>R0/R=$f_{src}(I_{src})$</td><td>26/30</td><td>25/30</td><td>24/30</td><td>23/30</td></tr>
<tr><td>Isrc_trim I_{src}</td><td>1000</td><td>1001</td><td>1010</td><td>1011</td></tr>
<tr><td>R0/R=$f_{src}(I_{src})$</td><td>38/30</td><td>37/30</td><td>36/30</td><td>35/30</td></tr>
<tr><td>Isrc_trim I_{src}</td><td>1100</td><td>1101</td><td>1110</td><td>1111</td></tr>
<tr><td>R0/R=$f_{src}(I_{src})$</td><td>34/30</td><td>33/30</td><td>32/30</td><td>31/30</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>ISNS_TRIM[3:0]</td><td>1000</td><td>Itrim = 150+ISRC_TRIM*6+ISNS_TRIM.
ISNS_TRIM is for current sense ratio 1157 trimming, the actual ratio: 1157-14*step+ISNS_TRIM*step, where step=18.</td></tr>
</table>

DET Status1 Register

Address: 02h, Bit[7:0]

Type: Read

Bits	Name	Defaults	Description
7	VIN_DET	0	One of VIN_EN_DETI or VIN_EN_DETR (14H Reg) should be enabled. 0: VIN<=vth2x (around 1.6V) 1: VIN>vth2x
6	L_DET	0	One of L_EN_DETI or L_EN_DETR (14H Reg) should be enabled 0: VOUTL<=vth2x (around 1.6V) 1: VOUTL >vth2x
5	R_DET	0	One of R_EN_DETI or R_EN_DETR (14H Reg) should be enabled 0: VOUTR<=vth2x (around 1.6V) 1: VOUTR >vth2x
4	OT	0	0: No over temperature. 1: Over temperature detected

3	TAG	0	0: (Default) Initialed by POR or cleared during when DET disable or when ADC done, ADC_CODE<TAG_DET. 1: Set when in DET state and ADC done and ADC_CODE>=TAG_DET.
2	TMO	0	0: (Default) Initialed by POR or cleared when not in DET_TMO state. 1: Set by YHM4001A/YHM4002A in DET_TMO state.
1	ADC	0	0: ADC is not done yet 1: ADC detection is done
0	WD_TO	0	0: Watch dog without time-out 1: Watch dog time-out

SW Status2 Register

Address: 03h, Bit[7:0]

Type: Read

Bits	Name	Defaults	Description
7	L_RCB	0	If VIN_HIGH=1, 0: VOUTL<VIN 1: VOUTL>VIN+20mV If VIN_HIGH=0, 0: VIN<VOUTL 1: VIN>VOUTL+20mV
6	L_UV	0	0: L path max of VIN & VOUTL is not UVLO 1: L path max of VIN & VOUTL is UVLO
5	L_SHT	0	0: L path short not detected 1: L path short detected
4	L_OCP	0	0: L path OCP not detected 1: L path OCP detected
3	R_RCB	0	If VIN_HIGH=1, 0: VOUTR<VIN 1: VOUTR>VIN+20mV If VIN_HIGH=0, 0: VIN<VOUTR 1: VIN>VOUTR+20mV
2	R_UV	0	0: R path max of VIN & VOUTR is not UVLO 1: R path max of VIN & VOUTR is UVLO
1	R_SHT	0	0: R path short not detected 1: R path short detected
0	R_OCP	0	0: R path OCP not detected 1: R path OCP detected

CMP Status3 Register

Address: 04h, Bit[7:0]

Type: Read

Bits	Name	Defaults	Description
7	ADC_CMP	0	0: Measured ADC input<ADC_CODE 1: Measured ADC input>=ADC_CODE (*This bit has no interrupt*)
6	VMAX_UV	0	0: VMAX is not in UVLO state 1: VMAX is in UVLO state
5	VIN_UV	0	0: VIN is not in UVLO state 1: VIN is in UVLO state

4	LR_CMP	0	0: L is less than R 1: R is less than L
3	RSTB_CMP	0	0: RSTB>vth of RSTB 1: RSTB<vth of RSTB
2	VIN_CMP	0	0: VIN>vth of VIN 1: VIN<vth of VIN
1	L_CMP	0	0: VOUTL>vth of L 1: VOUTL<vth of L
0	R_CMP	0	0: VOUTR>vth of R 1: VOUTR<vth of R

VMC Status4 Register

Address: 05h, Bit[7:0]

Type: Read

Bits	Name	Defaults	Description
7	VMC_EXP	0	0: VMC timer not expired 1: VMC timer expired
6	VMC_FAIL	0	0: VMC not failed 1: VMC failed
5	VMC_DONE	0	0: VMC not done 1: VMC done
4	ISNK_ON	0	0: Sink current is off 1: Sink current is on
3	L_IMIN	0	0: L path current > IMIN 1: L path current <=IMIN
2	R_IMIN	0	0: R path current > IMIN 1: R path current <=IMIN
1	L_ON	0	0: L path fet off 1: L path fet on
0	R_ON	0	0: R path fet off 1: R path fet on

DET Int Register

Address: 06h, Bit[7:0]

Type: Read/Clear

Bits	Name	Defaults	Description
7	VIN_DET_I	0	If VIN_DET status changes (both direction LH or HL), this bit will be 1
6	L_DET_I	0	If L_DET status changes, this bit will be 1
5	R_DET_I	0	If R_DET status changes, this bit will be 1
4	OT_I	0	If OT status changes, this bit will be 1

3	TAG_I	0	If TAG status changes from 0 to 1, this bit will be 1
2	TMO_I	0	If TMO status changes from 0 to 1, this bit will be 1
1	ADC_I	0	If ADC status changes from 0 to 1, this bit will be 1
0	WD_TO_I	0	If WD_TO status changes from 0 to 1, this bit will be 1

SW Int Register

Address: 07h, Bit[7:0]

Type: Read/Clear

Bits	Name	Defaults	Description
7	L_RCB_I	0	If L_RCB status changes from 0 to 1, this bit will be 1
6	L_UV_I	0	If L_UV status changes from 0 to 1, this bit will be 1
5	L_SHT_I	0	If L_SHT status changes from 0 to 1, this bit will be 1
4	L_OCP_I	0	If L_OCP status changes from 0 to 1, this bit will be 1
3	R_RCB_I	0	If R_RCB status changes from 0 to 1, this bit will be 1
2	R_UV_I	0	If R_UV status changes from 0 to 1, this bit will be 1
1	R_SHT_I	0	If R_SHT status changes from 0 to 1, this bit will be 1
0	R_OCP_I	0	If R_OCP status changes from 0 to 1, this bit will be 1

CMP Int Register

Address: 08h, Bit[7:0]

Type: Read/Clear

Bits	Name	Defaults	Description
7	Reserved	0	
6	VMAX_UV_I	0	If VMAX_UV status changes, this bit will be 1
5	VIN_UV_I	0	If VIN_UV status changes, this bit will be 1
4	LR_CMP_I	0	If LR_CMP_I status changes, this bit will be 1
3	RSTB_CMP_I	0	If RSTB_CMP_I status changes, this bit will be 1
2	VIN_CMP_I	0	If VIN_CMP_I status changes, this bit will be 1
1	L_CMP_I	0	If L_CMP_I status changes, this bit will be 1
0	R_CMP_I	0	If R_CMP_I status changes, this bit will be 1

VMC Int Register

Address: 09h, Bit[7:0]

Type: Read/Clear

Bits	Name	Defaults	Description
7	VMC_EXP_I	0	If VMC_EXP status changes from 0 to 1, this bit will be 1
6	VMC_FAIL_I	0	If VMC_FAIL status changes from 0 to 1, this bit will be 1
5	VMC_DONE_I	0	If VMC_DONE status changes from 0 to 1, this bit will be 1
4	ISNK_ON_I	0	If ISNK_ON status changes, this bit will be 1

3	L_IMIN_I	0	If L_IMIN status changes, this bit will be 1
2	R_IMIN_I	0	If R_IMIN status changes, this bit will be 1
1	L_ON_I	0	If L_ON status changes, this bit will be 1
0	R_ON_I	0	If R_ON status changes, this bit will be 1

DET Mask Register

Address: 0Ah, Bit[7:0]

Type: Read/Write (All Mask Register bit default 0, Interruption not masked)

Bits	Name	Defaults	Description
7	VIN_DET_M	0	0: VIN_DET_I is not masked. VIN_DET_I=1 will trigger interrupt. 1: VIN_DET_I is masked, VIN_DET_I=1 won't trigger interrupt.
6	L_DET_M	0	L_DET_I interrupt mask
5	R_DET_M	0	R_DET_I interrupt mask
4	OT_M	0	OT_I interrupt mask
3	TAG_M	0	TAG_I interrupt mask
2	TMO_M	0	TMO_I interrupt mask
1	ADC_M	0	ADC_I interrupt mask
0	WD_TO_M	0	WD_TO_I interrupt mask

SW Mask Register

Address: 0Bh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	L_RCB_M	0	L_RCB_I interrupt mask
6	L_UV_M	0	L_UV_I interrupt mask
5	L_SHT_M	0	L_SHT_I interrupt mask
4	L_OCP_M	0	L_OCP_I interrupt mask
3	R_RCB_M	0	R_RCB _I interrupt mask
2	R_UV_M	0	R_UV_I interrupt mask
1	R_SHT_M	0	R_SHT_I interrupt mask
0	R_OCP_M	0	R_OCP_I interrupt mask

CMP Mask Register

Address: 0Ch, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	Reserved	0	
6	VMAX_UV_M	0	VMAX_UV_I interrupt mask
5	VIN_UV_M	0	VIN_UV_I interrupt mask

4	LR_CMP_M	0	LR_CMP_I interrupt mask
3	RSTB_CMP_M	0	RSTB_CMP_I interrupt mask
2	VIN_CMP_M	0	VIN_CMP_I interrupt mask
1	L_CMP_M	0	L_CMP_I interrupt mask
0	R_CMP_M	0	R_CMP_I interrupt mask

VMC Mask Register

Address: 0Dh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	VMC_EXP_M	0	VMC_EXP_I interrupt mask
6	VMC_FAIL_M	0	VMC_FAIL_I interrupt mask
5	VMC_DONE_M	0	VMC_DONE_I interrupt mask
4	ISNK_ON_M	0	ISNK_ON_I interrupt mask
3	L_IMIN_M	0	L_IMIN_I interrupt mask
2	R_IMIN_M	0	R_IMIN_I interrupt mask
1	L_ON_M	0	L_ON_I interrupt mask
0	R_ON_M	0	R_ON_I interrupt mask

Enable Register

Address: 0Eh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	Reserved	0	
6	VMC_MODE	0	1: Logic VMC mode 0: Normal VMC mode Note: When use Logic VMC mode, must turn OFF master VOUTL switch (if select VOUTL pin for VMC) or VOUTR switch (if select VOUTR pin for VMC)
5	INTB_ENB	0	1: INTB is ENB input 0: INTB is INTB
4	DSLEEP_EN	0	0: Quit Deep Sleep 1: Deep Sleep<1uA, only VIN or INTB(SCL=0>150us) may clear the bit to 0
3	CG_EN	0	0: Disable watchdog clock gating 1: Enable watchdog clock gating
2	ENB	0	0: Enable the Chip 1: Disable the Chip(I^2C works and RESET command from VIN to RSTB works） Note: SCL=0>150us, INTB pin input logic voltage override ENB logic (for YHM4001A, INTB=0, make ENB=0; INTB=1, make ENB=1. for YHM4002A, INTB=1, make ENB=0; INTB=0, make ENB=1), otherwise ENB bit takes control by I^2C setting. INTB to Enable the chip will then turn on VIN to VOUTL and VOUTR switches and quit deep sleep. But I^2C to set ENB=0 will not impact SWL_ENB and SWR_ENB status
1	FSM_RST	0	Writing a 1 to this bit will reset the FSM to the master/slave detection state

0	DET_EN	0	0 (Default) Written by processor via I2C or cleared during POR. VIN or VOUTL/VOUTR impedance Detection is not applied until the state of this bit changed. The detection related registers will not be reset. 1 Written by processor via I2C. VIN or VOUTL/VOUTR impedance Detection turned on If Slave's VIN voltage is lower than VIN_UVLO_F and power path off or VOUTL or VOUTR voltage is lower than 1.8V and Power Path off. ISRC and ADC will be applied on VIN or VOUTL or VOUTR in tDET.

IO_CONFIG Register

Address: 0Fh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	Reserved		
6	N_UART	1	0: CMOS Path 1: NMOS Leve shift Note: YHM4001A Slave chip side INTB compatible with 1.8V IO while VIN logic with 3.3V high.
5	INTB_VIN	0	0: INTB to VIN Off, 1: INTB to VIN ON
4	INTB_VL	0	0: INTB to VOUTL Off, 1: INTB to VOUTL ON
3	INTB_VR	0	0: INTB to VOUTR Off, 1: INTB to VOUTR ON
2	INTB_IO[1]	0	0: PMOS is off. 1: PMOS is on
1	INTB_IO[0]	1	0: NMOS is off. 1: NMOS is on
0	RSTB_WD	0	0: RSTB NOT From WD Logic level, 1: RSTB From WD Logic level

L_ISNS_OCP Register

Address: 10h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
6:5	L_OCP_SEL[1:0]	11	00: 150mA 01: 300mA 10: 600mA 11:1500mA
4	L_ISNS_AUTO	0	0: No Auto Scale 1: Auto change ISNS_SCALE Note: change R and FET to make ISNS result in ADC range based on ISNS CMP output
3:0	L_ISNS_SCALE[3:0]	1100	L_ISNS_SCALE[3:2] to control switch Ron & current ratio. 00: Switch Ron 3.2, current ratio Iout/Isense=21:1 01: Switch Ron 0.4, current ratio Iout/Isense=161:1 11: Switch Ron 50m, current ratio Iout/Isense=1157:1 L_ISNS_SCALE[1:0] to control current sense R 00: 25k/2 01:25k/4 10: 25k/8 11:25k/16 Notes: Io=adc_dac*1.8/10'h3ff/N/R0*fsrc(Isrc)* (1157-14*step+Isns_trim*step), where R0=25kohm, step=18. For other current ratio, Io=adc_dac*1.8/10'h3ff/N/R0*fsrc(Isrc)* (1157-

			14*step+Isns_trim*step)/1157*ratio. N=1/2,1/4,1/8,1/16 based on L_ISNS_SCALE[1:0]

R_ISNS_OCP Register

Address: 11h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
6:5	R_OCP_SEL[1:0]	11	00: 150mA 01: 300mA 10: 600mA 11:1500mA
4	R_ISNS_AUTO	0	0: No Auto Scale 1: Auto change ISNS_SCALE Note: change R and FET to make ISNS result in ADC range based on ISNS CMP output
3:0	R_ISNS_SCALE[3:0]	1100	R_ISNS_SCALE[3:2] to control switch Ron & current ratio. 00: Switch Ron 3.2, current ratio Iout/Isense=21:1 01: Switch Ron 0.4, current ratio Iout/Isense=161:1 11: Switch Ron 50m, current ratio Iout/Isense=1157:1 R_ISNS_SCALE[1:0] to control current sense R 00: 25k/2 01:25k/4 10: 25k/8 11:25k/16 Notes: Io=adc_dac*1.8/10'h3ff/N/R0*fsrc(Isrc)* (1157-14*step+Isns_trim*step), where R0=25kohm, step=18. For other current ratio, Io=adc_dac*1.8/10'h3ff/N/R0*fsrc(Isrc)* (1157-14*step+Isns_trim*step)/1157*ratio. N=1/2,1/4,1/8,1/16 based on R_ISNS_SCALE[1:0]

SW OPTION Register

Address: 12h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7:6	ISNS_CMP_SEL[1:0]	0	IMIN comparator threshold Vimin selection IMIN=Vimin/Rsns*Iratio 00: 60mV 01: 120mV 10: 240mV 11: 480mV
5	VMC_SW_OFF	0	0: No Action for SW ON/OFF status while VMC 1: Turn Off SW while VMC
4	INT_EXP	1	0: Disable 1 second Interrupt expiration auto clear. 1: Enable 1 second Interrupt expiration auto clear.
3	HIGH_SW_ON	0	0: No action 1: If LR_CMP=1, turn on the switch L, otherwise turn on switch R
2	LOW_SW_ON	0	0: No action 1: If LR_CMP=0, turn on the switch L, otherwise turn on switch R
1	RCB_SW_OFF	0	0: When L_RCB or R_RCB is high, no action 1: When L_RCB is high, turn off VIN to VOUTL switch, when R_RCB is high, turn off VIN to VOUTR switch

0	WD_SW_OFF	0	0: Watch Dog timeout, no action 1: Watch Dog timeout, turn off switches

SW Ctrl Register

Address:13h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	L_EN_SW	0/1	1 (YHM4001A Default) Written by processor via I2C or cleared during YHM4001A POR. Turned on the VIN to VOUTL power path(switch) if UV, OV, OC, OT condition cleared and detection not being implemented. 0(YHM4002A Default): Written by processor via I2C. VIN to VOUTL Power path OFF During YHM4002A POR. *Turned off the power path if UV, OC, OT conditions occur and turn off the power switch before do Vin with Isink, Isrc and Voltage detection*
6	L_EN_ISNS	0	0: Disable L switch current sense 1: Enable L switch current sense
5	L_GND_SW	0	0: L switch is not ground switch 1: L switch is ground switch (Tells chip if this switch is used as GND switch, if it is GND switch, current sense, ocp features can't be used, because chip only integrates power side current sense)
4	L_VIN_HIGH	1	0: VOUTL is higher than VIN 1: VIN is higher than VOUTL (Tells chip which side is source)
3	R_EN_SW	0	1: Written by processor via I2C. Turned on the VIN to VOUTR power path(switch) if UV, OV, OC, OT condition cleared and detection not being implemented. 0(YHM4001A/2 Default): Written by processor via I2C. VIN to VOUTR Power path OFF During YHM4001A/2 POR. *Turned off the power path if UV, OC, OT conditions occur and turn off the power switch before do Vin with Isink, Isrc and Voltage detection*
2	R_EN_ISNS	0	0: Disable R switch current sense 1: Enable R switch current sense
1	R_GND_SW	0	0: R switch is not ground switch 1: R switch is ground switch
0	R_VIN_HIGH	1	0: VOUTR is higher than VIN 1: VIN is higher than VOUTR

DET Ctrl Register

Address: 14h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	EN_UV	0	0: Disable switch UV detection 1: Enable switch UV detection
6	EN_SHT	0	0: Disable switch short detection 1: Enable switch short detection
5	VIN_EN_DETI	0	0: Disable VIN pin 0.2uA isrc for plug detection 1: Enable VIN pin 0.2uA isrc for plug detection
4	VIN_EN_DETR	0	0: Disable VIN pin 500k pulldown 1: Enable VIN pin 500k pulldown
3	L_EN_DETI	0	0: Disable VOUTL pin 0.2uA isrc for plug detection 1: Enable VOUTL pin 0.2uA isrc for plug detection
2	L_EN_DETR	0	0: Disable VOUTL pin 500k pulldown 1: Enable VOUTL pin 500k pulldown
1	R_EN_DETI	0	0: Disable VOUTR pin 0.2uA isrc for plug detection 1: Enable VOUTR pin 0.2uA isrc for plug detection
0	R_EN_DETR	0	0: Disable VOUTR pin 500k pulldown 1: Enable VOUTR pin 500k pulldown

Comp Vth Register

Address: 15h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7:6	RSTB_SEL[1:0]	00	RSTB comparator threshold 00: 0.325V 01: 1.2V 10: 1.8V 11: invalid
5:4	VIN_SEL[1:0]	11	VIN comparator threshold 00: 0.1V 01:0.5V 10: 1.0V 11:1.8V
3:2	VOUTL_SEL[1:0]	11	VOUTL comparator threshold 00: 0.1V 01:0.5V 10: 1.0V 11:1.8V
1:0	VOUTR_SEL[1:0]	11	VOUTR comparator threshold 00: 0.1V 01:0.5V 10: 1.0V 11:1.8V

Comp En Register

Address: 16h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	EN_ICMP	0	0: switch ISNS>1.8V, ISNS<0.6V comparators enabled by state machine 1: These two comparators are enabled. These comparators are used to set ISNS_SCALE to let ISNS voltage in range 0.6V to 1.8V

6	EN_VMAX_UV	0	0: VMAX Under Voltage Protection Disable 1: VMAX Under Voltage Protecton Enable
5	EN_VIN_UV	0	0: VIN Under Voltage Protection Disable 1: VIN Under Voltage Protection Enable
4	EN_CMP_LR	0	0: CMP_LR Disable 1: CMP_LR Enable
3	EN_CMP_RSTB	0	0: CMP_RSTB Disable 1: CMP_RSTB Enable
2	EN_CMP_VIN	0	0: CMP_VIN Disable 1: CMP_VIN Enable
1	EN_CMP_VL	0	0: CMP_VOUTL Disable 1: CMP_VOUTL Enable
0	EN_CMP_VR	0	0: CMP_VOUTR Disable 1: CMP_VOUTR Enable

DISCHG Register

Address: 17h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7:6	Reserved		
5:4	DISC_TIME[1:0]	01	00: OFF 01: 10ms 10: 200ms 11: ON (always on or by logic pattern freq)
3:2	DISC_ISEL[1:0]	11	00: 60mA 01:80mA 10:100mA 11:120mA
1	DISC_RES	0	Reserved
0	ISINK_CTRL	0	0: Turn Off ISINK 1: Turn On ISINK. (Auto Clear after DISC_TIME)

Watch Dog Timer Register

Address: 18h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	Reserved	0	
6	Post Pulse	0	0: No Post Pulse State, directly to WD_IDLE state 1: stay in post pulse state
5:4	Pulse Time	01	00: WDO pulse time 100ms 01: WDO pulse time 200ms 10: WDO pulse time 400ms 11: WDO pulse time 1000ms
3:0	WDI Wait Time	0100	0000: Wait 1s, 0001: Wait 2s,0010: Wait 4s, 0011: Wait 8s 0100: Wait 16s, 0101: Wait 32s,0110: Wait 64s, 0111: Wait 128s

Watch Dog Control Register

Address: 19h, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	WD CLK EN	0	1: Enable WD 0: Disable WD

6	WDO OD	1	1: WDO open drain 0: WDO push pull
5	WDO DEF	0	0: wdo_tx=0 during WDO PULSE, wdo_tx=1 in IDLE & TIMER states 1: wdo_tx=1 during WDO PULSE, wdo_tx=0 in IDLE & TIMER states
4	WDO EN	0	1: WDO output buffer forced enable. 0: WDO output buffer enabled by FSM
3:2	WD Post Pulse[1:0]	01	00: wdo_tx=0, wdo_en_fsm= 0 01: wdo_tx=1, wdo_en_fsm= 0 10: wdo_tx=~WDO_DEF, wdo_en_fsm=1 11: wdo_tx=WDO_DEF, wdo_en_fsm=1 wdo_en = wdo_en_fsm || WDO_EN
1	WD Mode	1	1: Use I2C WD reset
0	WD RST (W/C)	0	0: default 1: Reset WD wait timer (Clear to 0 after write)

ISRC Time Register

Address: 1Ah, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7:4	ISRC_TDET	0	4'b0000 200μs 4'b0001 400μs 4'b0010 1ms 4'b0011 2ms 4'b0100 4ms 4'b0101 10ms 4'b0110 20ms 4'b0111 40ms 4'b1000 100ms 4'b1001 200ms 4'b1010 400ms 4'b1011 1s 4'b1100 2s 4'b1101 4s 4'b1110 10s 4'b1111 Always ON
3:0	ISRC_TBLK	0	4'b0000 Single Pulse 4'b0001 10ms 4'b0010 20ms 4'b0011 50ms 4'b0100 100ms 4'b0101 200ms 4'b0110 500ms 4'b0111 1s 4'b1000 2s 4'b1001 3s 4'b1010 6s 4'b1011 12s 4'b1100 30s 4'b1101 60s 4'b1110 120s 4'b1111 300s

Note: when 0x1B is set to 8'hF0 (conflict as single pulse and always ON), always on mode will be dominating.

Isource DAC Register

Address: 1Bh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7:6	ISRC_SEL[1:0]	00	00: Disable ISRC 01: ISRC to VIN 10: ISRC to VOUTL 11: ISRC to VOUTR
5:4	ISRC_UNIT[1:0]	00	00: 1uA 01: 10uA 10: 100uA 11: 1mA
3:0	ISRC_DAC_CODE[3:0]	0000	Code can be from 0 to 11, code >11 is invalid

			0000: 0 0001: 1 …. 1011: 11 1xxx: invalid

Tag of DET H&L Registers

Address: 1Ch, Bit[7:0], 1Dh, Bit[1:0]

Type: Read/Write

Bits	Name	Defaults	Description
1CH 7:0	TAG_DET[9:2]	FFh	Target ADC code, refer TAG_DIR for how TAG_DET is used to trigger TAG interrupt,
1DH 1:0	TAG_DET[1:0]	03h	

ADC OPTION Register

Address: 1Eh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	Reserved	0	
6	TAG_DIR	0	0: If ADC_CODE>=TAG_DET, TAG=1 1: If ADC_CODE<TAG_DET, TAG=1
5	ADC_RATIO	0	0: 1:1 1: 1:4
4:2	ADC_SEL[2:0]	000	000: VOUTR 001: VOUTL 010: VIN 011: RSTB 100: r_isns 101: l_isns
1:0	ADC CLKDIV[1:0]	10	ADC Clock Divided by 00: 2 01: 4 10: 8 11: 16

ADC Control Register

Address: 1Fh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	ADC_TRACK	0	0: ADC uses track & hold 1: ADC always track Note: W/R
6	ADC_DONE	1	Use DET_EN to start ADC, when ADC finished its SAR operation, ADC_DONE will be set to 1
5	ADC_AUTO	1	0: ADC MANNUAL control, adc_track set to 1 1: User SAR state machine
4	EN_ADC	0	0: ADC enabled by FSM 1: ADC enabled
3:2	DEB_MASK[1:0]	11	XX: Compare ADC_CODE[9:XX] with previous code for debounce
1:0	DEB_NUM[1:0]	10	ADC debounce times 00: 1 Time 01: 2 Times 10: 4 Times 11: 8 Times

ADC Code H&L Registers

Address: 20h, Bit [7:0] ,21h, Bit[1:0]

Type: Read/Write

Bits	Name	Defaults	Description
20H 7:0	ADC_CODE[9:2]	0	DAC code in ADC, can be manually set or automatically set by SAR ADC state machine. If ADC_ATUO is 0, user can write these two registers and read ADC_CMP status and do SAR manually
21H 1:0	ADC_CODE[1:0]	0	

L_SW_STS Register

Address: 22h, Bit [7:0]

Type: Read

Bits	Name	Defaults	Description
7:6	Reserved	0	
5	L_ICMP_1P8	0	L ISNS>1.8V comparator output This comparator is enabled if 16H EN_ICMP=1, or L_ISNS_AUTO=1
4	L_ICMP_0P6	0	L ISNS<0.6V This comparator is enabled if 16H EN_ICMP=1, or L_ISNS_AUTO=1
3:0	L_SCALE	1100	Refer definition of scale in L_ISNS_OCP register, the real scale L_ISNS_SCALE[3:2] to control switch Ron & current ratio. 00: Switch Ron 3.2, current ratio Iout/Isense=21:1 01: Switch Ron 0.4, current ratio Iout/Isense=161:1 11: Switch Ron 50m, current ratio Iout/Isense=1157:1 L_ISNS_SCALE[1:0] to control current sense R 00: 25k/2 01:25k/4 10: 25k/8 11:25k/16 Notes: Io=adc_dac*1.8/10'h3ff/N/R0*fsrc(Isrc)* (1157-14*step+Isns_trim*step), where R0=25kohm, step=18. For other current ratio, Io=adc_dac*1.8/10'h3ff/N/R0*fsrc(Isrc)* (1157-14*step+Isns_trim*step)/1157*ratio. N=1/2,1/4,1/8,1/16 based on L_ISNS_SCALE[1:0]

R_SW_STS Register

Address: 23h, Bit [7:0]

Type: Read

Bits	Name	Defaults	Description
7:6	Reserved	0	
5	R_ICMP_1P8	0	R ISNS>1.8V comparator output This comparator is enabled if 16H EN_ICMP=1, or R_ISNS_AUTO=1
4	R_ICMP_0P6	0	R ISNS<0.6V This comparator is enabled if 16H EN_ICMP=1, or R_ISNS_AUTO=1
3:0	R_SCALE	1100	Refer definition of scale in R_ISNS_OCP register，the real scale

			R_ISNS_SCALE[3:2] to control switch Ron & current ratio. 00: Switch Ron 3.2, current ratio Iout/Isense=21:1 01: Switch Ron 0.4, current ratio Iout/Isense=161:1 11: Switch Ron 50m, current ratio Iout/Isense=1157:1 R_ISNS_SCALE[1:0] to control current sense R 00: 25k/2 01:25k/4 10: 25k/8 11:25k/16 Notes: Io=adc_dac*1.8/10'h3ff/N/R0*fsrc(Isrc)* (1157-14*step+Isns_trim*step), where R0=25kohm, step=18. For other current ratio, Io=adc_dac*1.8/10'h3ff/N/R0*fsrc(Isrc)* (1157-14*step+Isns_trim*step)/1157*ratio. N=1/2,1/4,1/8,1/16 based on R_ISNS_SCALE[1:0]

FUSE Register

Address: 2Ah, Bit [7:0]

Type: Read

Bits	Name	Defaults	Description
7	Reserved	0	
6:5	SLV_ADDR[1:0]	0	SLAVE address OTP1, OTP0
4	H or L SW	0	0: High_sw_on &Low_sw_on in SW_OPTION REG default 0 1: High_sw_on = bit4 & SLV_ADDR[0] Low_sw_on = bit4 & !SLV_ADDR[0]
3:0	ADC_OFFSET	0	ADC Offset 4 bits original code, Final adc code need add this offset.

CMD_TOG Register

Address: 2Bh, Bit [7:0]

Type: Read

Bits	Name	Defaults	Description
7:2	CMD_TOG[7:2]	0	
1:0	Reserved	0	

VMC FSM Register

Address: 2Ch, Bit[7:0]

Type: Read

Bits	Name	Defaults	Description
7	Reserved	0	
6:4	I_BYTE[2:0]	0	Current Byte index of current VMC, from 0 to 4
3	VMC_PAUSE	0	0: VMC is not paused 1: VMC is paused because full (TX_BYTES=4) buffer of data tx done. Or write 1 to pause VMC state machine (Need read VMC_FSM to determine if it is in TX state)
2:0	VMC_CS[2:0]	0	000: IDLE 001: PRE_TX 010: PRE_RX 011: DATA 100: DATA_ACK 101: DONE

VMC STATUS Register

Address: 2Dh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	Reserved	0	
6:4	I_BYTES[2:0]	0	Current Byte index of current VMC, from 0 to 4
3	Rserved	0	
2:0	RX_BYTE[3:0]	0	Total bytes of current VMC, max 4 bytes in one frame VMC

VMC Option Register

Address: 2Eh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7:6	VMC_PIN[1:0]	00	00: DISABLE 01: VIN 10: VOUTL 11: VOUTR
5:4	TWAIT_TMR[1:0]	01	00: No expire 01:10ms 10:100ms 11:800ms VMC Master's RX wait time after transmission
3:2	TX_FREQ[1:0]	00	00:Reserved 01:80us 10:320us 11:640us
1	ACK_RST	0	0: TWAIT_TMR is not reset during DATA_ACK state 1: TWAIT_TMR is reset during DATA_ACK state
0	M/S	0/1	0: Master (TX out from VOUTL or VOUTR) as YHM4002A default 1: Slave (TX out from VIN) as YHM4001A default

VMC Ctrl Register

Address: 2Fh, Bit[7:0]

Type: Read/Write

Bits	Name	Defaults	Description
7	Reserved	0	
6:4	TX_BYTES[2:0]	0	Total bytes of current VMC, max 4 bytes in one frame VMC To TX more than 3 Bytes continuous, need set TX_BYTES=4 for each VMC data pack, for final pack set TX_BYTES=N%4 to stop VMC. As I^2C is faster than VMC, I^2C should polls I_BYTE, if I_BYTE>=2, then it can write data to BUF0~BUF1, if I_BYTE<2 then write data to BUF2~BUF3.
3	IGNORE_ERR	0	0: Quit Transaction and VMC Fail while Parity Error Three times. 1: Ignore Parity Error
2	AUTO_PAUSE	1	0: VMC use interrupt to transfer data. 1: VMC auto pause to wait I2C to R/W buffer data & tx_bytes, rx_bytes Every time VMC TX transmits a full size buffer, VMC_PAUSE bit will be high and SOC can read or write buffer data, then write VMC_PAUSE to 0 to resume VMC
1	RX_EN	0	0: RX is disabled 1: RX is enabled
0	TX_EN	0	0: TX is disabled 1: TX is enabled

TX/RX Data Register

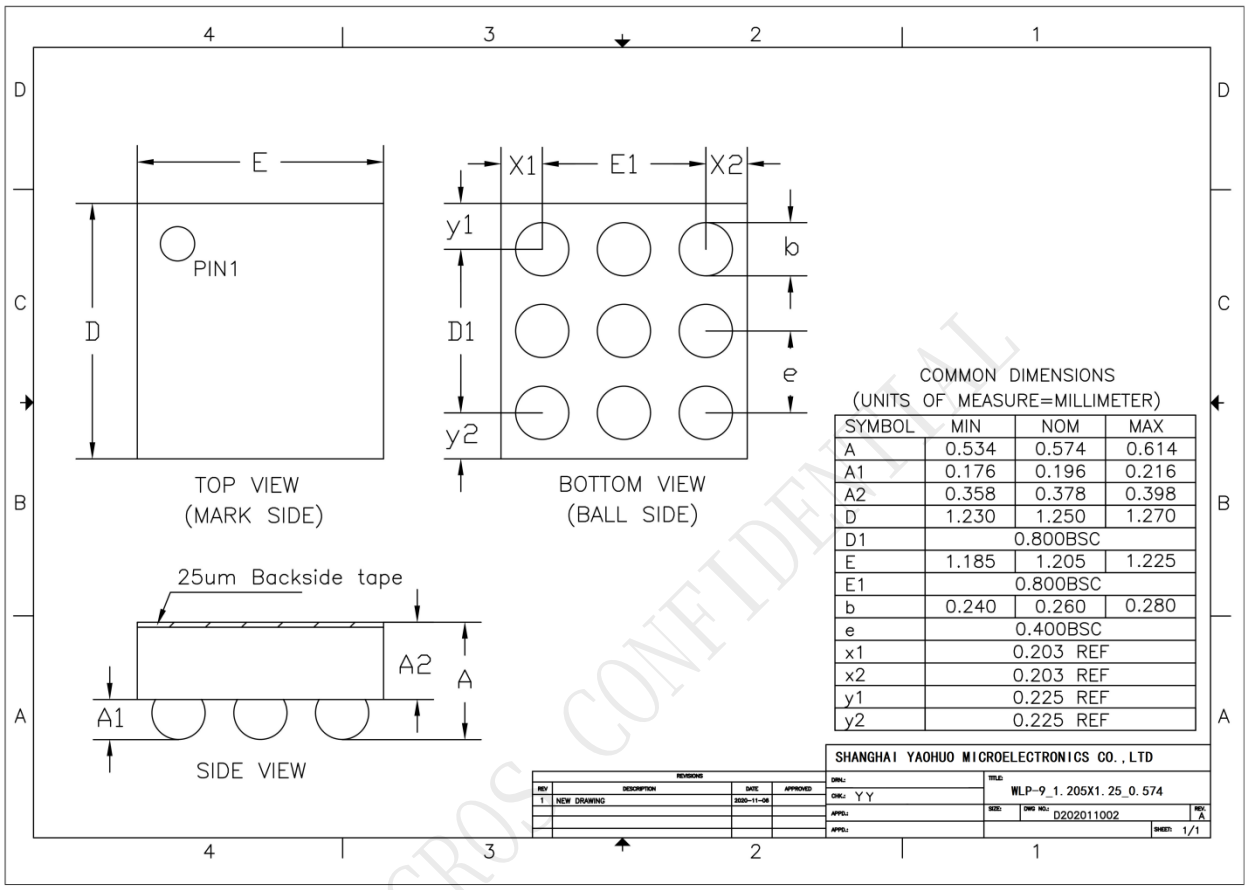
Address: 30h~33h

Type: Read/Write

Bits	Name	Defaults	Description
30h 7:0	R/TX0	0	Transmit Data Byte 0-3
31h 7:0	R/TX1	0	
32h 7:0	R/TX2	0	
33h 7:0	R/TX3	0	

Package Dimensions

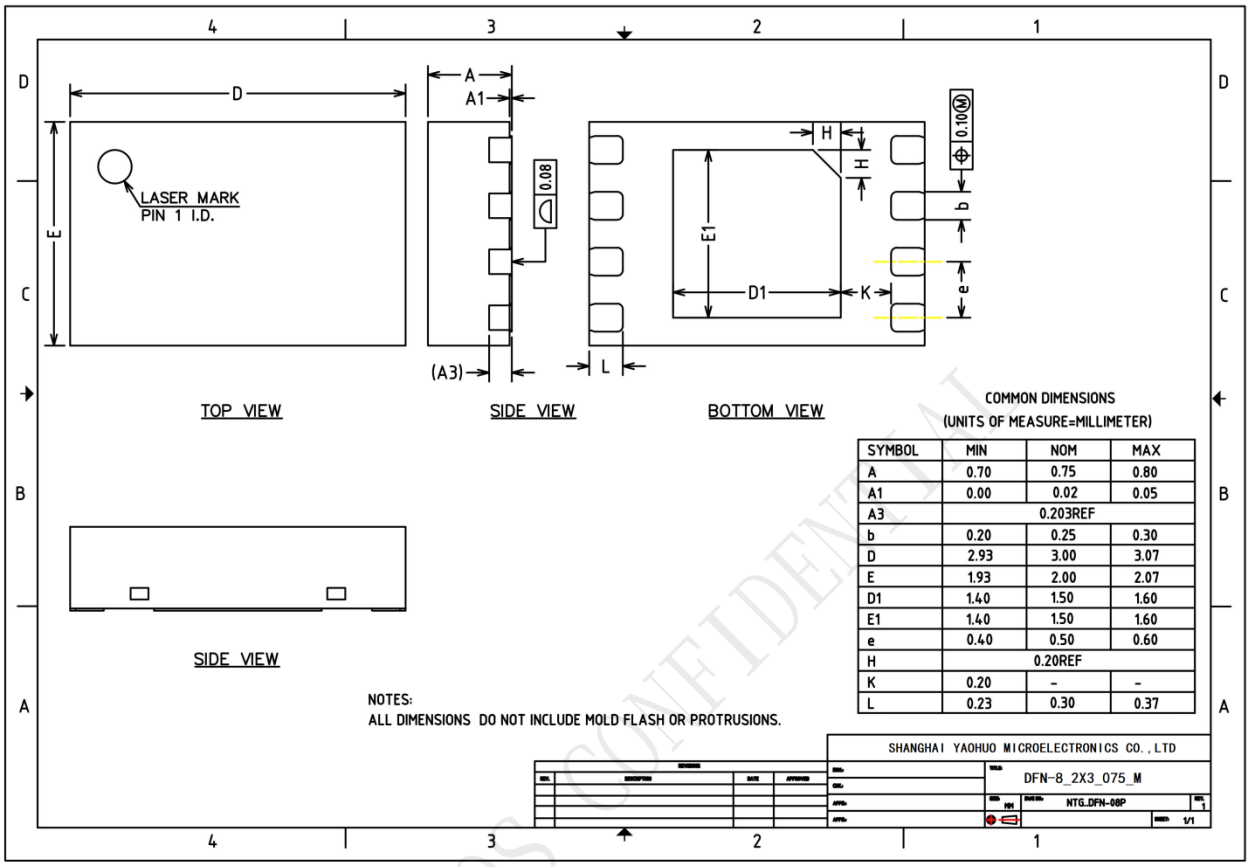
WLCSP-9 1.205x1.25x0.574



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.534	0.574	0.614
A1	0.176	0.196	0.216
A2	0.358	0.378	0.398
D	1.230	1.250	1.270
D1		0.800BSC	
E	1.185	1.205	1.225
E1		0.800BSC	
b	0.240	0.260	0.280
e		0.400BSC	
x1		0.203 REF	
x2		0.203 REF	
y1		0.225 REF	
y2		0.225 REF	

DFN-8 2mmx3mmx0.75mm



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.20	0.25	0.30
D	2.93	3.00	3.07
E	1.93	2.00	2.07
D1	1.40	1.50	1.60
E1	1.40	1.50	1.60
e	0.40	0.50	0.60
H		0.20REF	
K	0.20	-	-
L	0.23	0.30	0.37

Ordering Information

Part Number	Temp Range	Pin Package	Top Mark	MOQ
YHM4001AW9T	-40°C to 85°C	9 WLCSP	YH41 YYWW LOTI	3000
YHM4002AW9T	-40°C to 85°C	9 WLCSP	YH42 YYWW LOTID	3000
YHM4002AD8T	-40°C to 85°C	8 DFN	YH4002 YYWW	3000

T = Tape and reel.
YYWW: Date Code. YY = year, WW = week.
LOTI: The last three number of LOTID.