DATA SHEET

SUNPLUS

SPG290A

32-bit Video Console

Preliminary

OCT. 6, 2004

Version 0.1

32-BIT VIDEO CONSOLE

1. GENERAL DESCRIPTION

SPG290A, an SoC designed specifically for TV game and handheld game products, is composed of *S*$^{+}$*core*â (a 32-bit CPU developed by SUNPLUS Technology), Picture Processing Unit (PPU), Sound Processing Unit (SPU) and other primary functions for video game and ELA applications. SPG290A is able to generate graphics and sound for the television system (NTSC or PAL) and LCD. SPG290A features the integrated CD servo circuit for reading CD contents. With the ability to access CD titles, the huge amount of data for generating gorgeous video images and pleasing sound can be stored on the disc. SD card and NAND-type flash are also supported for mass data storage. The operating voltage supply range is 2.7V through 3.6V and CPU speed is 27~135 MHz. Plus, it offers 16 dedicated general purpose I/O, six 16-bit timers, 32768Hz Real Time Clock, built-in voltage regulator, Low Voltage Detect, Low Voltage Reset, 12-bit ADC, UART interface, SPI interface, SIO interface, ^{2}IC master interface and many other features that facilitate connecting with varieties of I/O devices such as TFT LCD, color STN LCD, CMOS image sensor, TV decoder, Light Pen, Touch panel…etc. The SPG290A provides not only the latest video game technology, but also the full service and support of SUNPLUS.

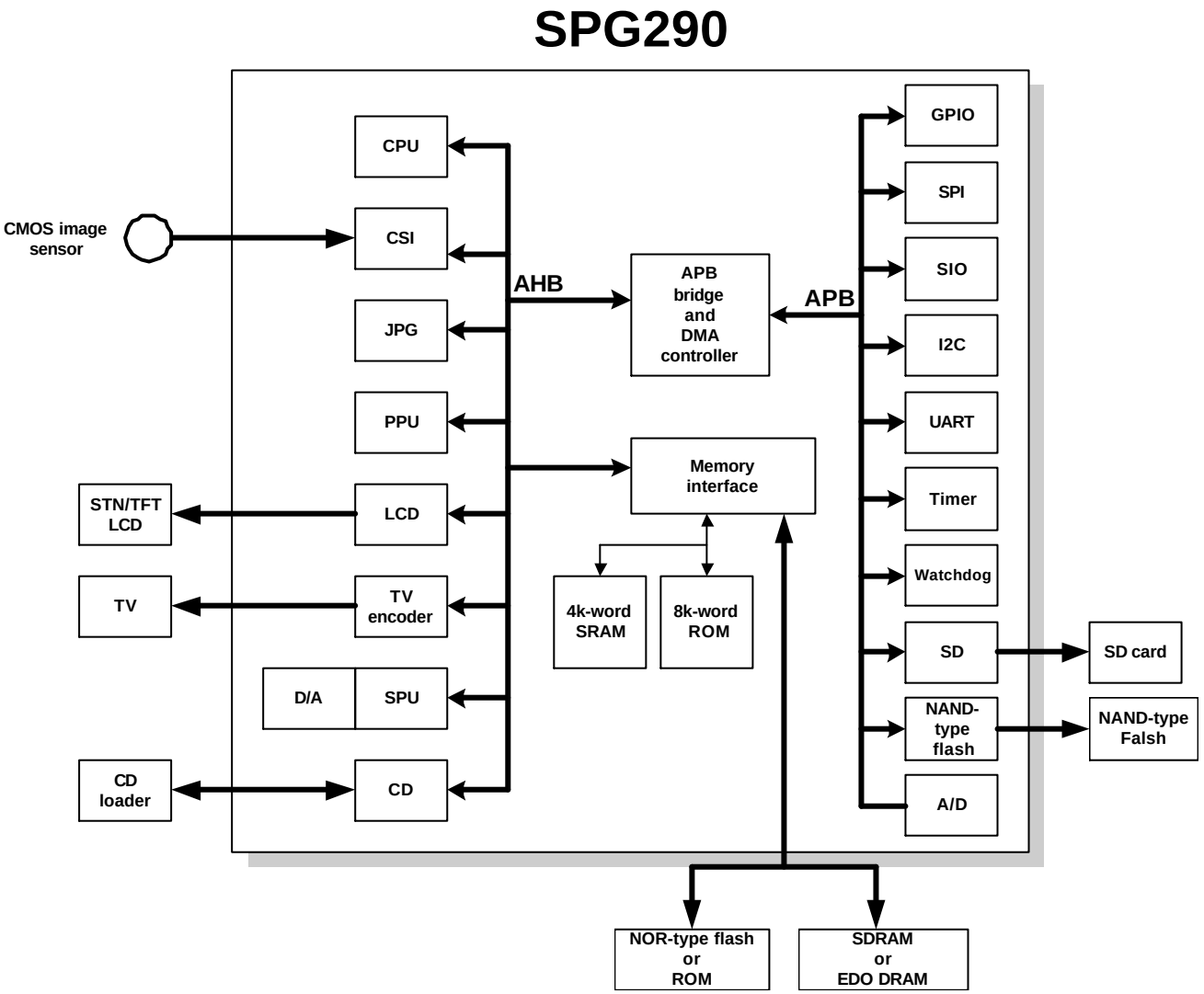
2. APPLICATION FIELD

- TV game product
- Handheld game product
- Education learn aids
- Karaoke product

3. FEATURES

- Operating Voltage: VDD is 2.7V ~ 3.6V (core voltage is 1.8V)
- CPU speed: 27 ~ 135 MHz
- Supports SDR DRAM and EDO DRAM with capacity up to 16 Mbytes
- Supports 16-bit or 8-bit DRAM data bus
- Maximum 64M x32 memory space(256 Mbytes)
- Integrated CD servo: supports CD-DA, CD-ROM, CD-ROM/XA, and CD-I
- Supports interlace/non-interlace NTSC/PAL composite video output
- Graphic resolution: VGA(640 pixels x 480 pixels) and CIF(320 pixels x 240 pixels)
- Supports 65536 colors(R/G/B is 5/6/5 format)
- Programmable 4/16/64/256/32768/65536 color mode
- 3 layer texts with size 1024 pixels x 512 pixels
- Provides character and pixel graphic operation modes
- Maximum 512 pieces of sprite are available
- Supports different size of character for sprite and text
- Hardware Horizontal / Vertical Flip function
- Provide blending control
- Provides 4-channel DMA: source and destination can be any region in the memory space
- Supports vertical blanking, any position, DMA end IRQ sources
- Provide 24 PCM/ADPCM sound channels
- Automatically volume control function (Compressor)
- Built-in 4-band digital equalizer
- Two 16-bit high speed DACs for stereo sound quality
- Fully ADSR envelope control
- PPU and SPU addressing are not limited by bank (64K)
- 2 programmable built-in PLLs to provide system clocks
- Built-in configurable voltage regulator
- 6MHz crystal for NTSC/PAL system
- Real Time Clock (RTC): 32768Hz
- Six 16-bit timers/counters (Programmable and Auto Reload)
- 16 dedicated general purpose I/Os (to be finalized)
- 16 interrupt sources: SPU, PPU, Timer, Time-base, External Input, Key wakeup
- Key wake-up function
- 8 channels 12-bit AD converter with 9-bit accuracy
- UART: Universal Asynchronous Receiver and Transmitter
- SPI: Serial Peripheral Interface(master and slave)
- SIO: Sunplus Serial Input/Output Interface
- Built-in Watchdog function
- Light Pen interface
- TFT LCD interface
- STN LCD interface
- Support Sunplus CMOS image sensor interface to connect with Sunplus CMOS image sensor device
- Support CCIR-601/656 CMOS image sensor / TV decoder interface
- Supports SD card and NAND-type flash for data storage

4. BLOCK DIAGRAM



5. FUNCTIONAL DESCRIPTION

5.1. CPU

The SPG290A is equipped with *S+core â 7*, the latest 32-bit CPU developed by SUNPLUS, pronounced as *score-seven*. The S+core â 7 is a 32-bit RISC with Sunplus-owned instruction set architecture (ISA). The ISA has 32/16-bit hybrid instruction mode and parallel conditional execution for high code density, high performance and versatile application. The micro-architecture includes AMBA bus for SoC integration, coprocessor and custom engine interface for function flexibility, and SJTAG for efficient debugging and In-Circuit Emulation (ICE).

The S+core â 7 is a single issue, 7-pipeline stage, high performance and high speed 32-bit RISC. For SPG290A, S+core â 7 can run up to 135 MHz. It supports 4-KB two-way set associative I/D-cache and 4KB LIM/LDM (local instruction/data memory). The MMU (memory management unit) is also supported for RTOS. We also define two custom engine and three coprocessor interfaces for user defined function extension. The custom engine supports 32-bit sign/un-sign multiply and divider. The bus interface of the processor is compliance to the AHB v2.0 for easy integration into SoC implementation.

Up to sixty-three prioritized vector interrupts are supported for fast interrupt service. The high performance Sunplus-patented unaligned load/store and pre/post increment addressing instructions are provided for string copy or memory moving. The powerful bit operation instructions and branch instructions using the counter register as loop iteration counter are provided for control application, and sleep instruction is provided for low-power application

5.2. Memory Interface

5.2.1. External DRAM

The SPG290A can connectwith SDR DRAMs or EDO DRAMs, which are used for storing CPU program, video data, and audio data. The maximum addressing ability to DRAM is 16 Mbytes. 16-bit DRAM data bus can provide the higher bandwidth, but 8-bit data bus is also supported.

5.2.2. External ROM/NOR-type flash

The SPG290A can access the external ROM or NOR-type flash via the shared pin of DRA M interface. The external ROM or flash can be used to store the alternative boot program or the application program. The access speed of ROM/flash can be programmed to meet the ROM/flash specification.

5.2.3. SRAM

The embedded 4K-word SRAM is used as the working buffer for transmitting bulk data between CPU and peripheral blocks. It can also be accessed by the other functional blocks which have the AHB bus linked to the memory interface.

5.2.4. ROM

The embedded 8k-word ROM stores the default boot program for CPU. The memory interface decides which boot ROM to be accessed (embedded or external) by pin configuration. To protect the application program in the external ROM, the program code in the external ROM can be encrypted. In this case, the embedded ROM contains the key to decode the encrypted data., and the decoding process is done by hardware.

5.3. CD servo

SPG290A integrates CD servo block which contains the digital servo, the analog servo, and the RF circuit to control the CD loader and receive data from the laser pickup. The CD servo module writes the CD data to memory, and then these data are post-processed by CPU. Since the post-processing is accomplished by CPU, the data stream on the CD disc can be actually in any format. If the data is CD-DA, it can be routed to SPU(sound processing unit) directly for playing music without post-processing. If the data is CD-ROM, such as MP3 bitstream, CD servo will write the data to DRAM first, and then the data will be decoded by CPU into PCM data.

5.4. Timer

SPG290A provides six 16-bit timers. The operating clock of each timer can be selected from various clock sources, which can be 32768Hz clock from the external crystal, divided clocks of various frequencies from PLLs, and other external clock sources through GPIOs. When the timer overflows, a timeout signal is sent to the interrupt controller to generate a timer interrupt signal to CPU.

5.5. Interrupt Controller

The interrupt controller collects all interrupt signals from functional blocks and generates a vector interrupt to CPU. The vector interrupt has the configurable priority inside CPU. The current interrupt handling routine can set a register bit to enable another interrupt with higher priority before the current interrupt routine is completed.

5.6. Sleep, Wakeup and Watchdog

5.6.1. Sleep

After power on reset, CPU starts working until a sleep command is given. When a sleep signal is accepted, IC will turn off system clock (PLL) and enter sleep mode. After entering sleep, program counter will stop at the next address and will start to execute once wakeup activates.

5.6.2. Wakeup

Waking up from sleep mode requires a wakeup signal to turn on the system clock (PLL). At the same time, a wakeup IRQ is also generated. The IRQ signal leads CPU to complete the wakeup process as well as initialization. After wakeup interrupt completed, program counter will continue to execute the next command.

5.6.3. Watchdog

The purpose of watchdog is to monitor if system operates normally. Within a certain period, watchdog must be cleared. If the watchdog is not cleared for some reasons, CPU assumes the program has been running in an abnormal condition and therefore, CPU will reset the system to the initial state and start running the program all over again. Watchdog function can be removed by setting a register.

5.7. PLLs and System Clock

SPG290A is equipped with 2 PLLs, named PLL1 and PLL2. Both of them use the base frequency (6MHz), but pump to different frequencies. PLL1 pumps to the multiple of 27MHz. The divided clocks from PLL1 are the operating clock for CPU, CSI, PPU, SPU, TV encoder, LCD controller, and memory interface. PLL2 pumps to 33.8688MHz for the CD servo operation.

5.8. ADC (Analog to Digital Converter)

The *SPG290A* has a 12-bit ADC (Analog to Digital Converter) with 9-bit accuracy. The function of an A/D converter is to convert analog quality signal such as a voltage into a digital word. Eight ADC input ports are provided by *SPG290A*.

5.9. UART

UART block provides a standard asynchronous interface, built-in 8x8 bits receiving FIFO, full-duplex communication with other devices. The maximum baud-rate can be up to 921600bps. This function can be accomplished by using I/O PortC and INT(UART IRQ). The Rx and Tx of UART are shared with IOC5 and IOC6.

5.10. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) interface is a master and slave interface that enables synchronous serial communication with Motorola SPI-compatible peripherals. The SPI performs parallel-to-serial conversion on data written to an internal 8x8-bit transmit FIFO. It also performs serial-to-parallel conversion on the serial input data, and buffers it in a 8x8 bits receiving FIFO. The SPI asserts interrupts to request service to the transmitting FIFO and to the receiving FIFO, and to indicate an overrun condition in the receiving FIFO.

5.11. Sunplus Serial Input/Output Interface (SIO)

SIO (Serial Interface I/O) is Sunplus's proprietary serial interface, which can be used to communicate with other devices. This serial interface is capable of transmitting or receiving data via 2 pins, SCK and SDA.

5.11.1. SIO protocol

The SIO protocol is composed of start bit, read/write control bit, address word, data word, and stop bit. The figures below show the SIO protocol for the read and write mode respectively. If the SDA make a transition from 1 to 0 during the SCK is high, it stands for the "start bit" of the SIO transfer. If the SDA make a transition from 0 to 1 during the SCK is high, it means the "stop bit" occurred. In the SIO waveform other than the "start & stop bit", the SDA can only change its logic level during the SCK is low. User should note that the address word & data word are transmitted with MSB first. And if the data word is 16 bits in width, then the **low** byte is transmitted/received first.

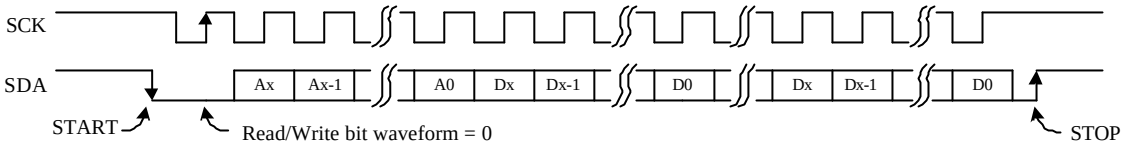
5.11.2. SIO Feature

The SIO interface supports the following features.

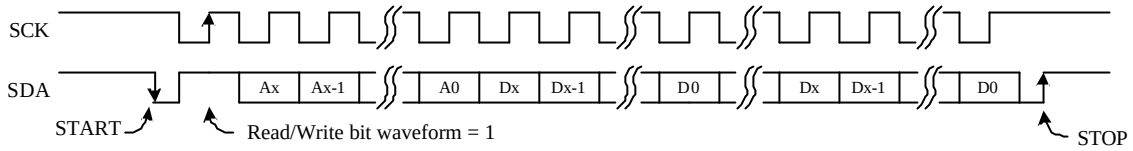
1. Support "master read" and "master write" function via SCK and SDA.
2. Support 4 address modes (No address, 8-bit address, 16-bit address, 24-bit address).
3. Support burst reading or writing function.
4. Support 8-bit and 16-bit data width.
5. Support interrupt and polling function.
6. Support 4 SIO baud rates.

Provide automatic bit-stream transmitting mode when communicating with SPDS301 IC.

SIO Write Mode:



SIO Read Mode :



5.12. Inter-IC Serial Interface (I^2C)

The SPG290 support I^2C master only and 3 types of transaction: 8 bits type, 16 bits type and 8 bits * n type. For 8 bits * n type transferring, each transaction is controlled by software and total number of transactions are variable. Hence, total number of transactions for 8 bits type R(W) are 4(3). The total number of transactions for 16 bits type R(W) are 5(4).

5.13. DMA controller

SPG290A provides Direct Memory Access (DMA) function to relieve CPU for data transfer between CPU and low-speed peripherals. CPU can set the DMA controller to initialize the data transfer between the embedded 4k-word SRAM and peripherals. For example, CPU writes data to the SRAM before activates the DMA transfer which moves data from SRAM to SD card. CPU can do other jobs when the data is written to SD card.

5.14. Picture Processing Unit

The size of a visible screen is 640 pixels (**H**orizontally) x 480 pixels (**V**ertically). In general, a screen consists of up to two **Text** layers and 512 **Sprites**. **Character,** a basic component for Text and Sprite, is a rectangular block in which vertical / horizontal size can be defined independently among 8, 16, 32, and 64 pixels. **Text** is a two dimensional array consisting of characters or horizontal lines. The size of a Text is 1024 pixels (H) x 512 pixels (V), which is capable of expressing a background picture. **Sprite,** a small picture (consisted of characters) to represent a roll in a game, can be placed anywhere on the screen and it is useful to express moving picture. Each picture component also involves a **Depth** parameter for expressing the top-bottom relation.

5.14.1. Text

Text Screen consists of a set of characters (character mode) or lines (bitmap mode). The characters within a text must be the same size. Each text contains the following parameters

(X,Y) position : define the text expressed area (-512~511)

Character Size: define the vertical/horizontal size of the characters in text

Vertical Size (pixel)	Horizontal Size (pixel)			
	8	16	32	64
8	8 x 8	8 x 16	8 x 32	8 x 64
16	16 x 8	16 x 16	16 x 32	16 x 64
32	32 x 8	32 x 16	32 x 32	32 x 64
64	64 x 8	64 x 16	64 x 32	64 x 64

Depth: define the layer depth of the text. Four depth layers are selected.

Flip: vertical/ horizontal flip control

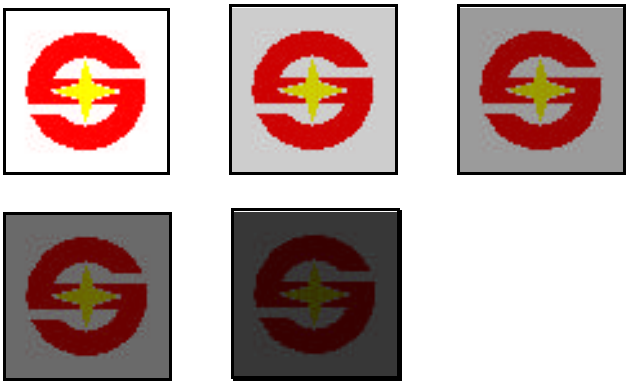
Color Mode: 4/16/64/256/32768/65536 colors mode are available.

5.14.2. Sprites

SPG290A provides 512 sprites. Each sprite consists of **X position** (–512~511 or 0~1023)**, Y position** (–512~511 or 0~1023), **depth** (4-layers), **palette**, **size** (16 kinds), **character number**, **flip** (horizontal/vertical), **blending**, and **color mode** (4/16/64/256 colors). These parameters are stored in the Sprite Memory that is able to be accessed directly by CPU.

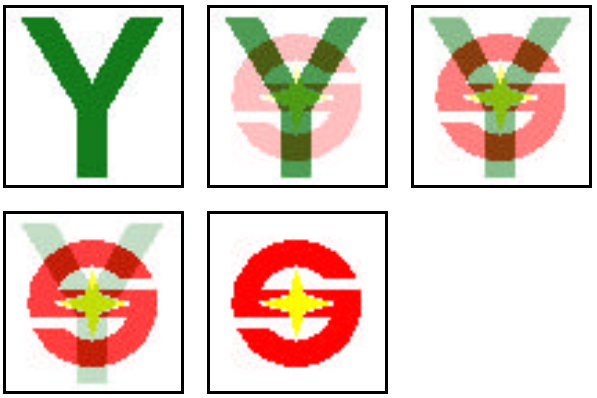
5.14.3. Fade Effect

Fade effect provides the fade-in and fade-out control. The Fade_offset value defines the fade-out level. In other words, the intensity of all pixels on the displayed area will be substrated with the Fade_offset. The following diagrams are the example of the fade effect. The right side diagram has the smaller Fade_offset value than those in the left side.



5.14.4. Blending Effect

Blending effect is used to mix two pictures as shown in the following figures. The text blending effect is controlled by the bit8 in $2813 and $2819. When the blending effect of a sprite or text is enabled, it will mix with the pixels that with the depth lower than it.



Four blending level can be selected by the Blend_level at port $282A. These four levels are shown in the above figures. The first one is of no blending effect, and the other four are the blending effects with different blending levels control.

5.14.5. Interrupt

There are three interrupt sources, **DMA Interrupt** (DMA_IRQ), **Vertical Blanking Interrupt** (BLK_IRQ) and **Video Timing Interrupt** (VDO_IRQ) in PPU. The DMA_IRQ is employed to detect at the end of the sprite DMA transferal. CPU is able to detect by enabling the DMA_IRQ. When the DMA_IRQ is enabled, the DMA_IRQ will be propagated to CPU through IRQ0. The BLK_IRQ occurs at the vertical blanking period in every frame. The BLK_IRQ will be cleared automatically at the end of the vertical blanking period if it's not cleared by CPU. VDO_IRQ is used to synchronized with the luster on TV screen. When the luster reaches the point defined by **VideoIRQVposition** and **VideoIRQHposition**, VDO_IRQ activates.

5.14.6. Color Palette

The Color Palette generates the Pixel color information. Color Palette is placed in the local memory in picture processor, and it stores parameters for 256 colors. Pixel color is expressed by **Red** (32 levels), **Green** (64 levels) and **Blue** (32 levels) in Color Palette. Color Palette Memory is a look up table that translates the pixel number into the physical color information. There are 256 colors stored in the Color Palette Memory, and each contains the **red** (5 bits), **green** (6 bits) and **blue** (5 bits). Any color in the color palette can be assigned as transparent color, i.e. 256 transparent colors are available in *SPG290A*

5.15. Sound Processing Unit

Sound processing unit(SPU) in *SPG290A* provides the 24 stereo PCM or ADPCM channels. It is able to simulate all types of musical instruments by programming the tone memory and controlling the envelope slope for each channel. PCM method is easy to process and high quality but requires large size of memory. In *SPG290A*, ADPCM method requires less memory with little loss of tone quality.

To avoid that output signal exceeds the maximum range (saturate), the compressor can properly increase the overall volume without saturation, so the sound quality is obtained. The internal digital equalizer has 4bands, the gain and cut-off frequency of each band can be adjusted individually.

5.15.1. Features

1). 8-bits /16-bits (software mode) stereo PCM
2). Built-in 4-bits ADPCM hardware decoder each channels
3). 7 bits Main volume control
4). MIDI Format Gain control for each R/L channel of 24 channels
5). Max. 256 piece-wise slope with repeat for envelope control
6). 24-channel IRQ functions and Beat event IRQ and Envelope IRQ
7). The Tone-Color & envelope can be controlled by hardware or manual (software) mode respectively
8). Automatic tone-color interpolation function
9). Max. 281.25KHz tone-color sampling rate
10). Note-Off Release control
11). Channel Ramp-Down function for each channel
12). Channel Pitch Band function
13). Automatically volume control function (Compressor)
14). 4-bands digital equalizer

5.16. CMOS Image Sensor Interface

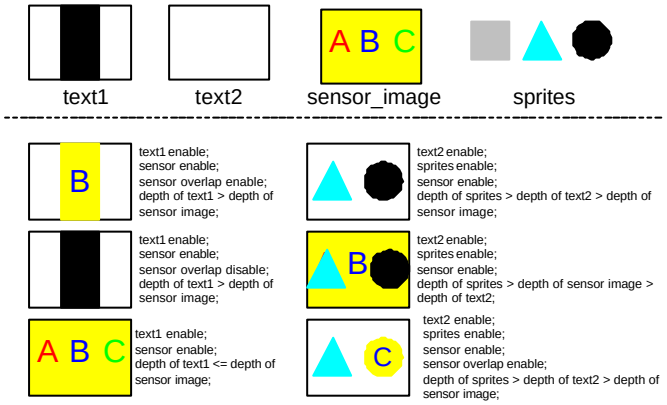
SPG290 supports several interfaces: Sunplus CMOS sensor interface (CIF), CCIR601 / CCIR656, and sensor master interface (QVGA / VGA). In addition, SPG290 also supports several functions, the major functions are: blending, overlap, blue screen effect, capture, De-saturation, Halftone, and motion detect.

Color mode

Gray mode

5.16.1. Sensor overlapped

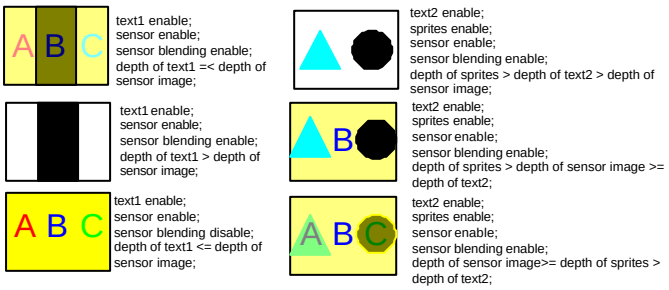
When SENSOR is enabled, the PPU layer with the color {R, G, B}={0,0,0} would be treated as the transparent color. If the depth of PPU layer is greater than the SENSOR layer's, the overlapped image would be the PPU layer.



Notes:
The color of black area in the text1 and sprites is R=0,G=0 and B=0;

5.16.2. SENSOR Blending Effect

SENSOR layer can be blended with the PPU layer with smaller depth than SENSOR_DEPTH when the SENSOR is enabled.

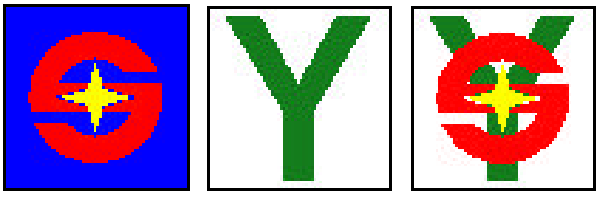


5.16.3. SENSOR De-saturate Effect

This effect is used to de-saturate the SENSOR layer or the PPU layer. If the de-saturate effect is enabled, the layer would be translated into the 128 gray levels instead of colors. SENSOR layer and PPU layer De-Saturation can be controlled independently.

5.16.4. SENSOR Blue Screen Effect

SENSOR blue screen effect is used to set the transparent color of the SENSOR image data. When the SENSOR pixel is transparent, the pixel color with a lower depth would be displayed, which is the same as the transparent color described in the **Color Palette** section. If blue screen effect is taken, the pixel would be treated as transparent. In the following example, we set the blue color in the SESOR layer as the transparent color. The value of the SR_BLUETOP and SR_BLUEBTM depends on the lighting of the environment and the sensor uniformity. In the following section, we provide a protocol to read the pixel data for the user to find the candidate value of SR_BLUETOP and SR_BLUEBTM.



SENSOR layer PPU layer Display Layer

5.16.5. Motion detect function

The SPG290 supports simple recognition function called Motion Detect. There are 2 types: one type contains 300 detect samples, another contains 1200 detect samples. For each referring frame, the comparison result of each sample pixel is calculated and stored concurrently in the working RAM. The different bit is calculated by the following equation:

DIFF bit = |Ynew [7:0] – Yold [7:0]| / 2 >= DIFFY_THRESHOLD [6:0]

5.16.6. SENSOR Frame Capture

The SENSOR frame capture function is able to capture a sensor image as a photograph. The capture operation is started at the coming end of vertical blanking. And it would be held for the whole frame or field. The SENSOR captured image would be stored in the external DRAM.

5.17. TFT LCD Interface

The built-in TFT LCD interface supports multiple TFT LCD panel input format, such as DataEnable(DE) mode, Hsync/Vsync mode, 15-bit parallel RGB mode, 8-bit delta RGB mode and CCIR601/656 mode etc., which with resolution 320(H) X 240(V) and NTSC/PAL formats. The configurable position and width of synchronous signal can fit various TFT LCD panel specifications.

5.18. STN LCD Controller

The *SPG290A* contains an STN LCD controller, which can support configurable resolution up to 320(H) X 240(V). The STN LCD controller supports 16 gray levels for monochrome STN or 64/125/4096 colors STRIPE/MOSAIC type color STN. Besides, the interface supports flexible 1-bit, 4-bit or 8-bit data interface to connect to different LCD panels.