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학번 :

이름 :

점수 :

[1] A 1-bit multi-purpose function unit is specified as below function table. There are three control signals, C0, C1, and C2, two data inputs, A and B, and one output. Design this function unit by using a 8:1 multiplexer and some gates. (10pts)

C0	C1	C2	Function	Comments
0	0	0	1	always 1
0	0	1	$A + B$	logical OR
0	1	0	$(A \bullet B)'$	logical NAND
0	1	1	$A \text{ xor } B$	logical xor
1	0	0	$A \text{ xnor } B$	logical xnor
1	0	1	$A \bullet B$	logical AND
1	1	0	$(A + B)'$	logical NOR
1	1	1	0	always 0

[3] Design a 4-bit BCD/binary adder circuit that can perform either BCD or binary addition under the control signal of a mode setting, M. If M=0, the circuit's outputs implement binary addition. If M=1, the outputs are BCD addition. Consider a 4-bit ripple carry adder structure. (20 pts)

[2] In two's complement numbering system, for any given n -bit positive number, N , its two's complement, denoted by N^* , can be represented as $N^* = 2^n - N$. When performing $(6-3)$ and $(-2)+(-5)$, we can obtain the correct result if we simply ignore the carry-out bit. Prove why this is true in mathematical analysis. (15 pts)

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[4] First, for the RS-Latch, explain when and why racing condition occurs. Second, for the master-slave RS-FF, show the waveform example showing one's catching problem, and explain why it occurs. (10 pts)

(2) Obtain encoded state transition table and minimized equations.

[5] Our vending machine will release a chewing gum after 15 cents are deposited. There is a single coin slot to insert only dimes and nickles. Also no change is returned when more than 15 cents are deposited. (20 pts)

(1) Obtain its state diagram by using Moore machine.

[6] Design a 4-bit Johnson counter which can count a sequence of 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001 states. Answer the

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following questions. (25 pts)

(1) Derive its state diagram and state transition table.

(3) Check whether this is a self starting counter or not. If not, design a self starting counter circuit by showing state diagram and its state transition table.

(2) Obtain its minimized state equation and design its circuit by using D-FFs and some gates.