[1] Simplify the following equation, X=(A,B,C) = A'B'C' + A'B'C + AB'C' + AB'C + ABC' + ABC. (10 pts)

[2] Obtain the complement of F(A,B,C,D). (10 pts)

F(A,B,C,D) = [A + (BCD)' ][(AD)' + B'(C' + ABD')]

[3] By using K-map method, find the minimized product-of-sums expression for f(A,B,C,D) = ∑ m(1,3,5,7,9) + ∑ d(6.12.13) (10 pts)

[3] Consider a 2-bit combinational divider. This has two 2-bit inputs, such as AB and CD, and generates two 2-bit outputs, quotient W,X, and the remainder Y, Z. Divide by zero is not allowed and thus considered as don't care state. Answer the following questions. (20 pts)

(1) Obtain the truth table for W, X, Y, and Z.

(2) Obtain the minimum sum of product from K-map for X.

[4] Obtain the minimum sum of product by using 5-variable K-map, F(A,B,C,D,E) = ∑m(2,5,10,13,15,17,19,21,23,24,29 31) + ∑d(7,8) (10 pts)

[5] Draw schematic diagram for this equation, Z = (A + (BC))(C' +D), by using NOR-only network. (10 pts)

[6] For this function, F(A,B,C,D) = ∑ m(0,2,4,5,6,7,13,15), describe static one hazard situation and obtain the minimum sum of product equation to remove this hazard. (10 pts)

[7] For this function, F(A,B,C,D) = B'CD + ABC', design this circuit by using a 4:1 Multiplexer and smallest number of logic gates. (10pts)

[8] Inverting tri-state buffer (input I, control signal OE', output T) is constructed as following figure. Show its operation by using a table and then design 2:1 MUX using this component. (10 pts)