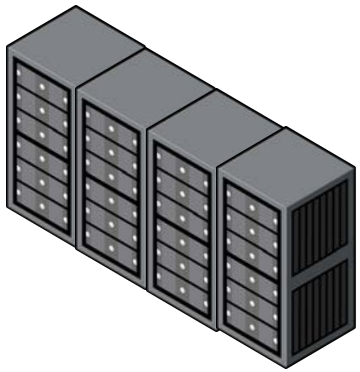
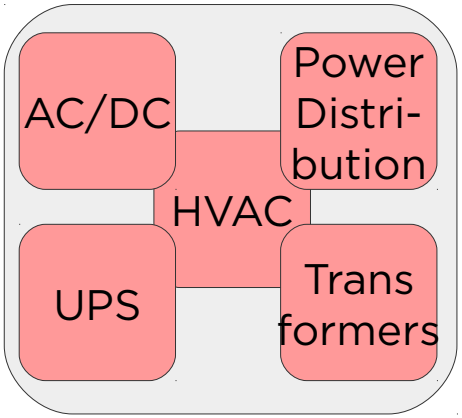
Power Capping
what works, what does not

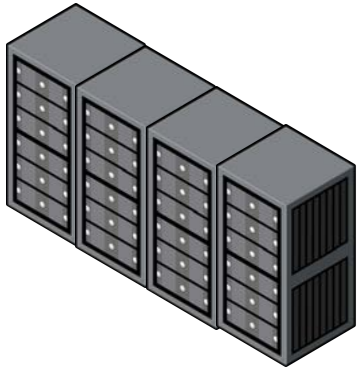
Pavlos Petoumenos
Lev Mukhanov, Zheng Wang
Hugh Leather, Dimitrios S. Nikolopoulos

Data center



Data center





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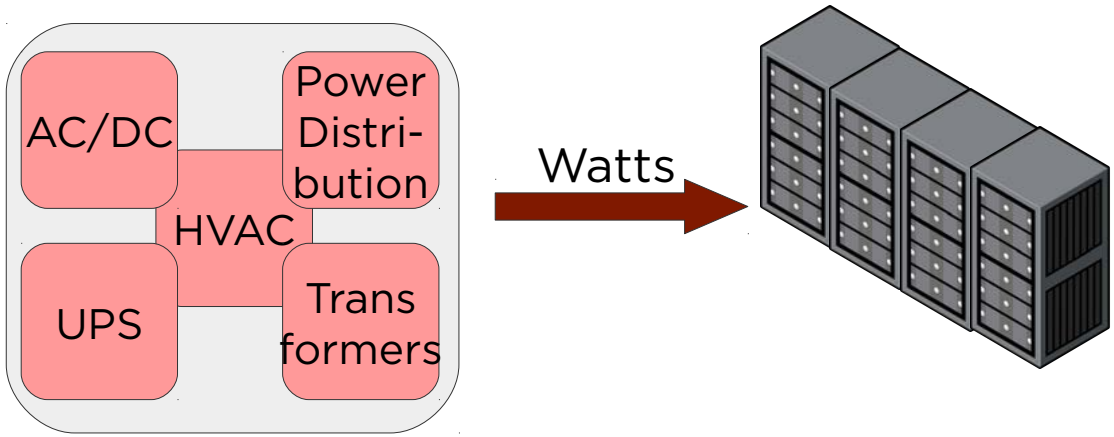

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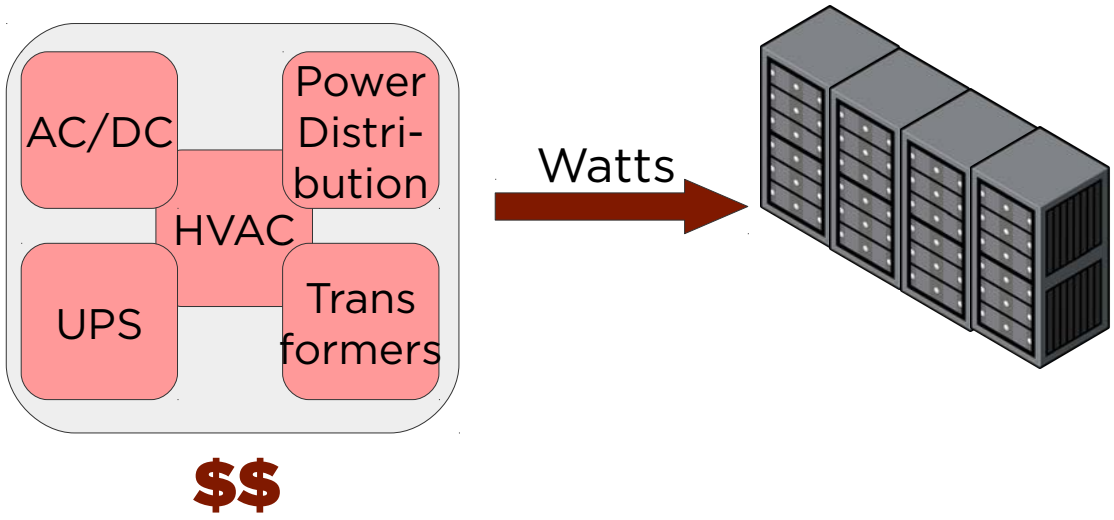

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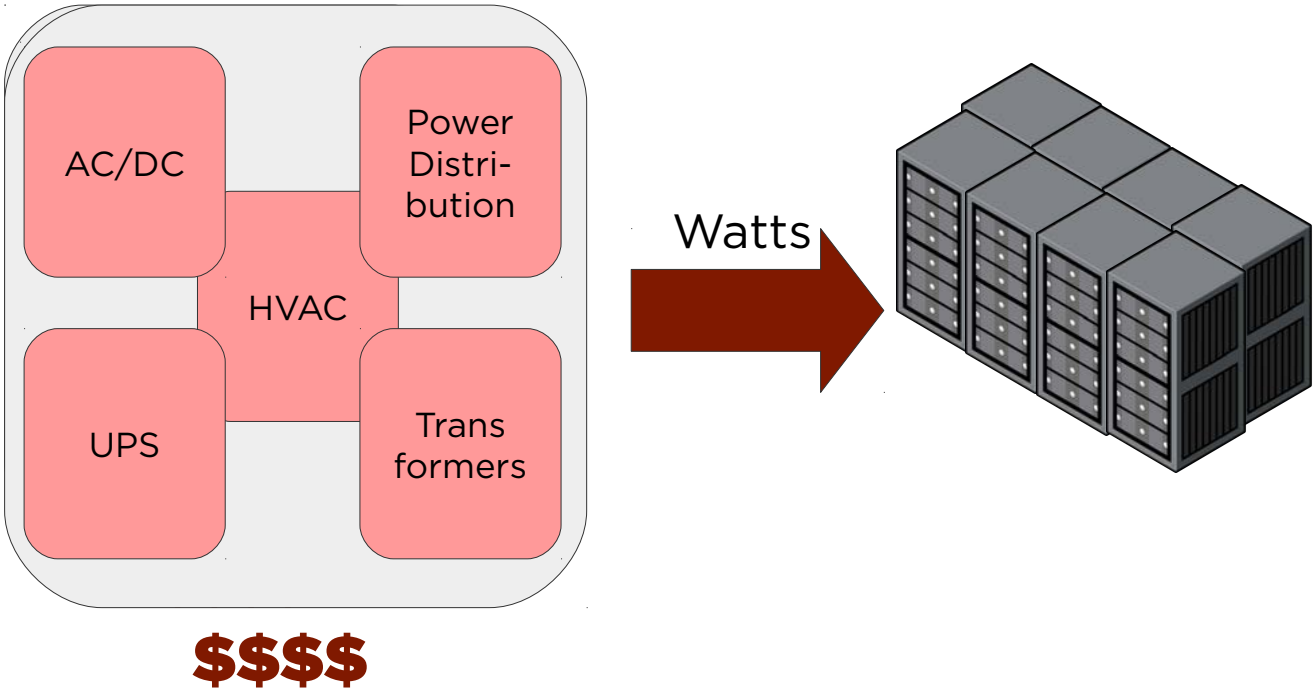

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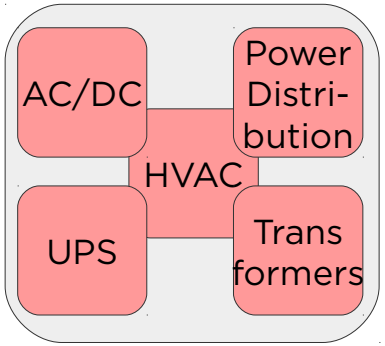
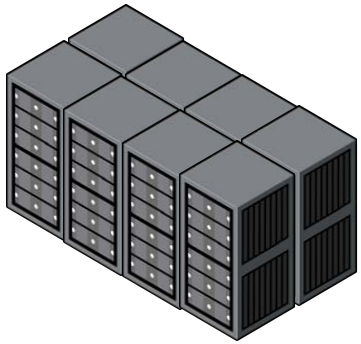
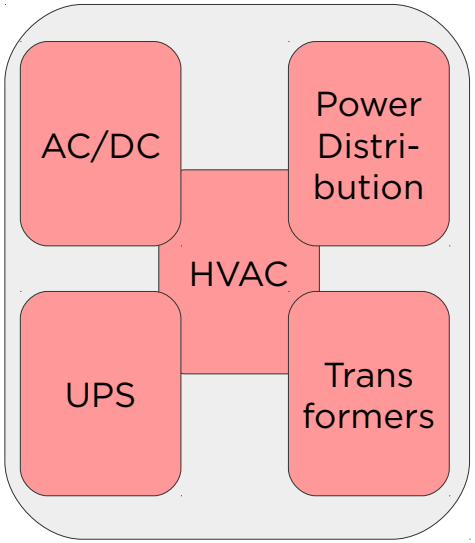
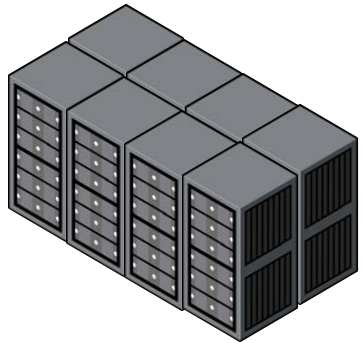

AC/DC
Power Distri-bution
HVAC
UPS
Trans formers

$$




AC/DC
Power Distri-bution
HVAC
UPS
Trans formers

$$$$



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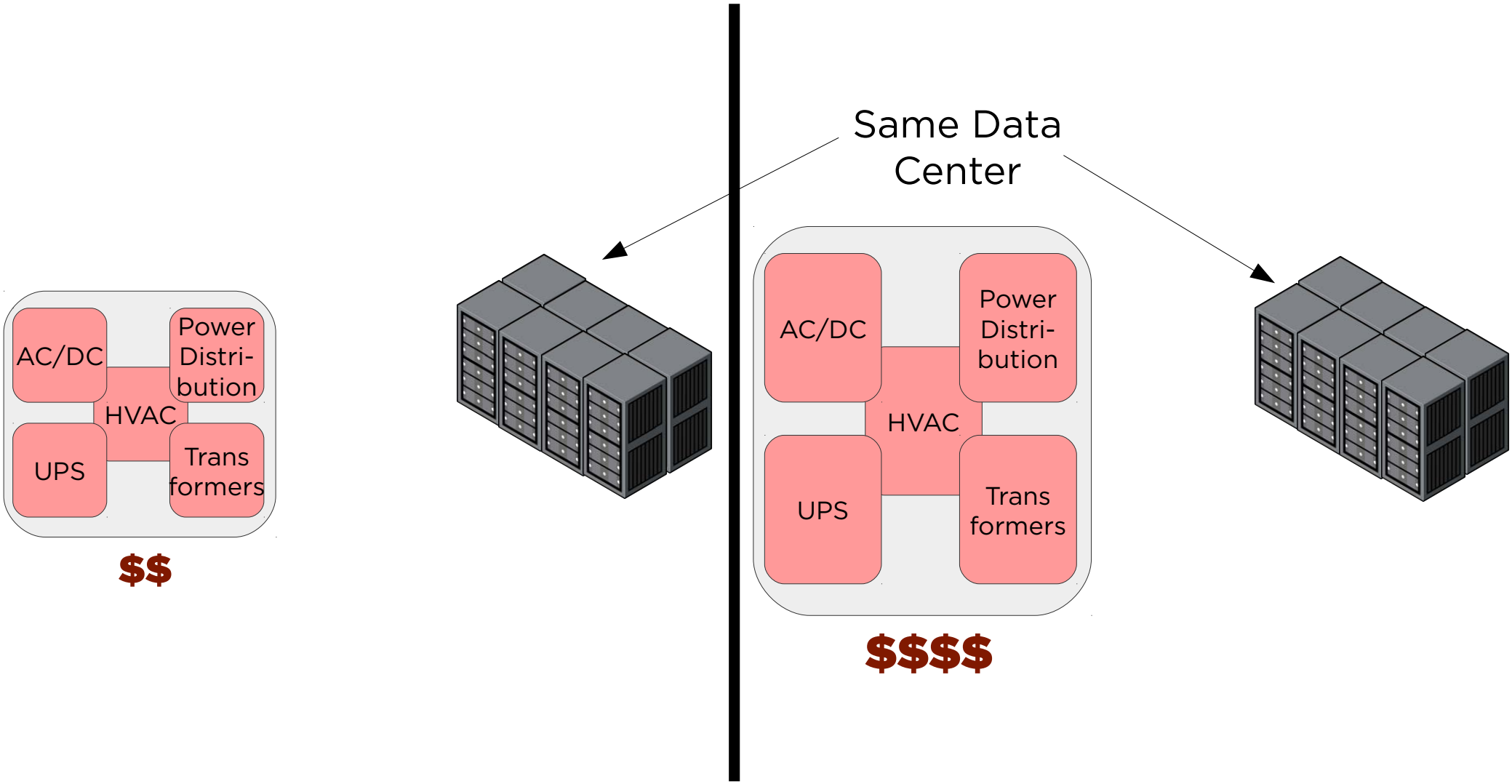
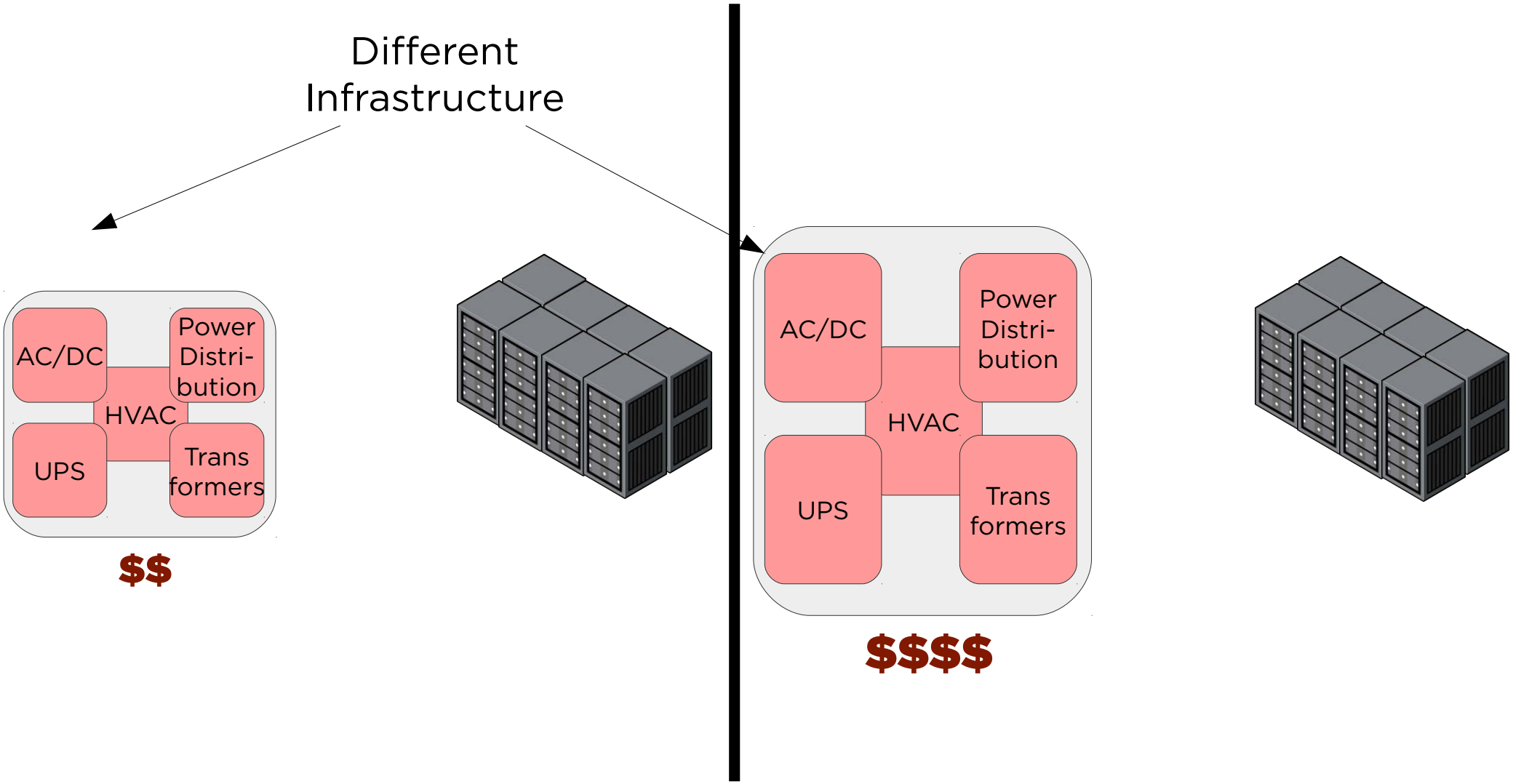
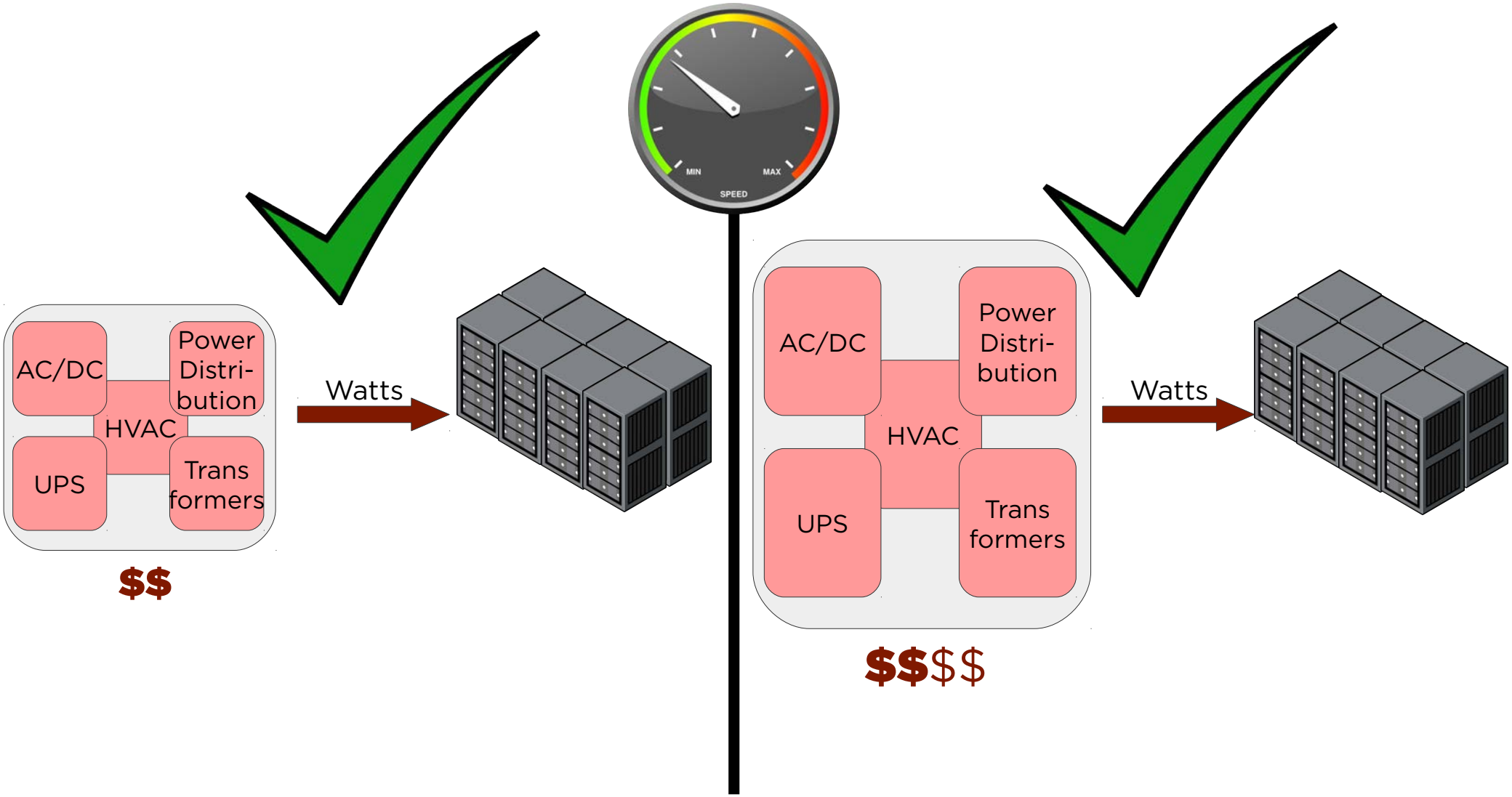

Same Data Center
AC/DC
Power Distri-bution
HVAC
UPS
Trans formers
$$
AC/DC
Power Distri-bution
HVAC
UPS
Trans formers
$$$$

Data center


Different
Infrastructure
AC/DC
Power Distri-bution
HVAC
UPS
Trans formers
$$
AC/DC
Power Distri-bution
HVAC
UPS
Trans formers
$$$$

Data center


MIN
MAX
SPEED
AC/DC
Power Distri-bution
HVAC
UPS
Trans formers
Watts
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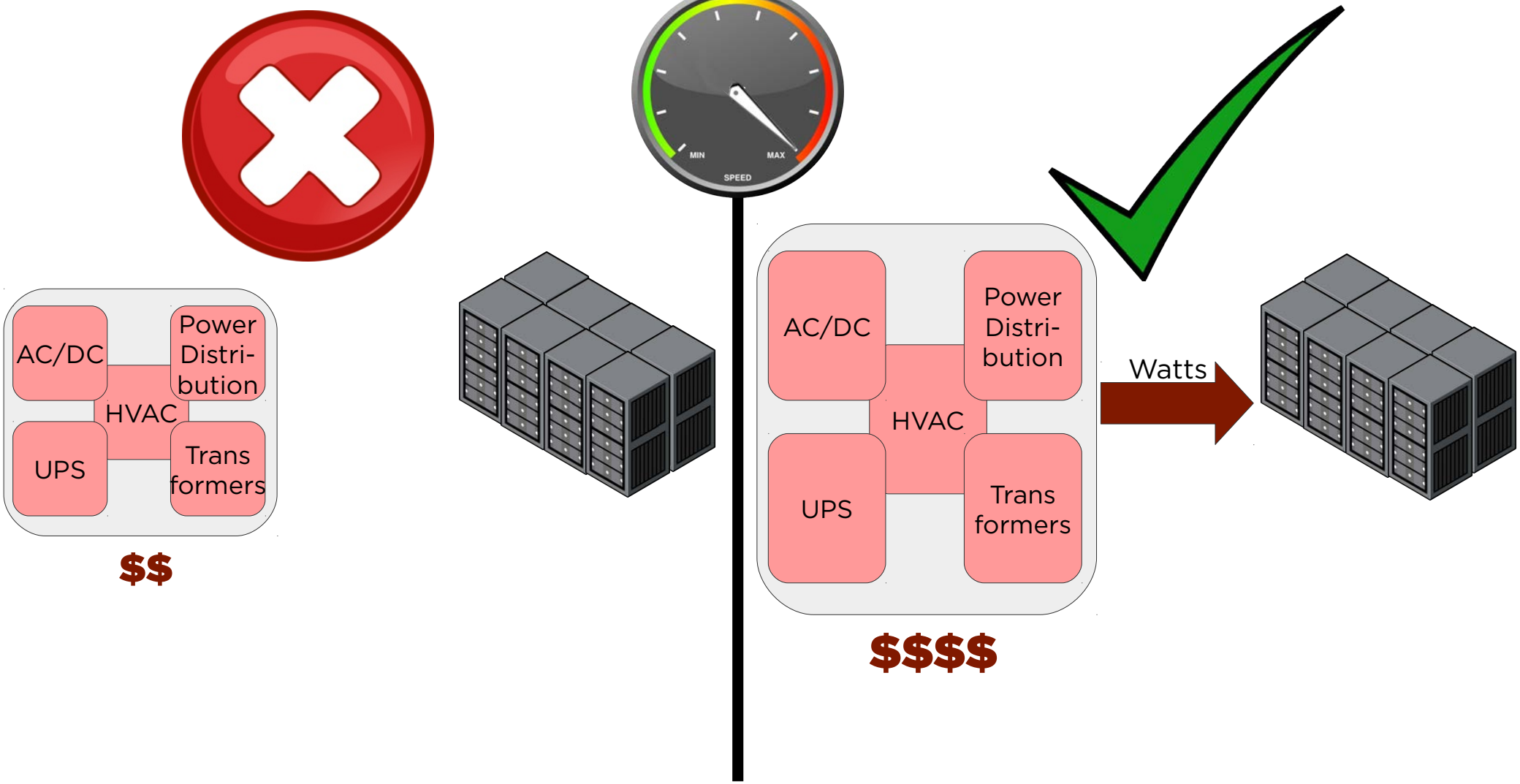
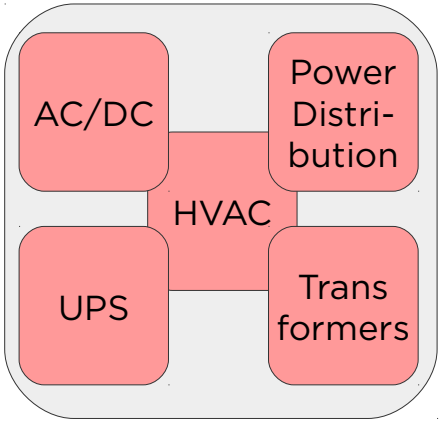
AC/DC
Power Distri-bution
HVAC
UPS
Trans formers
Watts
$$$$

Data center


MIN
MAX
SPEED
AC/DC
Power Distri-bution
HVAC
UPS
Trans formers
$$
AC/DC
Power Distri-bution
HVAC
UPS
Trans formers
$$$$
Watts

Power Capping



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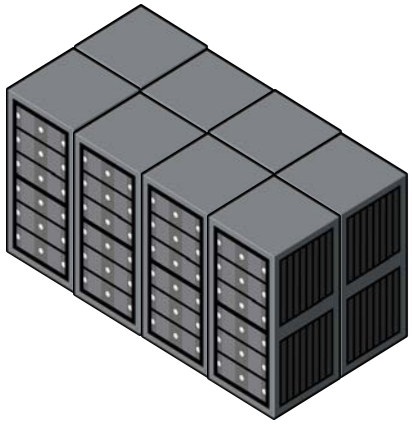
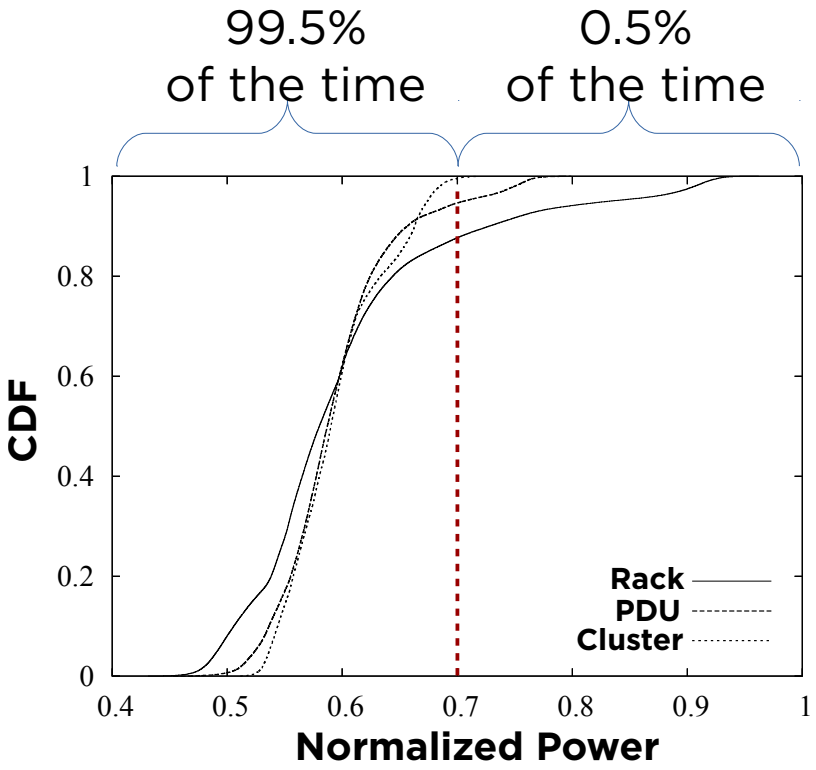
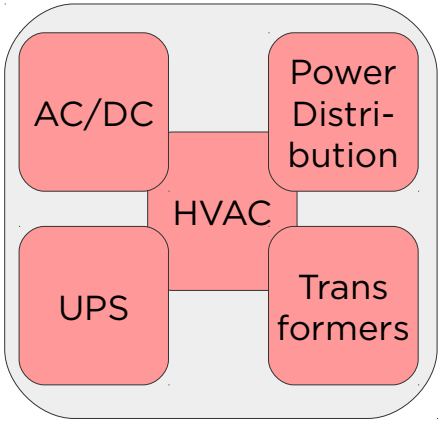


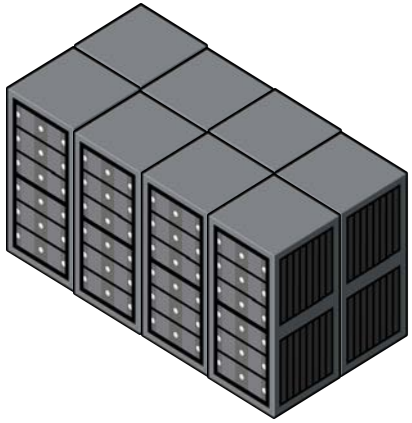


Fan et al. Power provisioning for a warehouse-sized computer. ISCA '07

Power Capping



Watts



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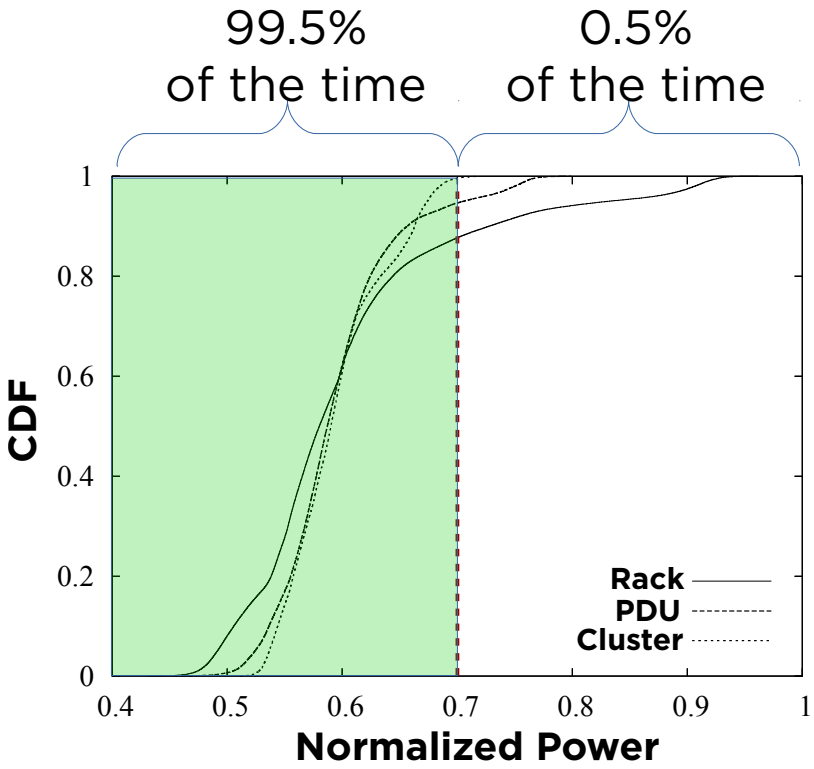

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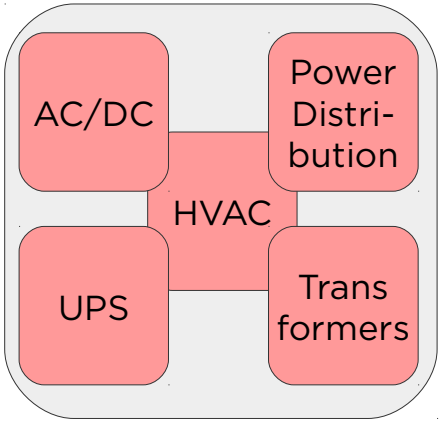
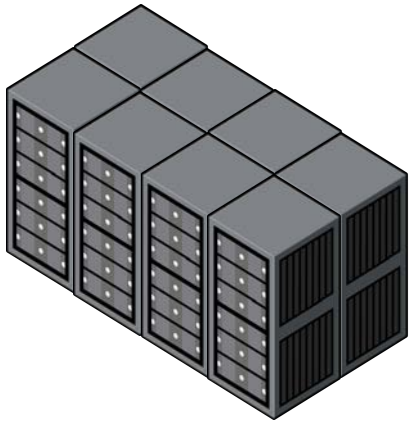
Power Capping



Watts



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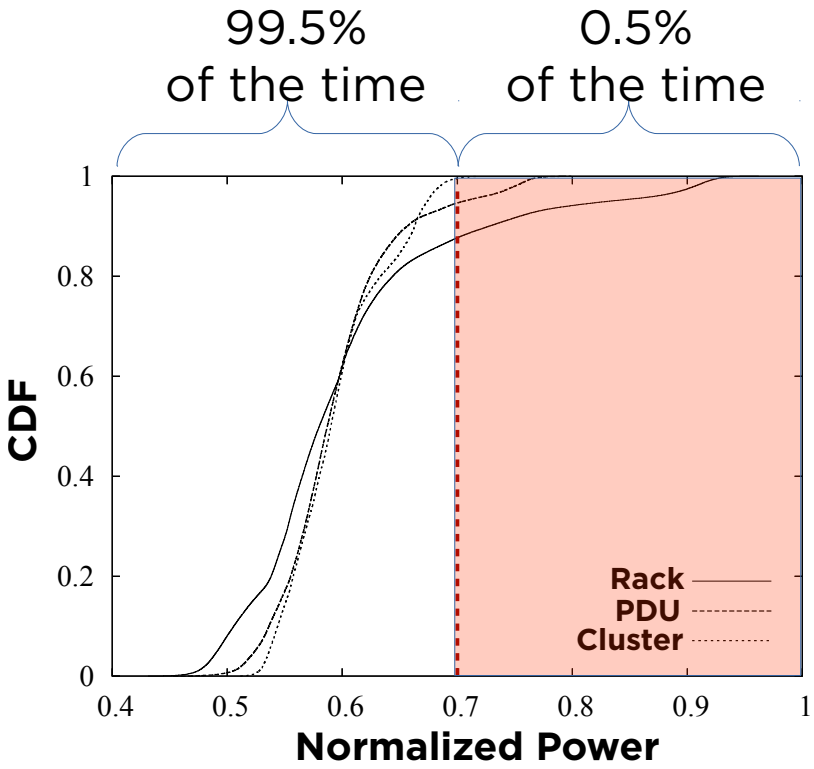

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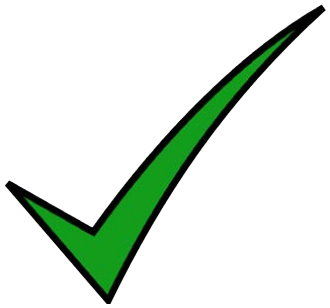
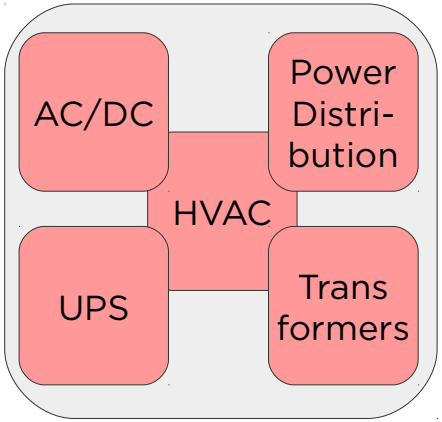
Power Capping





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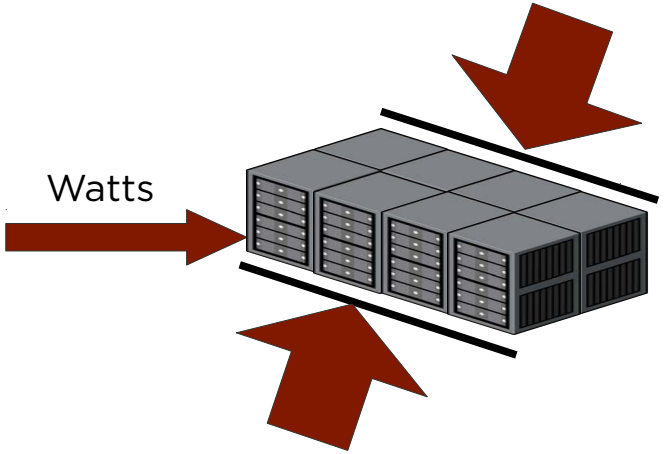

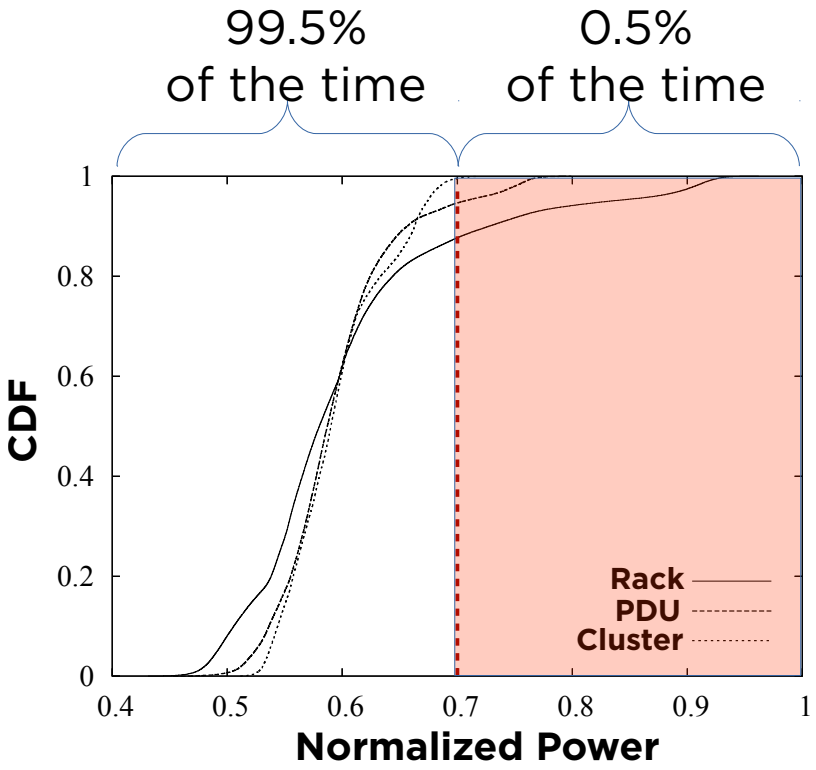

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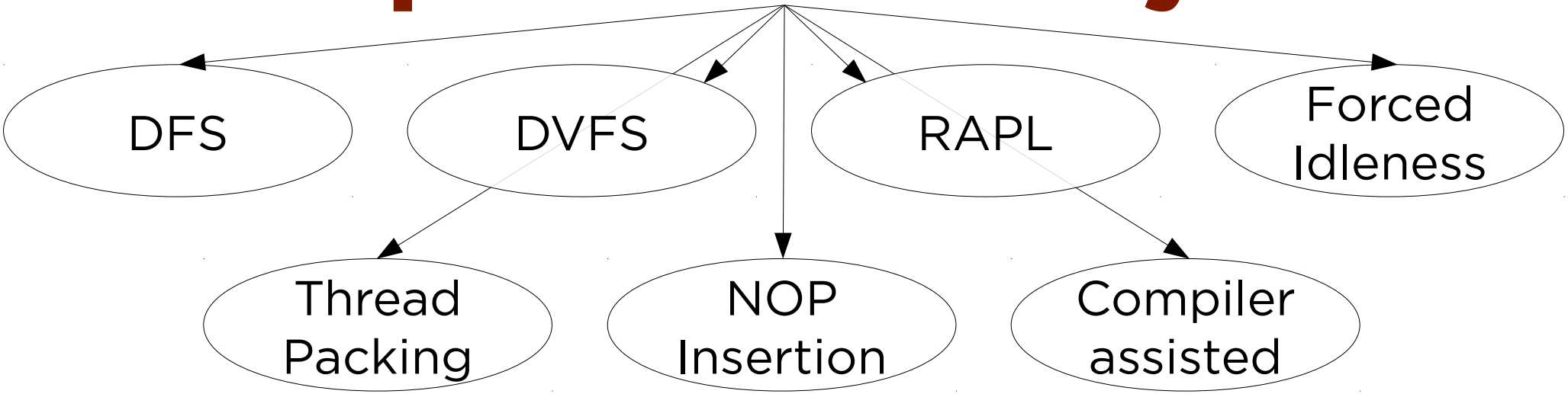
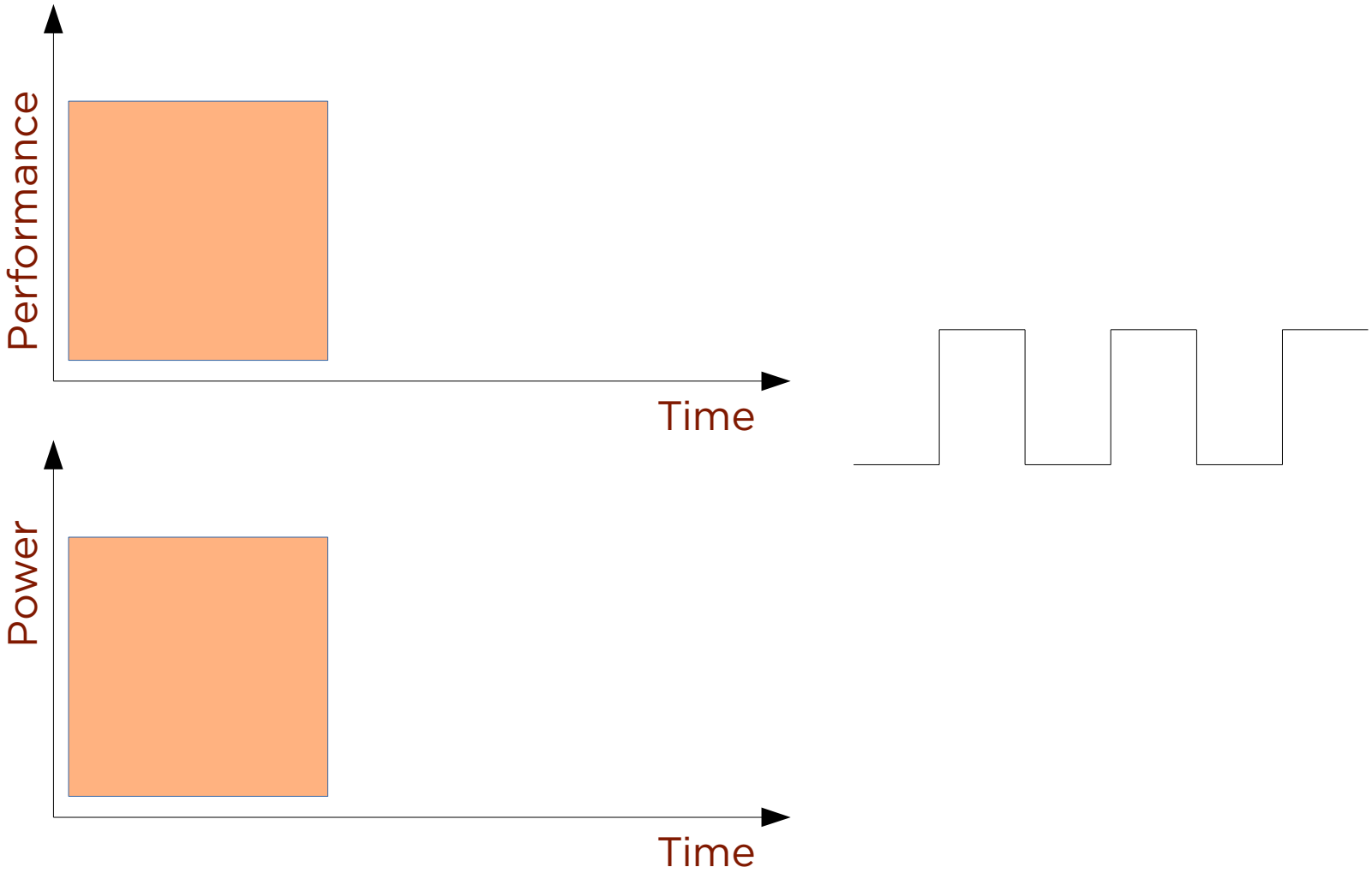
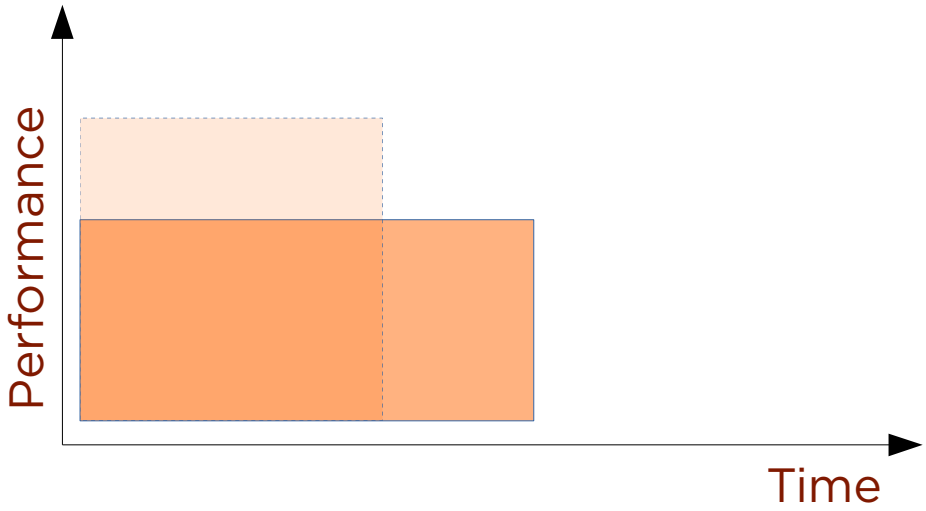
How do we enforce power limits locally?

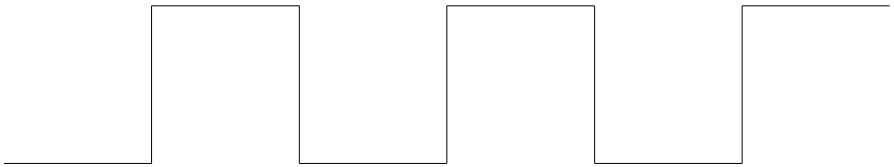


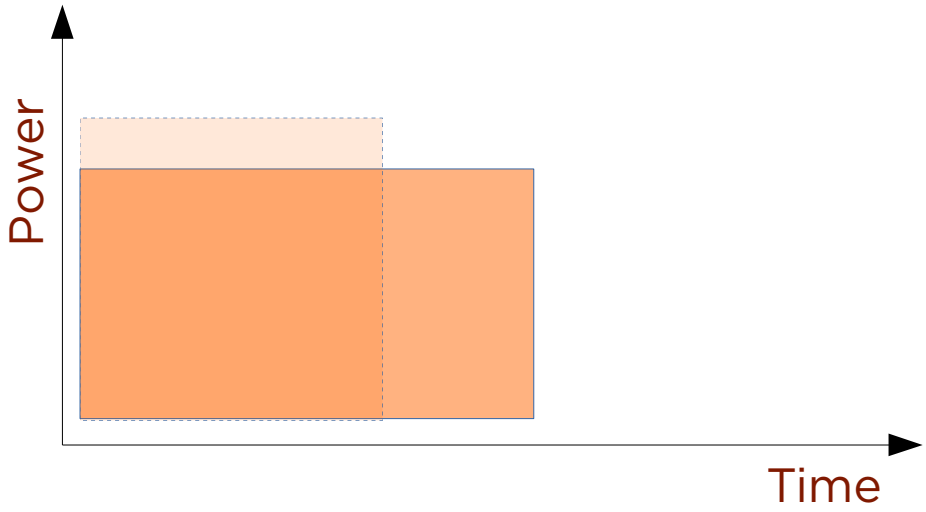
Power Capping – DFS



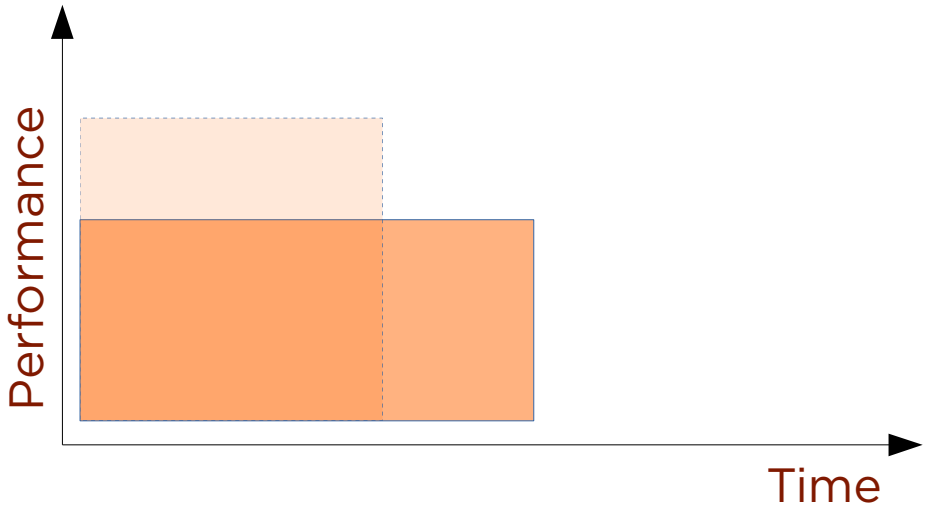
Power Capping – DFS

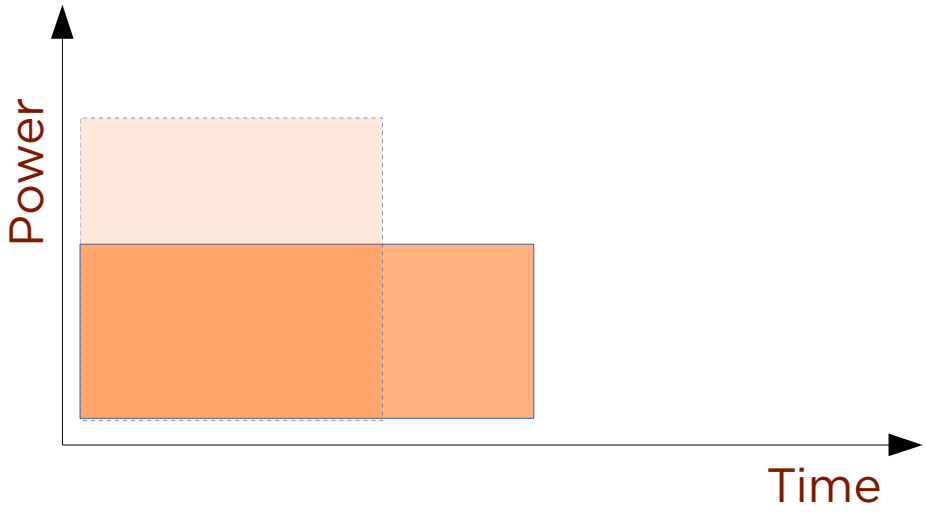


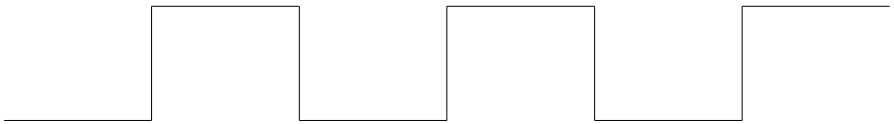




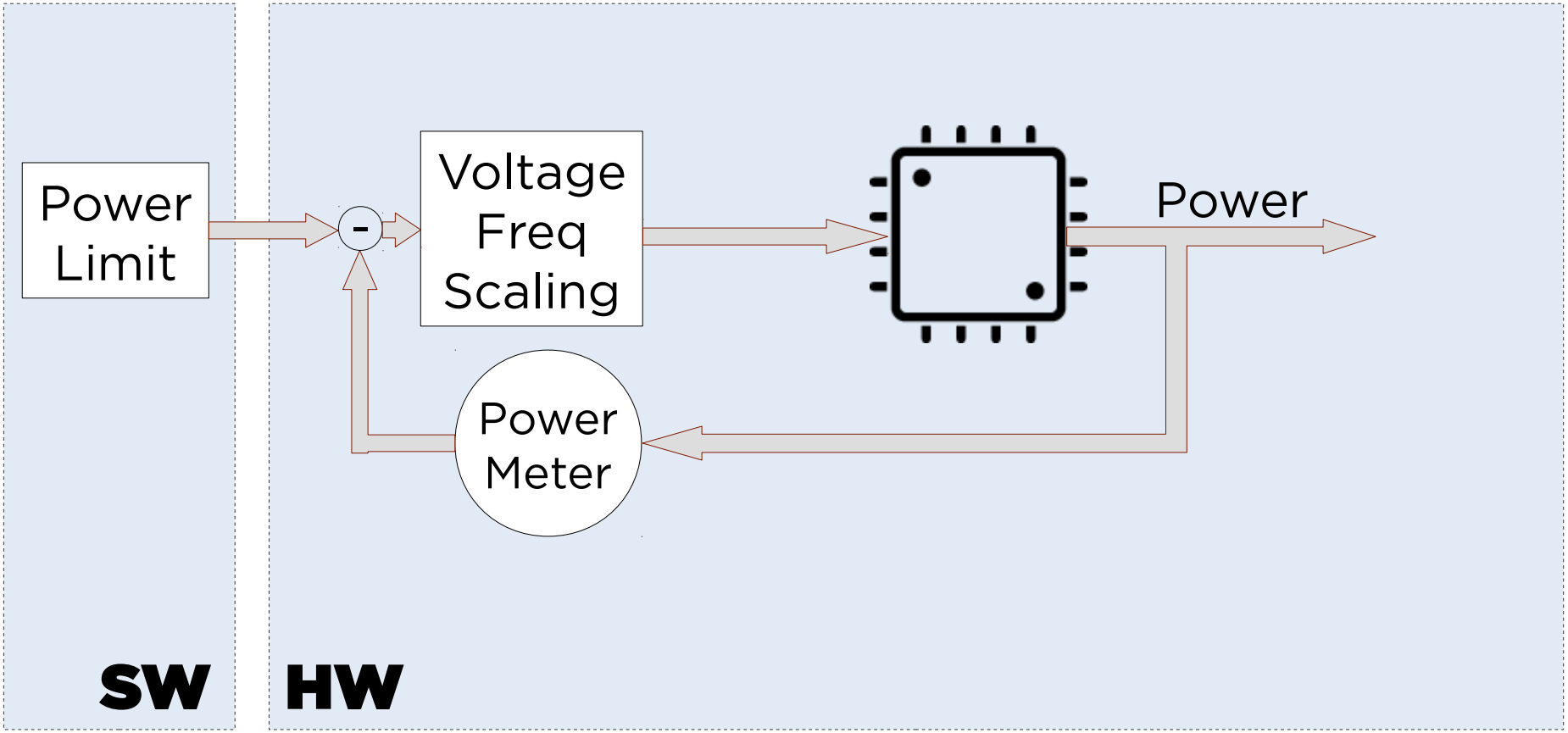
Power Capping – DVFS



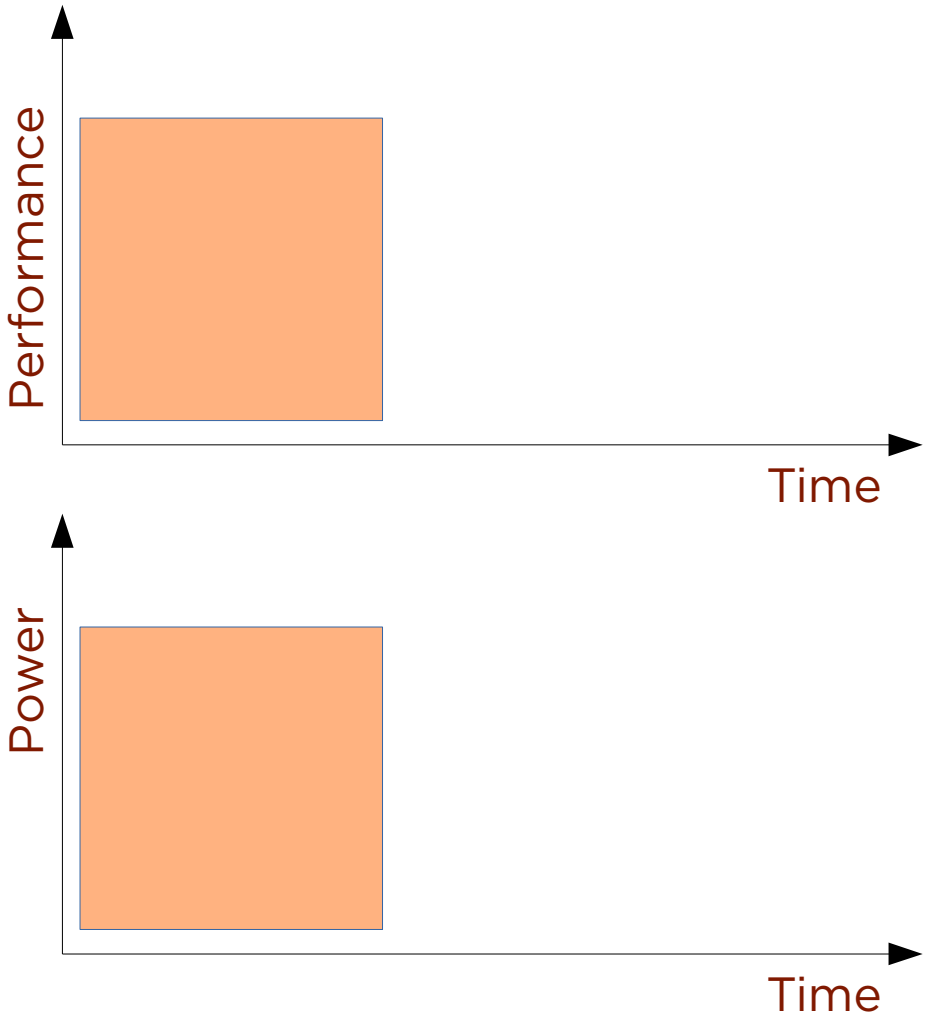




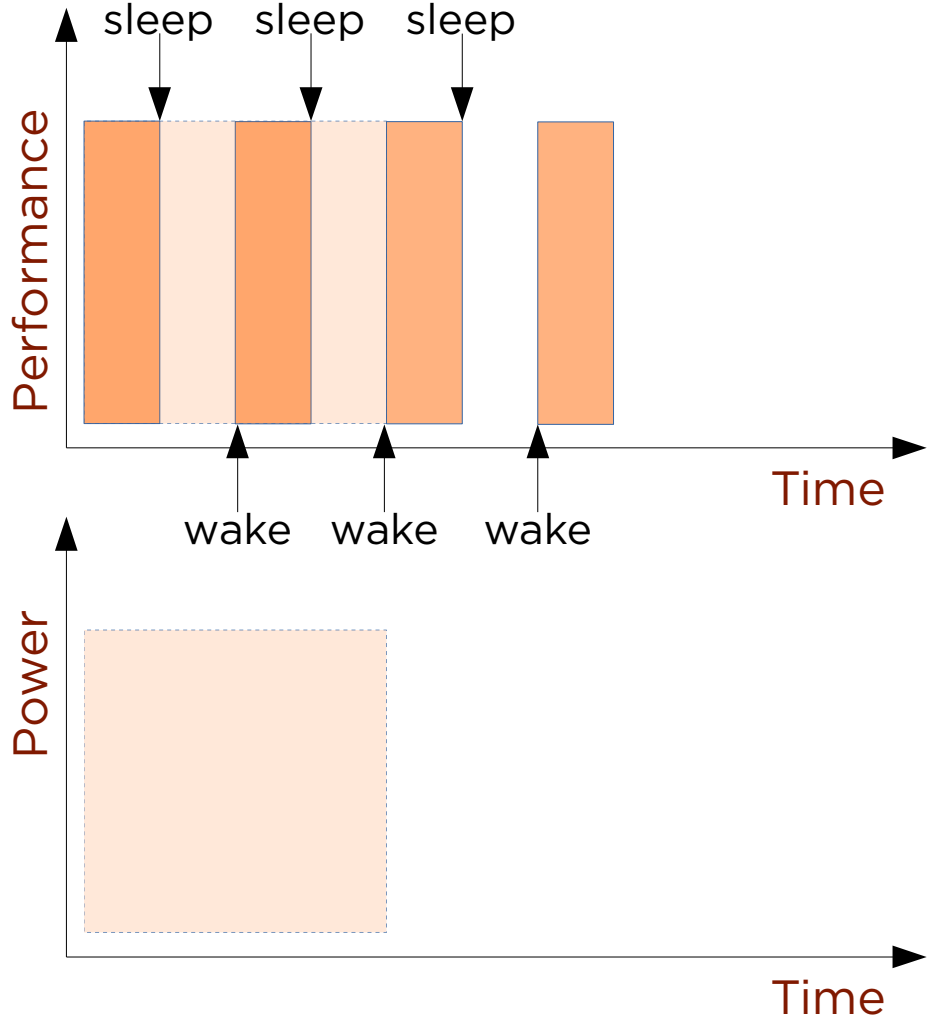
Power Capping – RAPL



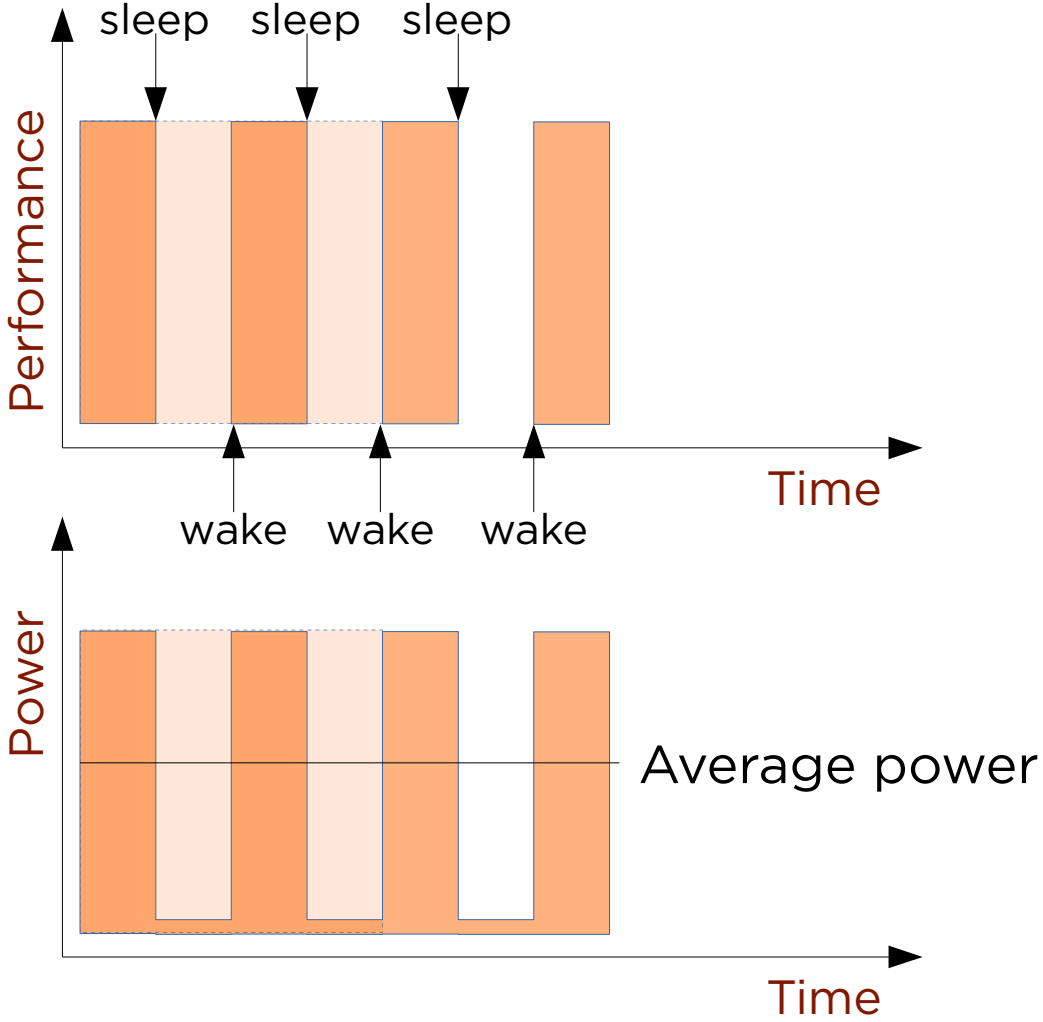
Power Capping – Forced Idleness



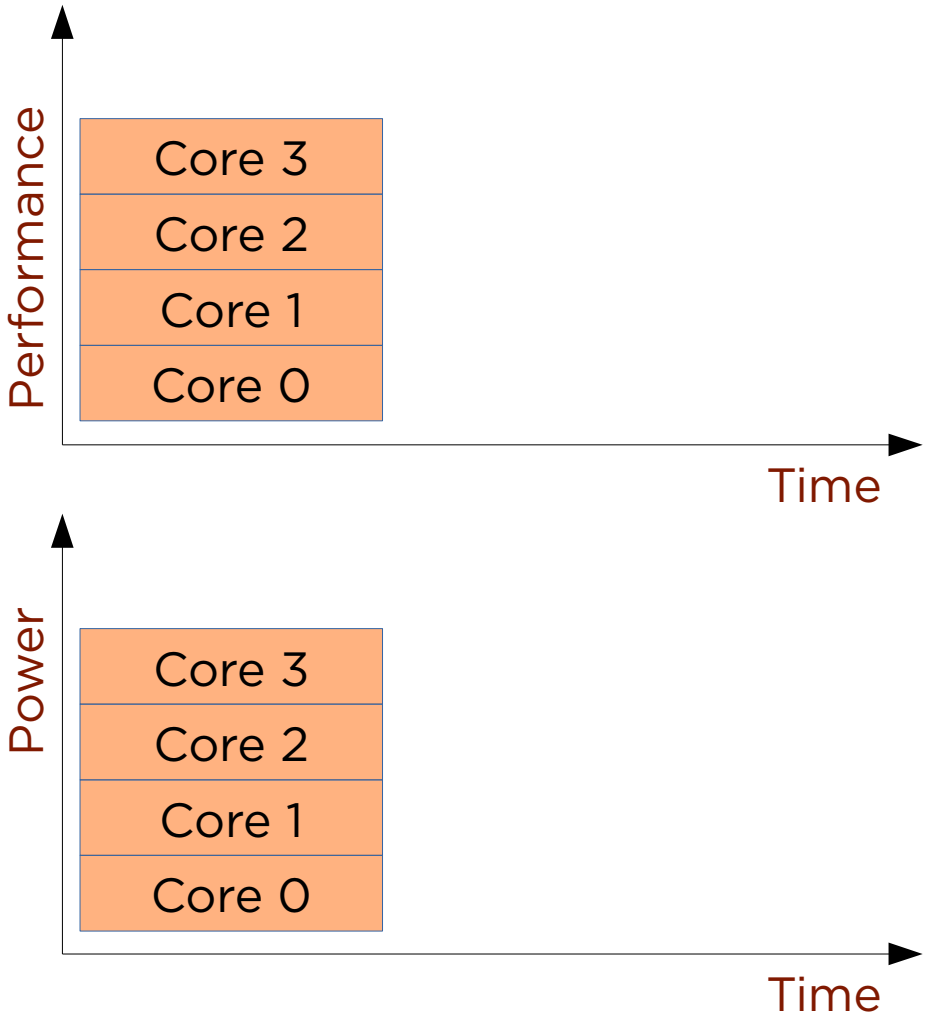
Power Capping – Forced Idleness



Power Capping – Forced Idleness



Power Capping – Thread Packing



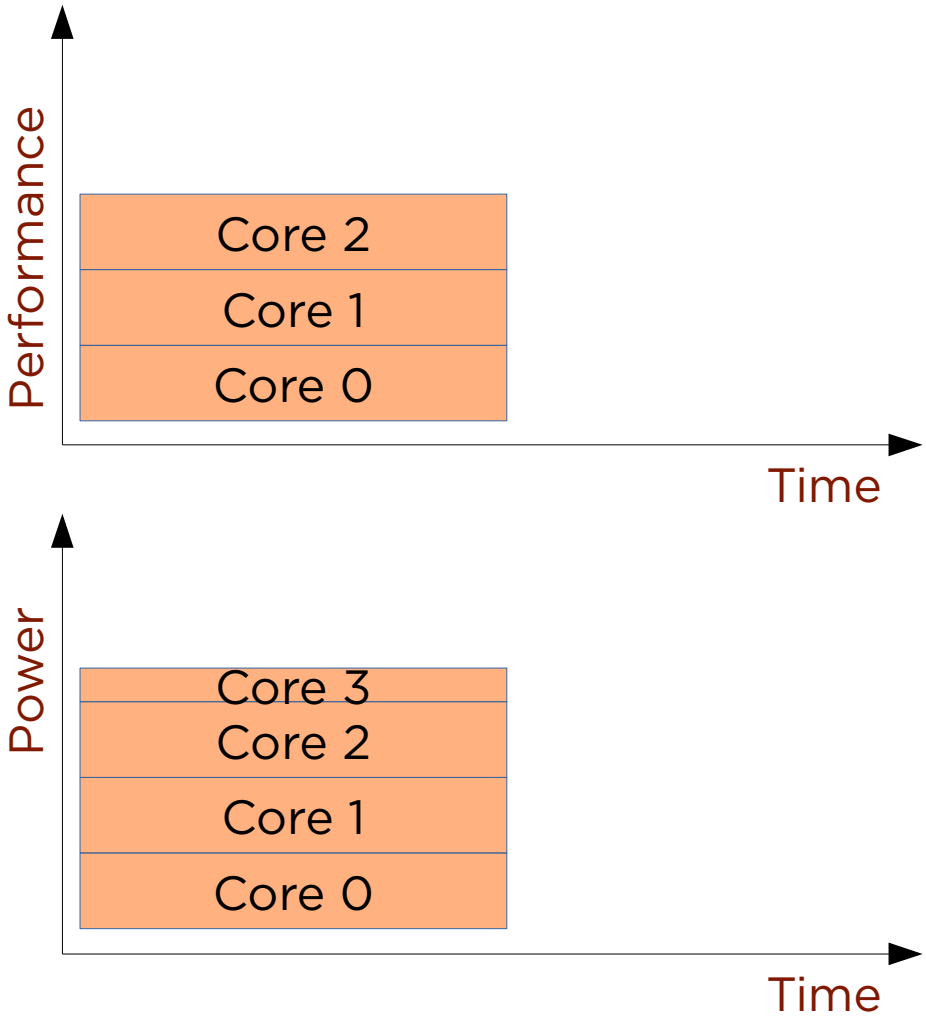
$thr0 \rightarrow core0$

$thr1 \rightarrow core1$

$thr2 \rightarrow core2$

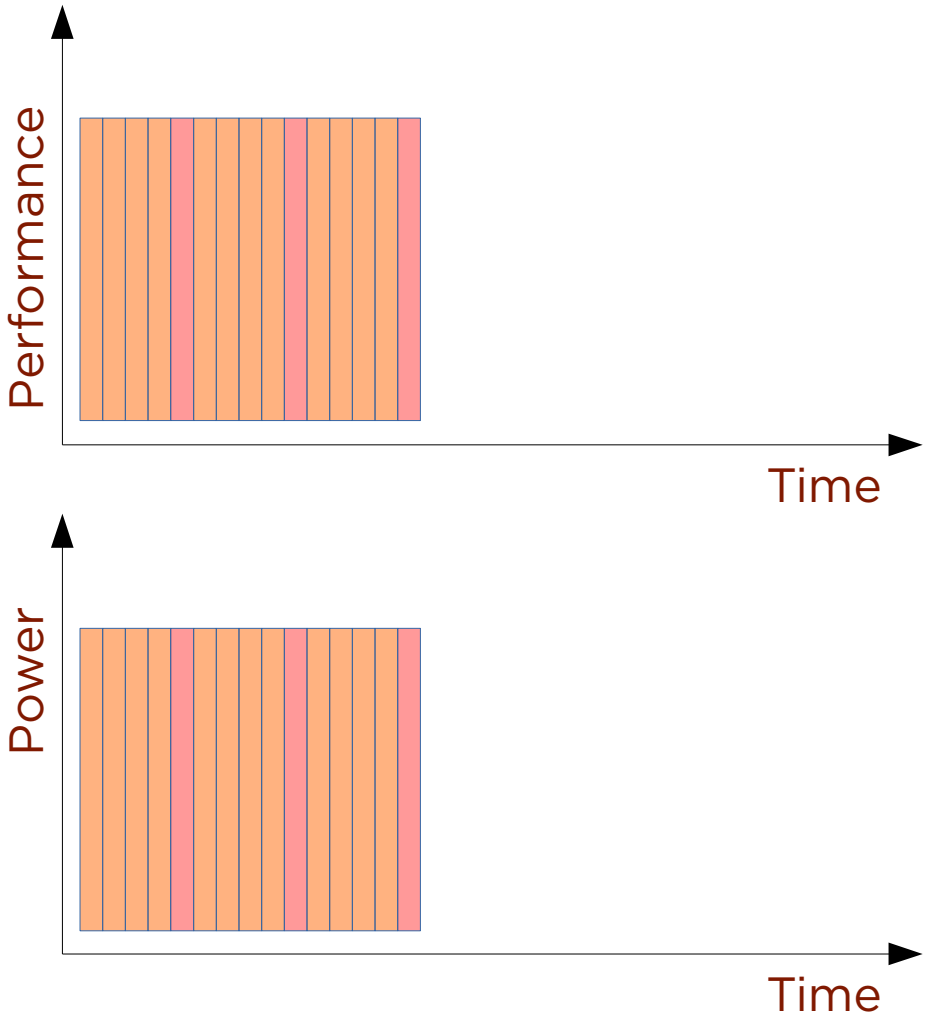
$thr3 \rightarrow core3$

Power Capping – Thread Packing



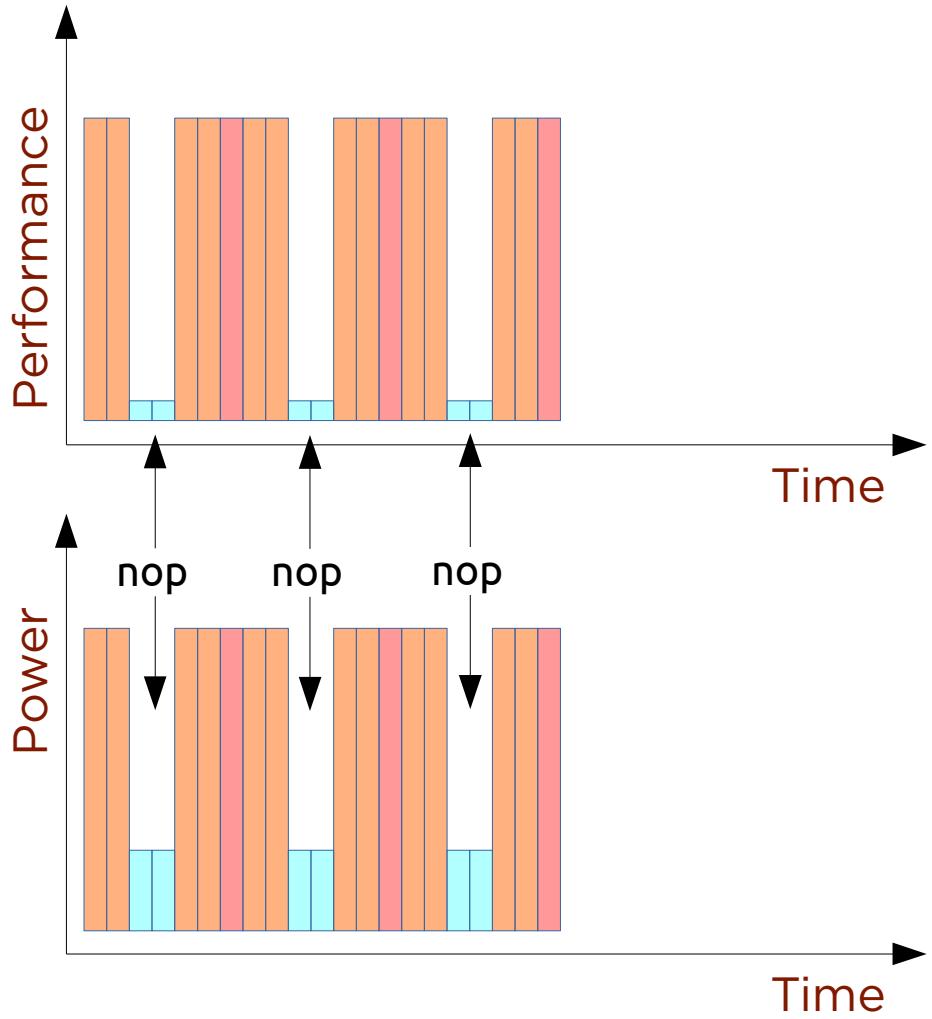
thr0 → core0
thr1 → core1
thr2 → core2
thr3 → core3

Power Capping – NOP Insertion



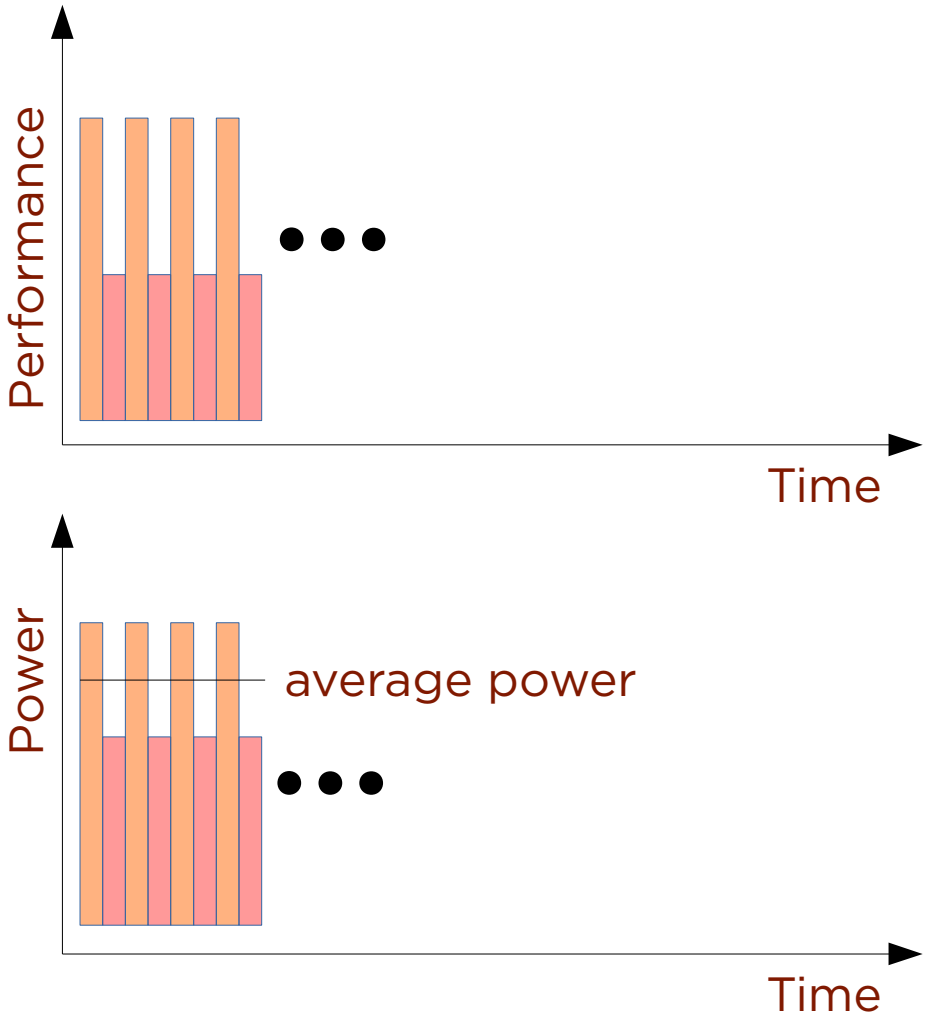

```
label1:
        instr_1
        instr_2
        instr_3
        instr_4
        jmp label1
```

Power Capping – NOP Insertion



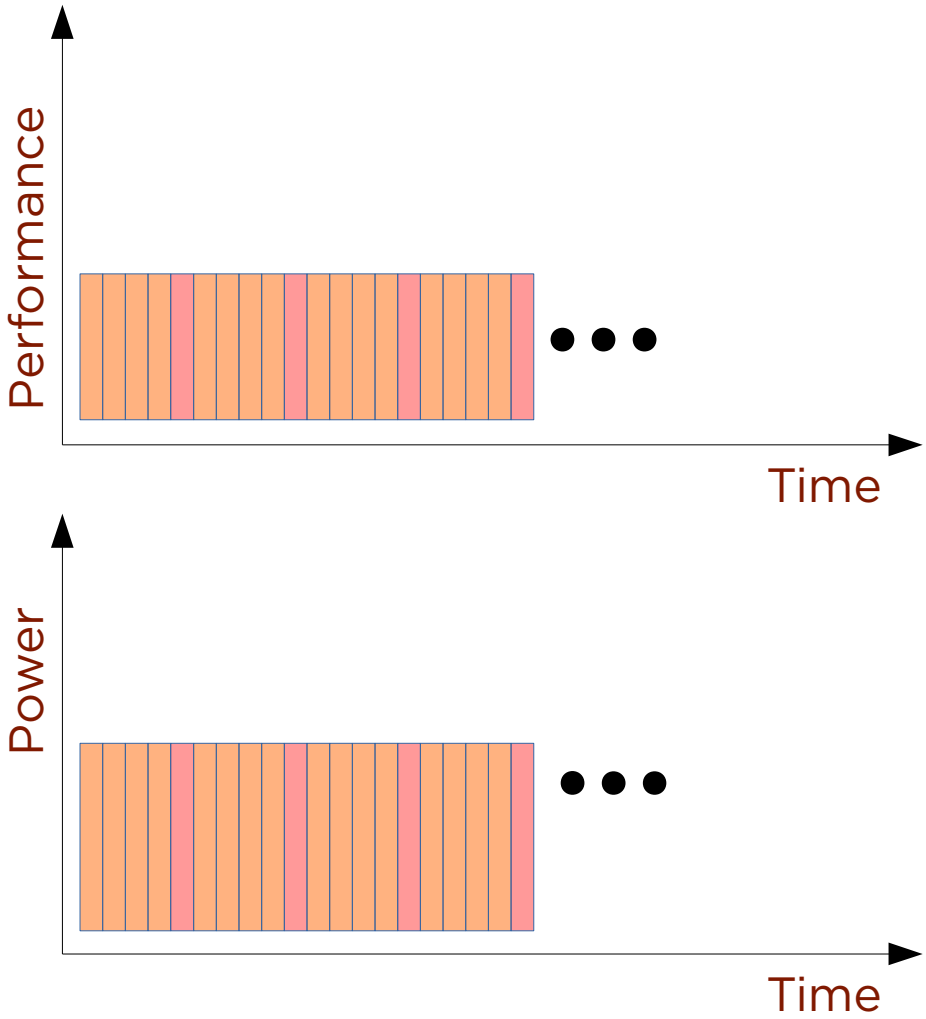

```
label1:
        instr_1
        instr_2
        nop
        nop
        instr_3
        instr_4
        jmp label1
```

Power Capping – Compiler assisted




```
label1:
        vector_instr
        jmp label1
```

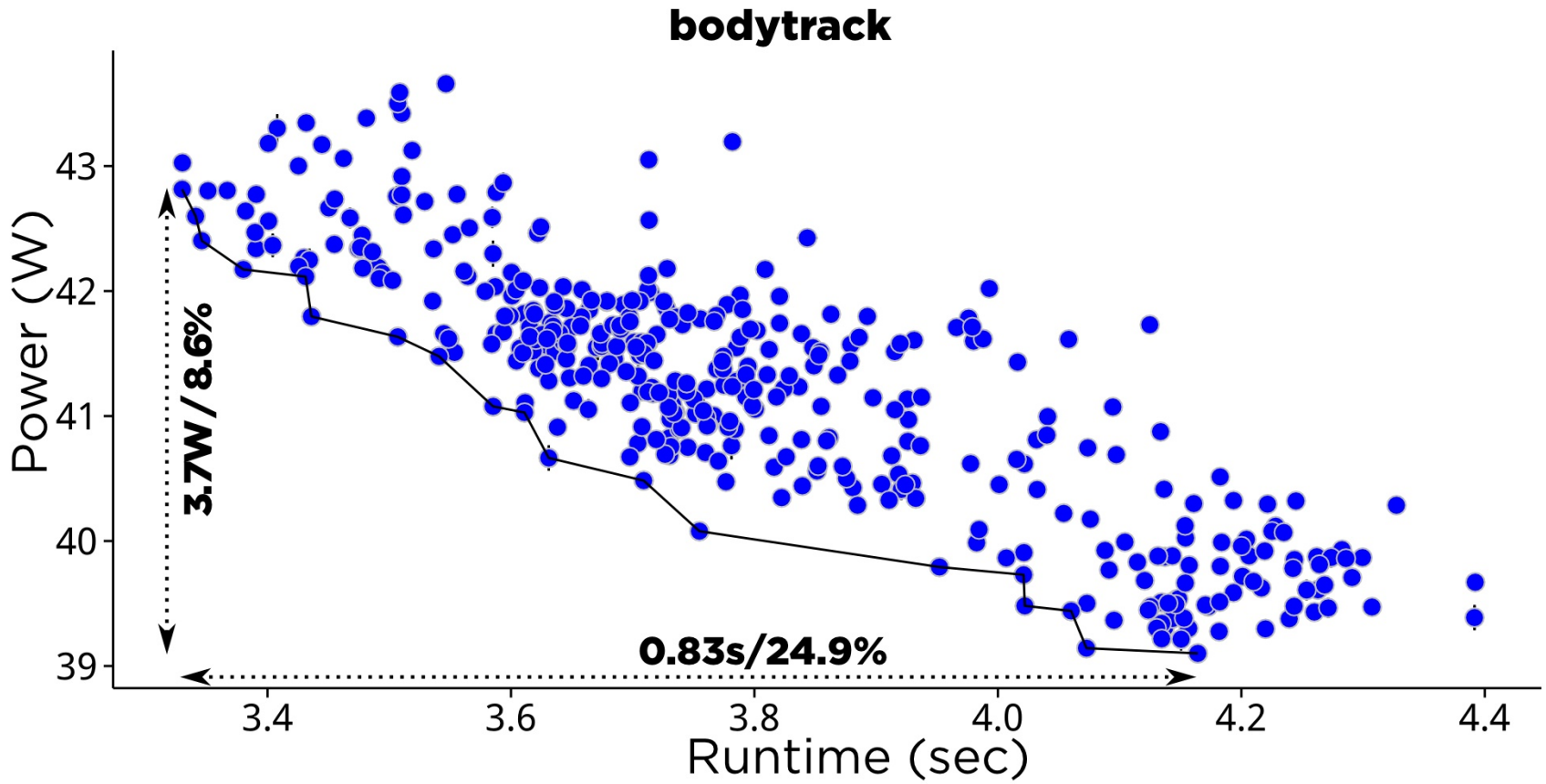
Power Capping – Compiler assisted




```
label1:
        instr
        instr
        instr
        instr
        jmp label1
```

Power Capping – Compiler assisted

With multiple transformations:



Evaluation

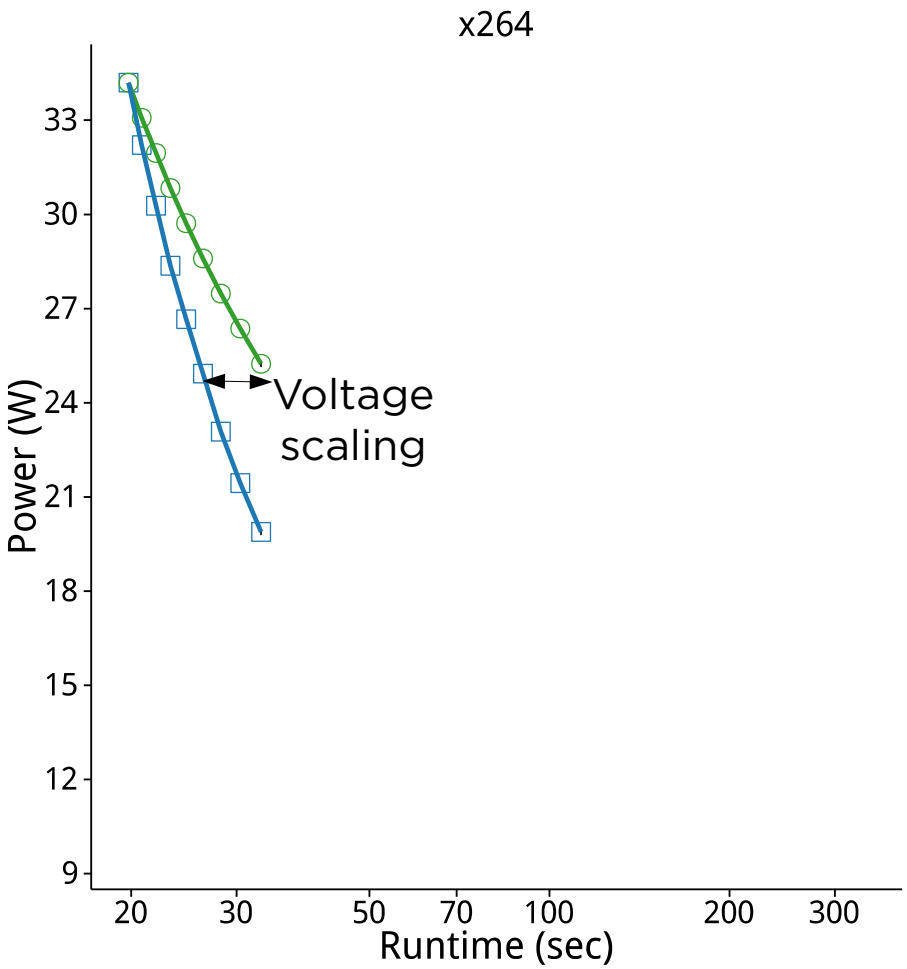
Effectiveness

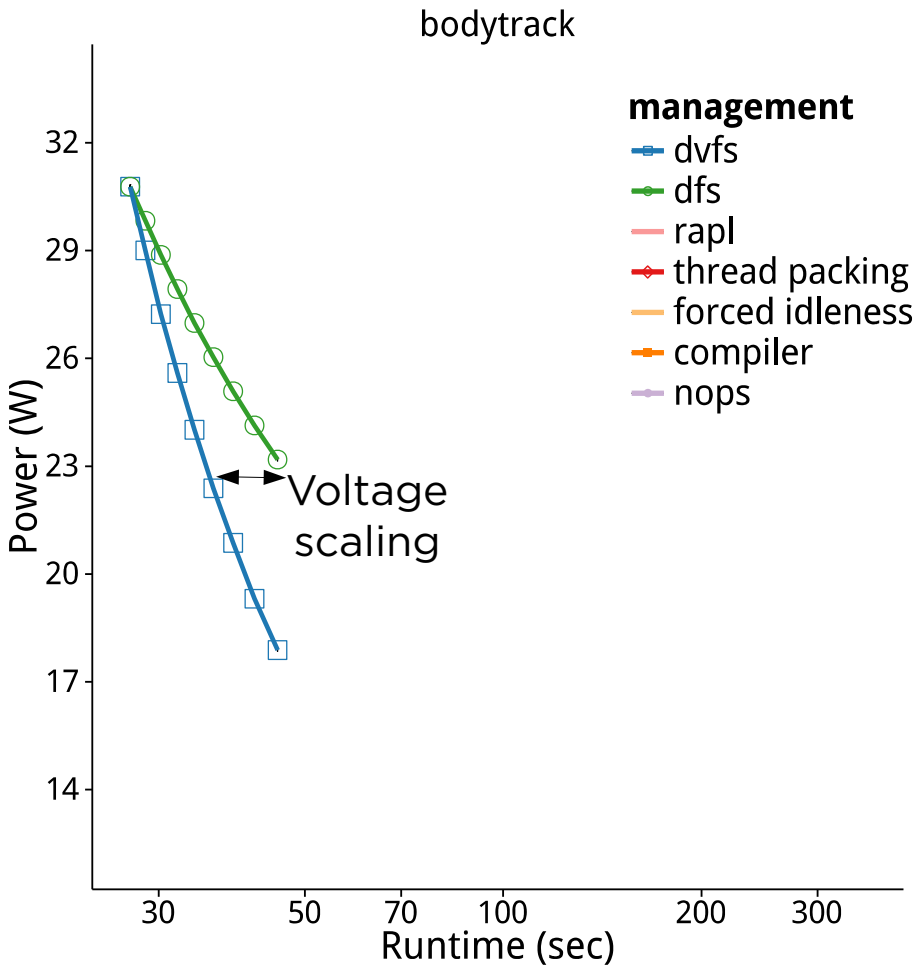
Overhead

Predictability

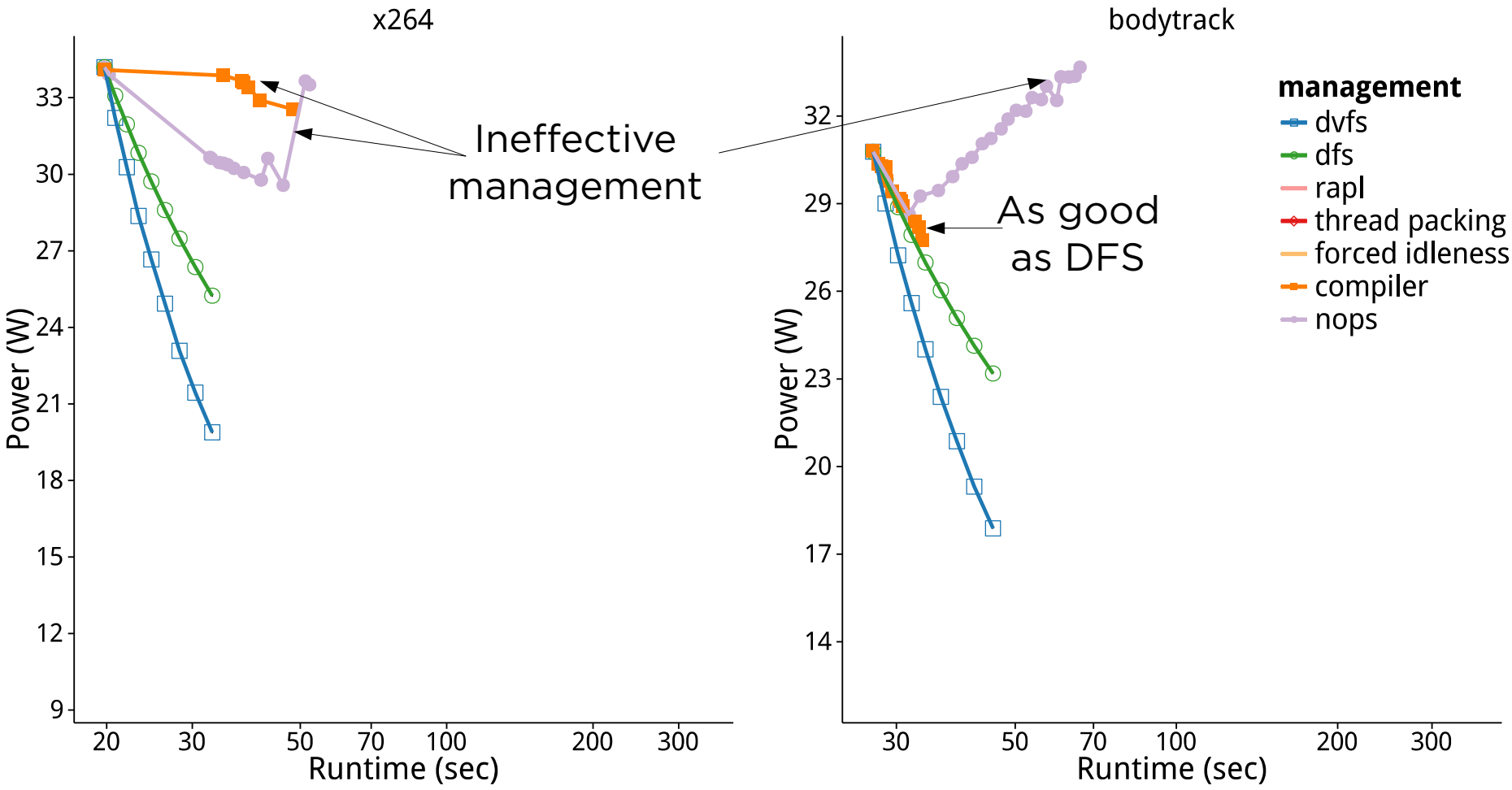
Optimal strategy?

Effectiveness

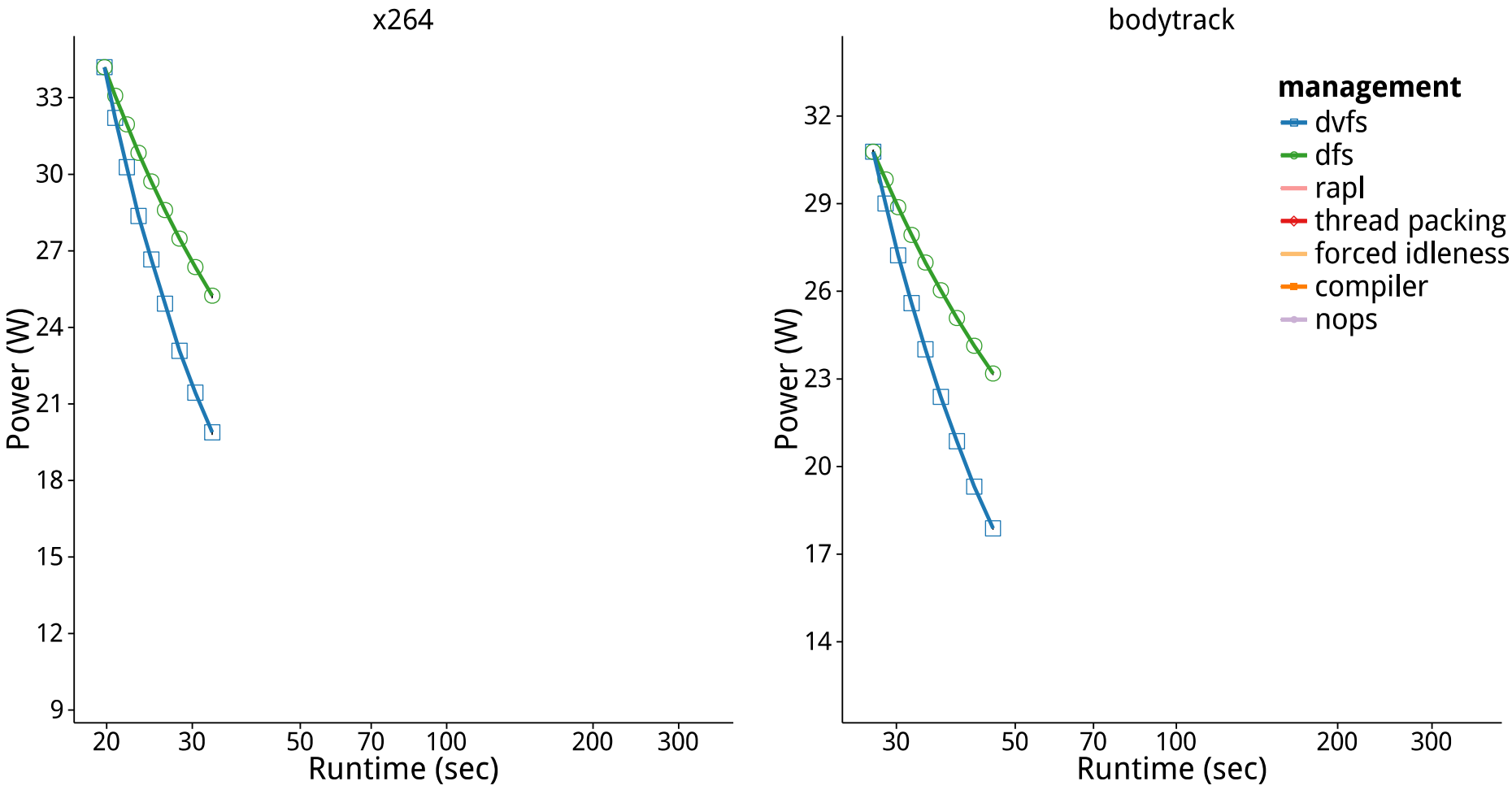




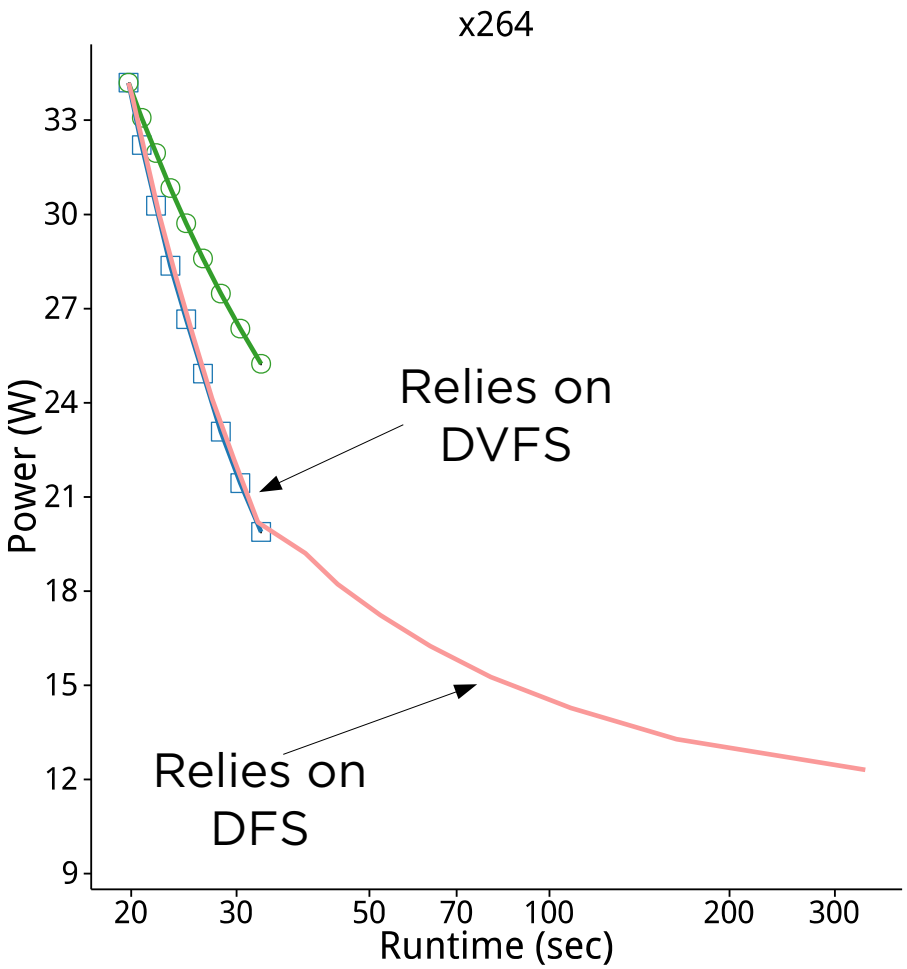
Effectiveness

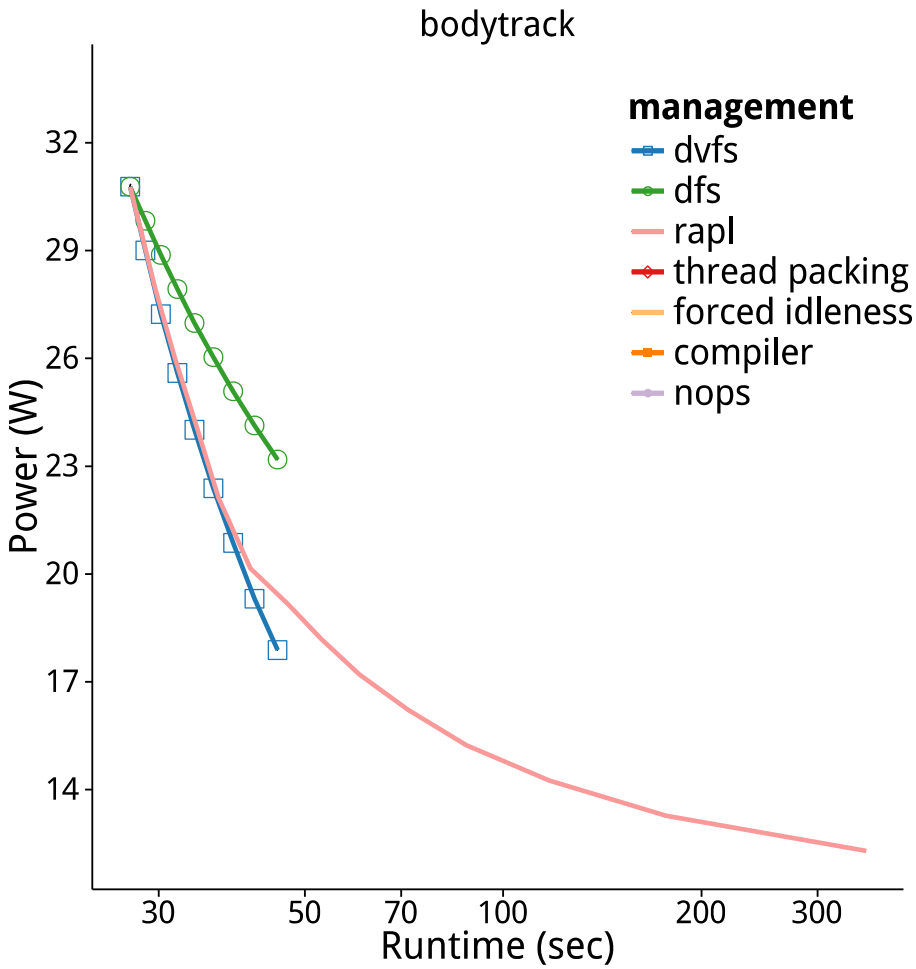


Effectiveness

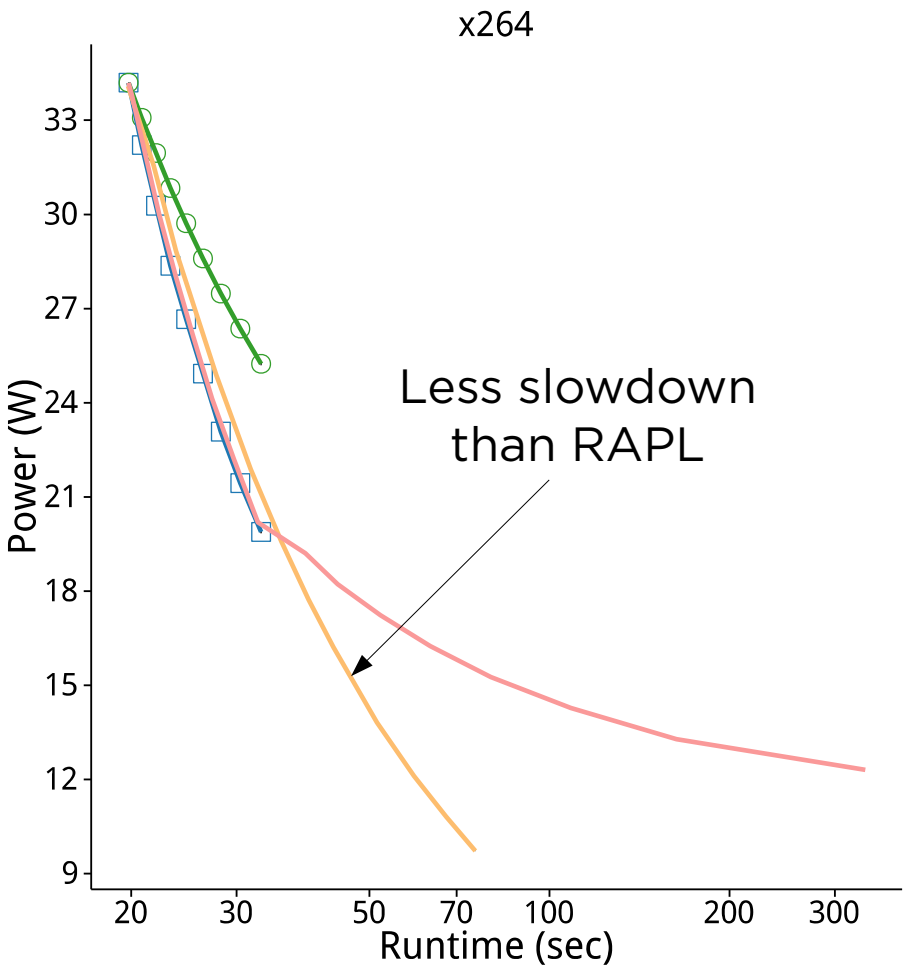


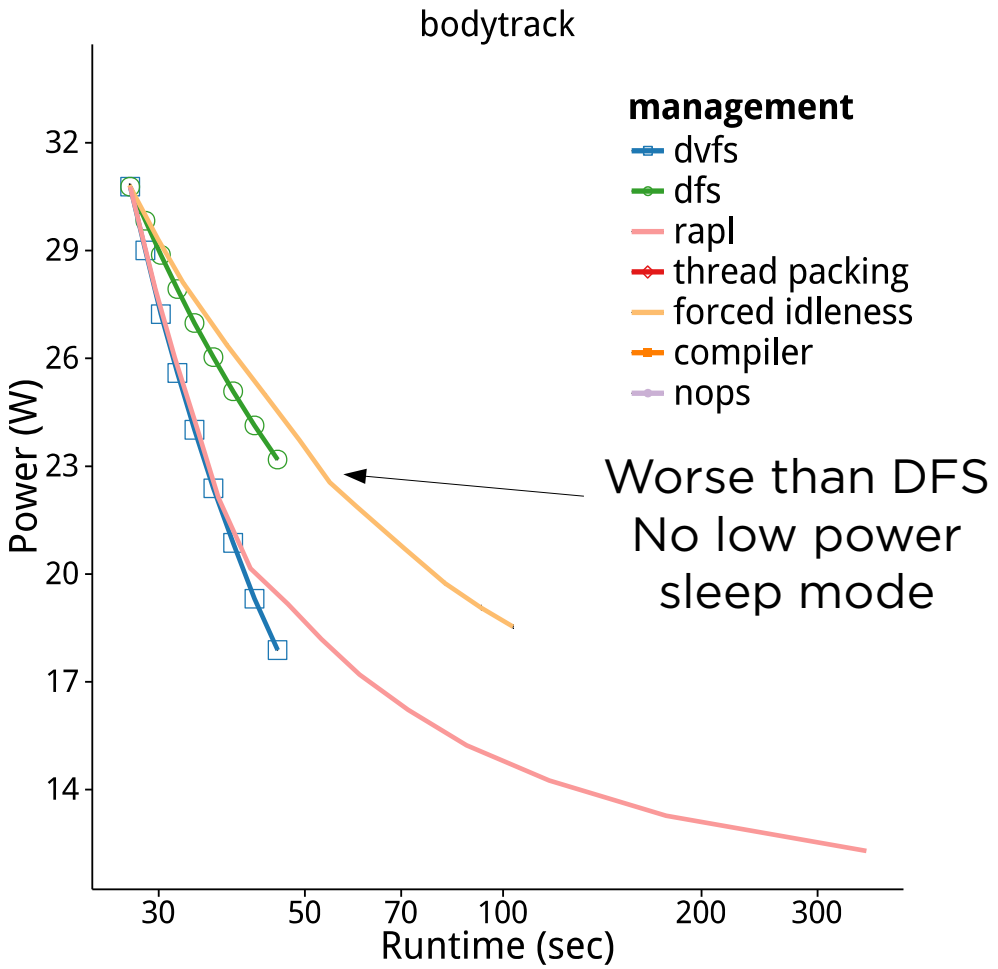
Effectiveness



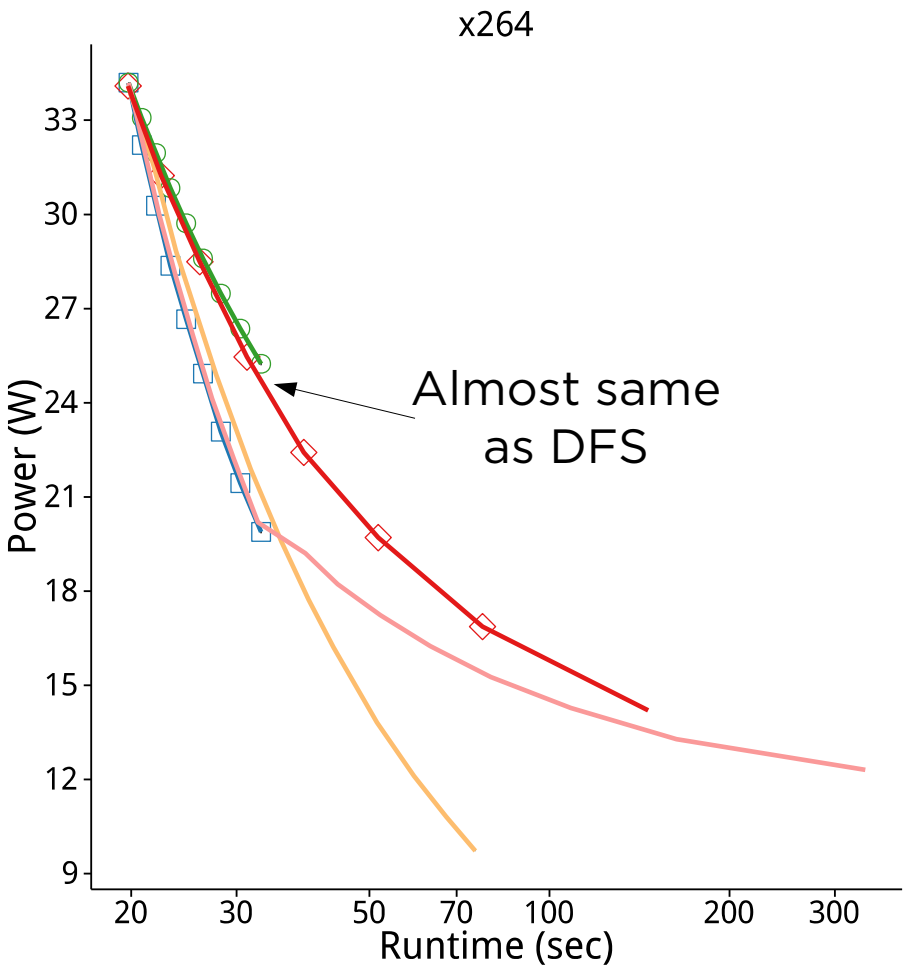


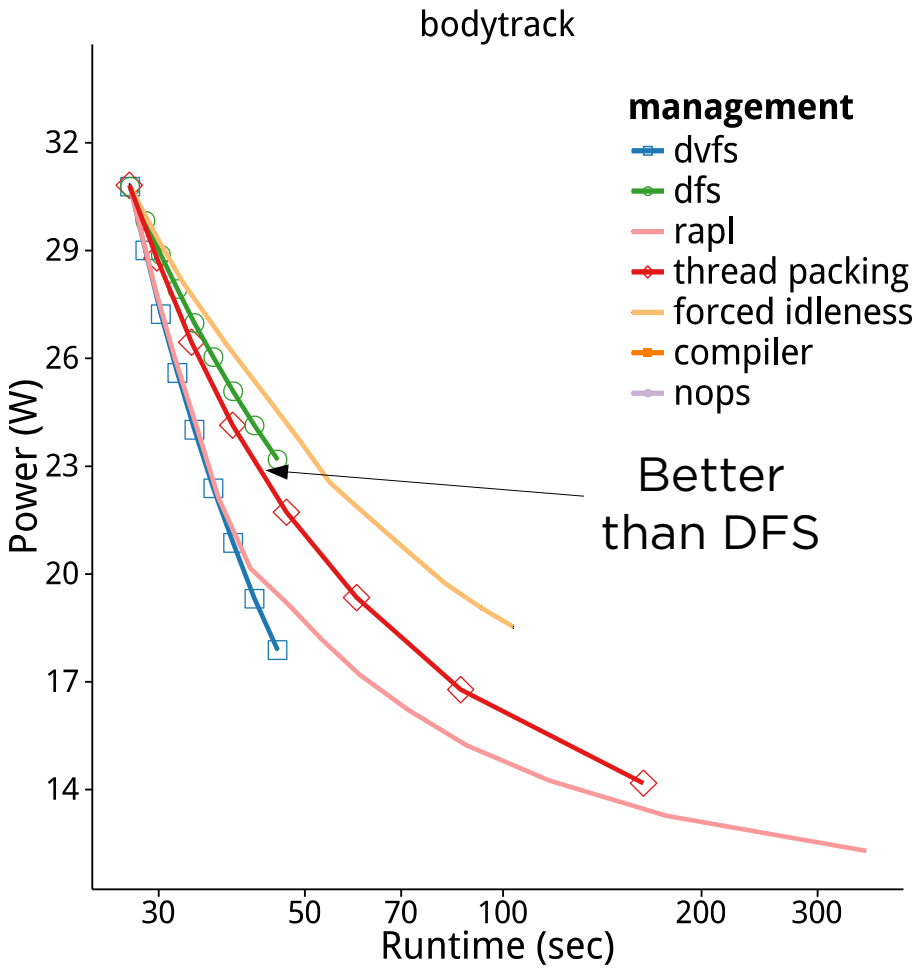
Effectiveness



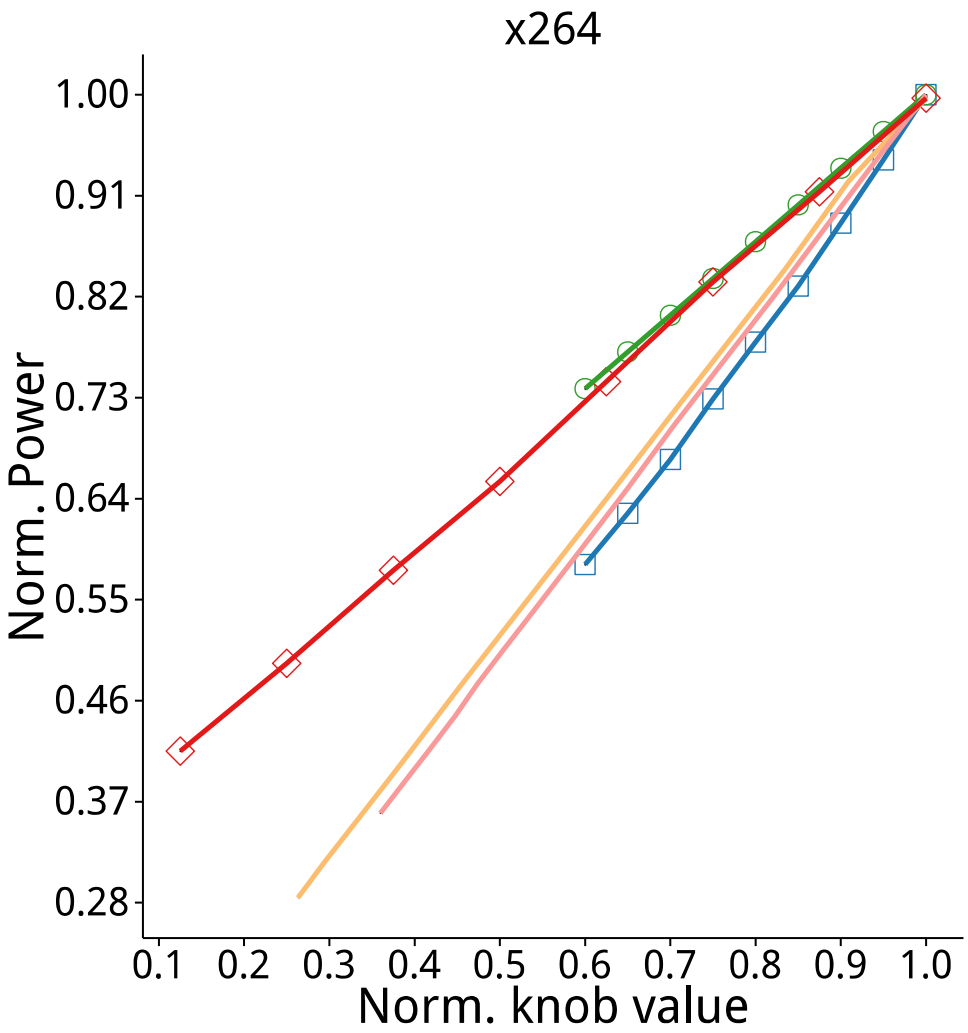


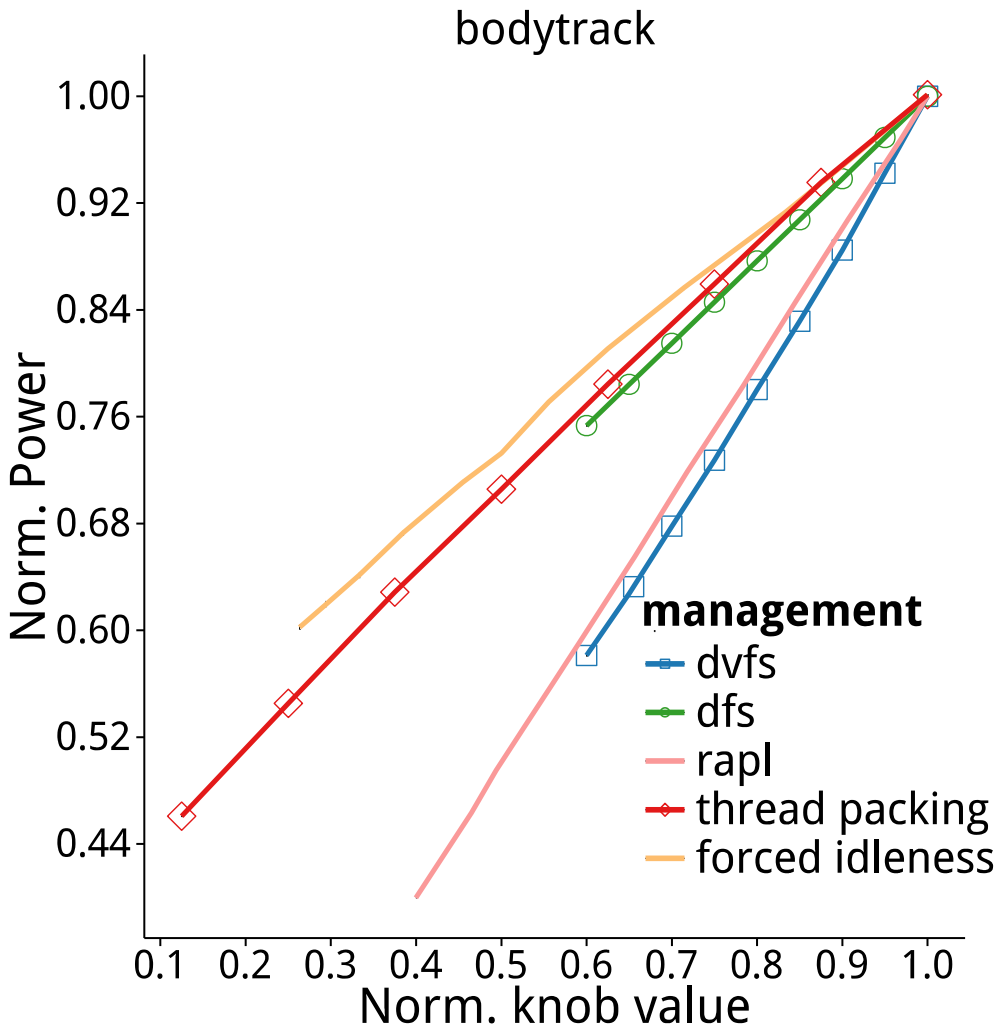
Effectiveness



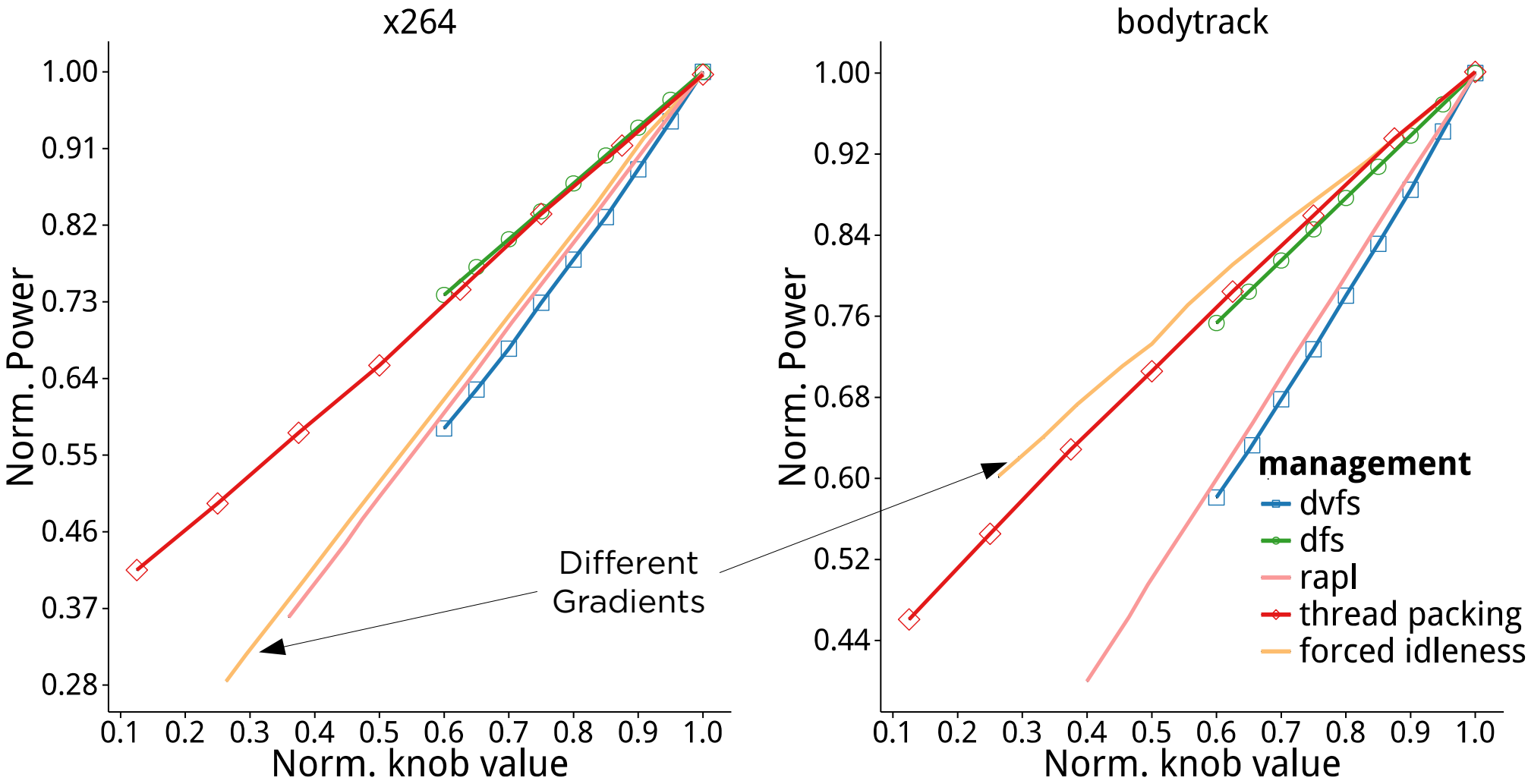


Predictability - Power

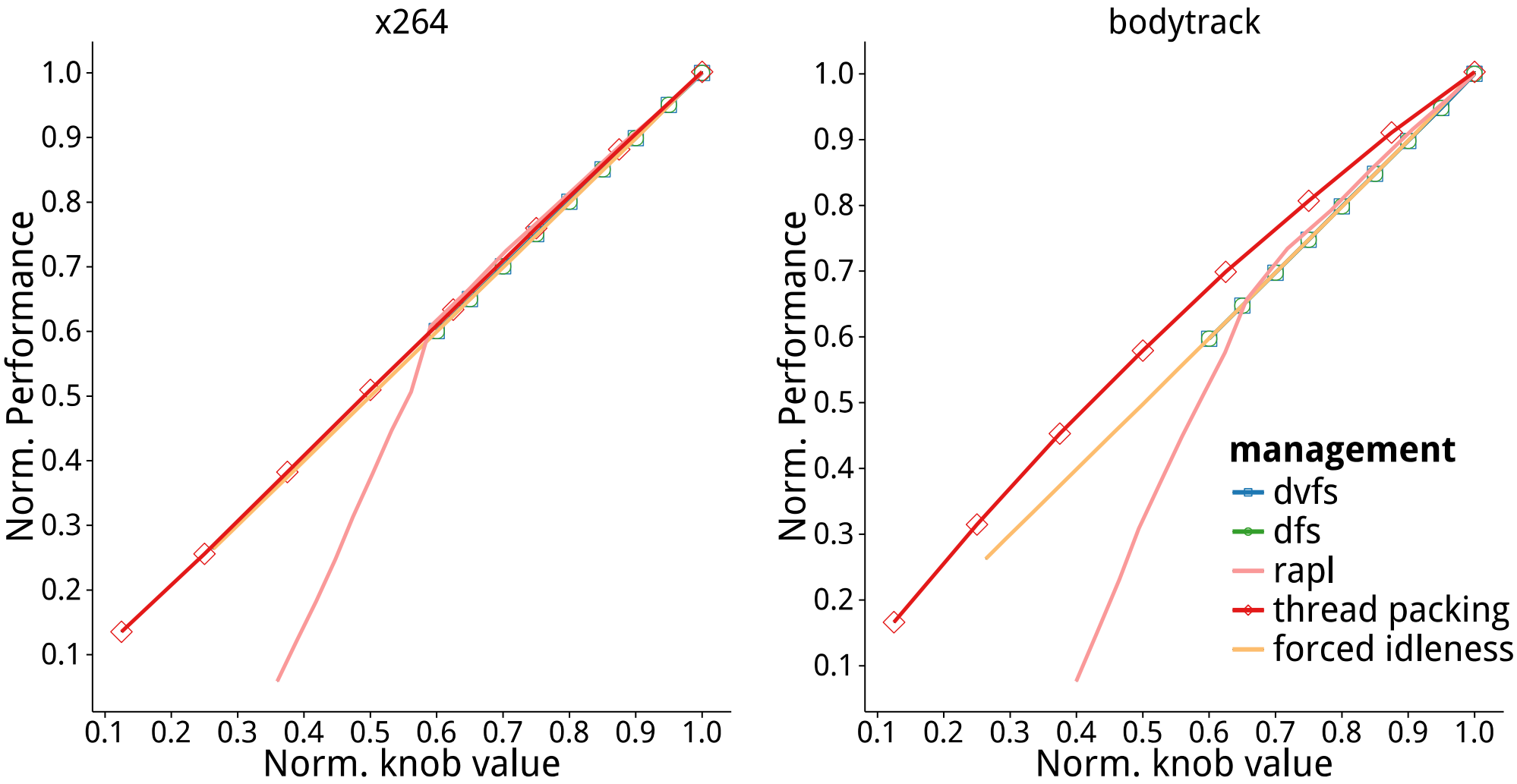




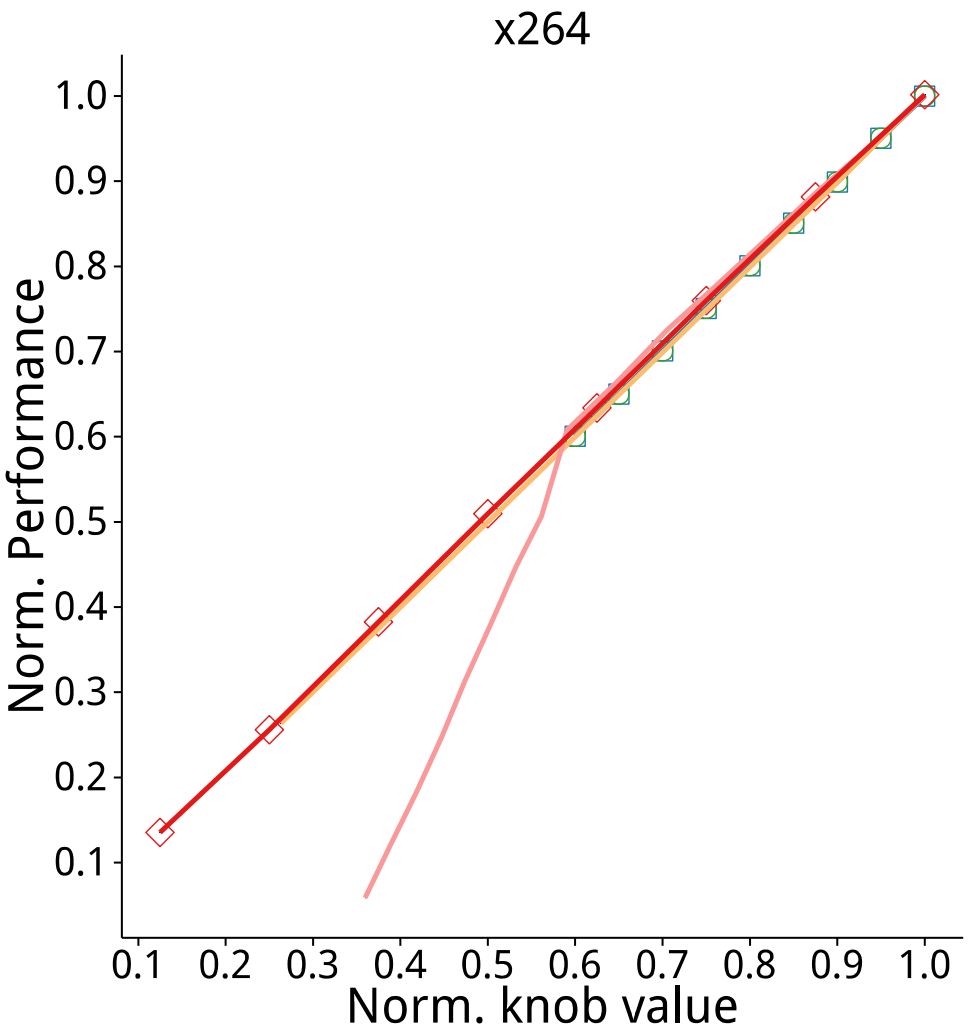
Predictability - Power

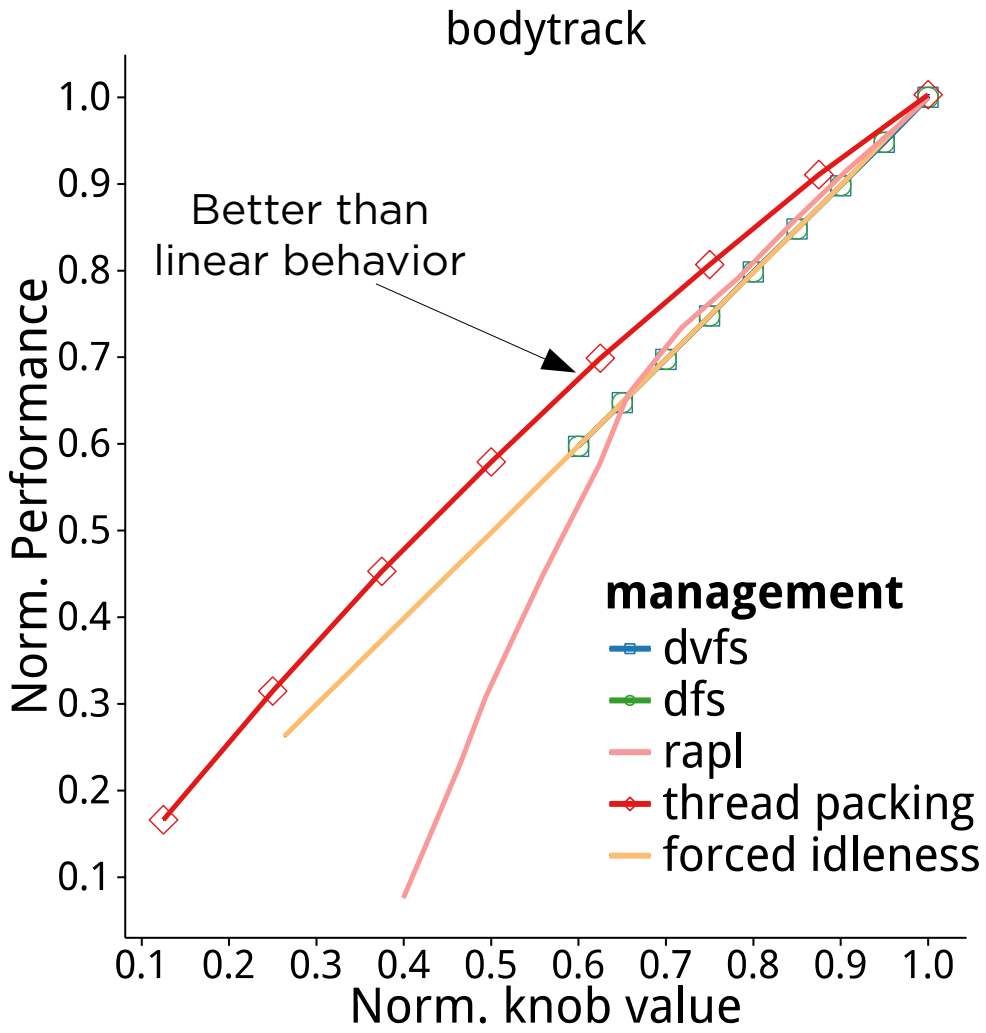


Predictability - Performance

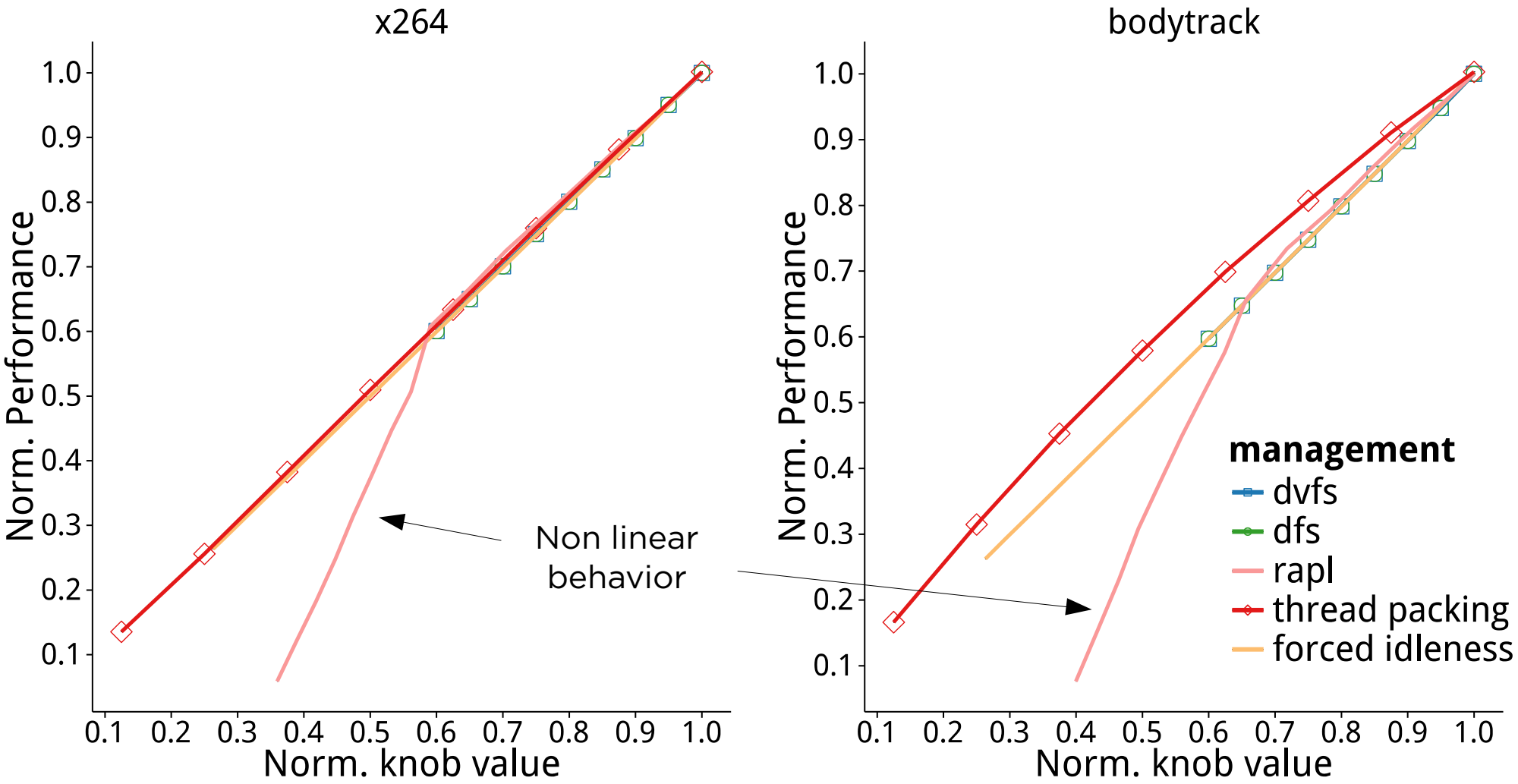


Predictability - Performance

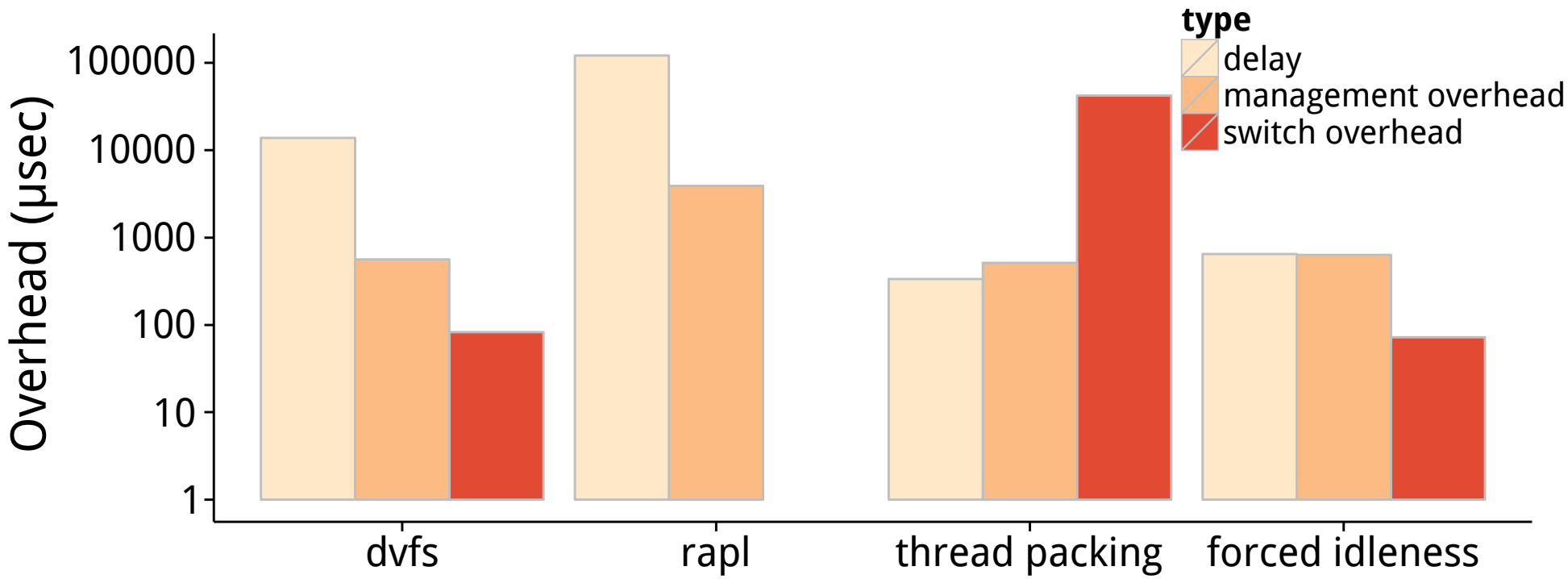




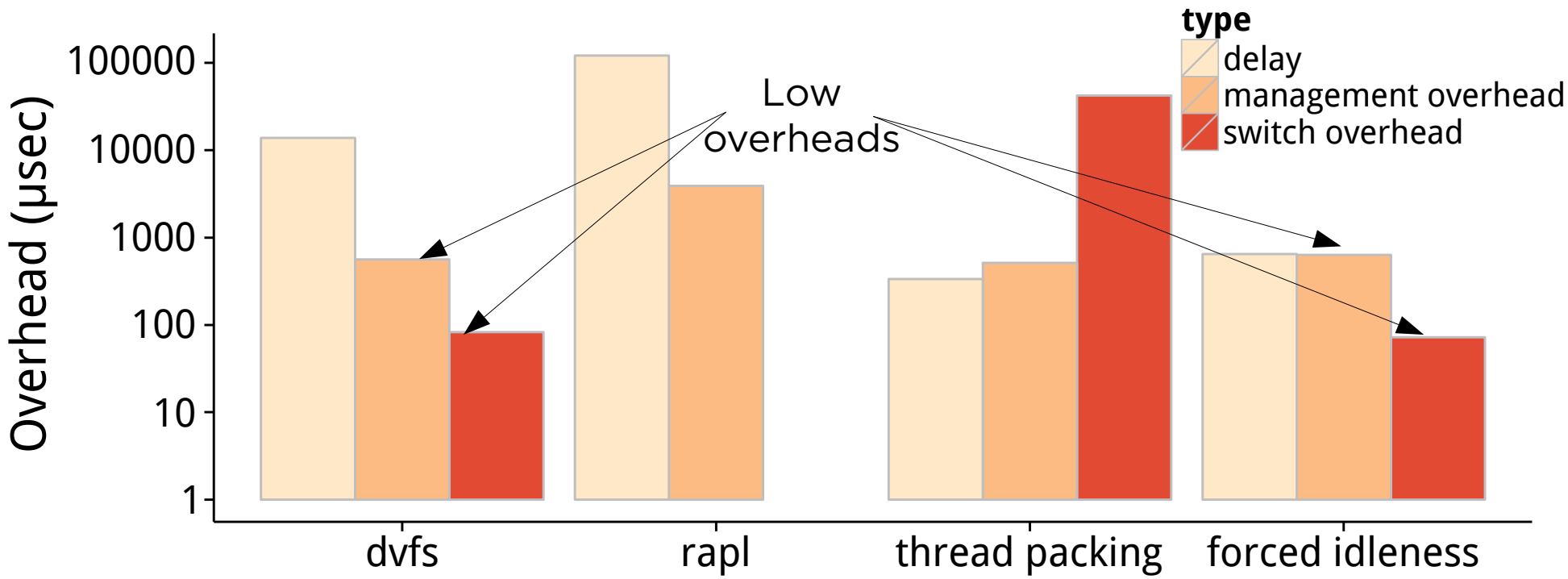
Predictability - Performance



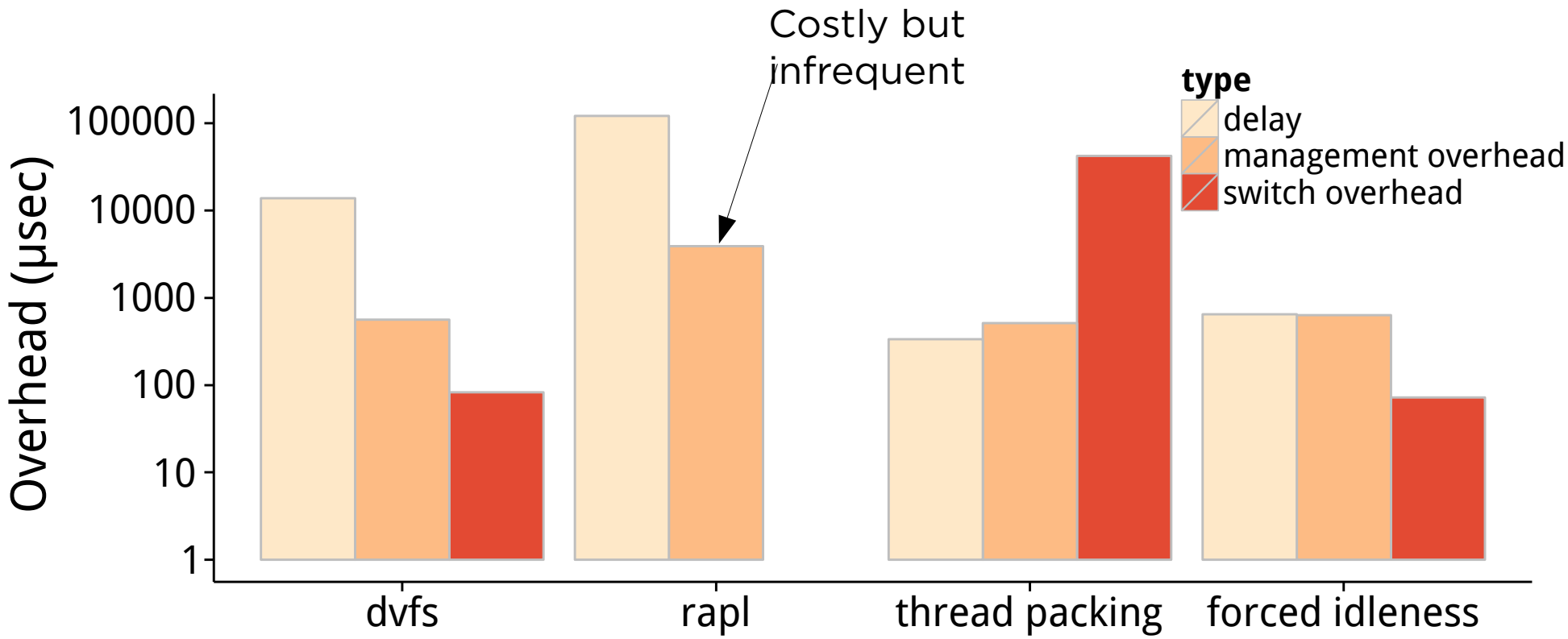
Overheads


type
delay
management overhead
switch overhead
Overhead (µsec)
100000
10000
1000
100
10
1
dvfs
rapl
thread packing
forced idleness

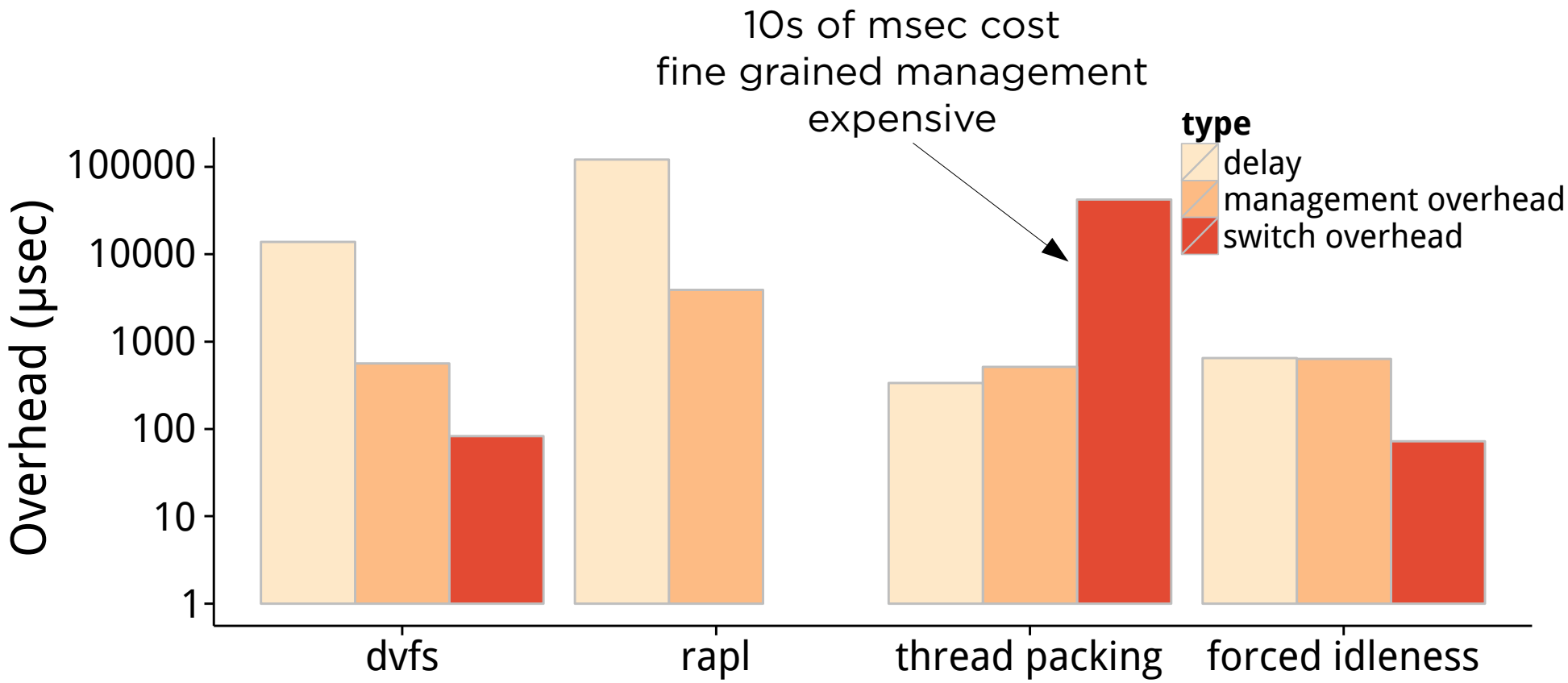
Overheads


type
delay
management overhead
switch overhead
Low overheads
Overhead (µsec)
100000
10000
1000
100
10
1
dvfs
rapl
thread packing
forced idleness

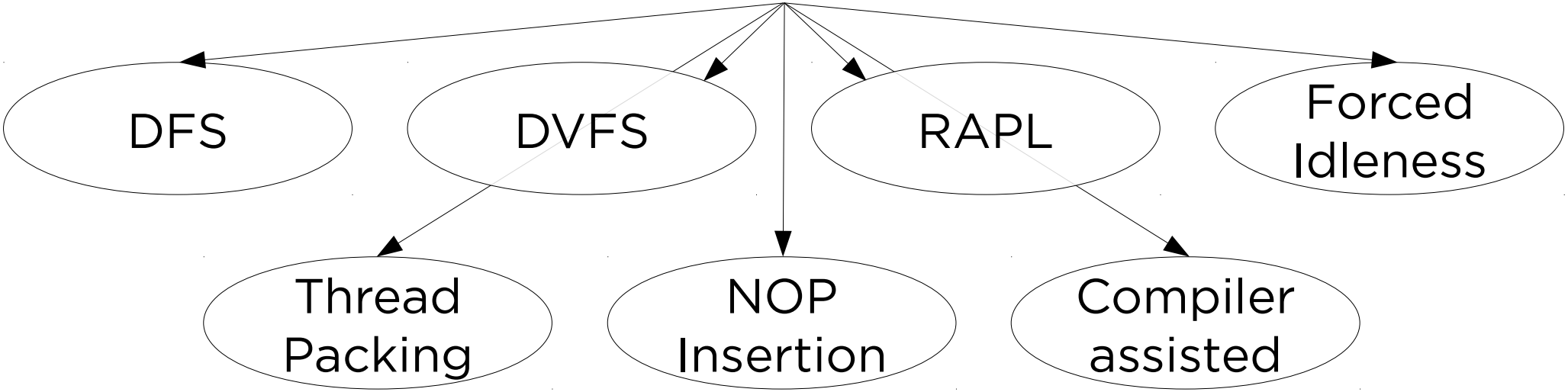
Overheads


Costly but infrequent
type
delay
management overhead
switch overhead
Overhead (µsec)
100000
10000
1000
100
10
1
dvfs
rapl
thread packing
forced idleness

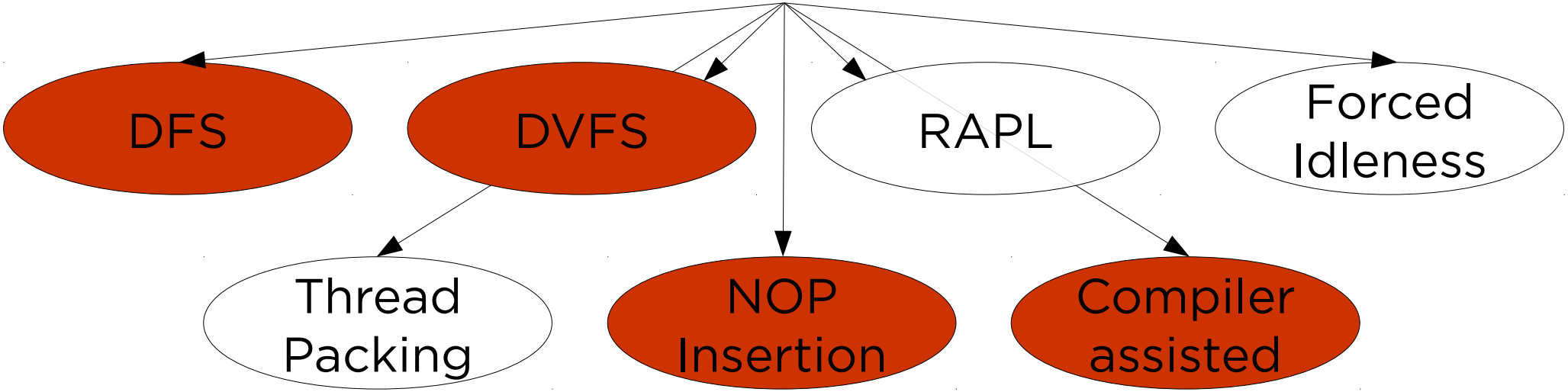
Overheads


10s of msec cost
fine grained management
expensive
type
delay
management overhead
switch overhead
Overhead (µsec)
100000
10000
1000
100
10
1
dvfs
rapl
thread packing
forced idleness

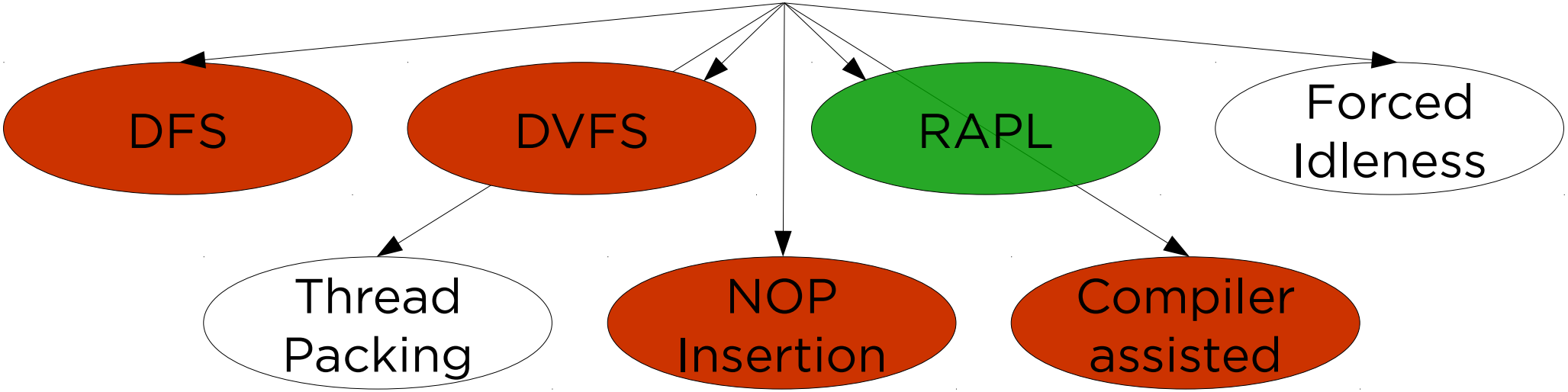
Can we do better?



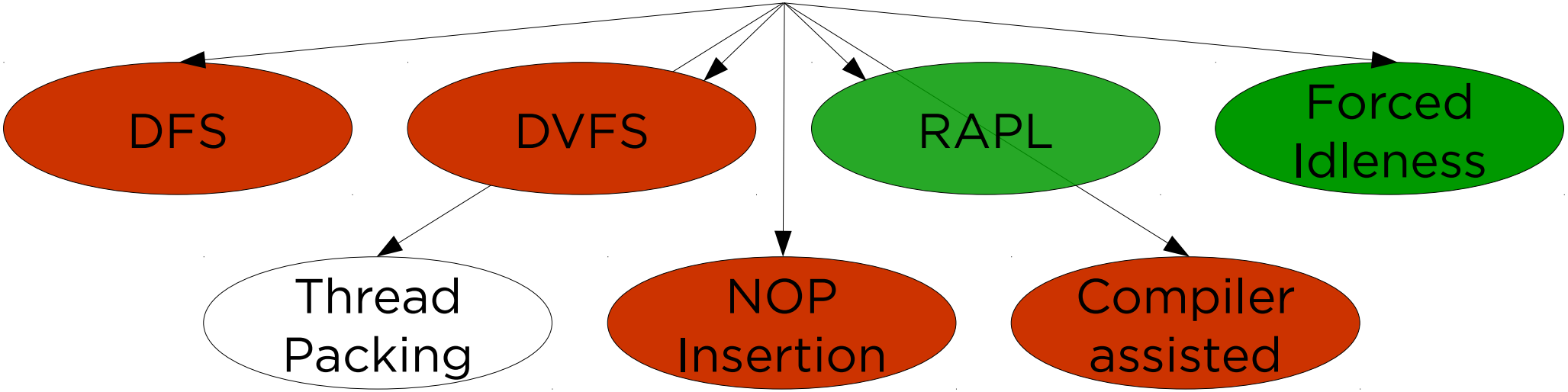
Can we do better?



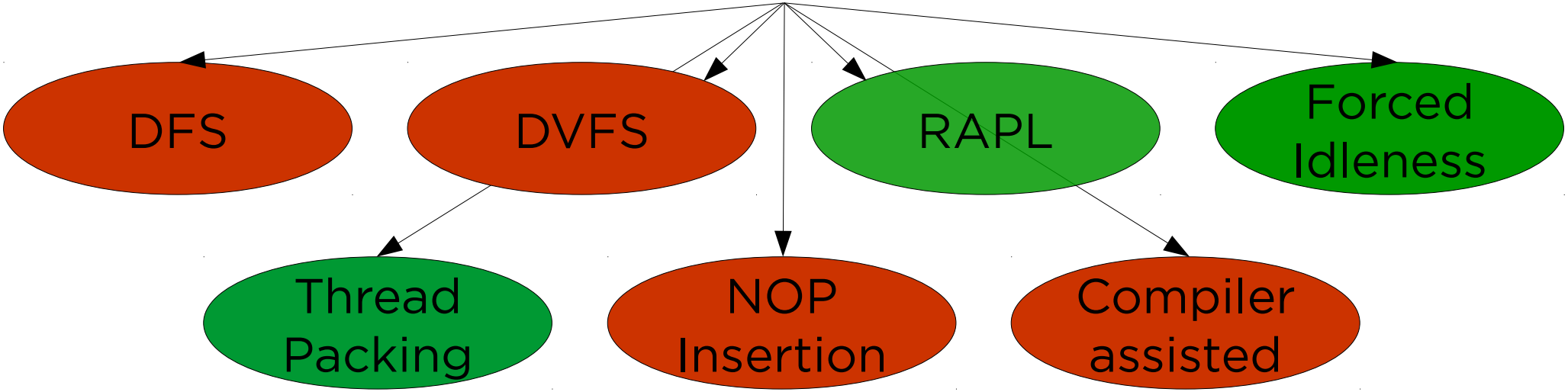
Can we do better?



Can we do better?

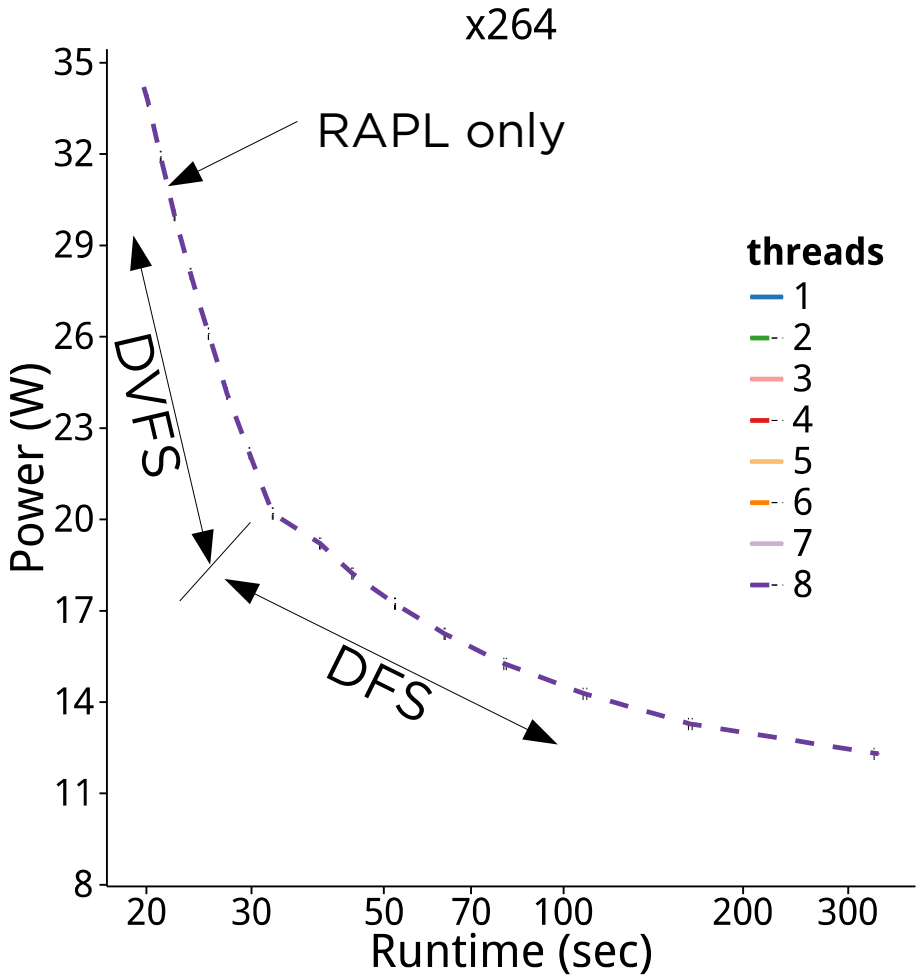


Can we do better?

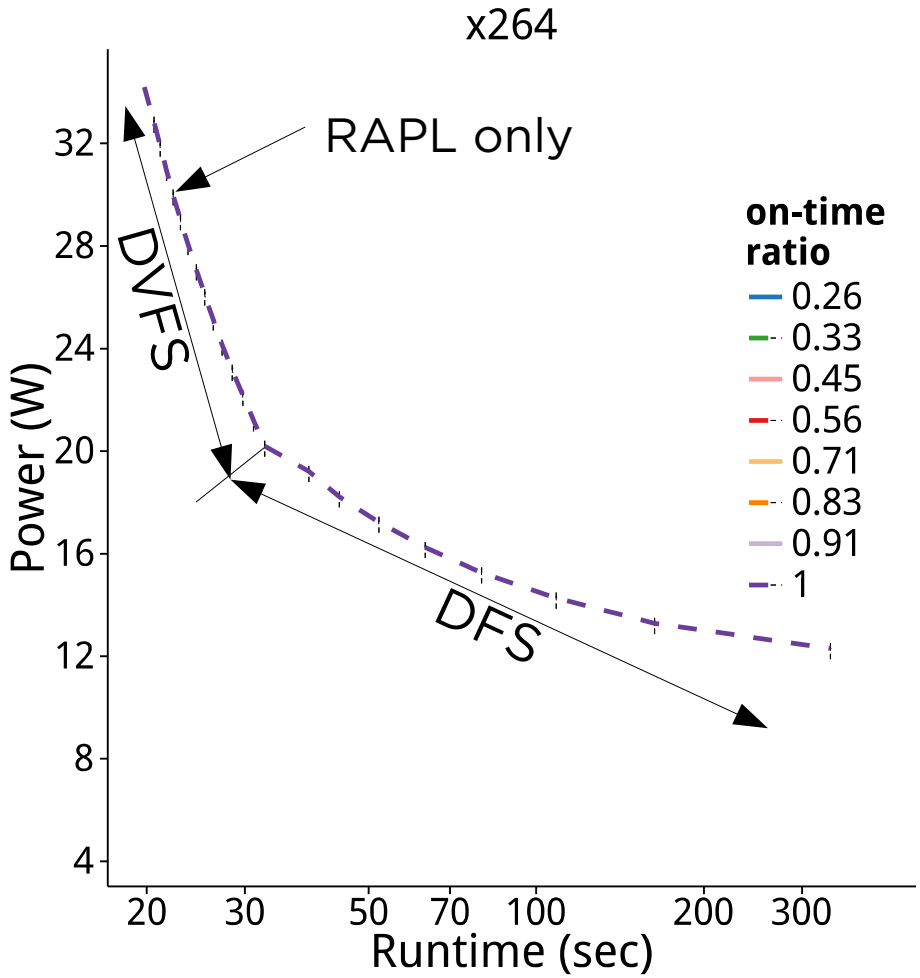


RAPL +

Thread Packing

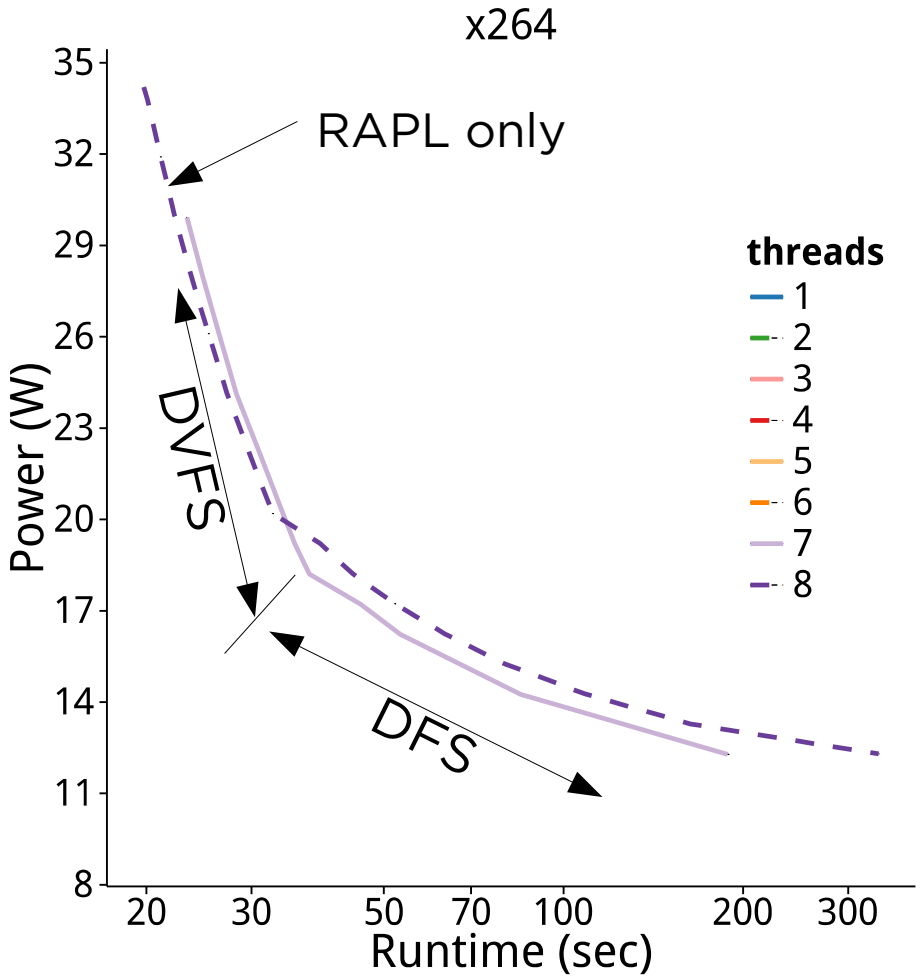


Forced Idleness

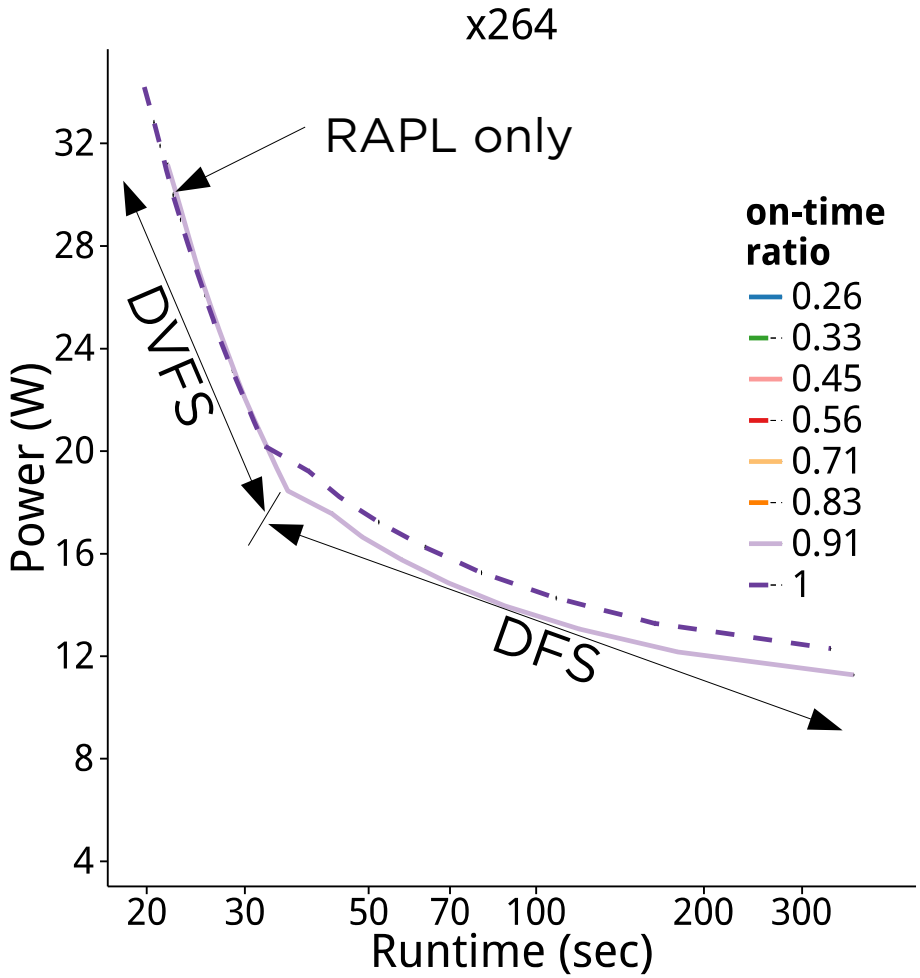


RAPL +

Thread Packing

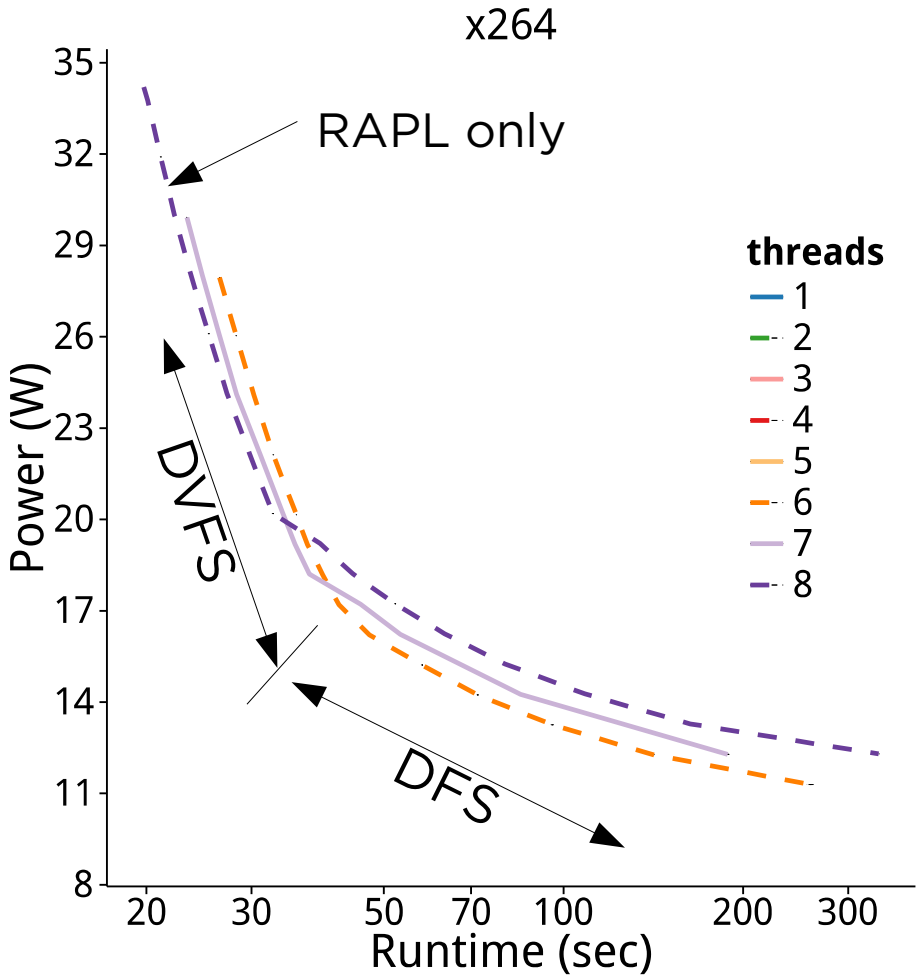


Forced Idleness

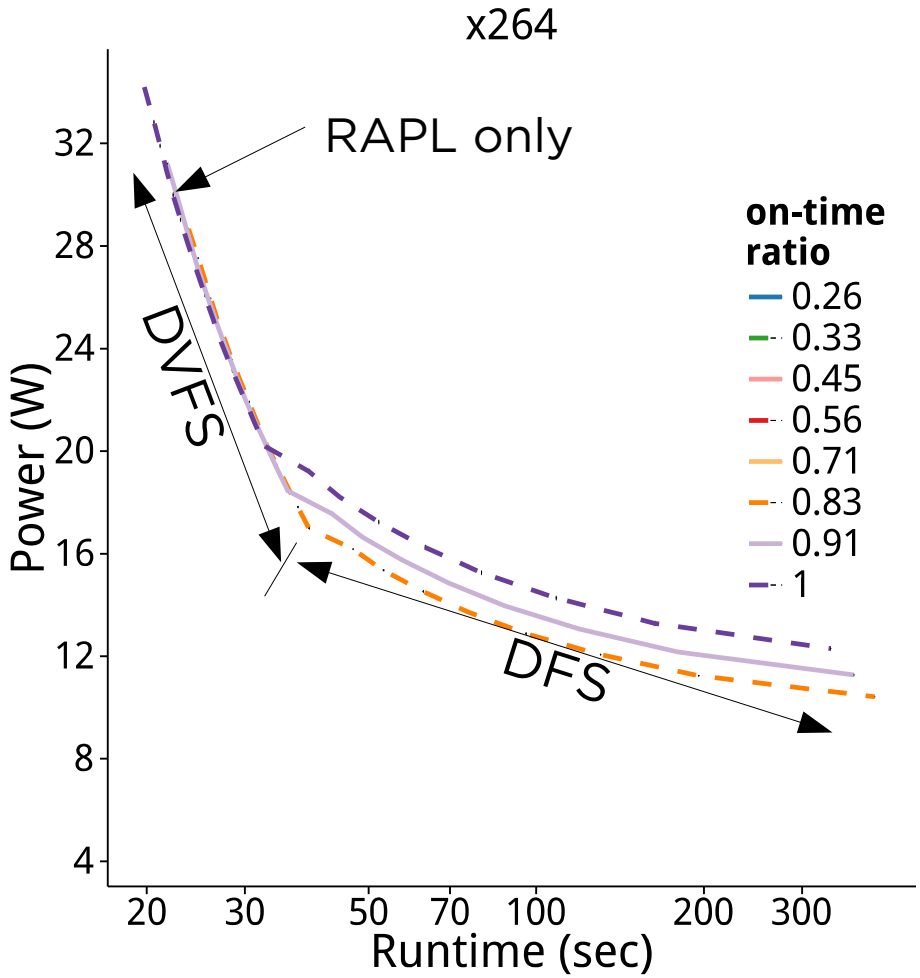


RAPL +

Thread Packing

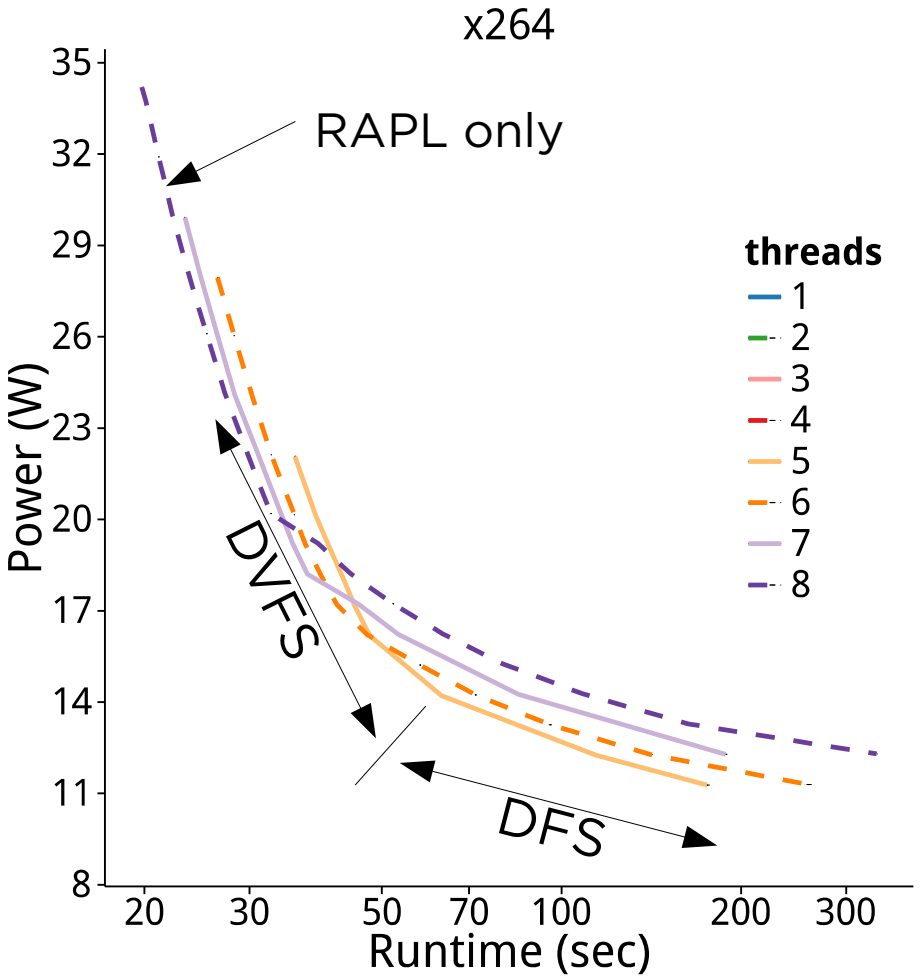


Forced Idleness

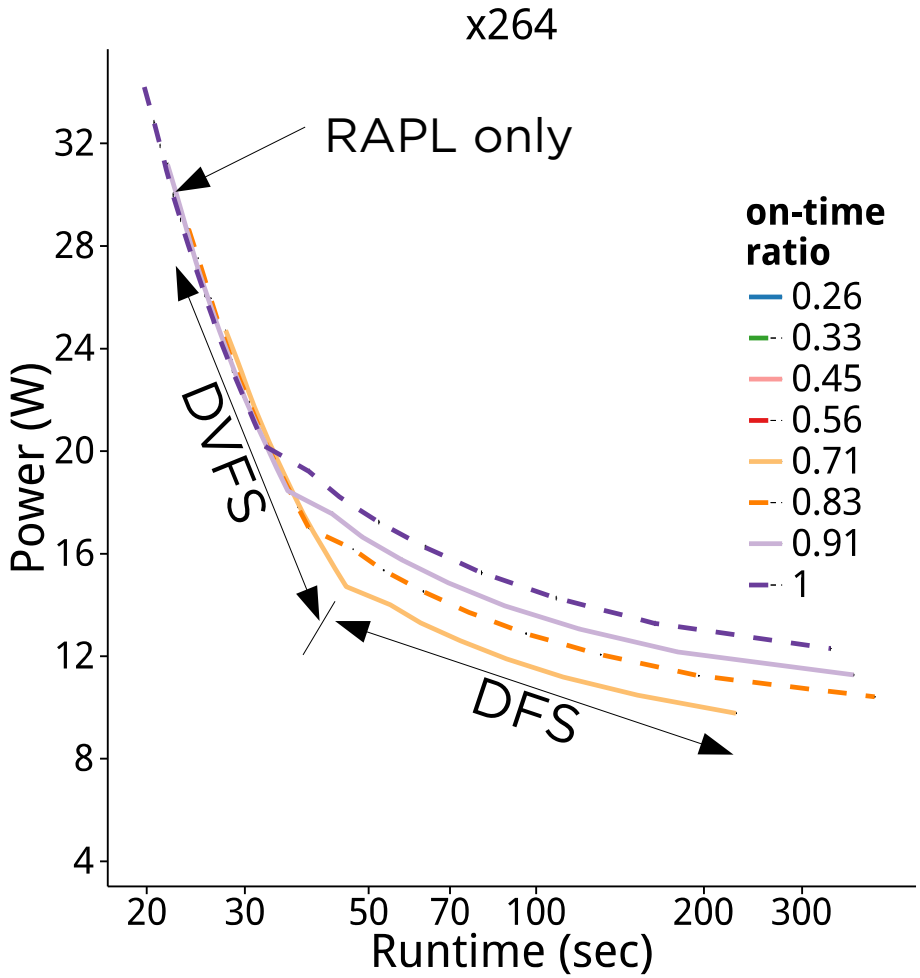


RAPL +

Thread Packing

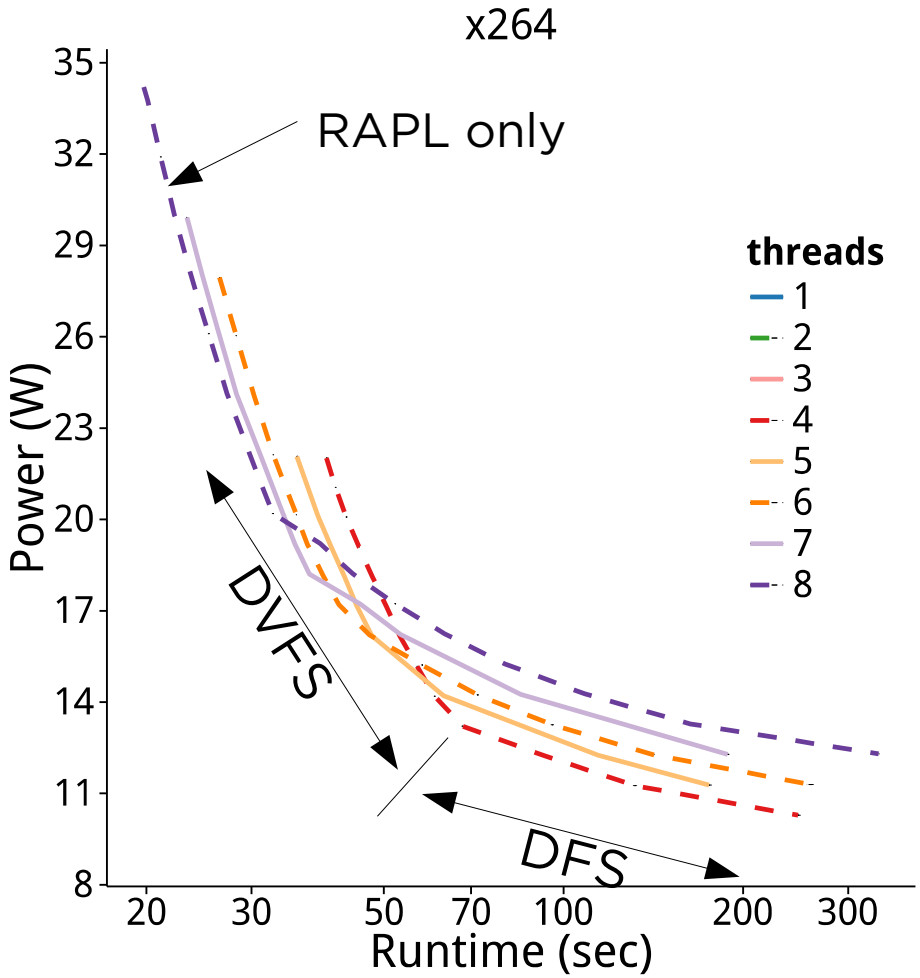


Forced Idleness

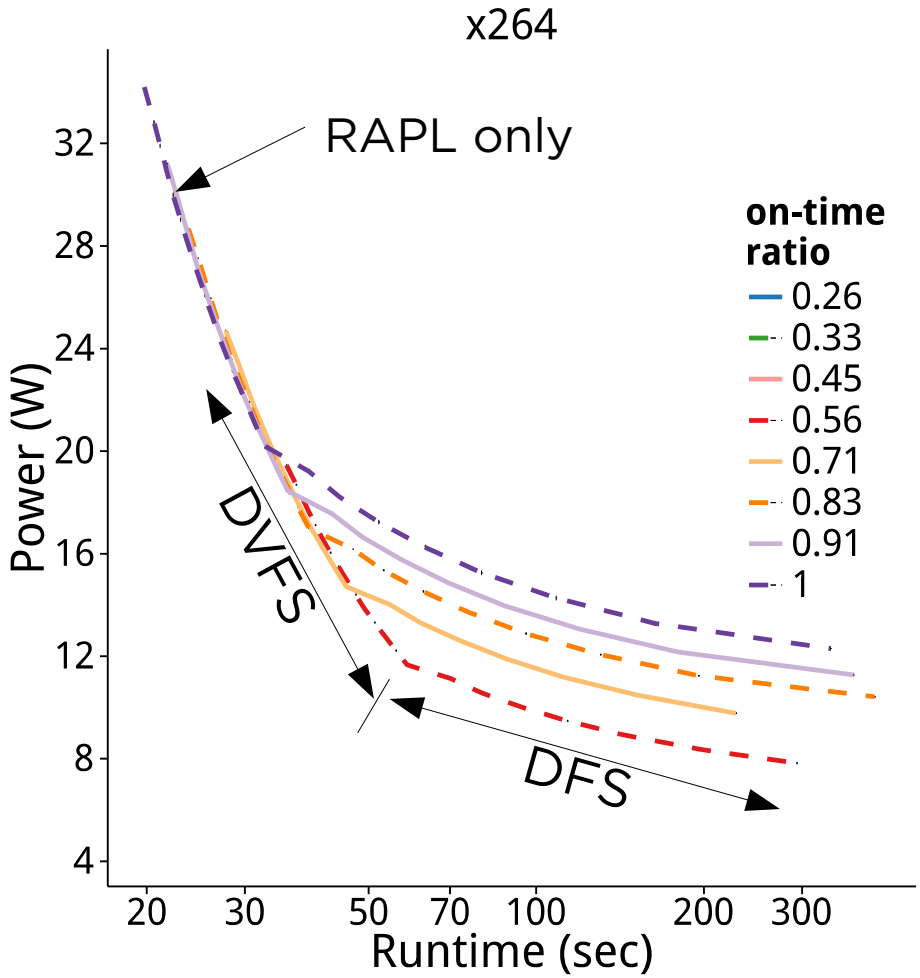


RAPL +

Thread Packing

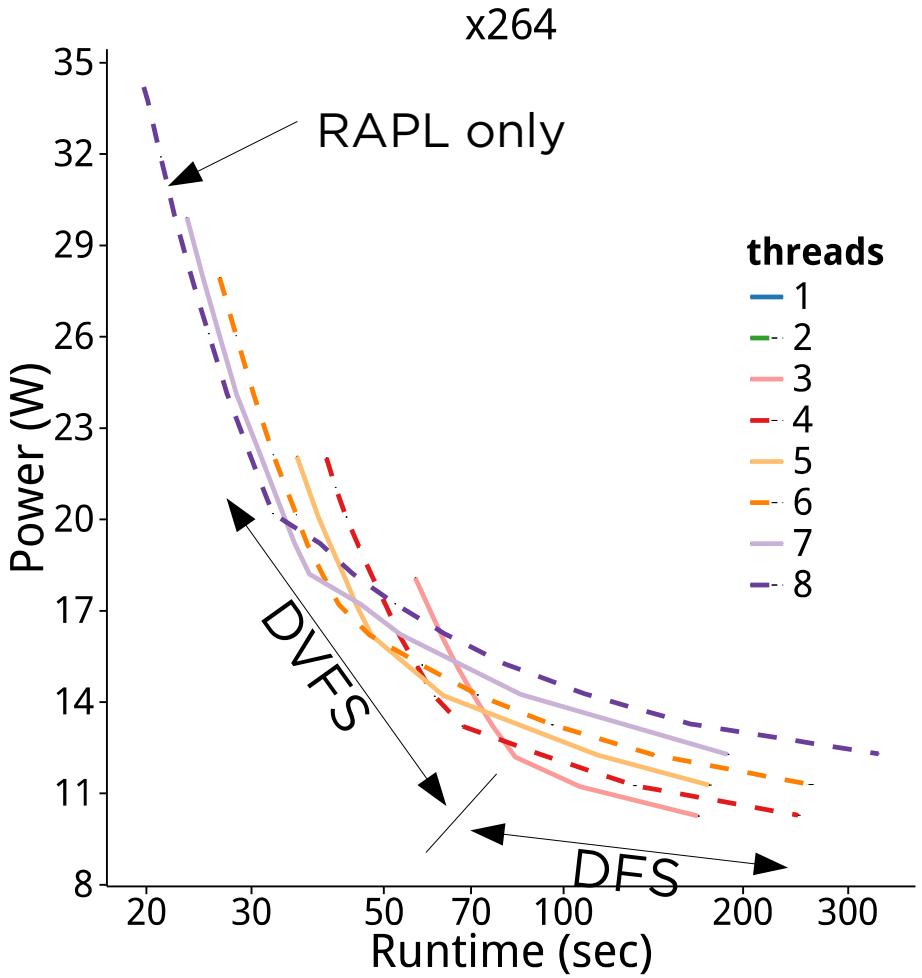


Forced Idleness

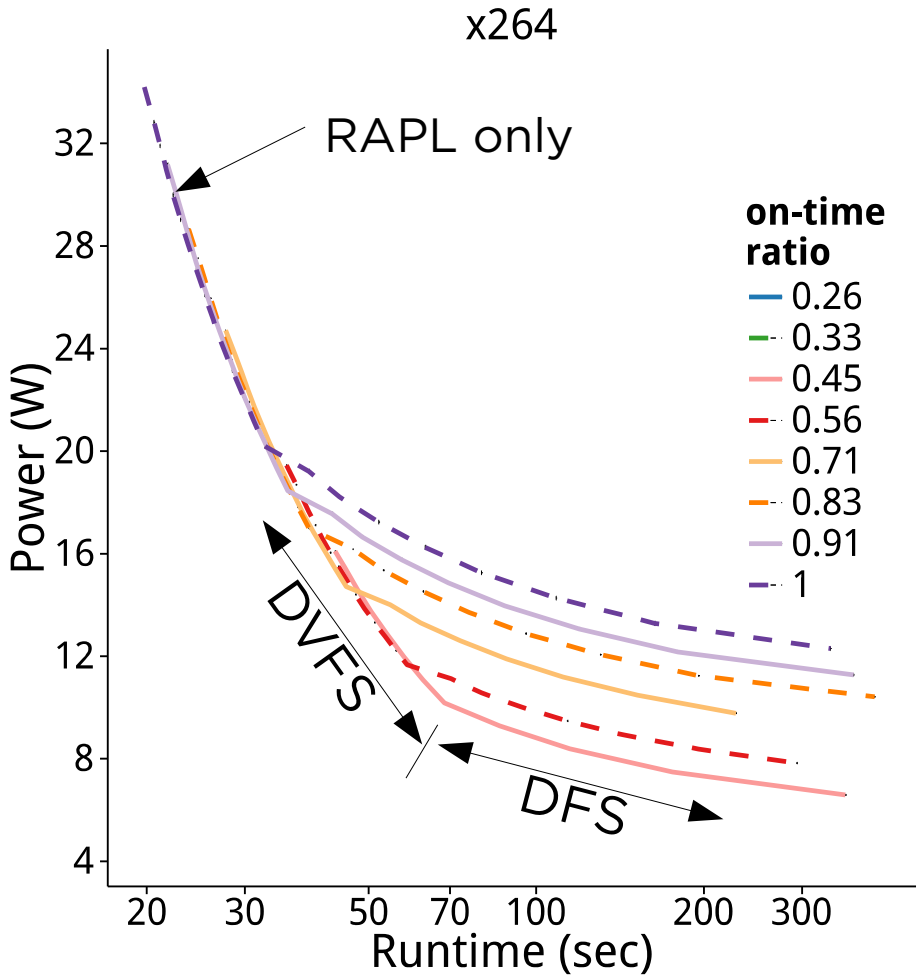


RAPL +

Thread Packing

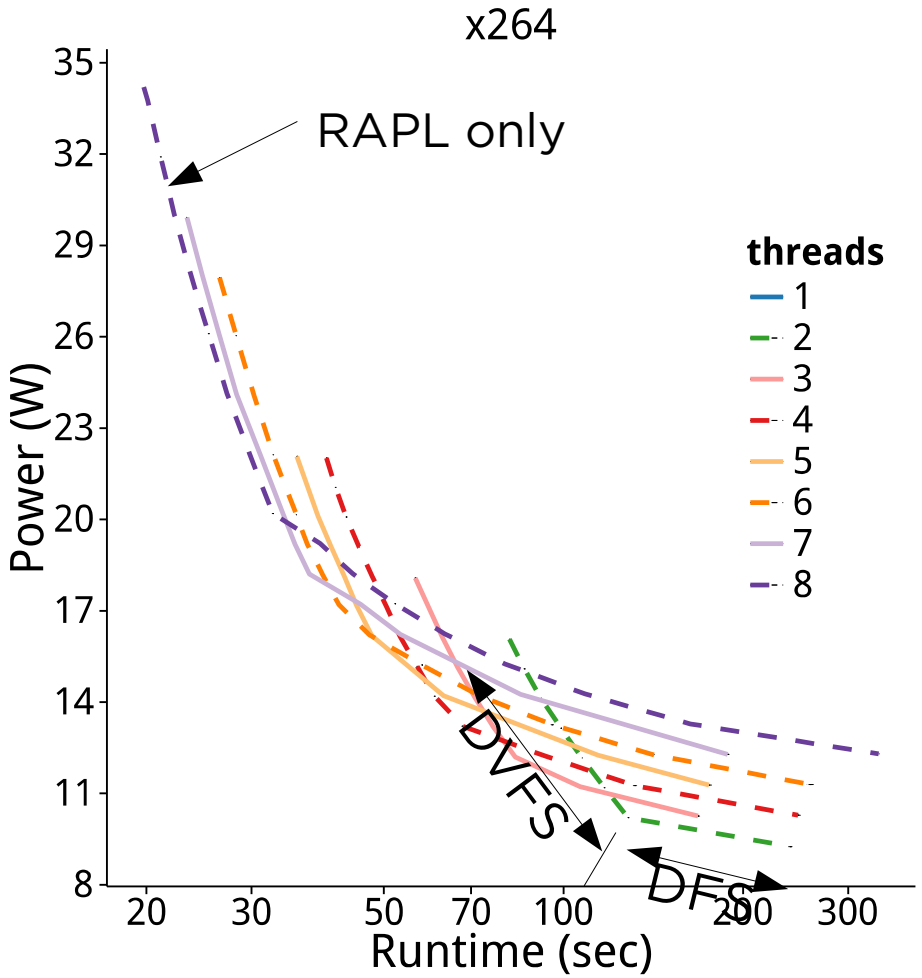


Forced Idleness

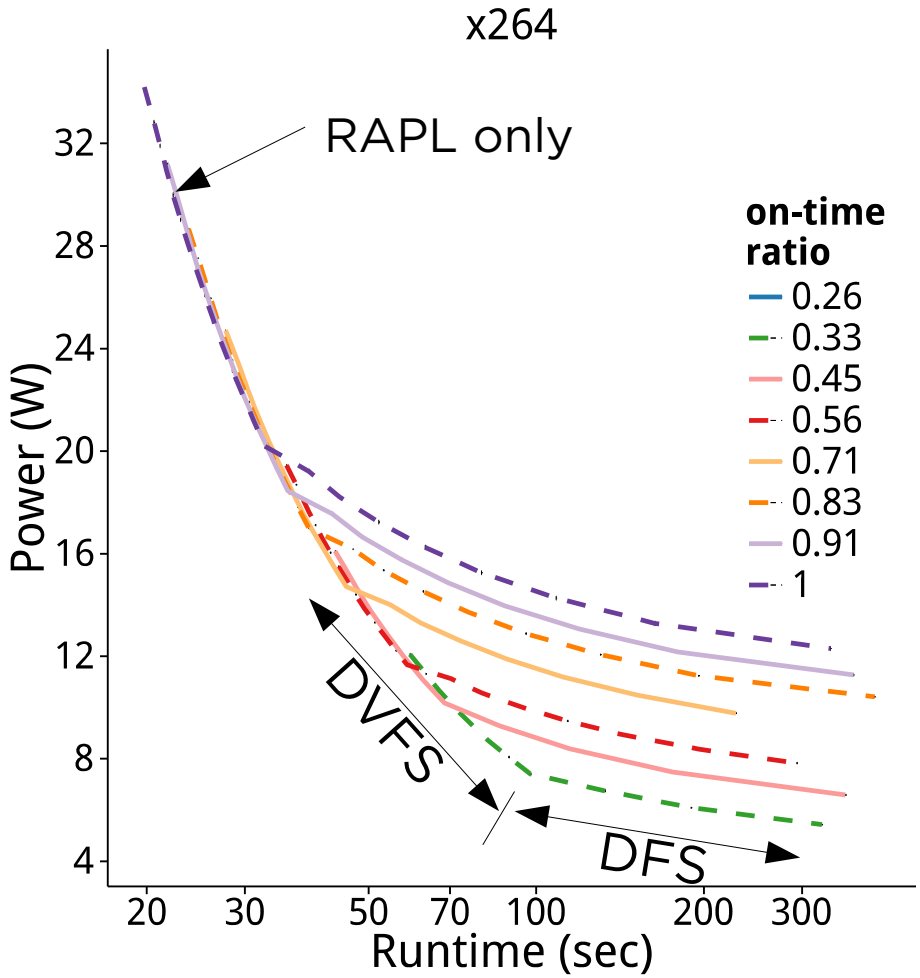


RAPL +

Thread Packing

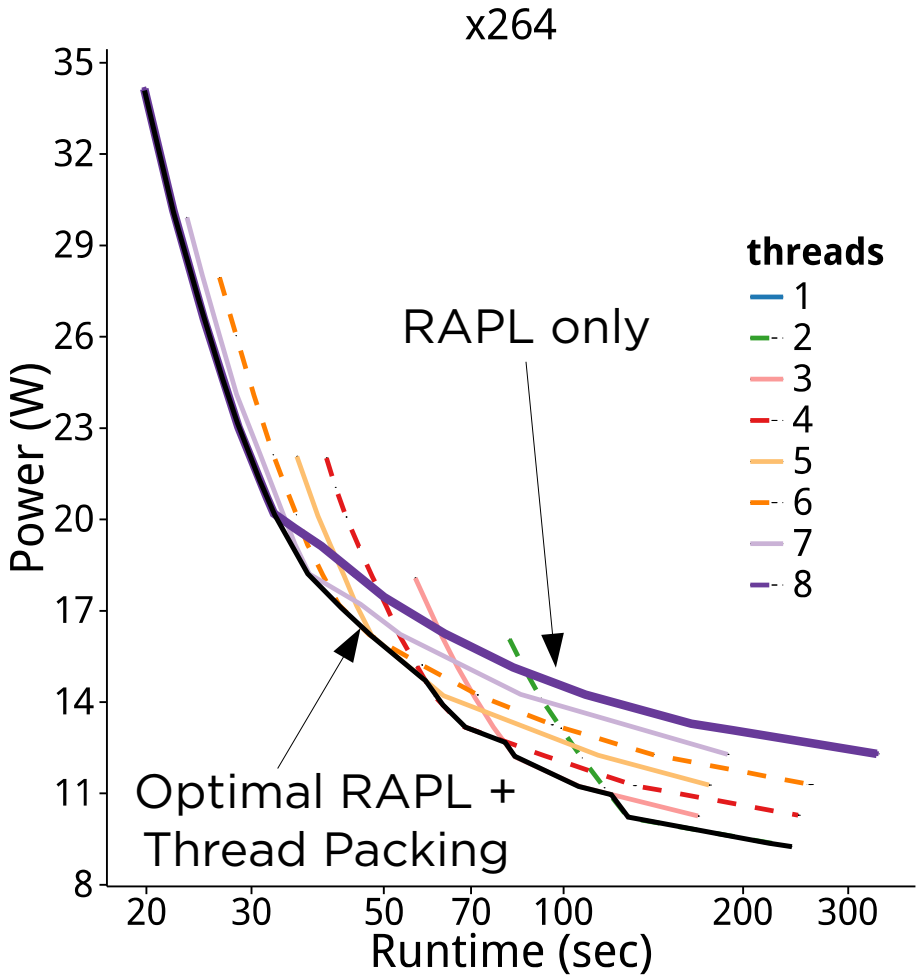


Forced Idleness

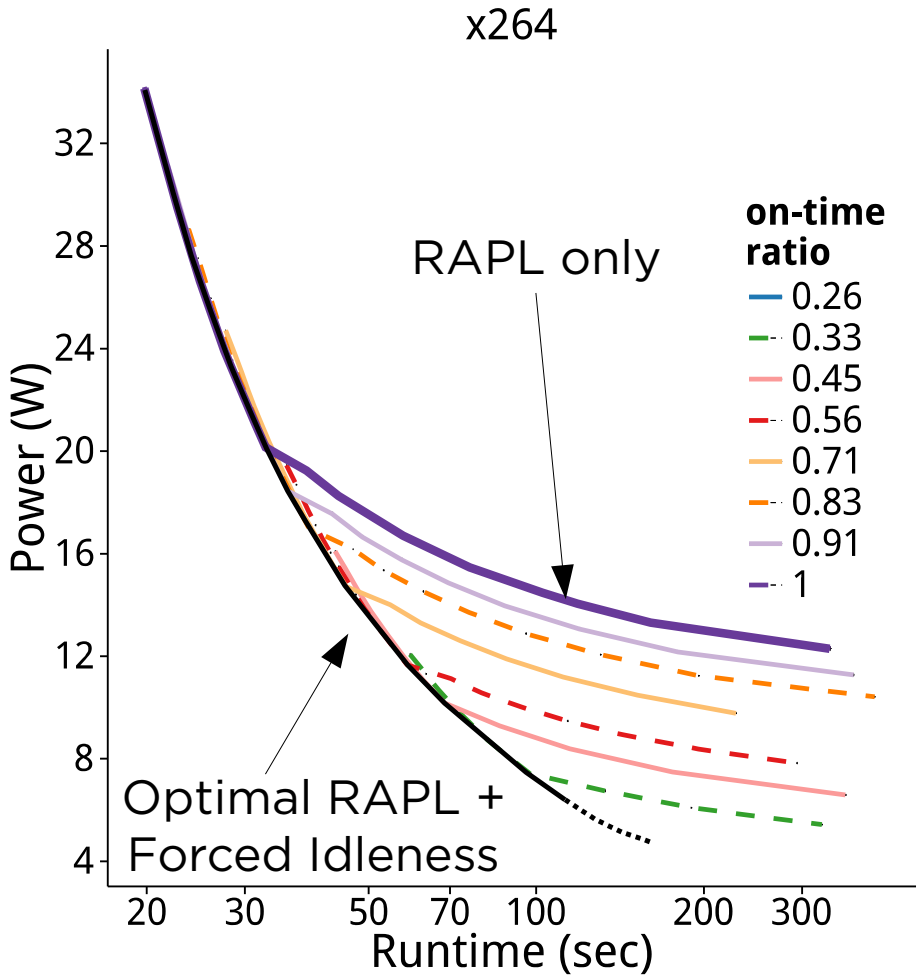


RAPL +

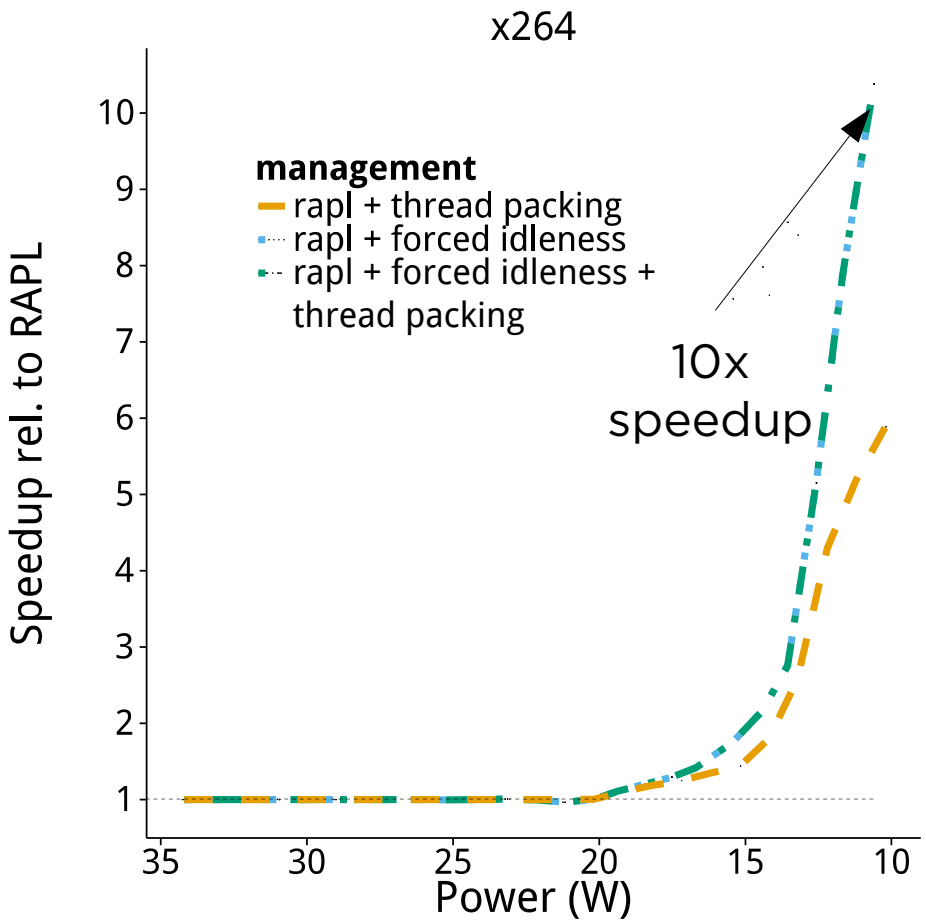
Thread Packing

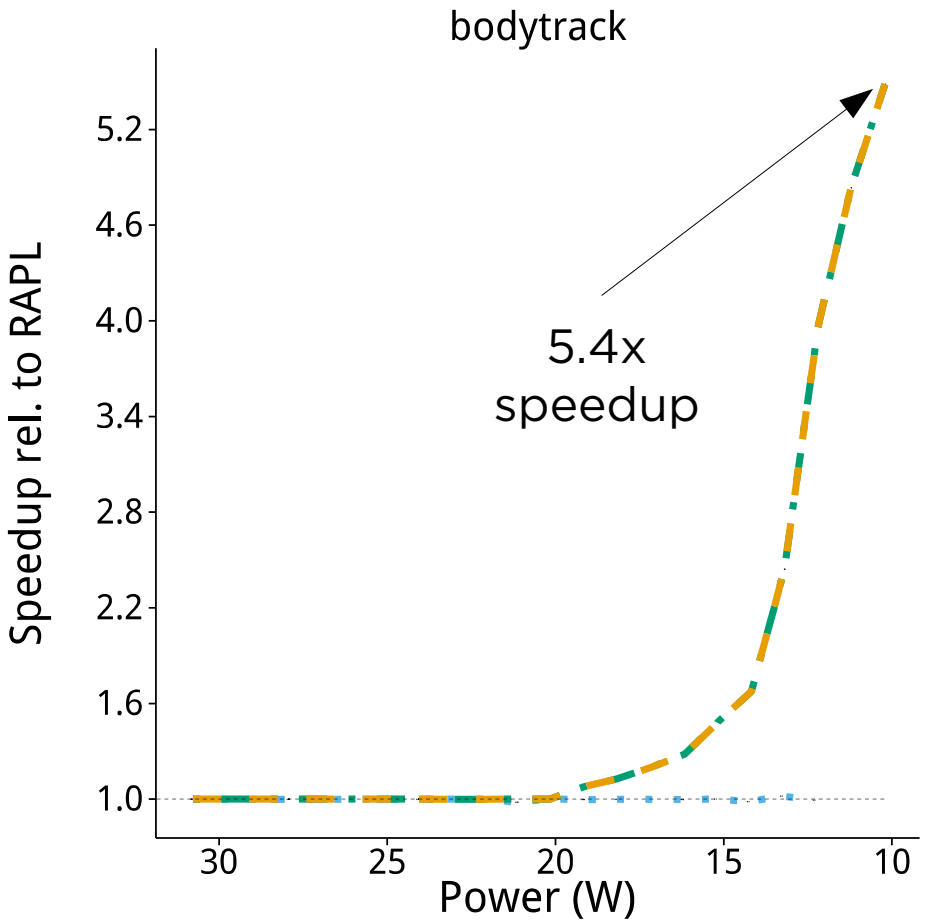


Forced Idleness

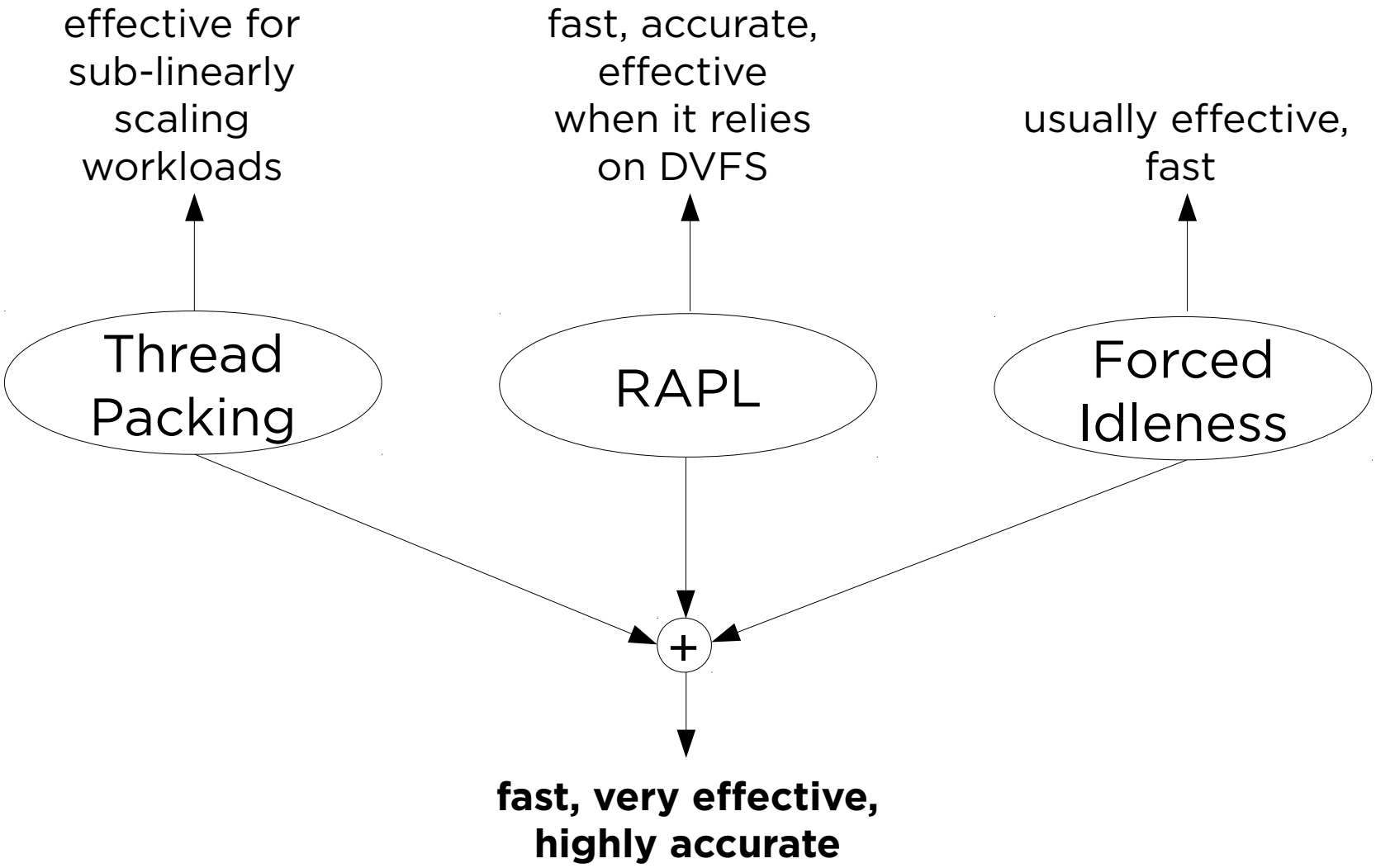


10x Speedup!


x264
Speedup rel. to RAPL
Power (W)
management
rapl + thread packing
rapl + forced idleness
rapl + forced idleness + thread packing
10x speedup
10
9
8
7
6
5
4
3
2
1
35
30
25
20
15
10


bodytrack
Speedup rel. to RAPL
Power (W)
5.4x speedup
5.2
4.6
4.0
3.4
2.8
2.2
1.6
1.0
30
25
20
15
10

Conclusions



Thank you!

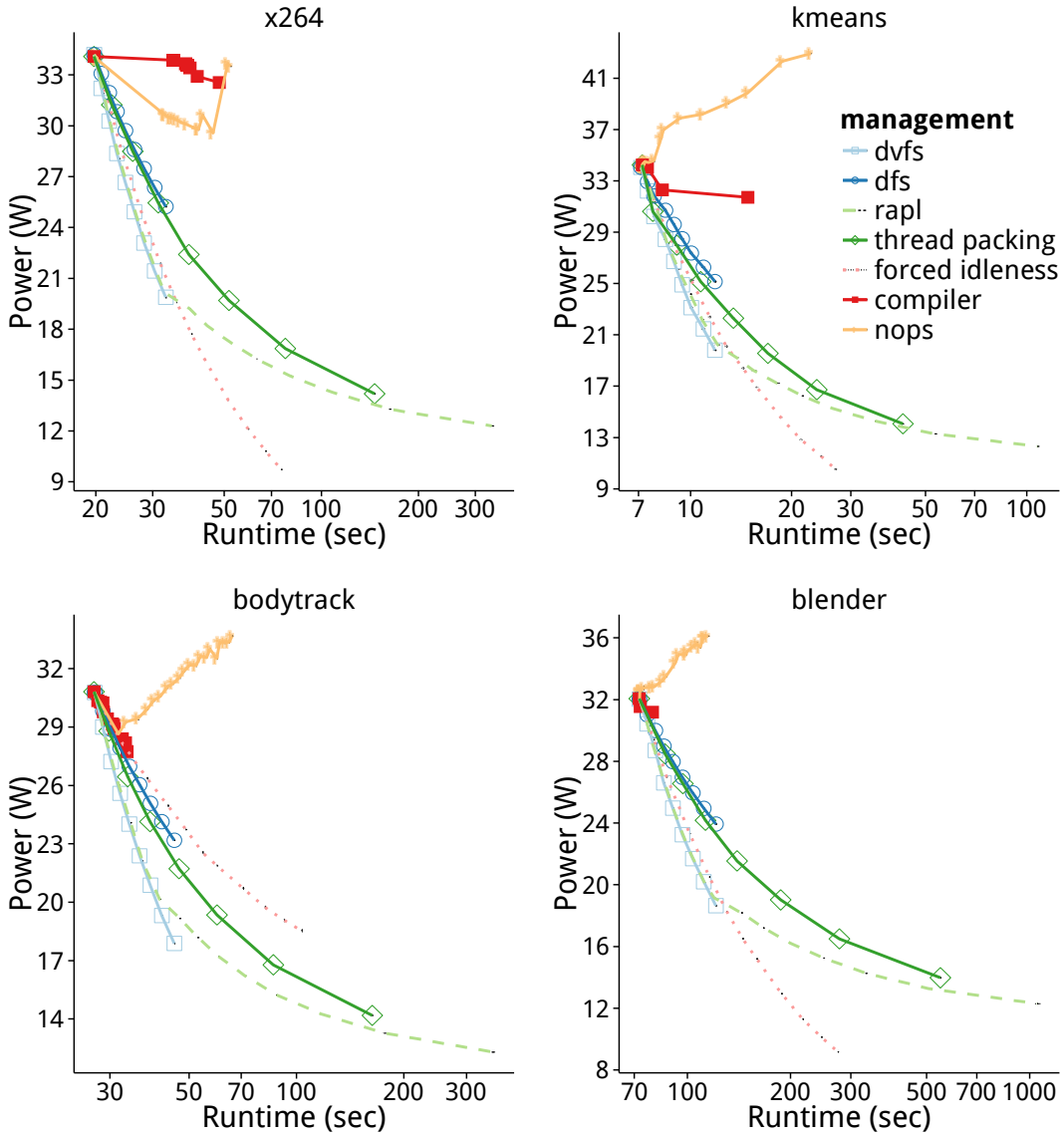
THE UNIVERSITY of EDINBURGH
informatics

Lancaster University

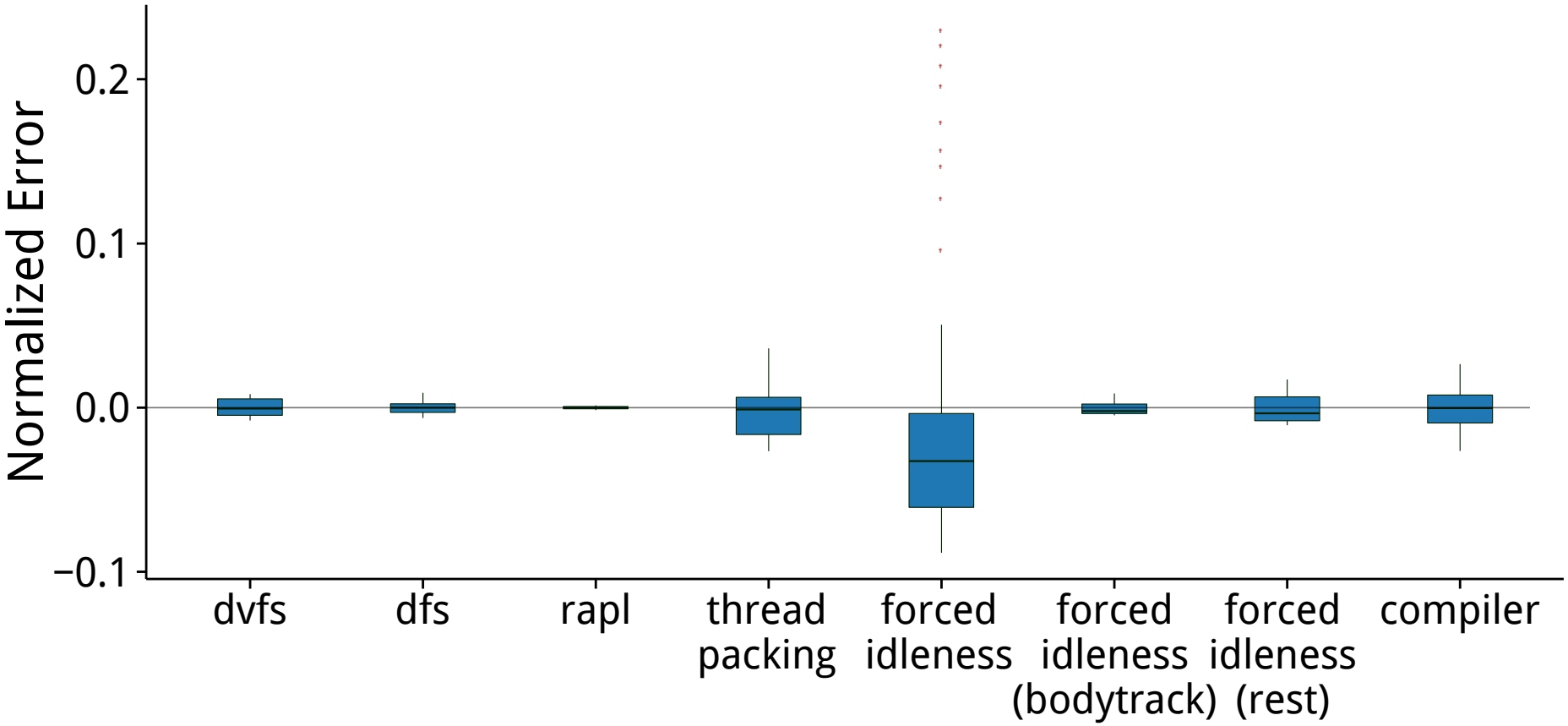
EPSRC
Engineering and Physical Sciences Research Council

Queen's UNIVERSITY

Effectiveness – all



Power predictability - Errors



Runtime vs Power Limit - all