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Overview of SOGI-Based Single-Phase Phase-Locked Loops for Grid Synchronization Under Complex Grid Conditions

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ABSTRACT Synchronization is the key part to ensure the high performance of grid-connected systems. Phase-locked loop (PLL) is one of the most popular synchronizations due to its simple implementation and robustness under certain grid variations. Particularly, in single-phase applications, PLL based on second-order generalized integrator (SOGI-PLL) is widely used because of its simple structure, certain filtering ability and frequency adaptability. The sensitivity of SOGI-PLL to the dc offset and low-order harmonics has been studied a lot in the literature and many solutions have been proposed. However, as more and more power electronic devices are integrated into the power grid recently, the grid condition becomes more complex. As a result, the nonlinear loop coupling phenomenon of SOGI-PLL is more severe and obvious and thus the performance of SOGI-PLL is degraded a lot, especially under the conditions of grid frequency variations and weak grid. A popular method is to use the frequency-fixed SOGI-PLL (FFSOGI-PLL) while how to eliminate the estimation error under frequency variations remain an important task. Though some scattered methods have been proposed, a simple yet effective strategy is still missing. Besides, it has been shown that the system stability margin will be reduced due to the negative-resistance behavior of PLL. However, the models derived in the current documents cannot accurately reveal the instabilities caused by the standard SOGI-PLL for missing the dynamics of the frequency feedback loop. Moreover, the PLL parameters are usually designed according to the PLL bandwidth to guarantee system stability under a weak grid. How to optimize the parameters is still unclear. In view of this, this article further summarizes and reviews the existing achievements of single-phase SOGI-PLL, and points out the problems to be solved and the development direction to improve the SOGI-PLL under more complex and non-ideal grid conditions.

INDEX TERMS Grid synchronization, single-phase phase-locked loop, second-order generalized integrator, complex grid condition.

I. INTRODUCTION

Due to the increasing depletion of fossil fuels and the environmental problems caused by their large-scale usage, renewable energy power generation has received extensive attention all over the world. As the penetration of renewable energy sources (RESs) such as solar and wind energy continues to increase, more and more power electronic devices are integrated into the power grid. As a result, the grid tends to exhibit very complex non-ideal characteristics (e.g., dc offset, harmonics, voltage drop, phase jump, frequency step or sweep and high grid impedance), and the stable operation and power quality of the utility grid is greatly challenged [1]–[3].

In grid-connected applications including active power filter, uninterruptible power supply (UPS), dynamic voltage restorer (DVR), flexible ac transmission (FACT), high voltage direct current (HVDC) transmission, controllable rectifier and distributed generation (DG), synchronization is one of the most important aspect [4]. Extracting the phase and frequency information from the grid voltage is of great significance for the monitoring, control and protection [5].

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At present, scholars have proposed many synchronization methods, such as zero-crossing detection, discrete Fourier transform, adaptive notch filter, Kalman filter, recursive weighted least squares method, artificial neural network, frequency-locked loop and phase-locked loop (PLL) [6]–[8]. Among them, the PLL technique is probably one of the most popular one used in grid-connected systems because of its relatively simple implementation and robustness under different grid conditions.

The PLL is a negative feedback closed-loop system, which is mainly composed of three parts: 1) a phase detector (PD), 2) a loop filter (LF), and 3) a voltage-controlled oscillator (VCO). The difference of various PLLs mainly lies in how the PD is constructed and how the phase error information is yielded. For PLLs in three-phase applications, a pair of orthogonal signals can be easily obtained through 3s/2s coordinate transformation (i.e., Clarke transform) from the measured three-phase voltage signal. However, in single-phase applications, for there is only one-phase voltage signal available, the PD structure of single-phase PLLs is more complicated, and many single-phase PLLs with different performance are derived in the literature.

The simplest single-phase PLL uses a multiplier as the PD, which is also known as the power-based PLL (pPLL) [9]–[12]. The PD output of the pPLL consists of a dc component and an ac component. The first term is the phase error signal while the latter one is a double-frequency term. The double-frequency component will generate oscillations in the pPLL and needs to be filtered out with an in-loop filter. However, the introduction of the filter greatly reduces the PLL bandwidth, resulting in a poor dynamic performance of this type of PLLs.

In order to solve the inherent double-frequency oscillation phenomenon in the pPLL, scholars turn to the PLLs based on the adaptive filter (AF-PLL) like enhanced PLL (EPLL) and the PLLs based on orthogonal signal generator (OSG-PLL). The EPLL is a frequency-adaptive PLL and can track the amplitude, phase and frequency of the input signal [13]. In the steady state, the double-frequency component is counteracted by the opposite component generated by the EPLL. Then, extra in-loop filter is not needed, and the dynamic performance is thus improved. However, the EPLL has large transient fluctuations, and is highly nonlinear due to the over use of sine and cosine operators, which can make the optimization of parameters and system performances very difficult. In comparison, the OSG-PLLs have received more attention.

For OSG-PLLs, common OSG construction methods include: $T/4$ (T is fundamental period) transfer delay (namely, the Delay-PLL) [14], first-order derivative operator (Deri-PLL) [15], all-pass filter (APF-PLL) [16], Hilbert transformation (Hilbert-PLL) [17], Kalman filter (KF-PLL) [18], [19], inverse Park transformation (Park-PLL) [20]–[22] and second-order generalized integrator (SOGI-PLL) [8], [23]–[25]. Among them, the Delay-PLL and Deri-PLL are simple, but their performances are greatly affected by grid frequency variations and harmonics [2]. Moreover, a differential operator is used in the Deri-PLL, which will amplify high-frequency components and deteriorate the performance under harmonics and noises. The APF-PLL uses an all-pass filter to shift the phase of the fundamental signal by 90°, but it does not perform well in presence of the frequency changes and harmonics. The ideal Hilbert transform cannot be realized directly because it violates the law of causality [3]. The practical Hilbert transform used is an approximation with a finite response filter (FIR) or an infinite response filter (IIR), and it is also affected by the changes in the grid frequency. The KF-PLL uses Kalman filtering technique to construct a pair of orthogonal signals at the cost of heavy computational burden. The Park-PLL and SOGI-PLL are two widely used single-phase PLLs that are immune to the change of the grid frequency, and have certain filtering ability. The Park-PLL uses a positive and an inverse Park transform and two low-pass filters (LPF) to form the PD, but the two coordinate transformation modules not only contribute to the difficulty of implementation, but also greatly increase the nonlinearity of the PD and thus the difficulty in modeling. In addition, the cut-off frequency of inner-loop LPFs of Park-PLL has significant impact on the dynamic performance, disturbance rejection capability, and even the stability of the whole PLL. Hence, a compromise is needed [3], yet further improvement is difficult. The SOGI-PLL uses two first-order integrator to construct the OSG based on second-order generalized integrator, which is easy to be implemented digitally, and the nonlinearity is lower than that of Park-PLL.

A well-known problem of the SOGI-PLL is the sensitivity to the dc offset and low-order harmonics. These problems have been studied long ago and now many useful methods are available. However, as the increasing integration of renewable energies and power electronic devices into the power grid, some other non-ideal grid conditions like frequency variation and weak grid are more severe and these new issues can affect the performance of SOGI-PLL a lot as well. To ensure the performance of SOGI-PLL under a more complex grid condition, it is necessary to comprehensively review recent advances and to point out the focus for future research. Note that the suppression strategies of dc offset and low-order harmonics are mature, while the loop coupling phenomenon is not well addressed until now. Hence, the solutions about the dc and low-order harmonics are briefly talked about hereinafter, and more attentions will be paid to the corresponding solutions under frequency variations and weak grid conditions, which can be the main contribution of the paper.

This study first introduces the working principles and basic characteristics of the SOGI-PLL. Then, the related studies are summarized from three aspects—dc offset and low-order harmonics suppression, nonlinear loop coupling phenomenon and grid frequency adaptability, and robustness in weak grid. The advantages and disadvantages of various methods are also reviewed. Finally, some discussions on the future research direction are presented.

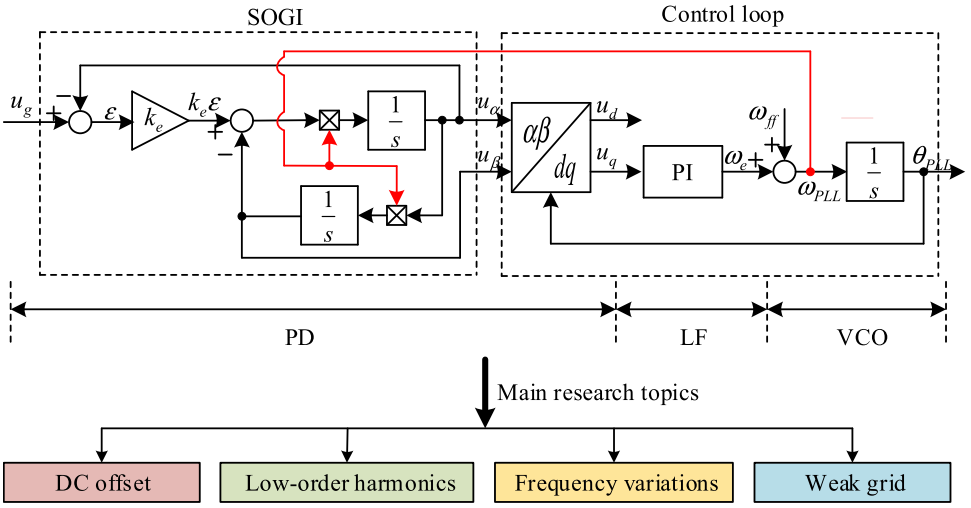

FIGURE 1. Block diagram of the SOGI-PLL and its main research topics.

II. WORKING PRINCIPLES AND BASIC CHARACTERISTICS OF SOGI-PLL

The structure of SOGI-PLL is shown in Fig. 1, in which u_g is the input signal, ω_{ff} (=$2\pi 50$ rad/s) is the central angular frequency, ω_{PLL} and θ_{PLL} are the estimated angular frequency and phase angle, respectively. It can be seen from Fig. 1 that the SOGI generates a pair of orthogonal signals (i.e., u_α and u_β), which are then sent to the Park transformation module (i.e., $\alpha\beta \rightarrow dq$) to obtain u_d and u_q

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} \cos\theta_{PLL} & \sin\theta_{PLL} \\ -\sin\theta_{PLL} & \cos\theta_{PLL} \end{bmatrix} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{1}$$

Assuming that the input signal is a pure sinusoidal in the form of $u_g = V_m \cos\theta_g$, and that the SOGI outputs a pair of signals with the same amplitude as the input signal and a phase difference of 90°, (1) can then be rewritten as

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} V_m \cos(\theta_g - \theta_{PLL}) \\ V_m \sin(\theta_g - \theta_{PLL}) \end{bmatrix} \tag{2}$$

It can be observed from (2) that u_d includes the amplitude information of the input signal while u_q includes the phase error information. By using the PI regulator as the LF to control u_q to zero and sending it to the VCO (represented by an integrator), the estimated phase angle θ_{PLL} can be equal to that of the input.

According to the Mason formula, the transfer functions from u_g to u_α and u_β can be deduced as

$$G_\alpha(s) = \frac{u_\alpha(s)}{u_g(s)} = \frac{k_e\omega_{PLL}s}{s^2 + k_e\omega_{PLL}s + \omega_{PLL}^2} \tag{3}$$

$$G_\beta(s) = \frac{u_\beta(s)}{u_g(s)} = \frac{k_e\omega_{PLL}^2}{s^2 + k_e\omega_{PLL}s + \omega_{PLL}^2} \tag{4}$$

where, in the steady state, ω_{PLL} is $2\pi 50$ rad/s. According to (3) and (4), the Bode diagrams of $G_\alpha(s)$ and $G_\beta(s)$ when k_e takes different values are drawn in Fig. 2.

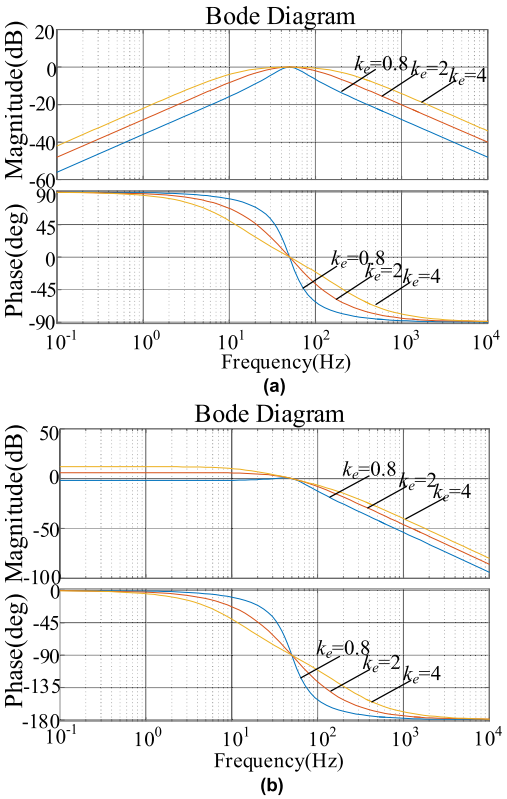

FIGURE 2. Bode plots of the transfer functions of the SOGI block for different values of k_e. (a) $G_\alpha(s)$; (b) $G_\beta(s)$.

As can be observed from Fig. 2, $G_\alpha(s)$ behaves as a band-pass filter (BPF) whose center frequency is equal to ω_{PLL}. The amplitude gain of $G_\alpha(s)$ at ω_{PLL} is unity and the phase lag is zero. Besides, $G_\beta(s)$ appears as a low-pass filter whose cut-off frequency is ω_{PLL} as well. The amplitude gain of $G_\beta(s)$ at ω_{PLL} is unity, and the phase lag is 90°. When k_e takes different values, the bandwidth of the system changes, but the amplitude gain and phase difference of $G_\alpha(s)$ and

$G_\beta(s)$ at ω_{PLL} always remain the same. It can be concluded that the output of the SOGI module is a pair of quadrature signals with the same amplitude as the input signal and a constant phase difference of 90°, and that the SOGI-PLL has a certain ability to suppress high-frequency disturbances. In addition, as shown in Fig. 1, the SOGI-PLL brings the estimated angular frequency ω_{PLL} back to the SOGI module to serve as the resonant frequency for SOGI (denoted as ω_r). In steady state, ω_{PLL} is equal to the frequency of the input signal, which makes the SOGI-PLL a frequency adaptive PLL.

However, it can also be found from Fig. 2(b) that $G_\beta(s)$ has almost no ability to suppress the dc components, indicating that the SOGI-PLL is sensitive to the dc offset in the input signal. Besides, reducing k_e to attenuate the characteristic low-order harmonics in the power grid can lead to a very poor dynamic response. To solve the tradeoff between the speed and accuracy, an extra filtering stage is usually utilized under distorted cases for the PLL. Moreover, the estimated angular frequency is fed back into the SOGI to ensure the frequency adaptability, but an additional feedback loop is also added in the SOGI-PLL. In other words, nonlinear coupling between the SOGI and the PLL control loop (from Park transform to θ_{PLL}) appears and makes the modeling and parameter design complicated. Furthermore, in the weak grid, the negative-resistance behavior of PLL can reduce the system stability margin [26], while the unique loop coupling problem of SOGI-PLL will become more prominent so that the estimation accuracy is seriously affected. The main research topics of the SOGI-PLL are shown in Fig. 1 and details will be described below.

III. SUPPRESSION OF THE DC OFFSET AND LOW-ORDER HARMONICS

A. SUPPRESSION OF THE DC OFFSET

A dc offset can be easily generated by many reasons, like grid faults, saturation phenomenon of the voltage/current sensor, dc injection of the distributed power generation system, and the AD conversion process of fixed-point digital signal processor [27], [28]. The presence of the dc component will result in oscillations at the fundamental frequency in the estimated frequency and phase angle of the PLL and thus cause the dc injection problem in the grid current since the current reference is generated by the PLL. Hence, many grid codes strictly restrict the dc value in the grid current. For example, in the standard IEC 61727, the dc offset is required to be less than 1% of the rated current [29].

To address the problem of the dc offset in single-phase PLLs, the existing solutions in the literature can be divided into three categories:

1) DIRECT FILTERING METHODS

When the input signal contains a dc component, using a filter is probably the most direct and effective method. Possible options are: sliding discrete Fourier transform (SDFT) [30], delayed signal cancellation (DSC) operator [31], moving average filter, notch filter (NF) [32], and complex coefficient filter (CCF) [33].

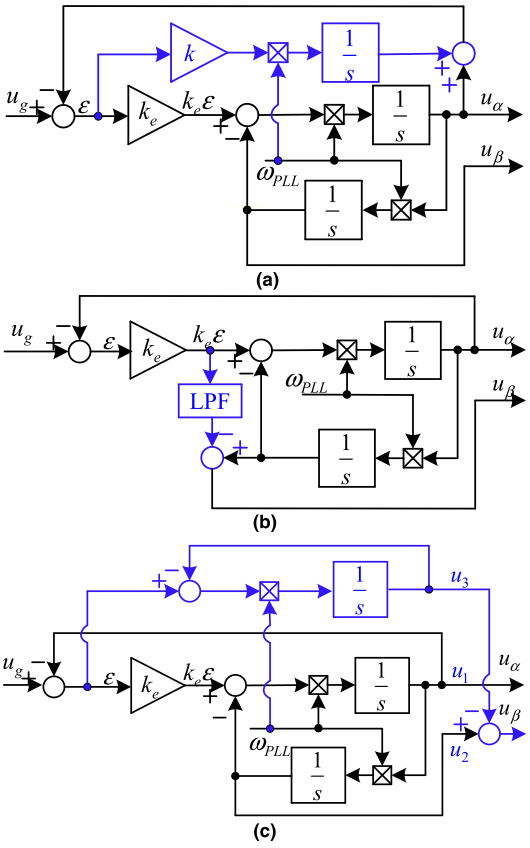

FIGURE 3. SOGI structures based on dc offset estimation. (a) Scheme proposed in [27]; (b) Scheme proposed in [39]; (c) Scheme proposed in [40].

Note that the core reason of the sensitivity to the dc offset in SOGI-PLL lies in the low-pass feature of $G_\beta(s)$, implying that reducing the dc gain of $G_\beta(s)$ may be another option to suppress the dc offset [34]. In [35], two SOGI blocks are connected in series (named the CSOGI-PLL) to reject the dc offset, and the dc gain of the new $G_\beta(s)$ decreases notably. Similar to [35], an all-pass filter is added behind the SOGI to obtain u_β [36]. In [37], a second-order SOGI-PLL (SO-SOGI-PLL) with a fourth-order transfer function is proposed, where the two first-order integrators in the typical SOGI-PLL are replaced by their second-order forms.

2) DC ESTIMATION AND SUBTRACTION METHODS

The second kind of methods to eliminate the dc component is to estimate the dc offset and then send it back to either the input side [27], [38] or the SOGI output (i.e., u_α and u_β) [39], [40] with a subtraction. The structures of three advanced solutions proposed in [27], [39], [40] are presented in Fig. 3.

3) NON-DC SIGNAL EXTRACTION METHODS

The third kind of dc elimination methods is to examine the transfer function from each signal point to the output of the

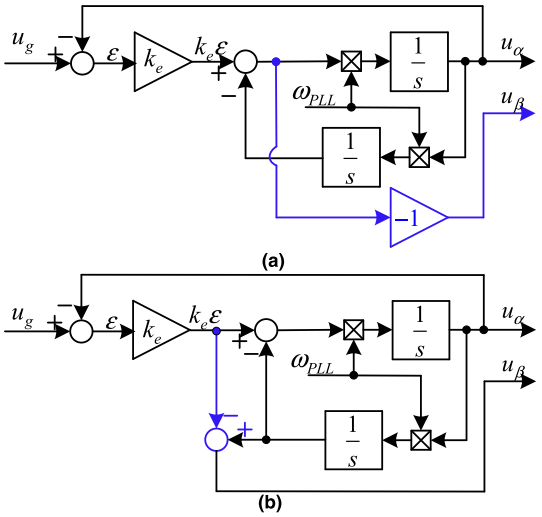

FIGURE 4. SOGI structures based on signals without dc offset. (a) Scheme proposed in [41]; (b) Scheme proposed in [42].

SOGI module, and then choose the signal that is not affected by the dc offset to create the new u_β.

Two equivalent methods are proposed in [41] and [42] and their structures are shown in Fig. 4. As shown in Fig. 4, a signal is drawn from $k_e\varepsilon - u_\beta$, which can be used as a new u_β after inverting. The transfer function of the new $G_\beta(s)$ is

$$G_\beta(s) = \frac{u_\beta(s)}{u_g(s)} = -\frac{k_e s^2}{s^2 + k_e\omega_{PLL}s + \omega_{PLL}^2} \tag{5}$$

Two zeroes appear in the new $G_\beta(s)$, which enhance the dc elimination by sacrificing the ability of suppressing the high-frequency disturbances.

B. SUPPRESSION OF LOW-ORDER HARMONICS

Due to the extensive use of various nonlinear loads, the grid voltage is often polluted with a large number of background harmonics, which cause certain fluctuations in the frequency and phase angle estimated by the PLL [43]. Correspondingly, the current reference generated by the PLL as well as the grid current will be distorted.

The commonly-used solution to suppress harmonics is to reduce the PLL bandwidth. However, this method sacrifices the dynamic performance and is not effective when the grid voltage contains large amount of low-order harmonics [44]. Existing solutions can be divided into three categories:

1) PRE-FILTERING METHODS

The first type of method is to place a filtering stage before the input signal passes into the PLL (i.e., pre-filtering) [45], [46]. This method, however, works well only when the grid frequency is the nominal value. Otherwise, a phase delay is unavoidable and an additional phase angle compensation unit or frequency adaptability link needs to be added [47].

2) IN-LOOP FILTERING METHODS

The second type of methods is to include an appropriate filter within the control loop of the PLL (i.e., in-loop filtering). Combined with the PI regulator, the disturbance suppression ability is improved a lot, but adverse effects are drawn on the stability and dynamic performance of the PLL itself [48].

3) OSG MODIFICATION METHODS

The third category is to enhance the filtering capability through the OSG modification of the PLL. For SOGI-PLL, its filtering capability comes from both the SOGI and the PI regulator. The PI regulator is located in the control loop of the PLL, which directly affects the stability and estimation accuracy. In other words, the PI ensures the PLL control loop to be a second-order system, which can achieve zero error in steady state under conditions of both phase and frequency jump. Without changing the structure of PLL control loop, the SOGI module can be modified to enhance the ability of harmonics suppression. In [37], based on this idea, the SO-SOGI-PLL is proposed to enhance the low-order harmonics rejection ability of the SOGI.

At the same time, some schemes reviewed in Section III-A can also be applied here to suppress the low-order harmonics for the SOGI-PLL [35]–[37].

IV. NON-LINEAR LOOP COUPLING PHENOMENON AND GRID FREQUENCY ADAPTABILTY

As Fig. 1 reveals, the SOGI-PLL has two interdependent feedback loops: one feeds the estimated phase angle θ_{PLL} back to the Park transform to obtain the phase error signal u_q, while the other feeds the estimated angular frequency ω_{PLL} back to the SOGI to dynamically adjust the resonant frequency ω_r for the SOGI. In other words, the SOGI and the control loop (also known as synchronous-rotating-frame PLL, SRF-PLL) are coupled together by this frequency feedback path and thus the performance of SOGI will be affected by the SRF-PLL. That is, however, a disturbance in either the SOGI or the SRF-PLL will influence each other. Note that the Park transform is a highly nonlinear part in the PLL so that the introduction of these feedback loops further increases the nonlinearity of the SOGI-PLL. As a result, the frequency adaptability is maintained with the feedback of the estimated angular frequency ω_{PLL} but at the cost of stability margin. Similar results can be found in [49] as well. Moreover, the SOGI and PLL control loop need to be considered together, which increases the complexity and difficulty in both the modeling and parameter design.

It is noted that, in the aspect of digital implementation, for the fixed frequency-based SOGI-PLL (where a fixed value of grid frequency is sent back to SOGI, named as FFSOGI-PLL), the computational burden is greatly reduced because the frequency of SOGI is not updated [50]. Meanwhile, the FFSOGI-PLL can achieve larger bandwidth, better stability margin and faster dynamic performance.

In view of this, some interests are attached to the study of FFSOGI-PLL. However, if the fixed resonant frequency of

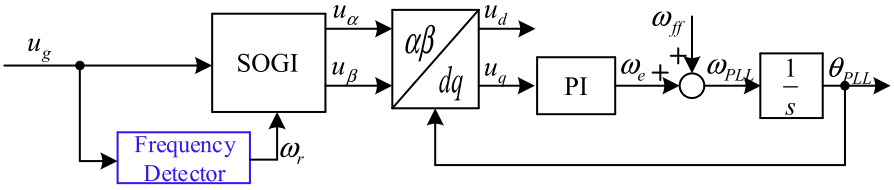

FIGURE 5. Block diagram of the FFSOGI-PLL based on parallel frequency detector.

the SOGI is not equal to the actual grid frequency, the estimated frequency of the PLL will contain a sinusoidal ripple at twice the grid fundamental frequency. The content of this second-order harmonic is closely related to the PLL bandwidth [35]. If the PLL bandwidth is increased larger, the total harmonic distortion (THD) of the current reference generated by the PLL can be larger and the current quality of the grid-connected converter is deteriorated. On the contrary, if the bandwidth is small, the settling time may be long and the transient performance is poor. Such case is undesirable in some cases like the low-voltage ride through (LVRT).

In order not to affect the PLL bandwidth and to eliminate or reduce the negative impact of the grid frequency variation on the FFSOGI-PLL, scholars have proposed many solutions, including parallel frequency detector based methods, phase error compensation methods and PLL structure modification based methods.

A. CATEGORY 1: PARALLEL FREQUENCY DETECTOR BASED PLL METHODS

By removing the original frequency feedback and connecting a frequency detector in parallel to the SOGI, the real-time frequency for the SOGI can be updated. Obviously, there is almost no coupling within the SOGI-PLL once the frequency feedback loop is replaced by the extra frequency detector. The basic structure of this method is shown in Fig. 5.

In [51], the fixed window DFT is adopted to obtain the fundamental frequency. Though the DFT technique cannot get an accurate result under time-varying cases due to the inherent spectral leakage and picket fence effect, such feature of the DFT is used to track the frequency of u_g adaptively. The main drawback of this method is the use of memory buffers to process the samples for the DFT operation.

In [52], Sun *et al.* combine the frequency-locked loop (FLL) together with the SOGI-PLL to realize the adjustment of the SOGI resonant frequency, named as SOGI with FLL (SOGI-WFLL). It should be noted that the FLL is actually a gradient estimator (GE) and three different GEs are proposed for the SOGI to estimate the fundamental frequency of the input in [53]. However, when the input signal contains the dc offset and harmonics, there will be certain fluctuations in the detected frequency, so that the accuracy of the PLL is affected. To reject the dc or harmonics, the methods in Section III or the multiple SOGI strategy can be used as a supplement. In addition, the proportional coefficient of the FLL has to be carefully chosen by the tradeoff between the detection speed and disturbance suppression capability.

In [54], a method based on the modulating function (MF) is used to detect the frequency. Since the product of the MF and the derivative of the input signal can be integrated into the product of the derivative of the MF and the input signal for integration, the high-frequency harmonics amplification of the input can be avoided. Moreover, the integral operation has low-pass filtering effect naturally so that this method is not sensitive to harmonics and noise. What should be taken into serious consideration is the selection of the window length or the forgetting factor value of the MF.

In [55], an approach based on fractional-order conformal mapping is adopted to construct the SOGI and is named as AFFSOGI-PLL. Its block is given in Fig. 6. The proportional gain k_e and the resonant frequency ω_r of the SOGI can be adjusted in real time by changing the fractional-order q to realize the frequency-adaptive feature for FFSOGI-PLL. The expression of φ / q is expressed as,

$$\frac{\varphi}{q} = \begin{cases} \pi - \tan^{-1}(\dfrac{\sqrt{4-k_e^2}}{k_e}), & 0 < k_e < 2 \\ \pi, & k_e > 2 \end{cases} \tag{6}$$

The AFFSOGI-PLL inherits the simplicity of FFSOGI-PLL and at the same time does not increase the system order. However, these features depend on the accurate value of q which is determined by the deviation of the grid frequency. It is hence indicated that the AFFSOGI-PLL requires an extra frequency detection link, but is not detailed in [55].

In [56], Shamim Reza *et al.* use a linear Kalman filter (LKF) to obtain a pair of orthogonal signals which are then sent into the FLL to estimate the frequency and amplitude of the input. This method is not sensitive to noise. However, the method proposed in [56] needs to know the initial value of the process noise, measurement noise and error covariance matrix in advance, and the initial estimation state also needs to be given manually. As a result, the implementation should be carefully dealt with.

The Teager energy operator (TEO) is introduced in [57] with only five consecutive samples and is easy to implement digitally. However, the TEO is shown to be sensitive to the frequency variation and harmonics in the input signal. Hence, the input signal must be pre-filtered first, and the frequency estimated by TEO is suggested to be fed back to the pre-filtering stage to avoid any phase offset errors caused by grid frequency variations.

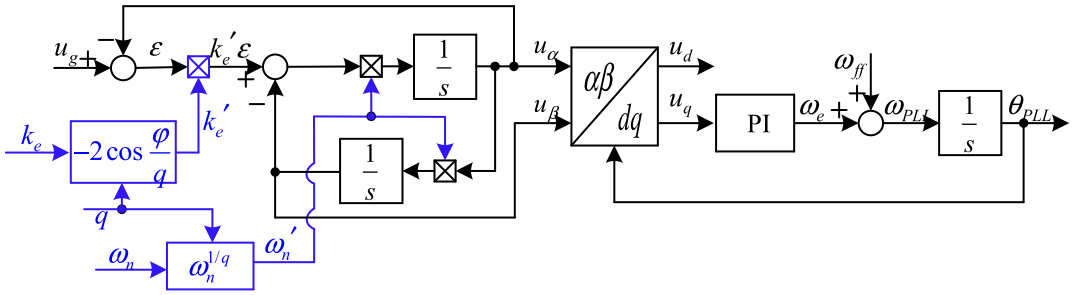

FIGURE 6. Block diagram of the FFSOGI-PLL based on fractional-order conformal mapping.

In summary, the parallel frequency detector based methods require a fast and accurate frequency detection. A simple yet effective solution is still ongoing. If the frequency detector has no filtering ability, the input signal must be pre-filtered, which means additional complexity in the implementation. It should be also noted that if the frequency of the input signal changes too fast, the resonant frequency of SOGI can keep on changing, which can eventually cause considerably large transient fluctuations in the quadrature signal output by SOGI and distortion in the grid current reference [58].

B. CATEGORY 2: PHASE ERROR COMPENSATION BASED PLL METHODS

The second kind for frequency adaptability of FFSOGI is to take the grid frequency deviation into consideration, and then to compensate for the generated phase difference under the off-nominal condition.

Assuming a pure sinusoidal grid voltage, i.e., $u_g = V_m \sin(\omega_g t + \Phi) = V_m \sin\theta_g$, with the help of (3) and (4), the steady state output of u_α and u_β can be obtained

$$u_\alpha = V_m \left|G_\alpha(j\omega_g)\right| \sin(\omega_g t + \phi + \angle G_\alpha(j\omega_g)) \tag{7}$$

$$u_\beta = -V_m \left|G_\alpha(j\omega_g)\right| \frac{\omega_r}{\omega_g} \cos(\omega_g t + \phi + \angle G_\alpha(j\omega_g)) \tag{8}$$

where

$$\left|G_\alpha(j\omega_g)\right| = \frac{k_e\omega_r\omega_g}{\sqrt{(k_e\omega_r\omega_g)^2 + (\omega_r^2 - \omega_g^2)^2}} \tag{9}$$

$$\angle G_\alpha(j\omega_g) = \arctan\frac{\omega_r^2 - \omega_g^2}{k_e\omega_r\omega_g} \tag{10}$$

Seen from (7) and (8), if $\omega_r = \omega_g$, the estimated phase angle is exactly the same as the input. However, a steady state phase error is unavoidable in the PLL output if $\omega_r \neq \omega_g$. In the following, two methods that compensate the phase difference are discussed.

Define

$$\theta_{error} = \arctan(-\frac{u_\alpha}{u_\beta}) - (\omega_g t + \phi + \angle G_\alpha(j\omega_g)) \tag{11}$$

With some mathematical manipulations [59], θ_{error} can be expressed as

$$\theta_{error} = \arctan\frac{(\frac{\omega_g}{\omega_r} - 1)\sin 2(\omega_g t + \phi + \angle G_\alpha(j\omega_g)}{2 + (\frac{\omega_g}{\omega_r} - 1)[1 - \cos 2(\omega_g t + \phi + \angle G_\alpha(j\omega_g)]} \tag{12}$$

Seen from (12), θ_{error} occurs as a second-order harmonic oscillation if $\omega_r \neq \omega_g$. Hence, once the oscillation caused by θ_{error} is filtered out, the fundamental frequency can be easily estimated with a differential operator.

Hence, in [59], Shamim Reza *et al.* propose to use a SOGI whose resonant frequency is larger than the fundamental frequency, and then compensate the errors of the estimated frequency and amplitude according to the frequency behavior of SOGI. Indeed, the dynamics is improved, for the settling time is inversely proportional to the product of k_e and ω_r. However, this method needs to use the phase unwrapping technique and a differential filter, which can be complicated. The computational burden is heavy. Furthermore, the phase angle cannot be estimated directly.

In [60], a different FFSOGI-PLL with using a phase error compensation (SOGI-WPEC) is proposed and its structure is shown in Fig. 7. It is analyzed that u_α and u_β have a constant phase difference of 90° at different frequencies while the amplitude difference relates with the ratio of ω_r/ω_{ff}. Then, if the amplitude of u_α and u_β is controlled the same, there will be no second-order harmonic oscillations in the steady state. However, seen from (7) and (8), there is a phase difference between the real phase angle θ_g and that of u_α, which can cause errors in the estimated phase angle. Hence, the core issue is to compensate the phase error at different frequencies accordingly. Compared with the typical SOGI-PLL, this PLL does not provided the significant improvement in the view of dynamic performance and harmonic suppression capability, but do have a better dc offset suppression capability [58]. In addition, unlike the SOGI-PLL, the FFSOGI-PLL proposed in [60] may be unable to estimate the grid voltage amplitude accurately under off-nominal frequencies.

It is pointed out in [61] that an inverse compensation filter can be added after the pre-filter to offset the error caused by the frequency offset. However, the frequency response

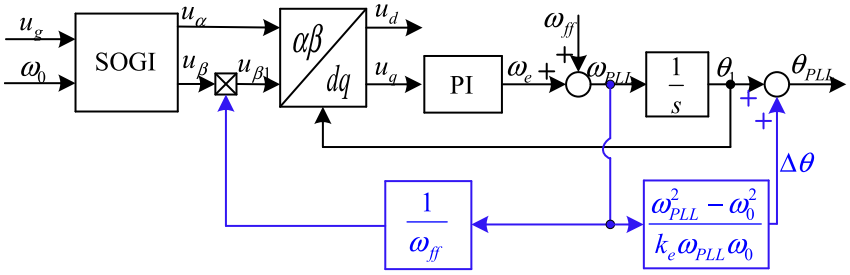

FIGURE 7. Block diagram of the FFSOGI-PLL based on phase error compensation.

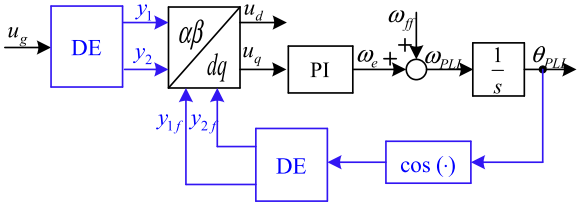

FIGURE 8. Block diagram of the FFSOGI-PLL based on derivative elements.

of this method near the fundamental frequency is relatively smooth, and the implementation of the inverse filter may be a little difficult because it is usually not a canonical system [62], [63]. At present, there is no literature attempting to apply the inverse filter into the FFSOGI-PLL under frequency variations.

To sum up, the key of the phase error compensation based methods is to find a proper way to accurately calculate the difference between the actual value and nominal value of the estimated phase angle under different working frequencies. It is noted that [58] and [60] examined the phase differences under some approximations (for instance, the assumption of $\omega_{PLL} = \omega_{ff}$), which can have a great influence on the accurate compensation. If the bandwidth of FFSOGI-PLL is small (e.g., in [60], the PLL bandwidth is only 32 Hz), it can be approximately considered that this assumption holds and the amplitude of u_α is nearly the same as that of $u_{\beta 1}$. In other words, the nonlinearity caused by feeding back the estimated frequency ω_{PLL} still exists but can be neglected under a small bandwidth condition. But, for a higher bandwidth, ripples in ω_{PLL} can turn larger and the amplitude of $u_{\beta 1}$ can have some oscillations which affecting the compensation accuracy. Therefore, under high bandwidth conditions, the phase angle error compensation still needs further study.

C. CATEGORY 3: PLL STRUCTURE MODIFICATION BASED METHODS

Contrary to the methods mentioned in Section IV-A and IV-B, the third category adjusts the structure of SOGI to obtain the necessary phase error information.

In [64], inspired by the idea of [60], Guan *et al*. propose a SOGI-PLL based on the differential elements (DE), named the DE-PLL or SOGI with DE (SOGI-WDE). The structure of DE-PLL is shown in Fig. 8. This PLL is not affected by grid frequency changes and does not introduce a frequency feedback loop into the OSG. It should be noted that the amplitude of the OSG output (i.e., y_1 and y_2 in Fig. 8) is not equal to the amplitude of the input signal, but the amplitude of y_1 and y_{1f}, y_2 and y_{2f} are the same in the steady state, respectively. Consequently, the product of y_1 and y_{2f}, y_2 and y_{1f} can be used to generate the phase error signal and the estimated phase angle. It is revealed that the DE-PLL can be transformed into a typical FFSOGI-PLL form whose phase angle feedback loop is equivalent to adding a SOGI into the feedback path [58]. Hence, from the perspective of small signal modeling, the DE-PLL is equivalent to the traditional SOGI-PLL.

D. DISCUSSIONS ON FREQUENCY VARIATIONS

Generally speaking, in order for the FFSOGI-PLL to be frequency-adaptive, most of the methods mentioned above have to add more algorithms which are usually a little complex. Here, to understand the performances of different methods, three relatively simple methods are selected for further comparisons, i.e., SOGI-WFLL [52], SOGI-WPEC [60] and SOGI-WDE [64]. Parameters follow the design methods in [58] and four cases are used to test their performances:

1) Case I: grid frequency steps from 50 Hz to 51 Hz and then to 55 Hz;
2) Case II: grid frequency sweeps from 50 Hz to 52 Hz at the rate of +10 Hz/s;
3) Case III: grid voltage sags from 1.0 p. u. to 0.6 p. u.;
4) Case IV: grid voltage contains 3^{rd} (5%), 5^{th}(4%), 7^{th} (3%) harmonics, and the total harmonic distortion is 7.07%.

The simulation is carried out in MATLAB/Simulink and corresponding results are shown in Fig. 9. As can been seen from Figs. 9(a) and (c), the SOGI-WFLL and SOGI-WDE behave larger overshoot than the SOGI-WDE. Besides, Fig. 9(d) indicates that both SOGI-WFLL and SOGI-WDE are sensitive to the harmonic contents in the grid voltage. As for the SOGI-WDE, it has a relatively nice performance but an oscillation at twice the grid fundamental frequency occurs in the PLL output, which is especially obvious if the difference between the real grid frequency and the nominal

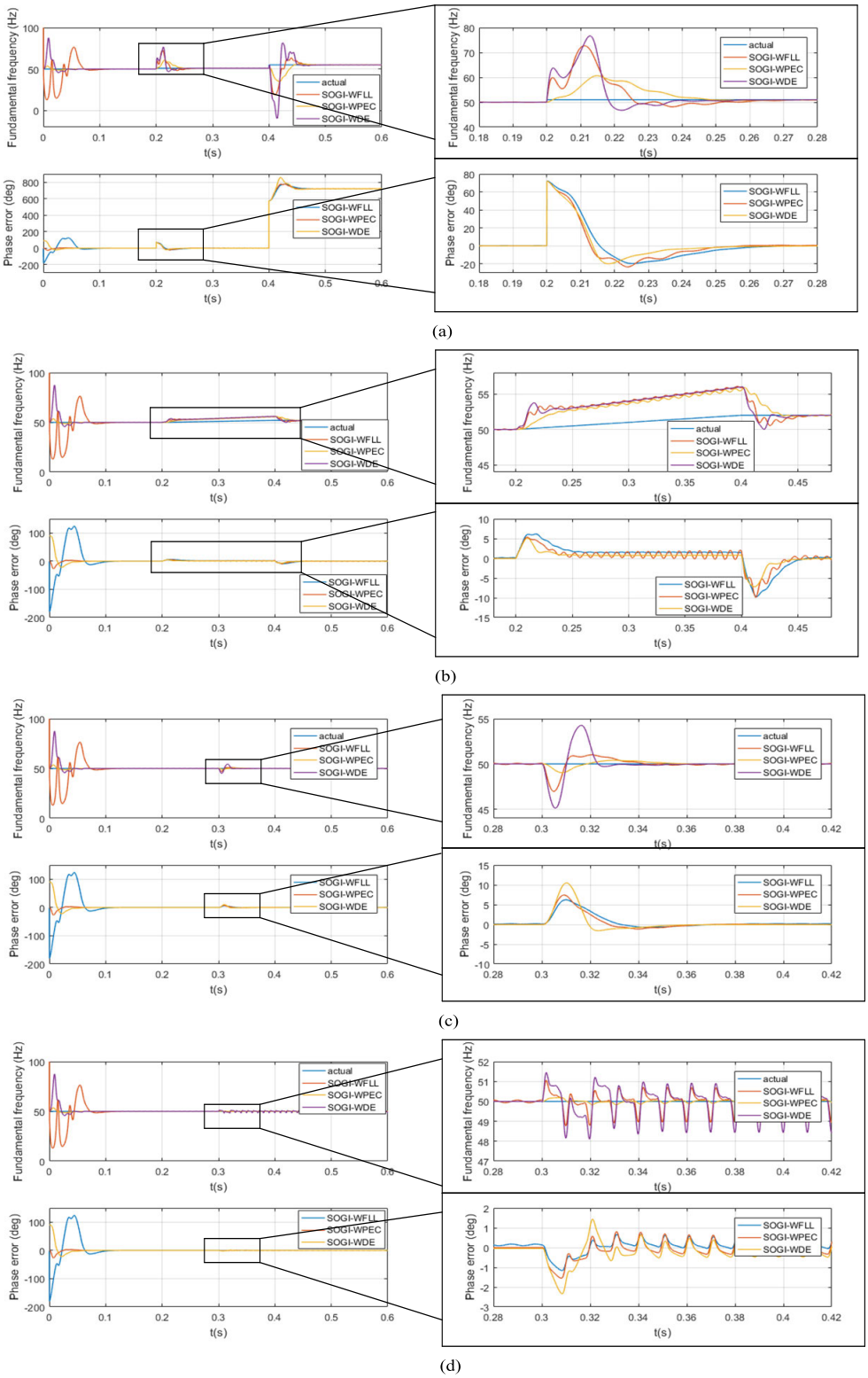

FIGURE 9. Simulation results of (a) Case I, (b) Case II, (c) Case III, (d) Case IV.

frequency is large. One interesting thing is that these PLLs have almost the identical performance in tracking a signal with frequency sweeping.

In summary, the FFSOGI-PLL is superior to the typical SOGI-PLL in terms of control design, dynamic performance and stability margin due to the absence of the coupled loops,

TABLE 1. Advantages and disadvantages of different frequency adaptability strategies for the FFSOGI-PLL.

Type of the FFSOGI-PLL	Example	Advantages	Disadvantages	Future direction
Category 1	Ref. [51] DFT-based PLL	➢ High filtering effect	➢ Resource-consuming ➢ Trade-off of the window size	Fast, accurate and relatively simple frequency detector
	Ref. [52] Combination of FLL and PLL	➢ Easy to implement ➢ Only one parameter is introduced in the PLL	➢ Limited filtering effect ➢ Trade-off of the frequency estimation parameter design	
	Ref. [54] MF-based PLL	➢ Inherent low-pass characteristic of the MF ➢ Fast tracking speed	➢ Resource-consuming ➢ Selection of the forgetting factor for the MF	
	Ref. [55] AFFSOGI-PLL	➢ Very easy to implement ➢ Adaptively adjust SOGI	➢ Need information of the frequency deviation ➢ No extra filtering effect	
	Ref. [56] LKF-based PLL	➢ High filtering effect ➢ Immune to the dc offset	➢ Prior knowledge of the LKF initial conditions ➢ Resource-consuming	
	Ref. [57] TEO-based PLL	➢ Fast tracking speed ➢ Easy to implement	➢ High computational burden ➢ Sensitive to harmonics	
Category 2	Ref. [59] SOGI with frequency error compensation	➢ No feedback loops ➢ Unconditionally stable ➢ High filtering effect	➢ Cannot estimate the phase angle directly ➢ Resource-consuming	More accurate PLL model
	Ref. [60] FFSOGI-PLL with phase error compensation	➢ Easy to implement	➢ Not accurate under high PLL bandwidth conditions	
Category 3	Ref. [64] DE-based PLL	➢ Low computational burden	➢ Sensitive to harmonics	New simple OSG with high-frequency disturbance rejection

but it is greatly affected by the grid frequency variations. The merits and drawbacks of three kinds of solutions listed in this section are summarized in Table 1. The principle of the parallel frequency detector methods is simple. The additional frequency detector does solve the influence of the coupled feedback loops, but increases the implementation cost. And, if the frequency detector does not have any filtering ability, an additional pre-filter is needed, which further complicates the implementation. The solutions based on the phase error compensations do not require additional frequency detector, but the accuracy of its output phase angle highly relies on the accuracy of modeling and error analysis. The third kind of methods (i.e., the modified PLL structure), requires neither the additional frequency detector nor the accurate calculation of phase angle errors, so that it might be a very promising solution. But the key of utilizing this solution is to ensure that the output of the phase detector is a pair of signals with a precise phase difference of 90° (note that the amplitude may be different from the input) and can suppress high-frequency components as well. Further research on the PLL structure modification methods can be necessary.

V. ROBUST PARAMETER DESIGN UNDER WEAK GRID CONDITIONS

With the rapid development of distributed power generations, the proportion of REPG is increasing year by year. Since the RESs are usually located far away from the main grid, the impedance of the transmission lines becomes non-negligible and the utility grid in remote areas tends to exhibit weak grid characteristics. In weak grid cases, the PLL and the grid are coupled through the grid impedance at the point of common coupling (PCC). Usually, the PCC voltage contains a large number of harmonics, which seriously affects the estimation accuracy of the PLL [65]–[69]. Meanwhile, previous studies have revealed that the PLL can exhibit negative-resistance characteristics within its bandwidth, resulting in significant phase reductions of the inverter output impedance. Thereby, the negative impact introduced by PLL would deteriorate the stability of the whole system [70]–[73]. However, the current research on the instability problems with PLL taken into consideration in the weak grid mainly focuses on the three-phase systems, yet the research on single-phase application is relatively few [74], [75].

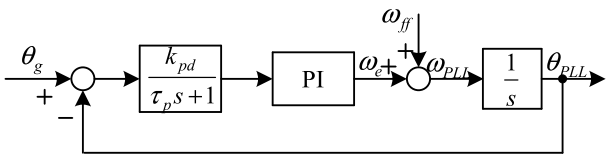

FIGURE 10. The conventional small-signal model of the SOGI-PLL.

A. MODELINGS OF THE SOGI-PLL

To analyze the influence of PLL on system stability, the PLL model must be derived first. The traditional modeling method is small-signal linear modeling. A well-known model of the SOGI-PLL is proposed in [8] and the structure is shown in Fig. 10, where $k_{pd} = V_m$ is the static PD gain of the SOGI-PLL and $\tau_p = 2/(k_e * \omega_{PLL})$ is the time constant [76]. The transfer function of the PI regulator is $k_p + k_i/s$.

In Fig. 10, the open-loop and closed-loop transfer function from θ_g to θ_{PLL} can be expressed as

$$G_{ol}(s) = \frac{k_{pd}(k_p s + k_i)}{s^2(\tau_p s + 1)} \tag{13}$$

$$G_{cl}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s)} = \frac{k_{pd}(k_p s + k_i)}{(\tau_p s + 1)[s^2 + k_{pd}(k_p s + k_i)]} \tag{14}$$

Seen from (13), two poles appear at the origin, making the model shown in Fig. 10 a typical type-II control system.

In early studies, for the sake of design simplicity, the PD dynamic of SOGI-PLL is usually neglected. Correspondingly, τ_p is viewed as zero, which makes the model shown in Fig. 10 a typical second-order system. Hence, (14) is rewritten as a typical second-order system transfer function, i.e.

$$G_{cl}(s) = \frac{k_{pd}(k_p s + k_i)}{s^2 + k_{pd}(k_p s + k_i)} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{15}$$

where ξ is the damping ratio and ω_n is the natural frequency.

For SOGI-PLL, the typical type-II control system model is more accurate than the typical second-order system model. However, both models only establish the transfer function from the phase angle of the input signal (i.e., θ_g) to the estimated phase angle of the PLL (i.e., θ_{PLL}). The relationship between the input signal and the PLL output (i.e., the current reference) is not revealed, which is of course more important in the modeling and stability analysis of the entire inverter-grid system in the presence of large grid impedance. In view of the above drawback, the perturbation and linearization method (also known as harmonic linearization) is proposed and the transfer function from the input signal perturbation to the PLL output perturbation can be established [74]. Then, by applying the impedance-based stability criterion, the influence of the PLL on the system stability can be analyzed.

Based on the perturbation and linearization method, the small-signal model of the Delay-PLL is derived in [74], and the impedance-based stability criterion is used to analyze the influence of current reference amplitude, power factor angle and PLL bandwidth on the system performance. In [77], the SOGI-PLL is regarded as the cascaded connection of SOGI and Delay-PLL, and the authors admit that the model might only be accurate when the considered frequency is smaller than the grid frequency. Then, in [78], Zhang *et al*. uses the perturbation and linearization method to further derive the small-signal models of the Delay-PLL and SOGI-PLL.

However, the studies mentioned above have all ignored the loop coupling characteristics of SOGI-PLL. In another word, the influence of the frequency feedback loop is not considered, and the feedback frequency ω_{PLL} is considered to be its steady-state value during the modeling process [79]. In other words, the SOGI-PLL is equivalently treated as the FFSOGI-PLL, so the theoretical analysis obtained using the existing model (ignoring the frequency feedback loop) may be inconsistent with the actual results, which is especially obvious in case of large grid impedance. As can be seen from the work presented in [49], the SOGI-PLL and FFSOGI-PLL do exhibit quite different characteristics under the weak grid. However, at present, the research on the accurate modeling of SOGI-PLL is still scarce.

It is pointed out in [80] that when the grid impedance or the PLL bandwidth is large, the frequency coupling effect of the PLL cannot be ignored anymore and the small-signal model at the fundamental frequency is no longer applicable. Therefore, in [80], a new modeling method of FFSOGI-PLL based on the extended harmonic linearization method has been proposed by considering the frequency coupling effect. Though the precision in stability prediction is improved, this model is a multi-input and multi-output (MIMO) system. As a result, some secondary components need to be ignored and the matrix order should be selected appropriately. A similar study using harmonic signal-flow graph has been done in [81] to investigate the frequency coupling under different bandwidth for the FFSOGI-PLL.

In addition, there are also some studies concerning the modeling methods under the large disturbance (for the three-phase SRF-PLL, while studies for the single-phase SOGI-PLL are lacking). The existing methods include the equivalent area criterion (EAC), the phase portrait, the Lyapunov stability analysis and the quasi-static large-signal analysis based methods [82]. These methods mainly take care of the characteristics of the PLL loop, while the inverter is modeled as a current source and the dynamic characteristics of the current loop and the output filter are ignored [83]. Hence, deficiencies are apparent of the modeling methods mentioned above in comprehensively studying the stability.

B. PARAMETER DESIGN IN WEAK GRID CASES

The parameters of PLLs are often designed under ideal grid conditions. Three parameters (i.e., k_e, k_p and k_i) of SOGI-PLL should be designed. The traditional trial-and-error method is very simple, yet a lot of trials and errors are needed to obtain a relatively satisfactory result. Currently, the parameters are mainly designed depending on the established PLL models as reviewed above.

TABLE 2. Merits and drawbacks of different models for the SOGI-PLL.

Model type	Merits	Drawbacks	Design method
Typical second-order system model [84], [85]	➢ Simple ➢ Can be used to design the PI regulator parameters	➢ The OSG is considered as a pure gain (steady state gain) ➢ Effect of the proportional coefficient k_e in SOGI is not included	Bandwidth-oriented method (the damping ratio is usually selected as 0.707)
Typical type-II control system model [8], [50]	➢ Can be used for systematically parameter design ➢ Effect of k_e is considered	➢ The OSG dynamics is simplified as an inertia unit ➢ Cannot be used in system impedance modeling	Symmetrical optimum method
Perturbation and linearization model [74], [77], [78]	➢ OSG dynamics is considered ➢ Can be used to analyze the PLL effect in weak grid cases	➢ Ignore the frequency feedback effect ➢ Ignore the high-frequency coupling components	Bandwidth-oriented method (the PLL model is simplified in the low-frequency range, i.e., several hundred Hz)
Extended perturbation and linearization model [80]	➢ Take frequency coupling effect into consideration	➢ System order is too high ➢ Still do not consider the frequency feedback effect	Not mentioned

The typical second-order system model in (15) are widely used to design parameters for PLLs, by ignoring the dynamic characteristics of SOGI. Then, only two parameters need to be designed: one is the damping coefficient ξ and the other is the natural frequency ω_n. Usually, choose ξ as 0.707 to balance the settling time and overshoot. In [84], Harnefors *et al.* recommend choosing ω_n to be one-tenth of the cut-off frequency of the current control loop from the perspective of avoiding interaction between the PLL and the current control. In [85], since a pre-filtering DSC is adopted, the in-loop disturbance suppression ability is not the main concern to design the PLL bandwidth. Hence, according to the design goal of optimal dynamic performance, ω_n is recommended to be ten times of the fundamental frequency. Then, based on the above guidelines, the PI parameters are obtained, while the proportional coefficient k_e for the SOGI (which is ignored in the PLL model) can be selected according to either the minimum settling time criterion ($k_e = 1.57$) [50] or the best damping ratio ($k_e = 1.414$) [32].

To be more accurate, as can be seen from (13), the model of Fig. 9 is a typical type-II control system. The commonly used design method for such system is the symmetrical optimum method whose main idea is to obtain the maximum phase margin at the cut-off frequency [86]–[88]. The parameters are usually determined by the requirements of stability margin, transient speed and harmonic suppression ability in [8], [12]. In particular, in [50], k_e and the PI parameters of FFSOGI-PLL are designed according to the criterion of the shortest SOGI settling time and the output unit vector (i.e., $\sin\theta_{PLL}$ and $\cos\theta_{PLL}$) distortion less than 1%.

However, when the grid impedance is non-negligible, the parameters designed above may not meet the requirements of robustness. Some documents have noticed this problem and conducted useful research on the parameter design of PLL in the weak grid. In [66], Zhu *et al.* use the type-II control system model of the PLL to establish the small-signal model of grid-connected converter, and delineate the satisfactory region to select parameters for the current loop and PLL by considering the gain margin (GM) and phase margin (PM) of the converter loop gain and the short circuit ratio (SCR). In [89], in the case that the current loop bandwidth is firstly chosen and the expected stability margins are set, the energy system analysis consortium (ESAC) criterion is applied to determine the forbidden area of parameters in order to select the appropriate PLL bandwidth for large grid impedance.

The studies mentioned here all consider the influence of the PLL on the current loop, but they are all for the three-phase SRF-PLL. In [68], the small-signal model of a single-phase PLL (i.e., Delay-PLL) is established with the perturbation and linearization method and the parameters of the Delay-PLL is designed. In [77], it is pointed out that with the same PI parameters, the SOGI-PLL is more robust with higher stability margin than the Delay-PLL. But, due to the loop coupling of SOGI-PLL, the current research on parameter optimization for SOGI-PLL under the weak grid is still challenging.

Furthermore, in [59], it is found that the two parameters (k_p and k_i) of the PI regulator in SOGI-PLL have opposite effects on estimation accuracy and system stability. The proportional coefficient k_p has no filtering effect and can amplify the disturbance in the PLL control loop. Under large disturbance cases, the estimation accuracy of the phase angle is deteriorated, or even causes oscillations. On the other hand, the integral coefficient k_i has low-pass characteristic in nature, which is useful to suppress high-frequency disturbances and is conducive to the system stability. However, a very small value of k_i may reduce the damping factor of the PLL itself, and also have a negative effect on the system stability. In other words, a too large or too small PLL bandwidth is both harmful to

the system stability, but the relevant mechanism needs further research.

C. DISCUSSIONS ON WEAK GRID APPLICATIONS

In summary, the existing modeling and parameter design methods for the SOGI-PLL still have some shortcomings, as summarized in Table 2. Traditional PLL model shown in Fig. 10 cannot describe the PLL characteristics under the weak grid condition and large signal disturbances. The perturbation and linearization model does fill in the gap of modeling, but such method needs to be further revised when either the grid impedance or the PLL bandwidth is large. Moreover, there are few studies that consider the loop coupling characteristics of SOGI-PLL in the process of modeling, and the accuracy of these models are difficult to guarantee if the PLL bandwidth is large. On the other hand, for the design, the existing research mainly focuses on the selection of PLL bandwidth under the weak grid, and only qualitatively stays at the level of designing the appropriate bandwidth to ensure the stable operation of the system under the weak grid. There is still lacking of unified approach for the selection of robust parameters for SOGI-PLL (with accurate modeling) under the weak grid condition, and the mechanism of the influence of each parameter on the system stability should be further explained. Therefore, the accurate modeling and parameter design considering the loop coupling of the SOGI-PLL will be the focus of further research.

One thing should be noted is how to guarantee the system stability with SOGI-PLL as the synchronization unit under a weak grid. Reducing the PLL bandwidth is a conventional method but leads to a sluggish dynamic response. Actually, the FFSOGI-PLL shows a more robust performance than the SOGI-PLL [49]. However, the current FFSOGI-PLL can be very complex if complex grid conditions (including frequency variation, harmonics and grid impedance) are considered simultaneously. Another possible option to improve the robustness is to modify the traditional SOGI-PLL. Adding a delay or inertial unit in the frequency feedback path to obtain a slow frequency adaptation has been confirmed effective in [81]. Hence, improvements are needed and will be one of the future research direction.

VI. BRIEF REVIEW OF SOME OTHER GRID SYNCHRONIZATION METHODS

A. SOME RECENT GENERALIZED INTEGRATORS

The concept of generalized integrator (GI) is introduced in [90] for current control of the active power filter. Focusing on the grid synchronization, the dc and harmonic components need to be well addressed.

In this case, high-order GIs are more attractive than the standard SOGI [91], [92]. As mentioned in Section III-A, three modifications are made: CSOGI-PLL [35], SO-SOGI-PLL [37] and MSTOGI-PLL [40]. Recently, even a fifth order GI is proposed [93]. Though the dc and harmonic attenuation is better, the design and implementation for high-order GIs are complicated. Another option to deal with the harmonics is to collaborate the SOGI together, such as the multiple-SOGI (MSOGI), where each SOGI is tuned at a specified harmonic frequency [94]. An equivalent structure of MSOGI is shown in [95] and it is demonstrated that the computational burden is reduced compared with the original MSOGI-PLL. A prior knowledge of the harmonic orders is one of the drawbacks of this method.

Apart from adding new paths or higher-order integrators into the standard SOGI-PLL, some researchers are trying to modify the SOGI recently [96]–[98]. The aim is to obtain a faster dynamic and simpler tuning process. Actually, it can be used to improve the performance of MSOGI or DSOGI.

B. ADAPTIVE OBSERVERS

In recent years, the adaptive observers (AO) are also widely used for the purpose of grid synchronization. With the help of adaptive observer, the grid frequency can be obtained by the arc-tangent operation of a pair of orthogonal signals that the adaptive observer estimates. Hence, no complex filtering or OSG is needed. The fast dynamic response is another advantage of the adaptive observer compared with the PLL. Generally speaking, the adaptive observer used in the grid-connected inverters can be divided into two categories.

The first method extracts the phase angle, frequency and amplitude information from the grid voltage at PCC, just like what most grid synchronization methods do [99]–[102]. As the adaptive observer is the combination of identification and observation, the grid fundamental frequency is viewed as an unknown parameter. The adaptation law to estimate the frequency should be carefully designed to satisfy Lyapunov stability criterion while the selection of Lyapunov function usually depends on the researchers' experience. Moreover, even some existing studies do consider the dc, fundamental component and main harmonics contained in the grid voltage (e.g. in [100], 5^{th}, 7^{th}, 11^{th}, 13^{th} harmonics are considered), error is unavoidable for neglecting higher-order harmonics and inter-harmonics. If more harmonics are included in the estimation model, the observer order and implementation complexity will increase a lot. That is, a balance between the estimation accuracy and implementation complexity should be made.

The second method takes the system output filter into the model to reconstruct the whole inverter system and to realize the 'sensorless' goal [103]–[105]. For instance, in [104], only one sensor for the grid current is needed. The grid voltage for synchronization and the capacitor current for active damping of the LCL filter resonance can be estimated by the observer. Apparently, the system works well if the parameters are all at their nominal values. However, the estimation accuracy may be low due to the parameter uncertainties.

If the grid voltage harmonics and system parameter variations are considered, the system control with an adaptive observer technique is rather complex. To mitigate the complexity of AO and to take advantage of fast dynamic of AO (that is, to improve the dynamics for the PLL by AO) at

TABLE 3. Current techniques and future direction for the SOGI-PLL under complex grid conditions.

Specific grid condition	Current techniques and the classification		Research status	Future direction
DC offset	➢ Direct filtering methods ➢ DC estimation and subtraction methods ➢ Non-dc signal extraction methods		Mature	Select one method for specific application
Low-order harmonics	➢ Pre-filtering methods ➢ In-loop filtering methods ➢ OSG modification methods		Mature	Select one method for specific application
Frequency variations	➢ Parallel frequency detector methods ➢ Phase error compensation methods ➢ PLL modification methods		Complex and inaccurate in some conditions	A fast, simple, accurate frequency estimator; More accurate compensation; New phase detector.
Weak grid condition	modeling	➢ Typical second order system model ➢ Typical type-II system model ➢ Perturbation and linearization model ➢ Extended perturbation and linearization model	Accurate under small bandwidth condition; Nonlinear loop coupling phenomenon is not considered	Taking the loop coupling into consideration
	design	➢ Bandwidth-oriented method ➢ Symmetrical optimum method	Design under ideal grid condition; Has to reduce the bandwidth under weak grid condition	Insight of each PI parameter design

the same time, some attempts are made to combine the AO and GI-based PLL together. The results in [106], [107] seem promising and further improvements are needed.

VII. CONCLUSION

The SOGI-PLL can be a high-performance single-phase PLL used in a wide range of applications. It has many merits like the simple structure, good filtering capability and frequency adaptability. However, as the grid is becoming more power electronics characterized, the SOGI-PLL is still required to be further improved, given that such PLL can be sensitive to the dc offset, low-order harmonics and high grid impedance.

Hence, this article collects and reviews the existing solutions and a summary is shown in Table 3. It is found that

1) The solutions for the dc offset and low-order harmonics suppression are relatively mature, and readers can select proper solutions based on specific requirements.
2) The FFSOGI-PLL shows better dynamics and less computational burden than the standard SOGI-PLL. One thing should be well addressed is the estimation error under grid frequency variations. The parallel frequency detector methods are intuitive in principle but a simple yet effective frequency estimator is not found. The phase error compensation methods are sufficient for PLLs with low bandwidth but may not be accurate enough if the bandwidth turns larger. The PLL structure modification methods also show fast dynamic response, but the filtering ability is poor and the transient overshoot can be high. For these methods, how to design the phase detector remains a tough task.
3) Because of the loop coupling, the existing modeling is not accurate enough under the conditions of high grid impedance and large PLL bandwidth. The conventional design methods for the SOGI-PLL may be insufficient in a weak grid and how to optimize the PLL parameters still needs further exploration.
4) Currently, some good attempts are made to combine the advantages of PLL and some other grid synchronization methods, such as the adaptive observer technique. This method can be another way to improve the SOGI-PLL performance and further investigations are needed.

As a result, for more complex grid conditions (especially for the grid frequency variation and high grid impedance), the effective single-phase PLL solutions still require further explorations, detailed of which can be found in the main text and tables of this study.

REFERENCES

[1] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
[2] R. R. Behera and A. N. Thakur, "An overview of various grid synchronization techniques for single-phase grid integration of renewable distributed power generation systems," in *Proc. Int. Conf. Electr., Electron., Optim. Techn. (ICEEOT)*, Chennai, India, Mar. 2016, pp. 2876–2880.
[3] Y. Yang and F. Blaabjerg, "Synchronization in single-phase grid-connected photovoltaic systems under grid faults," in *Proc. 3rd IEEE Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Aalborg, Denmark, Jun. 2012, pp. 476–482.
[4] V. D. Bacon, S. A. O. da Silva, L. B. G. Campanhol, and B. A. Angélico, "Stability analysis and performance evaluation of a single-phase phase-locked loop algorithm using a non-autonomous adaptive filter," *IET Power Electron.*, vol. 7, no. 8, pp. 2081–2092, Aug. 2014.
[5] Y. Yang, F. Blaabjerg, and Z. Zou, "Benchmarking of grid fault modes in single-phase grid-connected photovoltaic systems," *IEEE Trans. Ind. Appl.*, vol. 49, no. 5, pp. 2167–2176, Oct. 2013.
[6] Z. Zhang, Y. Yang, F. Blaabjerg, and R. Ma, "Challenges to grid synchronization of single-phase grid-connected inverters in zero-voltage ride-through operation," in *Proc. IEEE 2nd Annu. Southern Power Electron. Conf. (SPEC)*, Auckland, New Zealand, Dec. 2016, pp. 1–6.

[7] D. Yazdani, M. Pahlevaninezhad, and A. Bakhshai, "Single-phase grid-synchronization algorithms for converter interfaced distributed generation systems," in *Proc. Can. Conf. Electr. Comput. Eng.*, St. John's, NL, Canada, May 2009, pp. 127–131.

[8] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2167–2177, Jun. 2013.

[9] R. M. S. Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923–2932, Aug. 2008.

[10] A. Elrayyah, Y. Sozer, and M. Elbuluk, "Robust phase locked-loop algorithm for single-phase utility-interactive inverters," *IET Power Electron.*, vol. 7, no. 5, pp. 1064–1072, May 2014.

[11] I. Carugati, P. Donato, S. Maestri, D. Carrica, and M. Benedetti, "Frequency adaptive PLL for polluted single-phase grids," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2396–2404, May 2012.

[12] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Design and tuning of a modified power-based PLL for single-phase grid-connected power conditioning systems," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3639–3650, Aug. 2012.

[13] M. Karimi-Ghartemani and M. R. Iravani, "A nonlinear adaptive filter for online signal analysis in power systems: Applications," *IEEE Trans. Power Del.*, vol. 17, no. 2, pp. 617–622, Apr. 2002.

[14] Y. Yang, K. Zhou, and F. Blaabjerg, "Virtual unit delay for digital frequency adaptive T/4 delay phase-locked loop system," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, Hefei, China, May 2016, pp. 2910–2916.

[15] I. Galkin and M. Vorobyov, "Optimizing of sampling in a low-cost single-phase instantaneous AC-grid synchronization unit with discrete calculation of derivative function," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Yokohama, Japan, Nov. 2015, pp. 004538–004543.

[16] R.-Y. Kim, S.-Y. Choi, and I.-Y. Suh, "Instantaneous control of average power for grid tie inverter using single phase D-Q rotating frame with all pass filter," in *Proc. 30th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Busan, South Korea, Nov. 2004, pp. 274–279.

[17] P. Hao, W. Zanji, and C. Jianye, "A measuring method of the single-phase AC frequency, phase, and reactive power based on the Hilbert filtering," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 3, pp. 918–923, Jun. 2007.

[18] K. De Brabandere, T. Loix, K. Engelen, B. Bolsens, J. Van den Keybus, J. Driesen, and R. Belmans, "Design and operation of a phase-locked loop with Kalman estimator-based filter for single-phase applications," in *Proc. 32nd Annu. Conf. IEEE Ind. Electron. (IECON)*, Paris, France, Nov. 2006, pp. 525–530.

[19] A. J. C. Leal, C. L. T. Rodríguez, and F. Santamaria, "Comparison of synchronization techniques for a grid-tied photovoltaic system," in *Proc. IEEE 36th Central Amer. Panama Conv. (CONCAPAN)*, San Jose, CA, USA, 2016, pp. 1–5.

[20] S. M. Silva, B. M. Lopes, B. J. C. Filho, R. P. Campana, and W. C. Boaventura, "Performance evaluation of PLL algorithms for single-phase grid-connected systems," in *Proc. 39th IAS Annu. Meeting. Conf. Rec. IEEE Ind. Appl. Conf.*, Seattle, WA, USA, vol. 4, Oct. 2004, pp. 2259–2263.

[21] H. Fadil, D. Yousfi, Y. Aite Driss, and A. R. Nasrudin, "Synchronization techniques benchmarking of grid fault modes in single-phase systems," in *Proc. Int. Renew. Sustain. Energy Conf. (IRSEC)*, Ouarzazate, Morocco, Oct. 2014, pp. 191–196.

[22] M. Cacciato, A. Consoli, V. Crisafulli, G. Scarcella, and G. Scelba, "Robustness evaluation of phase-locked loop algorithms for single-phase distributed generation systems," in *Proc. SPEEDAM*, Pisa, Italy, 2010, pp. 914–919.

[23] L. N. Arruda, S. M. Silva, and B. J. C. Filho, "PLL structures for utility connected systems," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf., 36th IAS Annu. Meeting*, vol. 4, Sep./Oct. 2001, pp. 2655–2660.

[24] S. Golestan, M. Monfared, and J. M. Guerrero, "Second order generalized integrator based reference current generation method for single-phase shunt active power filters under adverse grid conditions," in *Proc. 4th Annu. Int. Power Electron., Drive Syst. Technol. Conf.*, Feb. 2013, pp. 510–517.

[25] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jeju, South Korea, Jun. 2006, pp. 1–6.

[26] Y. Gui, X. Wang, H. Wu, and F. Blaabjerg, "Voltage-modulated direct power control for a weak grid-connected voltage source inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11383–11395, Nov. 2019.

[27] M. Karimi-Ghartemani, S. A. Khajehoddin, P. K. Jain, A. Bakhshai, and M. Mojiri, "Addressing DC component in PLL and notch filter algorithms," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 78–86, Jan. 2012.

[28] S. Golestan, J. M. Guerrero, F. Musavi, and J. C. Vasquez, "Single-phase frequency-locked loops: A comprehensive review," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11791–11812, Dec. 2019.

[29] *Photovoltaic (PV) Systems-Characteristics of the Utility Interface*, IEC Standard 61727, 2004.

[30] H. Liu, Y. Sun, H. Hu, and Y. Xing, "A new single-phase PLL based on discrete Fourier transform," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Charlotte, NC, USA, Mar. 2015, pp. 521–526.

[31] M. Xie, H. Wen, C. Zhu, and Y. Yang, "DC offset rejection improvement in single-phase SOGI-PLL algorithms: Methods review and experimental evaluation," *IEEE Access*, vol. 5, pp. 12810–12819, 2017.

[32] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Single-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9013–9030, Dec. 2017.

[33] S. Prakash, J. K. Singh, R. K. Behera, and A. Mondal, "Comprehensive analysis of SOGI-PLL based algorithms for single-phase system," in *Proc. Nat. Power Electron. Conf. (NPEC)*, Tiruchirappalli, India, Dec. 2019, pp. 1–6.

[34] S. Golestan, J. M. Guerrero, and G. B. Gharehpetian, "Five approaches to deal with problem of DC offset in phase-locked loop algorithms: Design considerations and performance evaluations," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 648–661, Jan. 2016.

[35] A. Kulkarni and V. John, "Design of a fast response time single-phase PLL with DC offset rejection capability," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Long Beach, CA, USA, Mar. 2016, pp. 2200–2206.

[36] B. Liu, M. An, H. Wang, Y. Chen, Z. Zhang, C. Xu, S. Song, and Z. Lv, "A simple approach to reject DC offset for single-phase synchronous reference frame PLL in grid-tied converters," *IEEE Access*, vol. 8, pp. 112297–112308, 2020.

[37] Z. Xin, X. Wang, Z. Qin, M. Lu, P. C. Loh, and F. Blaabjerg, "An improved second-order generalized integrator based quadrature signal generator," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8068–8073, Dec. 2016.

[38] S.-H. Hwang, L. Liu, H. Li, and J.-M. Kim, "DC offset error compensation for synchronous reference frame PLL in single-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3467–3471, Aug. 2012.

[39] M. Ciobotaru, R. Teodorescu, and V. G. Agelidis, "Offset rejection for PLL based synchronization in grid-connected converters," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Austin, TX, USA, Feb. 2008, pp. 1611–1617.

[40] C. Zhang, X. Zhao, X. Wang, X. Chai, Z. Zhang, and X. Guo, "A grid synchronization PLL method based on mixed second- and third-order generalized integrator for DC offset elimination and frequency adaptability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1517–1526, Sep. 2018.

[41] S. Shinnaka, "A robust single-phase PLL system with stable and fast tracking," *IEEE Trans. Ind. Appl.*, vol. 44, no. 2, pp. 624–633, Apr. 2008.

[42] G. Fedele and A. Ferrise, "Non adaptive second-order generalized integrator for identification of a biased sinusoidal signal," *IEEE Trans. Autom. Control*, vol. 57, no. 7, pp. 1838–1842, Jul. 2012.

[43] S. Golestan, F. D. Freijedo, and J. M. Guerrero, "A systematic approach to design high-order phase-locked loops," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2885–2890, Jun. 2015.

[44] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 765–778, Feb. 2013.

[45] S. Golestan and J. M. Guerrero, "An analysis of modified demodulation-based grid voltage parameter estimator," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6528–6533, Dec. 2015.

[46] S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, and J. Doval-Gandoy, "PLL with MAF-based prefiltering stage: Small-signal modeling and performance enhancement," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4013–4019, Jun. 2016.

[47] S. Gude and C.-C. Chu, "Single-phase enhanced phase-locked loops based on multiple delayed signal cancellation filters for micro-grid applications," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7122–7133, Dec. 2019.

[48] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of phase-locked loops for power converters under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2039–2047, dec. 2009.
[49] J. Xu, H. Qian, S. Bian, Y. Hu, and S. Xie, "Comparative study of single-phase phase-locked loops for grid-connected inverters under non-ideal grid conditions," *CSEE J. Power Energy Syst.*, early access, doi: 10.17775/CSEEJPES.2019.02390.
[50] A. Kulkarni and V. John, "A novel design method for SOGI-PLL for minimum settling time and low unit vector distortion," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Vienna, Austria, Nov. 2013, pp. 274–279.
[51] M. S. Reza, M. Ciobotaru, and V. G. Agelidis, "Tracking of time-varying grid voltage using DFT based second order generalized integrator technique," in *Proc. IEEE Int. Conf. Power Syst. Technol. (POWERCON)*, Auckland, New Zealand, Nov. 2012, pp. 1–6.
[52] Q. Sun, J. M. Guerrero, T. Jing, J. C. Vasquez, and R. Yang, "An islanding detection method by using frequency positive feedback based on FLL for single-phase microgrid," *IEEE Trans. Smart Grid*, vol. 8, no. 4, pp. 1821–1830, Jul. 2017.
[53] J. Matas, H. Martín, J. de la Hoz, A. Abusorrah, Y. A. Al-Turki, and M. Al-Hindawi, "A family of gradient descent grid frequency estimators for the SOGI filter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5796–5810, Jul. 2018.
[54] G. Fedele, C. Picardi, and D. Sgro, "A power electrical signal tracking strategy based on the modulating functions method," *IEEE Trans. Ind. Electron.*, vol. 56, no. 10, pp. 4079–4087, Oct. 2009.
[55] M. A. Akhtar and S. Saha, "An adaptive frequency-fixed second-order generalized integrator-quadrature signal generator using fractional-order conformal mapping based approach," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5548–5552, Jun. 2020.
[56] M. S. Reza, M. Ciobotaru, and V. G. Agelidis, "Grid voltage offset and harmonics rejection using second order generalized integrator and Kalman filter technique," in *Proc. 7th Int. Power Electron. Motion Control Conf.*, Harbin, China, Jun. 2012, pp. 104–111.
[57] A. Sahoo, K. Mahmud, M. Ciobotaru, and J. Ravishankar, "Adaptive grid synchronization technique for single-phase inverters in AC microgrid," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Baltimore, MD, USA, 2019, pp. 4441–4446.
[58] S. Golestan, S. Y. Mousazadeh, J. M. Guerrero, and J. C. Vasquez, "A critical examination of frequency-fixed second-order generalized integrator-based phase-locked loops," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6666–6672, Sep. 2017.
[59] M. S. Reza, M. Ciobotaru, and V. G. Agelidis, "Estimation of single-phase grid voltage fundamental parameters using fixed frequency tuned second-order generalized integrator based technique," in *Proc. 4th IEEE Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Rogers, AR, USA, Jul. 2013, pp. 1–8.
[60] F. Xiao, L. Dong, L. Li, and X. Liao, "A frequency-fixed SOGI-based PLL for single-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1713–1719, Mar. 2017.
[61] P. Liu and S. Duan, "An open-loop synchronization technique with simple structure for phase error compensation and frequency estimation," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8936–8940, Oct. 2020.
[62] S. Golestan, A. Vidal, A. G. Yepes, J. M. Guerrero, J. C. Vasquez, and J. Doval-Gandoy, "A true open-loop synchronization technique," *IEEE Trans. Ind. Informat.*, vol. 12, no. 3, pp. 1093–1103, Jun. 2016.
[63] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "An open-loop grid synchronization approach for single-phase applications," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5548–5555, Jul. 2018.
[64] Q. Guan, Y. Zhang, Y. Kang, and J. M. Guerrero, "Single-phase phase-locked loop based on derivative elements," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4411–4420, Jun. 2017.
[65] S. Zhou, X. Zou, D. Zhu, L. Tong, Y. Zhao, Y. Kang, and X. Yuan, "An improved design of current controller for LCL-type grid-connected converter to reduce negative effect of PLL in weak grid," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 648–663, Jun. 2018.
[66] D. Zhu, S. Zhou, X. Zou, and Y. Kang, "Improved design of PLL controller for LCL-type grid-connected converter in weak grid," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4715–4727, May 2020.
[67] D. Zhu, S. Zhou, X. Zou, Y. Kang, and K. Zou, "Small-signal disturbance compensation control for LCL-type grid-connected converter in weak grid," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2852–2861, May 2020.
[68] Y. Han, H. Chen, Z. Li, P. Yang, L. Xu, and J. M. Guerrero, "Stability analysis for the grid-connected single-phase asymmetrical cascaded multilevel inverter with SRF-PI current control under weak grid conditions," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2052–2069, Mar. 2019.
[69] X. Chen, Y. Zhang, S. Wang, J. Chen, and C. Gong, "Impedance-phased dynamic control method for grid-connected inverters in a weak grid," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 274–283, Jan. 2017.
[70] L. Huang, H. Xin, Z. Li, P. Ju, H. Yuan, Z. Lan, and Z. Wang, "Grid-synchronization stability analysis and loop shaping for PLL-based power converters with different reactive power control," *IEEE Trans. Smart Grid*, vol. 11, no. 1, pp. 501–516, Jan. 2020.
[71] Z. Xie, Y. Chen, W. Wu, Y. Xu, H. Wang, J. Guo, and A. Luo, "Modeling and control parameters design for grid-connected inverter system considering the effect of PLL and grid impedance," *IEEE Access*, vol. 8, pp. 40474–40484, 2020.
[72] Y. Huang, X. Yuan, J. Hu, and P. Zhou, "Modeling of VSC connected to weak grid for stability analysis of DC-link voltage control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 4, pp. 1193–1204, Dec. 2015.
[73] X. Zhang, D. Xia, Z. Fu, G. Wang, and D. Xu, "An improved feedforward control method considering PLL dynamics to improve weak grid stability of grid-connected inverters," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5143–5151, Oct. 2018.
[74] H. Wu, X. Ruan, and D. Yang, "Research on the stability caused by phase-locked loop for LCL-type grid-connected inverter in weak grid condition," *Proc. CSEE*, vol. 34, no. 30, pp. 5259–5268, Dec. 2014.
[75] X. Wang and F. Blaabjerg, "Harmonic stability in power electronic-based power systems: Concept, modeling, and analysis," *IEEE Trans. Smart Grid*, vol. 10, no. 3, pp. 2858–2870, May 2019.
[76] C. Zhang, X. Wang, F. Blaabjerg, and W. Wang, "Benchmarking of small-signal dynamics of single-phase PLLs," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia (ICPE-ECCE Asia)*, Seoul, South Korea, Jun. 2015, pp. 1420–1427.
[77] J. Xu, Q. Qian, B. Zhang, and S. Xie, "Harmonics and stability analysis of single-phase grid-connected inverters in distributed power generation systems considering phase-locked loop impact," *IEEE Trans. Sustain. Energy*, vol. 10, no. 3, pp. 1470–1480, Jul. 2019.
[78] C. Zhang, X. Wang, F. Blaabjerg, W. Wang, and C. Liu, "The influence of phase-locked loop on the stability of single-phase grid-connected inverter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Montreal, QC, Canada, Sep. 2015, pp. 4737–4744.
[79] S. Shah and L. Parsa, "On impedance modeling of single-phase voltage source converters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Milwaukee, WI, USA, Sep. 2016, pp. 1–8.
[80] C. Zhang, O. Fosso, and M. Molinas, "Frequency domain modelling for assessment of Hilbert and SOGI based single-phase synchronisation," in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Lisbon, Portugal, Oct. 2019, pp. 1780–1785.
[81] S. Shah, P. Koralewicz, V. Gevorgian, and L. Parsa, "Small-signal modeling and design of phase-locked loops using harmonic signal-flow graphs," *IEEE Trans. Energy Convers.*, vol. 35, no. 2, pp. 600–610, Jun. 2020.
[82] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "An overview of assessment methods for synchronization stability of grid-connected converters under severe symmetrical grid faults," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9655–9670, Oct. 2019.
[83] Y. Xia, M. Yu, X. Wang, and W. Wei, "Describing function method based power oscillation analysis of LCL-filtered single-stage PV generators connected to weak grid," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8724–8738, Sep. 2019.
[84] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3323–3334, Dec. 2007.
[85] Y. F. Wang and Y. W. Li, "Analysis and digital implementation of cascaded delayed-signal-cancellation PLL," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1067–1080, Apr. 2011.
[86] S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki, "Modeling, tuning, and performance comparison of second-order-generalized-integrator-based FLLs," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10229–10239, Dec. 2018.
[87] Y. Han, M. Luo, X. Zhao, J. M. Guerrero, and L. Xu, "Comparative performance evaluation of orthogonal-signal-generators-based single-phase PLL algorithms—A survey," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3932–3944, May 2016.
[88] C. Tang, "Four design methods for proportional-integral controller of grid-connected inverter with LCL output filter," *Power Syst. Technol.*, vol. 37, no. 11, pp. 3268–3275, Nov. 2013.

[89] X. Li and H. Lin, "A design method of phase-locked loop for grid-connected converters considering the influence of current loops in weak grid," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2420–2429, Sep. 2020.
[90] X. Yuan, W. Merk, H. Stemmler, and J. Allmeling, "Stationary-frame generalized integrators for current control of active power filters with zero steady-state error for current harmonics of concern under unbalanced and distorted operating conditions," *IEEE Trans. Ind. Appl.*, vol. 38, no. 2, pp. 523–532, Apr. 2002.
[91] P. Shah, I. Hussain, B. Singh, A. Chandra, and K. Al-Haddad, "GI-based control scheme for single-stage grid interfaced SECS for power quality improvement," *IEEE Trans. Ind. Appl.*, vol. 55, no. 1, pp. 869–881, Feb. 2019.
[92] M. Z. Hasan, I. F. Shiam, T. T. Nova, and M. S. Reza, "A modified PLL based on second order generalized integrator for single-phase voltage system," in *Proc. Int. Conf. Electr., Comput. Commun. Eng. (ECCE)*, Cox's Bazar, Bangladesh, Feb. 2019, pp. 1–6.
[93] N. Kumar, I. Hussain, B. Singh, and B. K. Panigrahi, "Implementation of multilayer fifth-order generalized integrator-based adaptive control for grid-tied solar PV energy conversion system," *IEEE Trans. Ind. Informat.*, vol. 14, no. 7, pp. 2857–2868, Jul. 2018.
[94] J. Matas, M. Castilla, J. Miret, L. G. de Vicuña, and R. Guzman, "An adaptive prefiltering method to improve the speed/accuracy trade-off of voltage sequence detection methods under adverse grid conditions," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2139–2151, May 2014.
[95] J. Geng, X. Li, Q. Liu, J. Chen, Z. Xin, and P. C. Loh, "Frequency-locked loop based on a repetitive controller for grid synchronization systems," *IEEE Access*, vol. 8, pp. 154861–154870, 2020.
[96] N. Kumar, B. Singh, and B. K. Panigrahi, "Grid synchronisation framework for partially shaded solar PV-based microgrid using intelligent control strategy," *IET Gener., Transmiss. Distrib.*, vol. 13, no. 6, pp. 829–837, Mar. 2019.
[97] N. Hui, D. Wang, and Y. Li, "A novel hybrid filter-based PLL to eliminate effect of input harmonics and DC offset," *IEEE Access*, vol. 6, pp. 19762–19773, 2018.
[98] F. Ul Nazir, N. Kumar, B. C. Pal, B. Singh, and B. K. Panigrahi, "Enhanced SOGI controller for weak grid integrated solar PV system," *IEEE Trans. Energy Convers.*, vol. 35, no. 3, pp. 1208–1217, Sep. 2020.
[99] I. Askarian, S. Eren, M. Palevani, and A. Knight, "New frequency and amplitude estimation techniques for grid-connected DC/AC inverters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Cincinnati, OH, USA, Oct. 2017, pp. 5738–5743.
[100] R. Bimarta and K.-H. Kim, "A robust frequency-adaptive current control of a grid-connected inverter based on LMI-LQR under polytopic uncertainties," *IEEE Access*, vol. 8, pp. 28756–28773, 2020.
[101] H. Ahmed, M. Ahsan, M. Benbouzid, A. Albarbar, M. Shahjalal, and S. Biricik, "Coordinate transformation-free observer-based adaptive estimation of distorted single-phase grid voltage signal," *IEEE Access*, vol. 8, pp. 74280–74290, 2020.
[102] Z. Dai, W. Lin, and H. Lin, "Estimation of single-phase grid voltage parameters with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3867–3879, May 2016.
[103] T. V. Tran and K.-H. Kim, "Frequency adaptive grid voltage sensorless control of LCL-filtered inverter based on extended model observer," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7560–7573, Sep. 2020.
[104] R. A. Fantino, C. A. Busada, and J. A. Solsona, "Observer-based grid-voltage sensorless synchronization and control of a VSI-LCL tied to an unbalanced grid," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 4972–4981, Jul. 2019.
[105] M. Su, B. Cheng, Y. Sun, Z. Tang, B. Guo, Y. Yang, F. Blaabjerg, and H. Wang, "Single-sensor control of LCL-filtered grid-connected inverters," *IEEE Access*, vol. 7, pp. 38481–38494, 2019.
[106] Y. Park, H.-S. Kim, and S.-K. Sul, "Frequency-adaptive observer to extract AC-coupled signals for grid synchronization," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 273–282, Feb. 2017.
[107] H. Ahmed and M. Benbouzid, "On the enhancement of generalized integrator-based adaptive filter dynamic tuning range," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 10, pp. 7449–7457, Oct. 2020.

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