Three-Phase PLLs: A Review of Recent Advances

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***Abstract*—A phase-locked loop (PLL) is a nonlinear negative-feedback control system that synchronizes its output in frequency as well as in phase with its input. PLLs are now widely used for the synchronization of power-electronics-based converters and also for monitoring and control purposes in different engineering fields. In recent years, there have been many attempts to design more advanced PLLs for three-phase applications. The aim of this paper is to provide overviews of these attempts, which can be very useful for engineers and academic researchers.**

***Index Terms*—Frequency detection, phase detection, phase-locked loop (PLL), synchronization, synchronous reference frame PLL (SRF-PLL).**

I. Introduction

THE advent of the phase-locked loop (PLL) dates back to 1930s when it was first designed and used for the synchronous reception of radio signals [1]. Since then, it has found widespread applications in different areas, such as the estimation of fundamental parameters (phase, frequency, and amplitude) of power signals [2]–[83], measurement of harmonics, interharmonics, and power quality indices [84]–[90], implementing adaptive filters and robust controllers [91]–[93], control of ac and dc machines [94], [95], contactless energy transfer systems [96], [97], induction heating systems [98], [99], piezoelectric applications [100], [101], battery charge circuits [102], [103], magnetic encoders [104], islanding detection of microgrids [105]–[107], welding industry [108], grid fault and voltage sag detection [109], [110], synchronization of power quality instruments [111], [112], computation of synchrophasors [113], [114], etc.

Fig. 1 shows the schematic diagram of the conventional synchronous reference frame PLL (SRF-PLL) [2]–[5], which is a standard PLL in three-phase applications and the building block of almost all advanced PLLs. In this structure, the PD, LF, and VCO are abbreviations for the phase detector, loop filter, and voltage-controlled oscillator, respectively; $\hat{V}$, $\hat{\omega}_g$, and $\hat{\theta}$ are the amplitude, frequency, and phase angle estimated by the SRF-PLL, respectively; ω_n is the nominal frequency; k_p and k_i are the proportional and integral gains of the LF (which is a proportional–integral (PI) controller), respectively, and k_v is the cutoff frequency of the low-pass filter (LPF) used for the amplitude estimation. The PD in the SRF-PLL is implemented by applying the Clarke's transformation and then the Park's transformation to the three-phase input signals. The q-axis output of the PD, which contains the phase error information, is passed through the LF (the PI controller). The resultant signal, which is the estimated frequency, is applied to the VCO to provide an estimation of the phase angle.

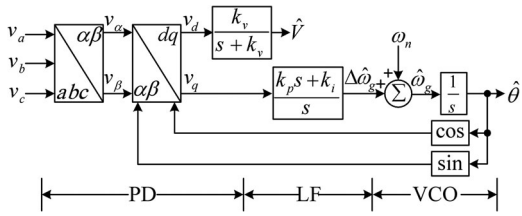

Fig. 1. Schematic diagram of the conventional SRF-PLL.

In recent years, there have been many attempts to design more advanced three-phase PLLs. The majority of these efforts have focused on enhancing the disturbance rejection capability of the conventional SRF-PLL and its relatives [6]–[64] so that they can deal with the ever increasing power quality issues in power systems. Other efforts in the field have been mainly on improving the dynamic behavior [65]–[67] and changing the steady-state characteristics of the conventional SRF-PLL and its relatives [15], [68]–[75]. Attempts to optimize the PLL implementation using low-cost industrial devices are also worth mentioning [23], [76]–[80].

The aim of this paper is to provide an overview of recent advances in three-phase PLLs, which can be useful for engineers and academic researchers.

II. Analysis of Conventional SRF-PLL

Let the three-phase input signals of the conventional SRF-PLL be as

$$\begin{aligned} v_a(t) &= V\cos(\theta) \\ v_b(t) &= V\cos\left(\theta-\frac{2\pi}{3}\right) \\ v_c(t) &= V\cos\left(\theta+\frac{2\pi}{3}\right) \end{aligned} \tag{1}$$

where V and θ are the amplitude and phase angle of the three-phase signals, respectively. Considering the Clarke's and Park's

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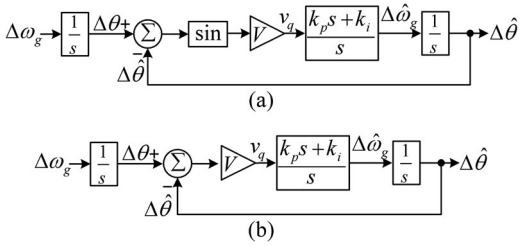

Fig. 2. (a) Nonlinear model and (b) linear model of the conventional SRF-PLL.

transformations as

$$T_{\mathrm{abc}\to\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{2}$$

$$T_{\alpha\beta\to\mathrm{dq}} = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix} \tag{3}$$

and applying them to (1) gives

$$\begin{aligned} v_d(t) &= V\cos(\theta-\hat{\theta}) \\ v_q(t) &= V\sin(\theta-\hat{\theta}) \end{aligned} \tag{4}$$

where

$$\begin{aligned} \theta &= \int \omega_g\,dt = \int (\omega_n + \Delta\omega_g)dt = \underbrace{\int \omega_n\,dt}_{\theta_n} + \underbrace{\int \Delta\omega_g\,dt}_{\Delta\theta} \\ \hat{\theta} &= \int \hat{\omega}_g\,dt = \int (\omega_n + \Delta\hat{\omega}_g)dt = \underbrace{\int \omega_n\,dt}_{\theta_n} + \underbrace{\int \Delta\hat{\omega}_g\,dt}_{\Delta\hat{\theta}}. \end{aligned} \tag{5}$$

Substituting (5) into (4) yields

$$\begin{aligned} v_d(t) &= V\cos(\Delta\theta-\Delta\hat{\theta}) \approx V \\ v_q(t) &= V\sin(\Delta\theta-\Delta\hat{\theta}) \approx V\left(\Delta\theta-\Delta\hat{\theta}\right). \end{aligned} \tag{6}$$

As can be seen, the signal v_q contains the phase error information, and signal v_d is a measure of the amplitude of the three-phase signals.

Using (5), (6), and the SRF-PLL structure (see Fig. 1), the nonlinear and linear models of the SRF-PLL can be simply obtained as shown in Fig. 2. These models provide very useful information about characteristics of the SRF-PLL. This information is as follows.

1) The amplitude V appears as a gain in the forward path of the model. It means that variations of the amplitude of the SRF-PLL input signals change the loop gain and, therefore, the stability margin and dynamic behavior of the SRF-PLL. Theoretically, the SRF-PLL remains stable even if V is very close to zero. This fact can be proven by applying the Routh–Hurwitz's stability test to the characteristic polynomial of the SRF-PLL, which can be simply obtained using Fig. 2(b) as $s^2 + Vk_ps + Vk_i = 0$. Despite this fact, to keep the dynamic and stability characteristics of the SRF-PLL decoupled from variations of V, an amplitude normalization scheme (ANS) is often included in the SRF-PLL structure [5]. The ANS in the SRF-PLL is often implemented by dividing the LF input signal, v_q, by an estimation of V, as highlighted in Fig. 3. Notice that the estimated value of V is first passed through a saturation block to avoid the division by zero in the startup transient. An alternative approach for the amplitude normalization is using the inverse tangent operation [15], [81], [82], which reduces the nonlinearity of the PLL control loop at the cost of a higher computational effort.

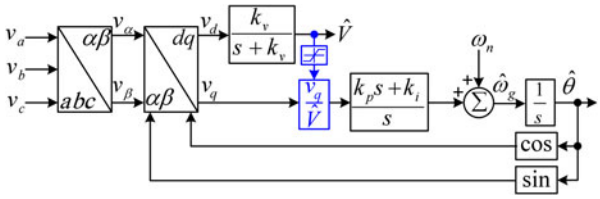

Fig. 3. SRF-PLL with an ANS.

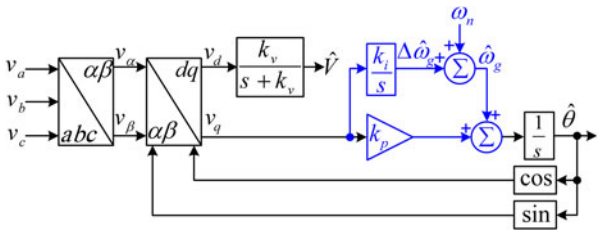

Fig. 4. Extracting the estimated frequency from the PI controller integrator output.

2) In the standard SRF-PLL, the VCO's input signal is considered as the estimated frequency. In this case, the closed-loop transfer function relating $\Delta\hat{\omega}_g$ to $\Delta\omega_g$ is

$$G_{cl}(s) = \frac{\Delta\hat{\omega}_g(s)}{\Delta\omega_g(s)} = \frac{Vk_ps + Vk_i}{s^2 + Vk_ps + Vk_i}. \tag{7}$$

An alternative way is to rearrange the PI controller as highlighted in Fig. 4 and consider the integrator output as an estimation of the frequency [10], [17], [62], [65], [80], [91]. For the same values of k_p and k_i as those in (7), this modification results in a higher filtering capability and a more damped transient response in the frequency estimation, because it removes the zero in (7) and makes the transfer function a standard second-order one, as shown in the following:

$$G_{cl}(s) = \frac{\Delta\hat{\omega}_g(s)}{\Delta\omega_g(s)} = \frac{Vk_i}{s^2 + Vk_ps + Vk_i}. \tag{8}$$

Notice that, for both SRF-PLLs, the closed-loop transfer function relating the estimated phase to the actual one is the same, as expressed below

$$G_{cl}(s) = \frac{\Delta\hat{\theta}(s)}{\Delta\theta(s)} = \frac{Vk_ps + Vk_i}{s^2 + Vk_ps + Vk_i}. \tag{9}$$

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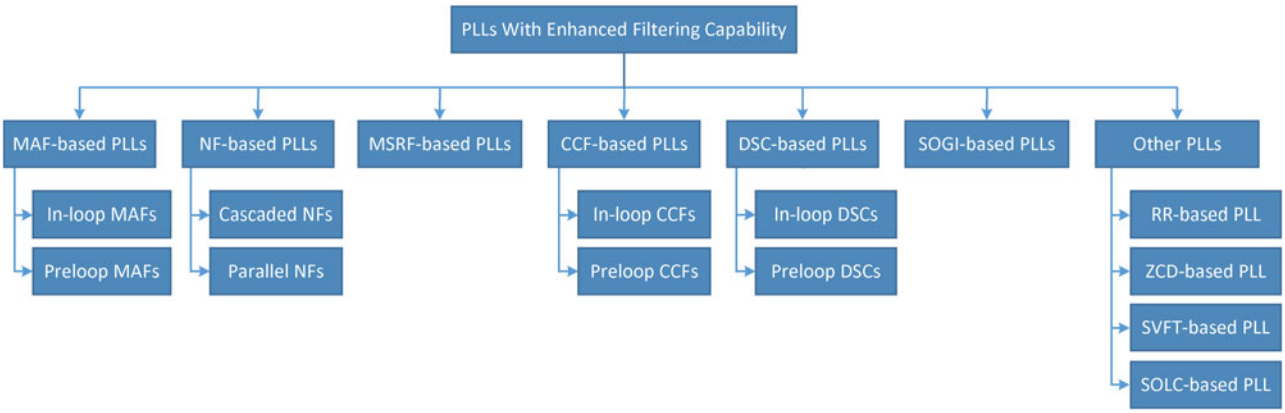

Fig. 5. General classification of PLLs with enhanced filtering capability.

3) The SRF-PLL is a type-2 control system, as it has two open-loop poles at the origin[1] [2], [3], [8], [15], [72]. This means that the SRF-PLL can track phase-angle jumps and frequency steps with zero steady-state phase error, but it fails to do so in the case of frequency ramps. To be more exact, there is a steady-state phase error equal to

$$e_{\rm ss}^{\Delta\dot{\omega}_g} = \sin^{-1}\left(\frac{A}{Vk_i}\right) \tag{10}$$

in the SRF-PLL output when the input frequency has a ramping change with slope A. Notice that this result can be simply obtained using the nonlinear model of the SRF-PLL [see Fig. 2(a)]. This error obviously can be reduced by selecting a large value for k_i, which is corresponding to a high bandwidth for the SRF-PLL when the standard design method for selecting the control parameters is used [2], [3]. Increasing the SRF-PLL's bandwidth, however, reduces its noise immunity. In addition, it increases the coupling between phase and frequency variables, which means the estimated frequency experiences large transients during the startup and under phase-angle jumps [65].

III. PLLs With Enhanced Filtering Capability

In recent years, the increased penetration of renewable energy sources to the power grid and the proliferation of domestic and industrial nonlinear loads have caused serious power quality issues and made the synchronization task more challenging than before. To deal with this problem, many advanced PLLs with enhanced disturbance rejection capability have been designed by different researchers. Almost all these PLLs can be understood as a conventional SRF-PLL with additions filters, which can be included inside the SRF-PLL control loop or before its input. A general classification of these PLLs can be observed in Fig. 5. This section provides an overview of these PLLs.

[1]The type of a control system in the classical control theory is defined as the number of open-loop poles of that system at origin [115].

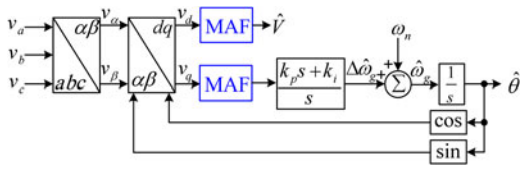

Fig. 6. Schematic diagram of the MAF-PLL.

A. Moving Average Filter-Based PLLs

Moving average filter (MAF) is a linear-phase filter that can be described in the Laplace domain as [6], [7]

$$G_{\rm MAF}(s) = \frac{1 - e^{-T_w s}}{T_w s} \tag{11}$$

where T_w is the MAF window length. The MAF passes the dc component and completely blocks frequency components of integer multiples of $1/T_w$ in Hertz [6]. That is the reason why the MAF is sometimes referred to as "quasi-ideal LPF" [7].

Fig. 6 illustrates the schematic diagram of the conventional SRF-PLL with in-loop MAFs, which is briefly referred to as the MAF-PLL [6], [8]–[10]. Including the MAF inside the SRF-PLL control loop significantly improves its filtering capability, but considerably slows down its dynamic response [6]. The reason is that the in-loop MAF causes a large phase delay in the control loop. This is particularly true when the MAF's window length is set to $T_w = T$, where T is the nominal period of the MAF-PLL input signals. This selection for the MAF's window length, i.e., $T_w = T$, is recommended when the grid harmonic pattern is unknown, and therefore, all harmonic components and the dc offset may be present in the PLL input [6]. Other choices for the window length of the MAF are $T_w = T/2$ and $T_w = T/6$, which, respectively, are suitable for applications where odd-order harmonics and non-triplen odd harmonics are present in the PLL input [6], [7], [13].

To improve the dynamic performance of the MAF-PLL while maintaining a good filtering capability for it, several approaches have been suggested in the literature. In [6] and [11], using a proportional–integral–derivative (PID) controller instead of the conventional PI controller as the LF of the MAF-PLL is

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suggested. The derivative action of the PID controller provides an additional degree of freedom and, therefore, enables the designer to effectively compensate for the phase delay caused by the MAF by arranging a pole-zero cancellation [6].

In [12], including a special lead compensator before the PI controller in the MAF-PLL structure is proposed. The transfer function of this lead compensator is almost the inverse of that of the MAF, and therefore, it is able to significantly reduce the phase delay in the MAF-PLL control loop.

In [13], it is suggested to narrow the MAFs' window length to $T/6$ and use them only for canceling the nontriplen odd harmonics of the PLL input. Notice that these harmonics are sensed as multiple of six harmonics in the MAF-PLL control loop. As a result, the MAF-PLL can achieve a faster dynamic response when compared to the cases where the window length of the MAFs is $T/2$ or T. In this condition, however, the MAF-PLL cannot reject the dc offset and the fundamental-frequency negative sequence (FFNS) component and, therefore, requires additional filters to block them. To deal with this problem, it is suggested in [13] to place three MAF-based high-pass filters in the MAF-PLL input to filter out the dc component and use a differentiation-based filter inside the MAF-PLL control loop to cancel out the double-frequency ripples caused by the FFNS component. This differentiation-based filter has been originally developed in [14].

Using a quasi-type-1 PLL (QT1-PLL) structure can also be an interesting approach for improving the MAF-PLL dynamic behavior while maintaining a high filtering capability for it [15]. This structure will be explained later in Section V-B.

In [7] and [16], removing the in-loop MAFs and placing them in a separate SRF before the SRF-PLL input is suggested. The MAFs in this SRF, which act as a preprocessing filter, effectively block disturbance components without (significantly) degrading the PLL dynamic behavior. Using this prefiltering stage, however, involves an additional frequency detector. This additional frequency detector, of course, can be avoided by correcting the phase shift and amplitude scaling caused by the nonadaptive MAF-based prefiltering stage in the SRF-PLL, as explained in [17].

B. Notch Filter-Based PLLs

A notch filter (NF) is a band-rejection filter that significantly attenuates signals within a narrow band of frequencies and passes all other frequency components with negligible attenuation. This feature makes the NF very interesting for the selective cancellation of the desired harmonic components in the PLL control loop [8], [18]–[23]. NFs can be adaptive or nonadaptive. The former one is often preferred by designers, as it allows them to select a narrow bandwidth for NFs and, therefore, minimize the phase delay in the PLL control loop. This advantage, of course, is at the cost of a rather considerable increase in the PLL computational effort [18]. The structure of NF-based PLLs (NF-PLLs) is the same as the standard MAF-PLL (see Fig. 6), except that the MAF is replaced with one or more NFs.

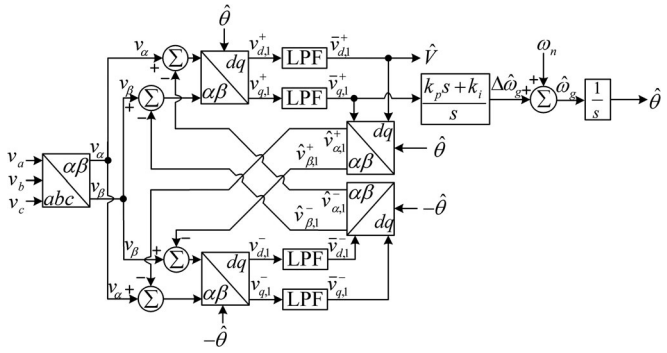

Fig. 7. Schematic diagram of the DSRF-PLL. For the sake of clarity, the sine and cosine of $\hat{\theta}$ are not shown here.

When including more than one NF in the PLL control loop is intended, two topologies can be considered. The first one is the cascade topology [18], [19] and the second one is the parallel topology [20]–[22]. The main difference between these topologies is in their frequency estimation part: the parallel topology uses the same frequency estimator for all NFs; however, in the cascade topology, each NF has its own frequency estimator. The number of NFs in both topologies involves a tradeoff between filtering capability and computational burden. To achieve a satisfactory compromise, often using three NFs with notch frequencies at $2\omega_g$, $6\omega_g$, and $12\omega_g$ is recommended.

C. Multiple SRF Filtering-Based PLLs

Fig. 7 shows the schematic diagram of the dual SRF filtering-based PLL (DSRF-PLL) [24]. As shown, this PLL uses two SRFs rotating at the same angular speed, but with opposite directions and a cross-feedback network to extract and separate the fundamental-frequency positive-sequence (FFPS) and FFNS components. As a result, the grid voltage imbalance has no steady-state negative effect on the DSRF-PLL performance. The presence of harmonics in the DSRF-PLL input, however, may cause oscillatory errors in the estimated quantities. This problem can be alleviated by adding several SRFs rotating at the targeted harmonic frequencies to the standard structure [24]–[26]. The resultant PLL structure is often called the multiple SRF-based PLL (MSRF-PLL). This approach, however, causes a considerable increase in the PLL computational effort.

A systematic approach for tuning the control parameters of the DSRF-PLL and its extended version, the MSRF-PLL, can be found in [31]. It is also worth mentioning that the DSRF-PLL is mathematically equivalent with the decoupled double SRF-PLL (DDSRF-PLL) [27]–[29] if the PI controller input signal in the DSRF-PLL is $v^+_{q,1}$ (instead of $\bar{v}^+_{q,1}$). The DDSRF-PLL is a well-known PLL in three-phase systems.

D. Complex-Coefficient-Filter-Based PLLs

Complex-coefficient filters (CCFs) are characterized by having an asymmetrical frequency response around zero frequency, which implies they can make a distinction between the positive and negative sequences (polarities) of the same frequency [116].

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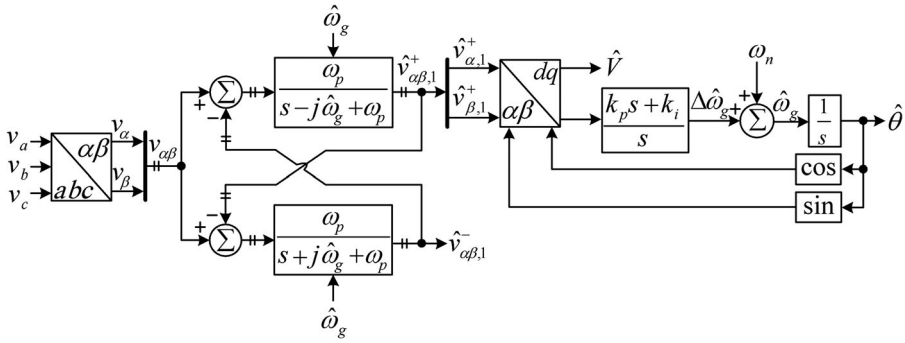

Fig. 8. Schematic diagram of the DCCF-PLL.

This feature of CCFs has made them very interesting for the selective extraction/cancellation of harmonic/disturbance components before the SRF-PLL input [30]–[33]. Fig. 8 shows the schematic diagram of a popular CCF-based PLL, which uses two complex-coefficient bandpass filters as the SRF-PLL prefiltering stage [30]. This structure is often referred to as the dual complex-coefficient filter-based PLL (DCCF-PLL). As shown, the CCFs in the input of the SRF-PLL are working in a collaborative way, each of which is responsible for extracting a particular component of the PLL input.

It is proved in [31] that the DCCF-PLL is mathematically equivalent with the DSRF-PLL (see Fig. 7) if the LPFs in the DSRF-PLL are of first-order with the cutoff frequency ω_p. In addition, the small-signal modeling, stability analysis, and a systematic method for tuning the control parameters of the DCCF-PLL can be found in [31]. It is worth mentioning that the DCCF-PLL can be easily extended to take into account the dominant harmonic components by using extra complex bandpass filters centered at the desired harmonic frequencies. It is also shown in [32] that the dynamic performance of the DCCF-PLL and its extended version can be improved by using a PID controller as the LF in the SRF-PLL and arranging a pole-zero cancellation, which minimizing the dynamic interaction between the CCFs and the SRF-PLL.

It should be mentioned that using CCFs in PLL is not limited to the case described above. Indeed, they may also be used as an in-loop filter inside the SRF-PLL control loop, as suggested in [34] and [35]. This topology, however, has not received much attention.

E. Delayed Signal Cancellation-Based PLLs

The delayed signal cancellation (DSC) operator is a highly popular filter for improving the filtering capability of the SRF-PLL mainly because it can be easily tailored for different grid scenarios [36]-[48]. This operator can be used as an in-loop filter in the SRF-PLL control loop or as a preprocessing tool before the SRF-PLL input. The latter case has received more attention mainly because the in-loop DSC operator increases the phase delay in the SRF-PLL control loop and, therefore, slows down the PLL dynamic response. Regardless of using the DSC operators as an in-loop filter or preprocessing tool, often a chain of them is employed to improve the filtering capability of the SRF-PLL [40]–[47]. Selecting the number of DSC operators in the chain depends on the anticipated harmonic components in the PLL input.

When the DSC operator(s) is employed as the prefiltering stage of the SRF-PLL, the frequency estimated by the SRF-PLL is often fed back to adapt them to the frequency variations[2] [40]–[42]. Adapting DSC operators, however, increases the implementation complexity and the computational effort, particularly when interpolation techniques are employed for this purpose [48]. In addition, the frequency feedback loop makes the system highly nonlinear and, therefore, difficult to analyze from the stability point of view [45]. An alternative approach is using a secondary frequency detector for adapting the DSC operator(s) to the frequency variations [44]–[47]. This method results in better stability properties, but it demands more computational effort. The third method is correcting the phase and amplitude errors at the SRF-PLL output, as suggested in [48]. This technique demands very low computational effort and effectively compensates for the phase and amplitude errors. In addition, as the length of delays of the DSC operators remains fixed in this method, the small-signal modeling and, therefore, the stability analysis can be easily carried out. The shortcoming of this strategy is that it does not correct the imperfect disturbance rejection capability of the nonadaptive DSC operator when the frequency deviates from its nominal value. This problem is not serious when the frequency is close to its nominal value, but it may become troublesome in the presence of large frequency drifts, particularly under severe asymmetrical voltage sags or faults.

F. Second-Order Generalized Integrator-Based PLLs

A second-order generalized integrator (SOGI) acts as a sinusoidal signal integrator and can be arranged to behave as a quadrature signal generator (QSG) and bandpass filter by feeding back its output signal, as shown in the dashed box in Fig. 9 [49], [50]. The bandpass filter and QSG based on the SOGI, briefly referred to as the QSG-SOGI, is a useful tool for the extraction and separation of the FFPS and FFNS components of three-phase signals [117], [118]. The application of this tool for

[2]Using nonadaptive DSC operators in the SRF-PLL input results in phase and amplitude errors and imperfect cancellation of harmonic components in the presence of frequency drifts.

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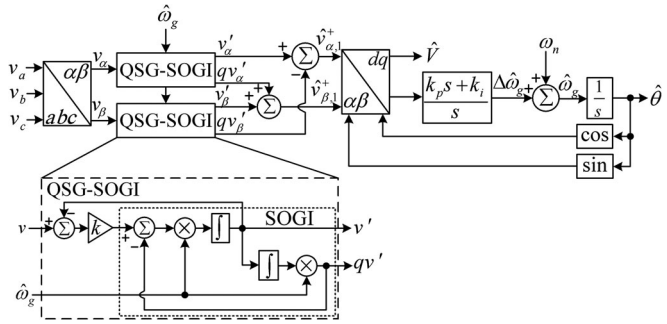

Fig. 9. Schematic diagram of the DSOGI-PLL.

the extraction of the FFPS component before the SRF-PLL input can be observed in Fig. 9 [29], [51]. As shown, two QSG-SOGIs are used to extract the filtered direct and quadrature versions of v_α and v_β. The FFPS component is then calculated based on the instantaneous symmetrical component method. This PLL structure, which under certain conditions is mathematically equivalent to the DSRF-PLL and the DCCF-PLL [31], [32], is often called the dual QSG-SOGI-based PLL (DSOGI-PLL). To improve the harmonic filtering capability of the DSOGI-PLL additional QSG-SOGIs tuned at harmonic frequencies can be added to the standard structure [117]. An alternative approach is to use the third-order generalized-integrator-based bandpass filter and QSG instead of the QSG-SOGI in the DSOGI-PLL structure [33].

It is worth mentioning that a similar PLL to the DSOGI-PLL can be found in [52]. The only difference is that it uses an adaptive notch filter (ANF) based on a least mean square algorithm with two adaptive weights instead of the QSG-SOGI in its structure. It is proved in [53] that this ANF and the SOGI-QSG are mathematically equivalent. Therefore, it can be concluded that the ANF-based PLL proposed in [52] and the DSOGI-PLL are mathematically the same systems.

G. Other PLLs

In [54] and [55], the selective cancellation of harmonic components inside the SRF-PLL control loop by using a repetitive regulator[3] (RR) is suggested. The great feature of this regulator, which is based on the discrete cosine transform, is that its computational burden is independent of the number of harmonics that are intended to be blocked. In other words, removing a single harmonic or m ($m > 1$) harmonics using this regulator requires the same computational effort. It should be mentioned that the computational burden of this regulator highly depends on the sampling frequency: Increasing the sampling frequency drives up the computational cost. Therefore, this regulator may not be suitable for applications where the sampling frequency is high and/or removing a very few harmonics in the PLL control loop is intended.

To remove the FFNS component in the PLL input, reforming the imbalanced signals to balanced ones using a zero-crossing detection (ZCD)-based method is suggested in [57]. The ZCD-based PLL is simple to implement and can operate effectively even in the presence of multiple zero crossings in the PLL input signals. However, it only considers the amplitude imbalance in the PLL input, which means it cannot remove the FFNS component caused by the phase imbalance. The harmonic filtering capability of this PLL is also limited.

In [59], employing the space vector Fourier transform (SVFT) as the SRF-PLL prefiltering stage is suggested. The SVFT, which can effectively reject all harmonic components, demands a low computational effort when implemented in the recursive form. However, the recursive implementation of the SVFT-based filter involves some stability problems [120]. This stability problem can also be avoided by implementing the SVFT in the nonrecursive form, but at the cost of a considerable increase in the computational cost.

In [60], including second-order lead compensators (SOLC) into the SRF-PLL control loop is suggested. These compensators have pairs of purely imaginary zeros and poles, which means they can provide a selective harmonic cancellation like NFs without causing phase delay in the SRF-PLL control loop. As a result, using these compensators improves the filtering capability of the SRF-PLL without limiting its bandwidth. This improvement, however, is at the cost of a low noise immunity for the SOLC-based PLL.

H. Performance Comparison

A performance comparison between some of the PLLs analyzed before can be observed in Table I. It should be mentioned that in all PLLs that benefit from a high disturbance rejection selectivity (i.e., the ability to decide which harmonics/disturbances should be rejected), there is a direct relation between the PLL filtering capability and its computational burden: the PLL filtering capability can be improved by adding more filter modules but at the cost of a higher computational burden. Here, the only exception, as discussed before, is the RR-based PLL. It should also be emphasized here that the results reported in Table I are corresponding to the typical structure of each PLL. For example, a high filtering capability and a slow dynamic response have been attributed to the in-loop DSC-based PLL because, in its typical structure, multiple *dq*DSC operators are used in the PLL control loop which result in a high filtering capability at the cost of a slow dynamic response.

I. Problem of DC Offset

Throughout Section III, the focus was mainly on PLLs with enhanced harmonic/imbalance rejection capability. The grid voltage imbalance and harmonic components, however, are not the only disturbances that PLLs should deal with. Indeed, in addition to these disturbances, PLLs must have a high dc offset rejection capability. This is particularly important for PLLs that are used for the synchronization of grid-connected current-controlled converters; otherwise, it may results in dc injection by the converter [61]. It is worth mentioning that the presence of the dc offset in the PLL input may be due to grid faults, measurement devices, dc injection from distributed generation

[3]Originating from the internal model principle, RRs are highly popular for tracking a period reference or rejecting period disturbances [56].

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TABLE I
PERFORMANCE COMPARISON BETWEEN SOME ADVANCED PLLS

Standard PLLs	Sub-classification	Features					
		Disturbance rejection selectivity	Filtering capability	Harmonic extraction	Dynamic response	Computational burden	Noise immunity
MAF-based PLLs	In-loop MAF-based PLL [6], [8]	Low	High	No	Slow[1]	Low	High
	Preloop MAF-based PLL [7], [17]	Low	High	No	Fast	Low	High
NF-based PLLs	Cascaded NF-based PLL [18], [19]	High	High	No	Fast	High[2]	High
	Parallel NF-based PLL [20], [21]	High	High	Yes[3]	Fast	High[2]	High
MSRF-based PLLs [24]-[27]	———	High	High	Yes	Fast	High	High
CCF-based PLLs	In-loop CCF-based PLL [34], [35]	High	High	Yes[3]	Fast	High	High
	Preloop CCF-based PLL [30], [32]	High	High	Yes	Fast	High	High
DSC-based PLLs	In-loop DSC-based PLL [41], [43]	Average	High	No	Slow[4]	Low	High
	Preloop DSC-based PLL [40], [44], [48]	Average	High	No	Fast	Depends on topology[5]	High
SOGI-based PLLs [31], [51]	———	High	High	Yes	Fast	High	High
Other PLLs	RR-based PLL [54], [55]	High	High	No	Average	High	High
	ZCD-based PLL [57]	——[6]	Low	No	Fast	Low	Low
	SVFT-based PLL [59]	Low	High	No	Fast	High	High
	SOLC-based PLL [60]	High	Average	No	Fast	Average	Low

[1] The dynamic response of the in-loop MAF-based PLL can be considerably improved by using the PID-type loop filter [6], [11], the lead compensator [12], or the QT1 structure in the implementation [15].
[2] From the computational burden point of view, parallel NFs are probably more interesting than cascaded NFs because they use the same frequency update loop.
[3] The harmonic extraction is carried out in the *dq*-frame.
[4] The dynamic response can be improved by using PID-type LF [43] or a lead compensator [61].
[5] Computational burden is low when non-adaptive DSC operators with phase/amplitude error compensators are used, and it can be high when DSC operators are adapted to the grid frequency variations using interpolation techniques [48].
[6] In this PLL, no particular filter for rejecting harmonics is used. The ZCD-based technique in the input of this PLL only removes the grid voltage imbalance.

systems, geomagnetic phenomena, half-wave rectification, etc. [61], [62].

To tackle the problem of dc offset in PLLs, different approaches have been proposed in the literature. In [62], adding an integrator-based dc offset estimation/rejection loop to the standard PLL structure is suggested. This approach is simple and effective. A detailed mathematical analysis of this technique can be found in [63]. In [64], subtracting the $\alpha\beta$-axis voltage components from their delayed versions and passing the result through a frequency-adaptive correction unit is suggested. This technique ensures a complete and fast rejection of the dc offset in PLLs. A performance comparison of five other dc-offset rejection strategies can be found in [61].

IV. ADAPTIVE LF-BASED PLLS

Sometimes, for particular control objectives, the LF parameters of PLL are dynamically adjusted [65]–[67]. Here, such PLLs are referred to as adaptive LF-based PLLs. A common characteristic of all these PLLs is that they are highly nonlinear, and therefore, their stability analysis is very difficult. This section briefly reviews these PLLs.

A. SRF-PLL With Adaptive Frequency Estimation Loop

In the SRF-PLL, particularly the one shown in Fig. 4, dynamics of the phase and frequency estimation loops are dominantly determined by the proportional gain k_p and the integral gain k_i, respectively. Despite this fact, there are some coupling between the phase and frequency estimation loops that depend on the SRF-PLL bandwidth: the higher the SRF-PLL bandwidth, the larger the coupling between phase and frequency variables. Consequently, increasing the SRF-PLL bandwidth (for example, to achieve a fast dynamic response) increases the coupling between phase and frequency variables and, therefore, causes a large transient in the estimated frequency during the startup and when a large phase-angle jump happens. To deal with this problem, an adaptive mechanism is suggested in [65], which dynamically adjusts the gain of the frequency estimation loop based on the level of phase deviations. This technique, as highlighted in Fig. 10, multiplies the integral gain k_i with

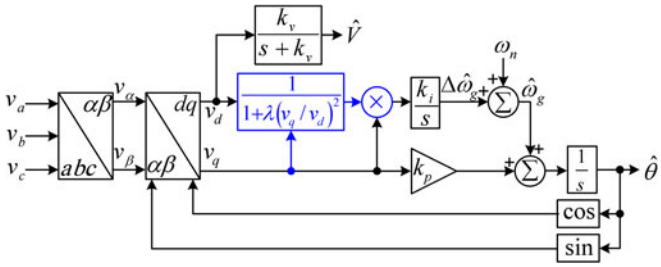

Fig. 10. SRF-PLL with adaptive frequency estimation loop.

$$\frac{1}{1+\lambda(v_q/v_d)^2} \tag{12}$$

in which λ is a positive constant. When a phase-angle jump happens, (12) becomes a small value, which reduces the gain of the frequency estimation and therefore prevent a large transient in the estimated frequency. When the signal v_q (which contains the phase error information) tends to zero, (12) approaches unity and restores the gain of the frequency estimation loop to its original value, i.e., k_i. Therefore, this adaptive mechanism has no adverse effect on the steady-state performance of the SRF-PLL. The ease of implementation and effectiveness are the key features of this technique.

B. SRF-PLL With Adaptive Loop Gain

The adaptive mechanism suggested in [66] and [67] is multiplying the PI controller input by a factor of the absolute value of its output, as highlighted in Fig. 11. It should be mentioned that this technique has been applied to a single-phase PLL in [66] and [67], but without any change, it is applicable to a three-phase PLL. When a transient happens, the signal v_q (which contains the phase error information) is amplified by the adaptive mechanism. This amplification is corresponding to increase the PLL loop gain, which results in a faster dynamic response. In the phase-locked condition, however, the signal v_q become zero, which nullifies the influence of adaptive mechanism on the PLL loop gain. The reported results in [66] and [67] show this

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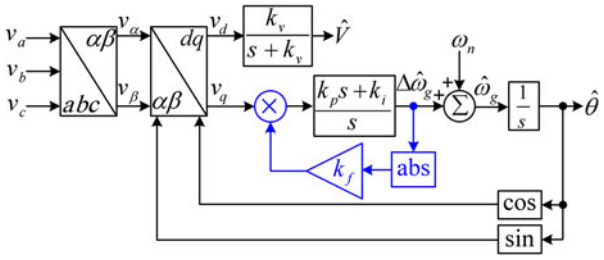

Fig. 11. SRF-PLL with adaptive loop gain.

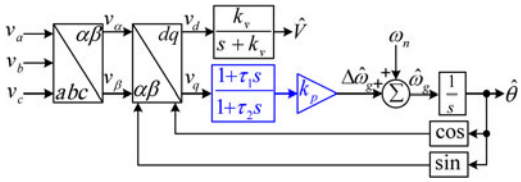

Fig. 12. Schematic diagram of a typical type-1 PLL.

technique makes the PLL dynamic response highly oscillatory, which causes a serious concern about the PLL stability.

V. Type-N and Quasi-Type-N PLLs

Most of PLLs employ a PI controller as the LF in their structure and, therefore, are of type 2. Sometimes, however, different LFs are selected for the PLL and/or a secondary control path is added to the PLL structure, which change the type of PLL, at least apparently. This section briefly discusses this issue.

A. Type-1 PLLs

A type-1 PLL is characterized by having only one integrator in its control loop [119]. There are different ways to implement a type-1 SRF-PLL. The easiest method is to replace the PI controller in the conventional SRF-PLL with a simple gain [58]. Alternative approaches are using lag filters or lag-lead filters as the LF is the conventional SRF-PLL [8], [15], [68], [69], [119]. The schematic diagram of a type-1 PLL with a lag/lead controller as the LF can be observed in Fig. 12.

A type-1 PLL is able to track phase-angle jumps with zero steady-state error, but it fails to do so in the presence of frequency drifts [2], [3], [8], [15], [119]. For example, in the case of the type-1 PLL shown in Fig. 12, there is a steady-state phase error equal to

$$e_{\rm ss}^{\Delta\omega_g} = \sin^{-1}\left(\frac{\Delta\omega_g}{k_p V}\right) \tag{13}$$

in its output when its input signals experience a frequency step change equal to $\Delta\omega_g$. Obviously, this steady-state error can be reduced by increasing the value of k_p. This measure, however, would be at the cost of degrading the PLL filtering capability. This drawback of type-1 PLLs has limited their usage to applications where the frequency is fixed or has small variations around its nominal value. Regardless of this drawback, the type-1 PLLs benefit from a fast dynamic response and a high stability margin.

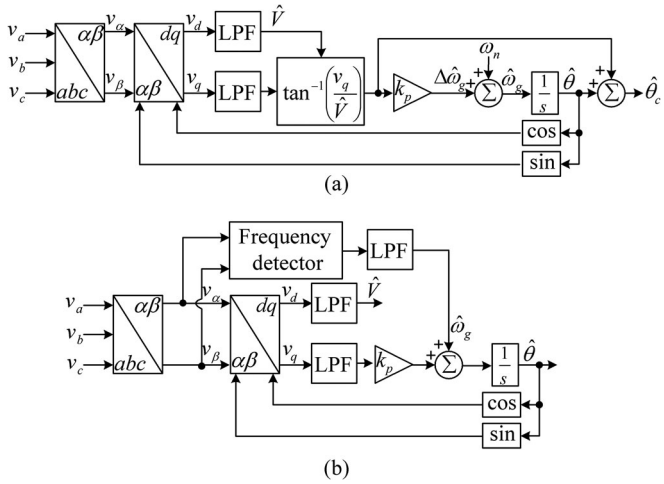

Fig. 13. Schematic diagram of two QT1-PLLs.

B. QT1-PLLs

QT1-PLLs have a similar structure to a type-1 PLL, but from the control point of view, they are type-2 control systems. That is the reason why they are referred to as "quasi-type-1."

Two different ways to implement a QT1-PLL have been proposed in the literature. The first one can be observed in Fig. 13(a) [15]. By neglecting the link that adds the gain k_p input signal to the PLL output, this structure is a type-1 PLL which uses a lag filter as the LF and employs an inverse tangent operation for the amplitude normalization. As mentioned before, using such ANS removes the nonlinearity of the PLL phase control loop. Therefore, in the presence of this ANS, the steady-state phase error of type-1 SRF-PLLs under frequency drifts is

$$e_{\rm ss}^{\Delta\omega_g} = \frac{\Delta\omega_g}{k_p}. \tag{14}$$

Therefore, adding the input signal of gain k_p [this signal is equal to $\Delta\hat{\omega}_g/k_p$ and, therefore, can be considered as an estimation of (14)] to the type-1 PLL output corrects its steady-state phase error under frequency drifts. It is worth mentioning that the LPF block in Fig. 13(a) can be any kind of LPF. In [15], it is considered to be an MAF, which results in a high filtering capability while maintaining a fast dynamic response for the PLL.

An alternative approach for implementing a QT1-PLL is dynamically adjusting the center frequency of the VCO of a type-1 PLL with an estimation of the frequency [70]. A typical structure for this QT1-PLL can be observed in Fig. 13(b). The frequency detector in this structure plays the same role as the integrator of PI controller in Fig. 4.

C. Type-3 PLLs and Quasi-Type-2 PLLs

Type-3 PLLs are characterized by having three pure integrators in their control loop, which enable them to track frequency ramps with a zero steady-state phase error [72], [119].

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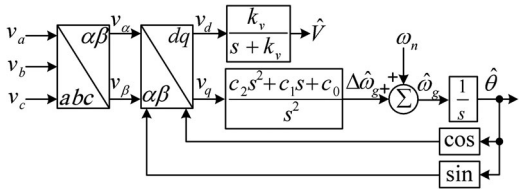

Fig. 14. Schematic diagram of a type-3 PLL.

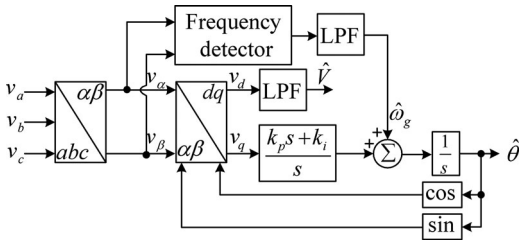

Fig. 15. Schematic diagram of a QT2-PLL.

The schematic diagram of a typical type-3 PLL can be seen in Fig. 14 [72]. Having a negative gain margin (GM) in dB and the risk of instability under low loop gains are other characteristics of these PLLs [72]. For this reason, using the ANS in these PLLs is vital.

Quasi-type-2 PLLs (QT2-PLLs) are type-3 control systems from the control point of view, which means they can track frequency ramps with zero steady-state phase error and they have a negative GM [71], [72]. Their difference with type-3 PLLs (like the one shown in Fig. 14) is that they are immune to the instability under voltage sags [71], [72]. Therefore, using the ANS for these PLLs is not mandatory, but it is recommended. The schematic diagram of a typical QT2-PLL is shown in Fig. 15 [71]–[74]. An alternative method for implementing QT2-PLLs can be found in [75].

VI. PLL Implementation Without Direct Computation of Trigonometric Functions

The PLL implementation involves the computation of trigonometric functions, which from some computational point of view can be a disadvantage. To solve this issue, several techniques have been proposed, which are examined in what follows.

A. PLL With a Square-Wave VCO

The first approach to get rid of the calculation of trigonometric functions in the PLL implementation is to use a square-wave VCO [76]. The schematic diagram of the conventional SRF-PLL with the square-wave VCO can be observed in Fig. 16.

According to the Fourier series, signals $f_c(\hat{\theta})$ and $f_s(\hat{\theta})$ can be expressed as

$$f_c(\hat{\theta}) = \cos(\hat{\theta}) - \frac{1}{3}\cos(3\hat{\theta}) + \frac{1}{5}\cos(5\hat{\theta}) - \cdots$$
$$f_s(\hat{\theta}) = \sin(\hat{\theta}) + \frac{1}{3}\sin(3\hat{\theta}) + \frac{1}{5}\sin(5\hat{\theta}) + \cdots . \quad (15)$$

It can be observed that signals $f_c(\hat{\theta})$ and $f_s(\hat{\theta})$ contain a high harmonic content, which results in a large oscillatory error in the PLL output even when the PLL input signals are free from any harmonics. In addition, if the PLL input signals have the same harmonic components as $f_c(\hat{\theta})$ and $f_s(\hat{\theta})$, an offset error in the PLL output happens. To deal with these problems, including an MAF before the PI controller and using a selective harmonic elimination (SHE) square-wave generator instead of the simple square-wave generator is suggested in [76]. The resultant PLL structure is referred to as the SHE-PLL. This PLL has two main drawbacks: 1) it has a slow dynamic response because of the presence of the MAF in its control loop; 2) it may not be suitable for applications where in addition to the estimated phase, frequency, and amplitude, the unit vector (the sine and cosine of the phase angle estimated by the PLL) is also required.

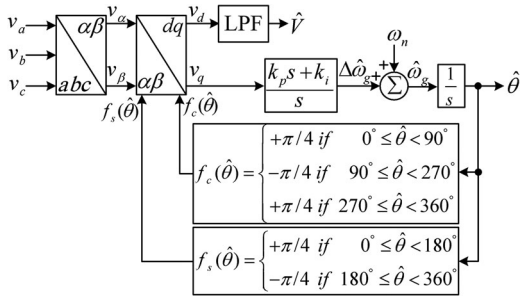

Fig. 16. Schematic diagram of the SRF PLL with a square-wave VCO.

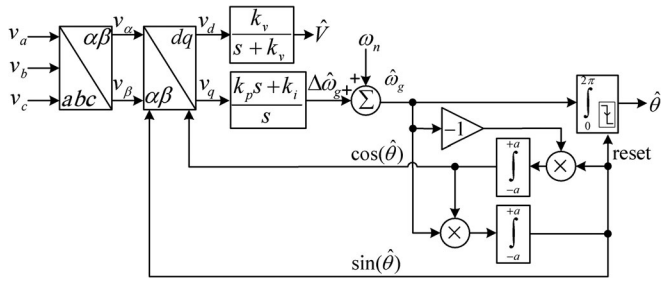

Fig. 17. Schematic diagram of the SRF PLL with a high-performance VCO.

B. PLL With a High-Performance VCO

Fig. 17 shows the conventional SRF-PLL with a high-performance VCO, which is based on the digital implementation of an *RC* electronic oscillator [23]. The operating principle of this VCO is as follows. The VCO oscillates at $\hat{\omega}_g$ and tends to become unstable because it has two poles on the imaginary axis. However, as the integrators are saturated, the amplitude of signals is controlled.

The calculation of trigonometric functions using this VCO is carried out with a low computational effort. However, the computed $\sin(\hat{\theta})$ and $\cos(\hat{\theta})$ are not pure sinusoidal waves, due to nonlinearities caused by the saturations. The total harmonic distortion (THD) of these sinusoidal waves highly depends on the sampling frequency: increasing the sampling frequency reduces the THD.

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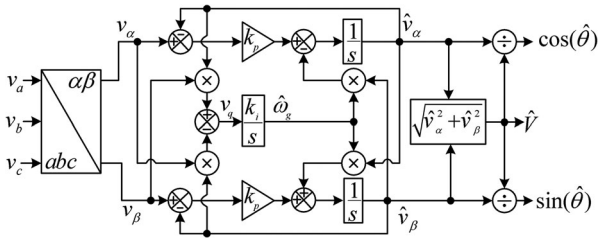

Fig. 18. VCO-less PLL.

C. VCO-Less PLL

The synchronization technique shown in Fig. 18 estimates the amplitude, frequency, and the unit vector [$\sin(\hat{\theta})$ and $\cos(\hat{\theta})$] without any need for the computation of trigonometric functions. This structure is often referred to as the frequency-locked loop-based synchronization technique [77] or non-PLL synchronization strategy [78], [79]; however, as [80] recommends, it is better to be called the VCO-less PLL because, under certain conditions, it is mathematically equivalent with the conventional SRF-PLL. As the equivalence of the VCO-less PLL (see Fig. 18) and the SRF-PLL (see Fig. 4) is largely unknown, the proof of equivalence is presented below.

1) Frequency Estimation: Using Fig. 18, differential equations describing dynamics of the VCO-less PLL can be obtained as

$$\dot{\hat{v}}_\alpha(t) = -\hat{\omega}_g \hat{v}_\beta(t) + k_p\left[v_\alpha(t) - \hat{v}_\alpha(t)\right] \tag{16}$$

$$\dot{\hat{v}}_\beta(t) = \hat{\omega}_g \hat{v}_\alpha(t) + k_p\left[v_\beta(t) - \hat{v}_\beta(t)\right] \tag{17}$$

$$\dot{\hat{\omega}}_g = k_i v_q(t) \tag{18}$$

where $v_q(t) = v_\beta(t)\hat{v}_\alpha(t) - v_\alpha(t)\hat{v}_\beta(t)$.

Differentiating (18) with respect to time gives

$$\begin{aligned}\ddot{\hat{\omega}}_g &= k_i \dot{v}_q(t)\\ &= k_i[\dot{v}_\beta(t)\hat{v}_\alpha(t) + v_\beta(t)\dot{\hat{v}}_\alpha(t) - \dot{v}_\alpha(t)\hat{v}_\beta(t) - v_\alpha(t)\dot{\hat{v}}_\beta(t)]\\ &= k_i\left(\omega_g - \hat{\omega}_g\right)v_d(t) - k_p\dot{\hat{\omega}}_g\end{aligned} \tag{19}$$

where $v_d(t) = v_\alpha(t)\hat{v}_\alpha(t) + v_\beta(t)\hat{v}_\beta(t)$. Under a quasi-locked state, the signal v_d can be well approximated by $v_d \approx V\hat{V} \approx V^2$.

Considering the definitions $\hat{\omega}_g = \omega_n + \Delta\hat{\omega}_g$ and $\omega_g = \omega_n + \Delta\omega_g$, (19) can be rewritten as

$$\Delta\ddot{\hat{\omega}}_g = k_i\left(\Delta\omega_g - \Delta\hat{\omega}_g\right)V^2 - k_p\Delta\dot{\hat{\omega}}_g. \tag{20}$$

Taking the Laplace transform of both sides (20) yields

$$\frac{\Delta\hat{\omega}_g(s)}{\Delta\omega_g(s)} = \frac{V^2 k_i}{s^2 + k_p s + V^2 k_i}. \tag{21}$$

Assuming k_p and k_i in Fig. 18 are the same as those in Fig. 4, it is clear from (21) and (8) that the VCO-less PLL and the SRF-PLL have the same dynamics in the frequency estimation if $V = 1$.

2) Amplitude Estimation: Using Fig. 18, the amplitude estimated by the VCO-less PLL can be expressed as

$$\hat{V} = \sqrt{\hat{v}_\alpha^2 + \hat{v}_\beta^2}. \tag{22}$$

Differentiating (22) with respect to time results in

$$\dot{\hat{V}} = \frac{\left(\dot{\hat{v}}_\alpha\hat{v}_\alpha + \dot{\hat{v}}_\beta\hat{v}_\beta\right)}{\hat{V}}. \tag{23}$$

Substituting (16) and (17) into (23) gives

$$\begin{aligned}\dot{\hat{V}} &= k_p\frac{\left[v_\alpha(t) - \hat{v}_\alpha(t)\right]\hat{v}_\alpha + \left[v_\beta(t) - \hat{v}_\beta(t)\right]\hat{v}_\beta}{\hat{V}}\\ &= k_p\frac{v_d - \hat{V}^2}{\hat{V}}\\ &\approx k_p\left(V - \hat{V}\right).\end{aligned} \tag{24}$$

Taking the Laplace transform of both sides (24) yields

$$\hat{V}(s) = \frac{k_p}{s + k_p}V(s). \tag{25}$$

Considering (25), Fig. 4, and what mentioned in Section II, it can be concluded that the VCO-less PLL and the SRF-PLL shown in Fig. 4 have the same dynamics in the amplitude estimation if k_p and k_v in the SRF-PLL are equal. Remember that it was already assumed that k_p and k_i in the SRF-PLL are the same as those in the VCO-less PLL.

3) Phase Estimation: The VCO-less PLL does not provide a direct estimation of the phase angle. However, if it is required, it can be estimated as

$$\hat{\theta} = \tan^{-1}\left(\frac{\hat{v}_\beta}{\hat{v}_\alpha}\right). \tag{26}$$

Following a similar procedure as above, it can be shown that the phase-estimation dynamics in the VCO-less PLL can be approximated by the following transfer function:

$$\frac{\Delta\hat{\theta}(s)}{\Delta\theta(s)} = \frac{k_p s + V^2 k_i}{s^2 + k_p s + V^2 k_i} \tag{27}$$

which is the same as that of the SRF-PLL [see (9)] if $V = 1$.

It is worth mentioning that for the case where $V \neq 1$, the equivalence of the VCO-less PLL and the SRF-PLL holds if signal v_q in Figs. 4 and 18 is divided by $\hat{V}$ and $\hat{V}^2$, respectively

VII. Conclusion

This paper provides overviews of recent attempts in designing advanced three-phase PLLs. Generally speaking, these attempts are:

1) exploring ways to realize PLLs of different type, particularly QT1-PLLs, QT2-PLLs, and type-3 PLLs;
2) investigating approaches to eliminate the need for the (direct) computation of trigonometric functions in the implementation of PLLs, which is advantageous from some computational point of view;
3) seeking methods to improve the dynamic performance of PLLs by dynamically adjusting their LF parameter(s);

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4) improving the filtering capability and disturbance rejection ability of PLLs by including different filters inside their control loop or before their input.

In each case, the operating principle of PLLs was explained and their advantages and disadvantages were briefly discussed. The information provided in this paper can be very useful for researchers who are new in the field and want to make a contribution to the area and also for engineers who want to select a proper synchronization technique for their particular application.

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