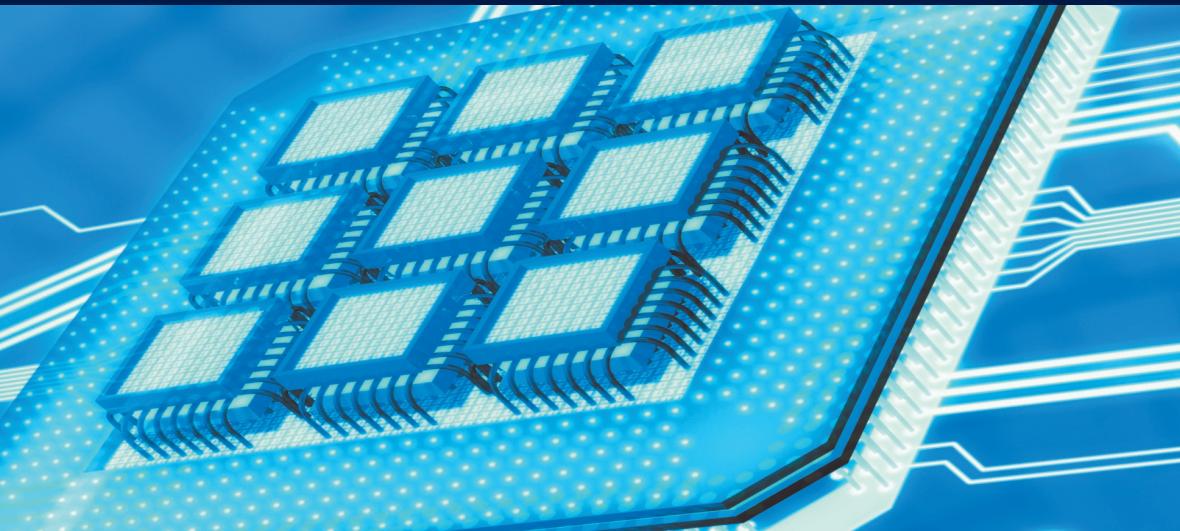


**FOCUS**

**ELECTRICAL ENGINEERING SERIES**



# **Analysis and Design of Multicell DC/DC Converters using Vectorized Models**

**Thierry Meynard**

**iSTE**

**WILEY**



# **Analysis and Design of Multicell DC/DC Converters using Vectorized Models**



**FOCUS SERIES**

*Series Editor Jean-Pascal Cambronne*

---

**Analysis and Design of  
Multicell DC/DC Converters  
using Vectorized Models**

---

Thierry Meynard

**iSTE**

**WILEY**

First published 2015 in Great Britain and the United States by ISTE Ltd and John Wiley & Sons, Inc.

Apart from any fair dealing for the purposes of research or private study, or criticism or review, as permitted under the Copyright, Designs and Patents Act 1988, this publication may only be reproduced, stored or transmitted, in any form or by any means, with the prior permission in writing of the publishers, or in the case of reprographic reproduction in accordance with the terms and licenses issued by the CLA. Enquiries concerning reproduction outside these terms should be sent to the publishers at the undermentioned address:

ISTE Ltd  
27-37 St George's Road  
London SW19 4EU  
UK

[www.iste.co.uk](http://www.iste.co.uk)

John Wiley & Sons, Inc.  
111 River Street  
Hoboken, NJ 07030  
USA

[www.wiley.com](http://www.wiley.com)

© ISTE Ltd 2015

The rights of Thierry Meynard to be identified as the author of this work have been asserted by him in accordance with the Copyright, Designs and Patents Act 1988.

Library of Congress Control Number: 2014956808

---

British Library Cataloguing-in-Publication Data  
A CIP record for this book is available from the British Library  
ISSN 2051-2481 (Print)  
ISSN 2051-249X (Online)  
ISBN 978-1-84821-800-0

---

---

# Contents

---

<b>CHAPTER 1. GENERAL PROPERTIES OF MULTILEVEL CONVERTERS . . . . .</b>	<b>1</b>
1.1. Time-domain: multilevel waveform and apparent switching frequency. . . . .	1
1.2. Frequency domain: harmonic cancellation. . . . .	4
1.3. Transient response . . . . .	5
1.4. Conclusion. . . . .	6
<b>CHAPTER 2. TOPOLOGIES OF MULTILEVEL DC/DC CONVERTERS . . . . .</b>	<b>9</b>
2.1. Series connection . . . . .	9
2.1.1. Direct series connection with isolated sources . . . . .	9
2.1.2. Flying capacitor. . . . .	11
2.2. Parallel connection . . . . .	14
2.2.1. Interleaved choppers with star-connected inductors . . . . .	14
2.2.2. Interleaved choppers with InterCell Transformers (ICTs). . . . .	17
2.3. Series-parallel connection . . . . .	20

<b>CHAPTER 3. CONCEPT OF VECTORIZATION IN PLECS . . . . .</b>	<b>23</b>
3.1. Vectorized components . . . . .	23
3.2. Star-connection block and parallel multicell converter . . . . .	25
3.3. Series connection block and series multicell converter . . . . .	27
3.4. Generalized multicell commutation cell . . . . .	28
3.5. Practice. . . . .	34
3.5.1. How to? . . . . .	34
3.5.2. Basic blocks . . . . .	34
<b>CHAPTER 4. VECTORIZED MODULATOR FOR MULTILEVEL CHOPPERS . . . . .</b>	<b>37</b>
4.1. General principle . . . . .	37
4.2. xZOH: equalizing multisampler for multilevel choppers . . . . .	38
4.2.1. Control as the main source of perturbation . . . . .	38
4.2.2. Handling duty cycle variation . . . . .	38
4.2.3. Frequency response of the equalizing sampler and modulator . . . . .	51
4.3. Practice. . . . .	53
<b>CHAPTER 5. VOLTAGE BALANCE IN SERIES MULTILEVEL CONVERTERS . . . . .</b>	<b>57</b>
5.1. Basic principles . . . . .	57
5.2. Linear circuits . . . . .	58
5.2.1. Internal balancers . . . . .	58
5.2.2. External balance boosters . . . . .	59
5.2.3. Pros and cons of internal/ external balance boosters . . . . .	64
5.3. Nonlinear variants . . . . .	65
5.3.1. Internal balance boosters . . . . .	65
5.3.2. External balance boosters . . . . .	66
5.4. Loss-based design . . . . .	67
5.4.1. Introduction . . . . .	67
5.4.2. Internal balance boosters . . . . .	68
5.4.3. External balance boosters . . . . .	68
5.5. Vectorized models of balance boosters . . . . .	69

<b>CHAPTER 6. FILTER DESIGN. . . . .</b>	<b>75</b>
6.1. Requirements . . . . .	75
6.1.1. Steady state: current ripple, voltage ripple and standards . . . . .	75
6.1.2. Transients . . . . .	83
6.1.3. Extra design constraints . . . . .	84
6.2. Design process . . . . .	85
<b>CHAPTER 7. DESIGN OF MAGNETIC COMPONENTS FOR MULTILEVEL CHOPPERS. . . . .</b>	<b>89</b>
7.1. Requirements and problem formulation . . . . .	89
7.2. Area product . . . . .	92
7.2.1. Low frequency – low ripple formulation for filtering inductors . . . . .	92
7.2.2. General formulation for filtering inductors . . . . .	94
7.2.3. Application to inductors for interleaved converters . . . . .	95
7.2.4. Extension to InterCell Transformers . . . . .	97
7.3. Optimal area product of magnetic components for interleaved converters . . . . .	99
7.3.1. Optimal area product for inductors . . . . .	99
7.3.2. Optimal area product for InterCell Transformers . . . . .	101
7.4. Weight-optimal dimensions for a given area product . . . . .	101
7.4.1. For inductors . . . . .	101
7.4.2. For InterCell Transformers . . . . .	107
7.5. Volume-optimal dimensions for a given area product . . . . .	118
7.6. Number of turns and air gap . . . . .	120
7.7. Accounting for current overload . . . . .	123
7.8. Optimal phase sequence for InterCell Transformers . . . . .	123
7.9. Vectorized reluctance model of magnetics . . . . .	125
7.9.1. Inductors . . . . .	125
7.9.2. Cyclic cascade InterCell Transformers . . . . .	126

7.9.3. Monolithic InterCell	
Transformers . . . . .	128
7.10. Design process . . . . .	130
<b>CHAPTER 8. CLOSED-LOOP CONTROL OF MULTILEVEL DC/DC CONVERTERS.</b>	
	131
8.1. Principle . . . . .	131
8.2. Corresponding PLECS block. . . . .	133
8.3. Average model of the macro- commutation cell for transient studies . . . . .	136
8.4. Conclusion. . . . .	140
<b>BIBLIOGRAPHY</b> . . . . .	141
<b>INDEX</b> . . . . .	145

---

# General Properties of Multilevel Converters

---

Multilevel converters use many different topologies depending on the type of conversion, the power range, etc., but the basic properties are always the same. These properties are reviewed here.

## 1.1. Time-domain: multilevel waveform and apparent switching frequency

Standard two-level converters use the variation of the duty cycle of these levels to regulate the average power flowing between a current source and a voltage source, which is generally referred to as pulse width modulation (PWM). Multicell converters combine such two-level waveforms to create multilevel waveforms. This is illustrated in Figure 1.1 with three of these two-level PWM waveforms of the same duty cycle and frequency but with a phase-shift of  $120^\circ$ . When the duty cycle is less than  $1/3$ , the sum of the three is also a square voltage taking values 0 and 1. But when the duty cycle increases, the overlapping creates higher levels as shown in case of a duty cycle of 50% (right). In practice, since each cell handles a fraction of the power, the composition of PWM results generally in an average rather than a sum, and the

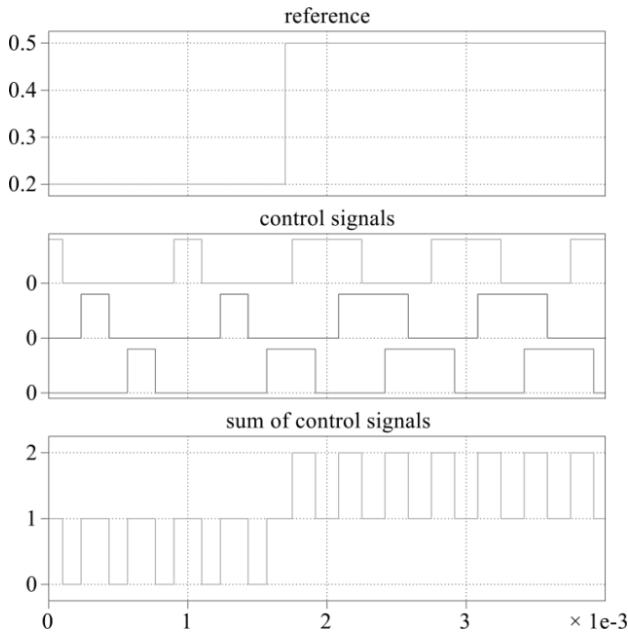
amplitude is then  $n$  times smaller. This property gave the name of multilevel converters that is in general used only for series connection and medium-voltage (MV) applications, although the same combinations of waveforms can be found on the current waveforms of parallel multicell converters used in low and very low-voltage (LV) applications.

In the same figure, we see that when the reference is constant the sum of the three signals is also a 2-level square voltage, but its frequency sometimes called “apparent switching frequency” is three times the frequency of each of the PWM signals. This property is interesting since higher switching frequency may reduce the size and weight of the filters, but it is generally obtained at the cost of increased switching losses; however multicell converters generate waveforms with a better trade-off between apparent switching frequency and switching losses. This property is generally highlighted for parallel multicell converters which are often called “interleaved converters”; interleaving or phase-shifting the PWMs is the key to generate higher switching frequency, but it is also found on voltage waveforms of a series multicell converter.

It can be seen that multilevel waveforms and higher apparent switching frequency are closely related and may apply to current and/or voltage waveforms of series and parallel multicell converters.

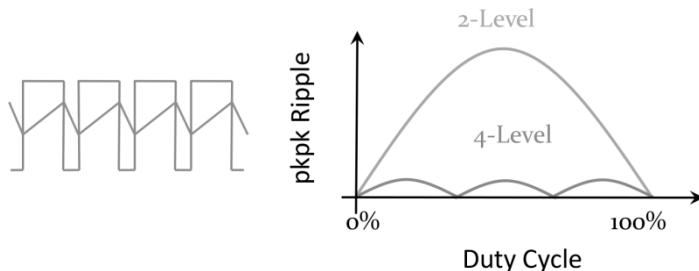
The PWM waveform generated by a commutation cell needs to be filtered. Filtering components act as integrators so the ripple is a triangular waveform and its amplitude reaches a maximum for a duty cycle of 50%. This property transfers to the sum of  $n$  PWM waveforms, but the maximum amplitude is reduced by a factor  $n^2$  due to both the reduction in amplitude of the square voltage and the increase in the apparent frequency. Interleaving also creates an “apparent duty cycle” that is different from the individual duty cycle:

$$D_{\text{apparent}} = \text{mod}(n.D, 1) \quad [1.1]$$



**Figure 1.1.** Time domain sum of PWM signals. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

The resulting ripple is shown in Figure 1.2. It can represent both the current ripple on the low-voltage side (LV side) of a series or parallel multicell commutation cell, and the voltage ripple on the high-voltage side of a parallel multicell commutation cell.



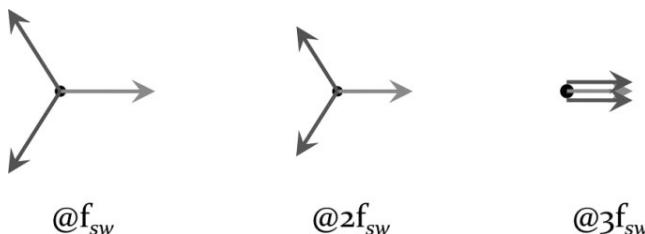
**Figure 1.2.** Ripple as the integral of a PWM waveform. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

## 1.2. Frequency domain: harmonic cancellation

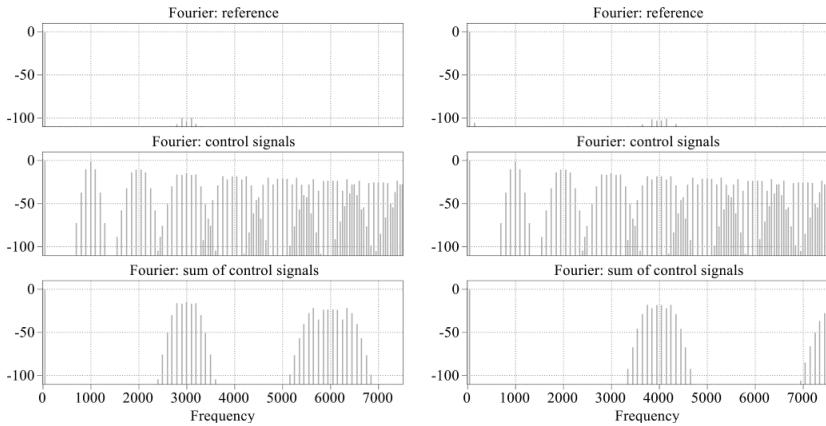
Using the term phase-shifted PWMs is not the best way to describe interleaved control especially to understand how harmonics compose in multicell converters; it would be more appropriate to speak of time-delayed PWM signals because the consequence on phase is different for each rank. If  $s_1$  is a signal of period  $T$  with amplitudes and phases of harmonics equal to  $a_n$  and  $\phi_n$ , and  $s_2$  is equal to signal  $s_1$  of period  $T$  but delayed by  $T_d$ , we get:

$$s_2(t) = s_1(t - T_d) = \sum_{n=0}^{\infty} a_n e^{j\left(\frac{n2\pi}{T}(t-T_d)+\phi_n\right)} = \sum_{n=0}^{\infty} a_n e^{j\left(\frac{n2\pi}{T}t+\phi_n-n\frac{2\pi T_d}{T}\right)} \quad [1.2]$$

Therefore, it can be seen that the phase of each harmonic in  $s_2$  is the phase of  $s_1$  augmented by the phase-shift of the fundamental multiplied by the harmonic rank. The vector diagrams corresponding to three PWM signals delayed by 1/3 of period are shown in Figure 1.3: the first diagram corresponding to the fundamental rank gives a zero-sequence, the second diagram related to rank 2 is a negative sequence and the third diagram corresponding to rank 3 is a zero-sequence. This means that if the three PWMs have the same amplitudes and duty cycles, the amplitude of the first and second harmonic of the sum will be zero, and the third will be the sum of those of the three signals.



**Figure 1.3.** Harmonic composition of time-delayed signals. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)



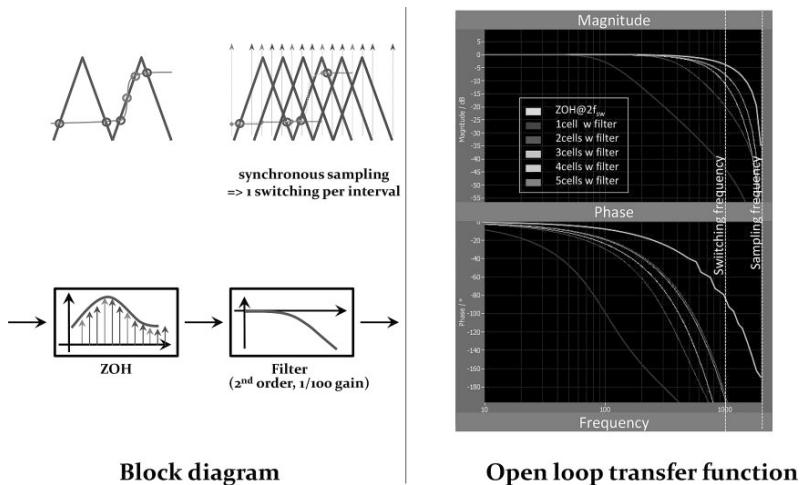
**Figure 1.4.** Spectrum resulting of interleaved PWM

This directly generalizes for the sum of  $n$  PWM signals that contain only harmonics at the multiples of  $n.f$ . When the PWM is modulated to generate an Alternating Current (AC) waveform, the property is maintained with a good accuracy if there is a sufficient difference between the modulation and switching frequency. This can be verified by looking at the waveforms in Figure 1.4.

### 1.3. Transient response

The dynamic response of converters is mainly influenced by the limitations of power semiconductors on the one hand, and by the energy stored in the filters on the other hand. Power semiconductors cannot accept more than a certain amount of switching losses, and cannot accept very short 'on' or 'off' pulses. For this reason, in two-level converters the switching frequency is generally precisely imposed by sampling the duty cycle reference at the switching frequency or at twice the switching frequency; that means that for a period, or half a period, the control cannot react to any perturbation and this is the first factor limiting the response

time. The square waveform generated by a two-level commutation cell needs to be filtered, and this 'inertia' is the second factor limiting the overall response time. If a second-order filter is used, the attenuation required determines its natural frequency directly. Output ripple must generally be limited to a very low value, and as a consequence, the transfer function and the response time of the commutation cell equipped with its filter is dominated by the filter. This is illustrated in Figure 1.5, the green curve corresponding to the sampling block and the blue line corresponding to a second-order filter with 1% ripple at the output. When multicell conversion is considered, the improved waveforms allow increasing the cutoff frequency of the filter, and as can be seen in the same figure, the influence of the sampling block rapidly becomes a the main limiting factor.



**Figure 1.5.** Factors limiting the dynamic performance. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

## 1.4. Conclusion

Multicell conversion has inherent advantages that makes it an increasingly attractive solution which can be considered

for any application. It provides more degrees of freedom to the designer, but it also makes design more complicated since many options can be considered. For this reason, it seems important to develop an approach that allows fast evaluation of several solutions with different numbers of series and parallel cells, the particular case of 1 cell in series and 1 cell in parallel corresponding to the case of standard two-level conversion. Exploring these degrees of freedom is the aim of this book and the models that are presented in it.



---

## Topologies of Multilevel DC/DC Converters

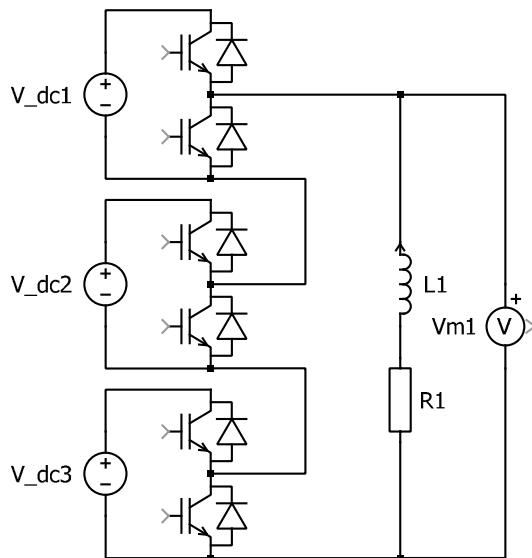
---

### 2.1. Series connection

#### 2.1.1. *Direct series connection with isolated sources*

When isolated sources are available, it is relatively easy to build multilevel voltage waveforms by series-connecting standard two-level commutation cells as shown in Figure 2.1. Inherently, this topology has few restrictions: the voltage sources can have different values, the power flowing in these sources can be equal or different, the duty cycles and even the switching frequencies can be different, and we can even generalize the concept with full bridges or connect some of the modules in the other direction to include negative voltages in the sum, etc. In some cases, these different configurations may not be of academic nature but also be justified by the application; for example, some modules with a high voltage (HV) may use semiconductors with an HV rating switching at a low frequency and deliver some active power, while others would be connected to lower voltage sources, use semiconductors with a lower voltage rating and switch at a higher frequency to act as active filters. In this book, we want to focus on direct current/direct current (DC/DC) converters; therefore, we will not investigate all the

cases here, but this is an opportunity to point out a limitation that is often encountered in DC/DC converters and explains that there are much less multilevel topologies for DC/DC applications than for DC/alternate current (AC) applications. If the current is always positive, any module in Figure 2.1 delivers active power (except for the trivial case where the duty cycle is always zero), which means that none of the voltage sources can be a simple capacitor and separate voltage sources are needed.



**Figure 2.1.** Series connection of choppers with isolated sources

So, the question is: in practice, when can this scheme be used? In what kind of application are such sources available and allow the use of this configuration? There are basically two cases:

- independent isolated DC voltage sources are available, their voltages are approximately equal and the power flowing in these sources should be similar/balanced. This can be the case of DC storage devices such as ultracapacitors or

batteries of low voltages that need to be series connected to generate the appropriate voltage, but it can also be panels or any other LV DC generator such as fuel cell;

– a single primary source is used to generate a group of isolated sources to make using this schematic possible and generate HV waveforms. The price to pay is high because the isolation stage involves a significant cost, especially because in addition to the DC voltages applied between the primary side and the secondary side, there are very high dV/dts that require a careful design; the complexity of such solutions limits its use to demanding applications such as HV generators.

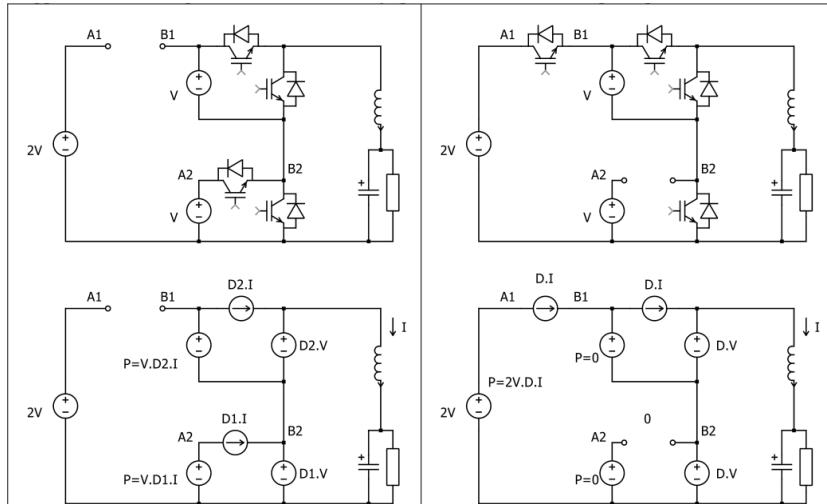
In both cases, the module voltages and powers are more or less equal so that all modules can use the same design and the same switching frequency; they will use almost the same duty cycles, and their control signals can be interleaved to produce balanced multilevel voltage waveforms at the output.

### 2.1.2. Flying capacitor

Figure 2.2 (top-left) represents the series connection of two choppers fed by two isolated voltage sources, each one with an amplitude  $V$ ; a voltage source of amplitude 2 V has been added on the left only for the purpose of the explanation that follows and can first be disregarded. Using the average model of the commutation cell (Figure 2.2 bottom-left), the power taken from each voltage source can be expressed as functions of  $D_1$  and  $D_2$ , the duty cycles of the two commutation cells; it can be seen that the two powers can be made equal by taking  $D_1 = D_2$ . Of course, the extra voltage source with amplitude 2 V, which is not really connected to the circuit, has a power equal to 0. It can also be seen that in this circuit the voltage between points  $B_1$  and  $B_2$  is directly imposed by the upper voltage source and that

the voltage between points  $A_1$  and  $A_2$  is imposed as the difference of two voltage sources so that we have:

$$\begin{cases} v_{A_1} - v_{A_2} = 2V - V = V \\ v_{B_1} - v_{B_2} = V \end{cases} \quad [2.1]$$



**Figure 2.2.** From series-connected choppers  
to the flying capacitor chopper

By subtracting the two equations of the system in [2.2], we get:

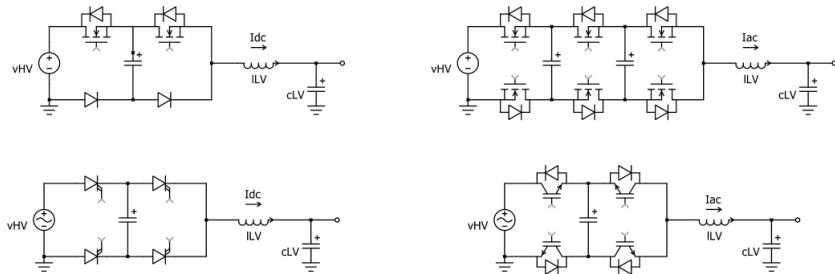
$$v_{A_1} - v_{B_1} = v_{A_2} - v_{B_2} \quad [2.2]$$

This may suggest studying a variant of this circuit with a switch connected between  $A_1$  and  $B_1$  instead of between  $A_2$  and  $B_2$  and controlled in the same way. This is done in the right part of Figure 2.2. Considering the previous comments, the voltages in all points of the circuit should not be modified, but the currents, and consequently the powers, are modified. The bottom source with amplitude  $V$  is now

disconnected, so its power is 0, and the average model shows that the power in the top source with amplitude  $V$  is also 0 if the duty cycles are equal because the current in this source is the difference of the average currents in two switches. The power delivered to the load is now fully taken from the voltage source with amplitude 2 V; the bottom source with amplitude  $V$  may be totally suppressed and the top source with zero average power can be made a simple capacitor.

This modified circuit is the first example of a quite general family of converters; the principle can be generalized to different types of applications. It is compatible with DC current, and in this case half of the semiconductors can be simple diodes (Figure 2.3 top-left, [MEY 92]). It can be generalized to any number of cells as shown in Figure 2.3 (top-right) showing the example of a voltage source inverter, but of course all the examples in this figure can be extended to higher numbers of cells [MEY 93]. It can also be used for series connection of reverse blocking devices in current source inverters (Figure 2.3 top-right and [MEY 91]) or cycloconverters (not shown here, but described in [MEY 91]), or to facilitate four-quadrant conversion with three-segment semiconductors in an AC chopper configuration (Figure 2.3 top-right and [LEF 01a, LEF 01b]). In these last two cases, the voltage of the main voltage source being an AC source, the voltage across the flying capacitors should also be AC voltages, which is more difficult to achieve because the dynamic of the natural or active balance must be high enough to follow the variations of the main source. This is difficult to achieve in the case of medium voltage and high power because the switching frequency is too low to allow following a typical 50/60 Hz variation. However, in LV applications, the switching frequency is typically high enough to facilitate such an operation.

Various aspects of the work done on these converters in Toulouse are presented in [MEY 02a, MEY 02b, GAT 02, TUR 02] and [BEN 02].



**Figure 2.3.** Flying capacitor converters for different applications

## 2.2. Parallel connection

### 2.2.1. Interleaved choppers with star-connected inductors

Duality is a powerful concept that makes possible exchanging the role of voltage and current (thus keeping power constant), and there are simple rules to systematically derive the dual topology of (almost) any circuit by using correspondence between loops and nodes, turning inductors into capacitors, converting resistances into conductances, etc. Therefore, if a circuit has certain merits, it is always interesting to study its dual because this dual will have many properties in common. The concept is theoretically quasi-perfect and allows us to derive complex properties of new circuit by writing the dual of the property of the original circuit that has been studied intensively. There are two main limits of this concept:

- technology limits are not maintained when applying duality; for example, the dual of the series resistance of a copper cable (losses induced by current) would be the conductance of the isolator between two points of the dual

circuit (losses induced by voltage), but in practice conduction losses in conductors are significant, while in most application leakage currents in isolators are negligible;

– not all circuits have a dual. From a topology point of view, power electronic circuits are mainly composed of dipoles, i.e. components connected between two nodes of a circuit, and two nodes only; however, a dipole can belong to more than two loops. In the dual circuit, the dual component must be connected to two nodes and two nodes only, these nodes representing the dual of the loops of the initial circuit. Therefore, an initial circuit with components belonging to more than two loops cannot have a dual. So, a necessary condition for a circuit to have a dual is that all components belong to only two loops. It can be shown that this condition is sufficient and that it is equivalent to saying that the circuit can be drawn on a sphere without any cable crossing.

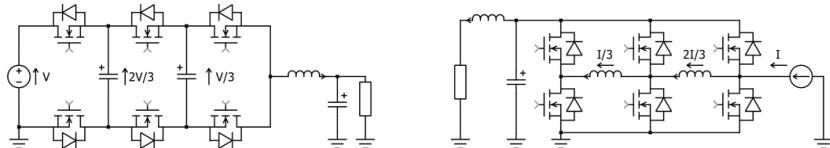
As an example, the dual of a three-cell flying capacitor buck converter is presented in Figure 2.4. It is a three-cell boost converter with three cells acting in parallel and all its properties, simple or complex, can be derived from those of the initial circuit:

– when a switch of the initial circuit is conducting (if the switch was ideal, it would impose  $v = 0$ ), its dual in the dual circuit should be blocking (if the switch was ideal, it would impose  $I = 0$ );

– interleaved control cancels *voltage* harmonics on the LV side of the *initial* circuit, so that interleaved control cancels *current* harmonics on the HV side of the *dual* circuit;

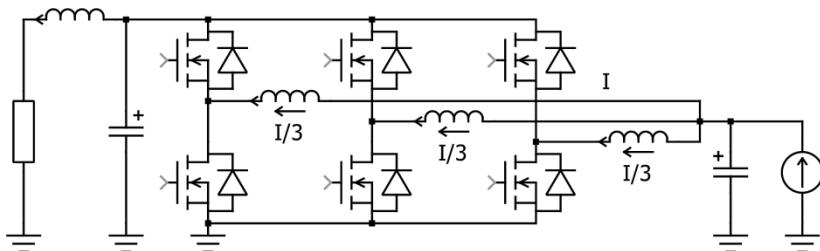
– having demonstrated that “a *non-infinite* impedance of the *current* source/LV side of the *series* three-cell converter guarantees natural balance and that a *series*-LC network tuned at the switching frequency and connected in *parallel* with the *current* source will act as a *voltage* balance booster”,

it can be directly derived that “a *non-zero* impedance of the *voltage* source/HV side guarantees balance and that a *parallel-LC* network tuned at the switching frequency and connected in *series* with the *voltage* source will act as a *current* balance booster”.



**Figure 2.4.** Flying capacitor converter and its dual

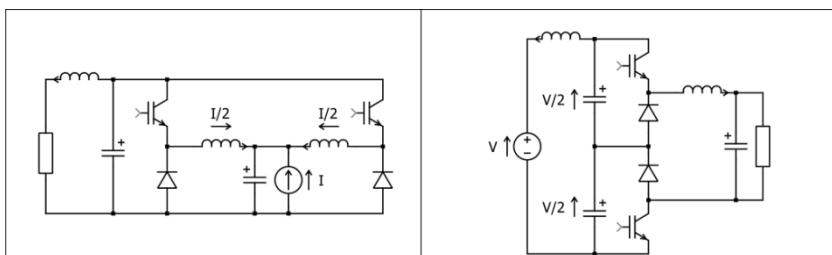
However, this circuit has the disadvantage of using inductances with different values (and inductors with different sizes), and it is less preferable than a circuit using equal inductances (Figure 2.5). Most of the properties are unchanged, including the interesting natural balance induced by non-zero impedance of the HV-side filter at the switching frequency.



**Figure 2.5.** Parallel multicell converter with star-connected inductors

It should be noted that this converter cannot be drawn on a sphere without cable crossing; so it generally has no dual, except for the case of two cells. This special case is illustrated in Figure 2.6; with two cells only, the drawing can

be modified to avoid cable crossing, and the dual circuit is then obtained by applying standard duality rules. This dual circuit is a very interesting configuration. It has only two disadvantages: the load is fully floating which is often a severe limitation and it cannot be generalized to series connect more than two cells.



**Figure 2.6.** Two-cell parallel multicell converter (left) and its dual (right)

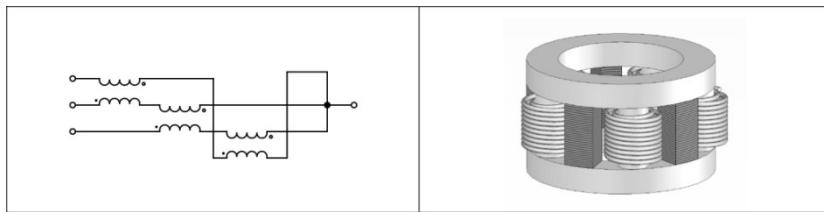
Interleaved converters with star-connected inductors have an important advantage in that they allow reducing the RMS current in the capacitor of the HV-side filter (property inherited by duality), and the RMS current in the LV-side capacitor and its voltage ripple (new property resulting from the topological modification). This property permits using lower values of the smoothing inductances, the high ripple in each inductor being divided by the number of cells after us the point of common connection.

### 2.2.2. Interleaved choppers with InterCell Transformers (ICTs)

The reduction of the value of the inductances allowed by interleaving and star-connection of uncoupled inductances is, however, realistic for a low number of cells only. Beyond three or four cells, the phase current ripple generally becomes the limiting factor and the inductance value cannot

be reduced. However, it is possible to overcome this limitation by using magnetically coupled components; if all currents are coupled, the relative phase current ripple (phase current ripple divided by the phase DC current) is equal to the relative full current ripple making configurations with higher numbers of cell more practical.

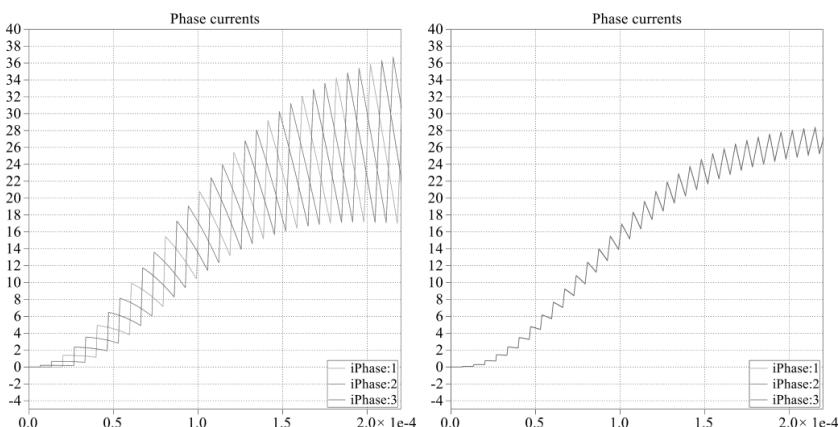
There are two typical ways to couple the  $n_P$  phases of a parallel multicell converter. In the cyclic cascade configuration, two-winding transformers are used to couple cyclically each phase with the next one (Figure 2.7 left); all currents are coupled together, but this is indirectly obtained by the series connection of transformer windings so that equal currents are in this case imposed by the electrical circuit. In the ideal monolithic configuration (Figure 2.7 right), all windings are magnetically coupled and currents are all imposed to be equal by imposing the same difference of magnetic potential across each winding.



**Figure 2.7.** *InterCell Transformers. Left: cyclic cascade configuration and right: monolithic configuration*

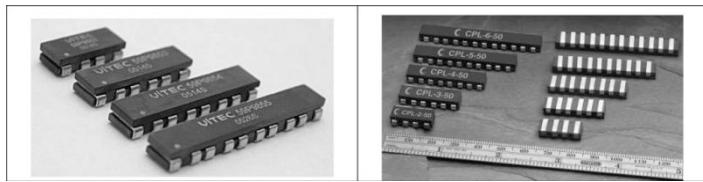
Examples of waveforms of the phase currents obtained with uncoupled and coupled magnetics are given in Figure 2.8. In the case of uncoupled inductors (left), the amplitude of the phase current ripple is very high and will potentially give a lot of importance to frequency effects in the windings; in the case of coupled windings (right), the

amplitude is substantially reduced and the currents in the windings should be more evenly distributed. Of course, if the number of cells increases, the difference between the two cases increases and the uncoupled inductors will need to be designed to limit not only the total current ripple but also the phase current ripple.



**Figure 2.8.** Phase currents in uncoupled (left) and coupled (right) three-cell parallel multicell converter

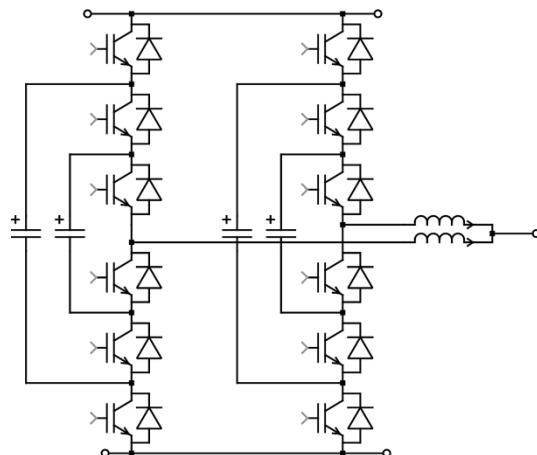
One of the advantages of using such magnetically coupled parallel multicell converters is that the total inductance can be very low because it is basically divided by  $n^2$  compared to a two-level converter. For this reason, these converters are already quite widely used to supply processors that may demand as much as 100 or 200 A with a voltage close to 1 V and behave as extremely dynamic loads; when a calculation terminates, the power consumption can collapse in a few clock cycles. Such requirements, generally described in the literature under the name of voltage regulator modules (VRM), are almost impossible to reach with standard two-level converters and give rise to the development of dedicated magnetic components.



**Figure 2.9.** *InterCell Transformers for voltage regulator modules  
(left: Vitec and right: Coiltronics)*

### 2.3. Series-parallel connection

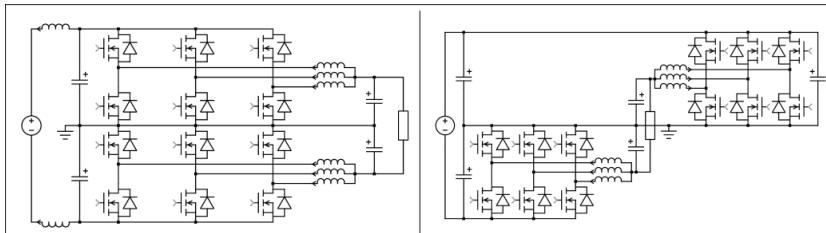
The series and parallel multicell concepts can be combined to generate series-parallel multicell converters. An example showing the parallelization of two three-cell series multicell converters is shown in Figure 2.10. The magnetic components on the LV side can be uncoupled inductors or they can be coupled with cyclic-cascade or monolithic ICTs. The number of series and parallel cells can also be modified, and this gives a lot of design options. This schematic will be used throughout the rest of the book to illustrate how vectorization and design masks at all levels allow to explore these degrees of freedom.



**Figure 2.10.** *An example of series-parallel multicell converter. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)*

There are other ways to combine series and parallel multicell commutation cells. The specific two-cell series topology mentioned earlier (Figure 2.6) can be used for connecting two parallel multicell commutation cells in series (Figure 2.10 left). The  $n_P$  windings of each parallel multicell commutation cell can be magnetically coupled, but top and bottom windings can also be magnetically coupled to obtain currents at  $2.n_P$  times the switching frequency in each winding. Such a topology with  $2 \times 4$  cells is described in [FOR 14] for a 137 kW chopper.

Another way to use two parallel multicell commutation cells is shown in Figure 2.11 (right). In this configuration, the voltage applied to each of the two parallel multicell commutation cells is different from both the input and output voltages, and it varies with the point of operation. This configuration is interesting when a high conversion ratio is needed. Here again the windings can be coupled, within each group or altogether. An example of such a converter is presented in [VID 13].



**Figure 2.11.** Some other series-parallel multicell converters

The configurations in Figure 2.11 can also be generalized to different numbers of cells in parallel and may use different magnetic configurations. Dedicated models with resizing capabilities can also be developed for these topologies, but in the remaining of this book, we will concentrate on the configuration shown in Figure 2.10.



---

## Concept of Vectorization in PLECS

---

### 3.1. Vectorized components

In PLECS, most components can be vectorized, which means that one symbol (component or subsystem) can be interpreted as several components. This feature is interesting to avoid drawing a part of a circuit several times and it allows to describe a big system within a smaller schematic. However, we will show that this functionality can be used more extensively to allow resizing of the system by simply changing the length of a vector or even a value in a parameter mask. This possibility of reconfiguration is a major advantage when studying multilevel converters and looking for the optimal number of cells for a given application.

However the condensed form of such drawings can also make them difficult to understand and design; a short training phase can be required, and specific blocks performing basic vectorizing functions can also help.

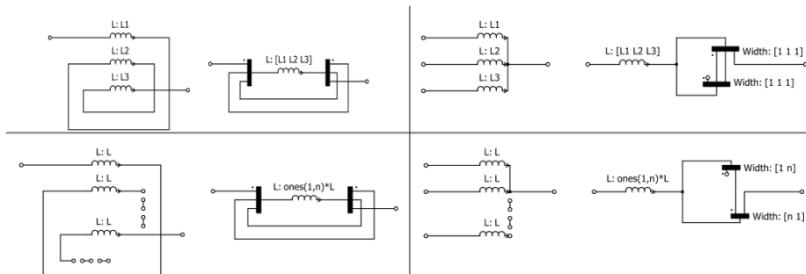
The simplest example of vectorization is shown in Figure 3.1. In this case the inductance on the right is configured as a vector of three values, which indicates that the symbol must be interpreted as the three inductors shown on the left. A second way to vectorize a component is to

connect it to a vectorized component: if a resistor with a value  $R$  was connected to the inductor on the right, it would be interpreted as three resistors connected in series with the three inductors. Of course, when connecting several components with vectorized values, they must all be of the same size.



**Figure 3.1.** Vectorized components; a) the real system, b) its vectorized representation

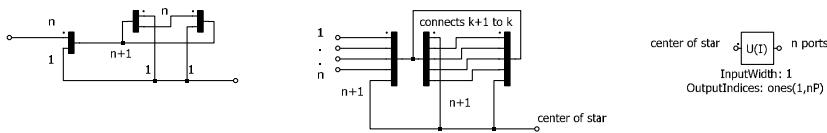
In general, vectorized components need to be connected to scalar components in some parts of the circuit. Wire multiplexers are very useful to perform this task and change locally, the size of connected systems. In Figure 3.2, examples of series connection and parallel connection of devices are shown. As can be seen, the size of the wire multiplexer can be defined by a fixed integer, a variable integer, or a vector of fixed or variable integers and applying these options is at the heart of these configurations.



**Figure 3.2.** Basic connexion of vectorized components  
left: series connection; right: star connection; top: for  
3 devices; bottom: resizable version

### 3.2. Star-connection block and parallel multicell converter

The principle of star-connecting vectorized inductors in Figure 3.2 can be used to star-connect full parts of a conversion system, and this can be turned into a versatile and reusable subsystem. Such an example is given in Figure 3.3 left and center. The same principles can be applied to generate a star-connection block that will be convenient for connecting parallel blocks to a single wire. Here again, the block must be designed in such a way that no vector of size negative or null is created in the wire multiplexer even when  $n = 1$ . Another way to obtain this function is to use a wire selector with parameters defined as shown in Figure 3.3 right.

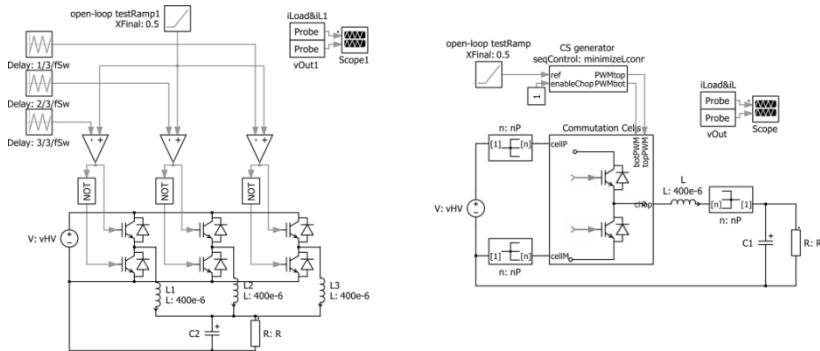


**Figure 3.3.** Resizable star connexion block

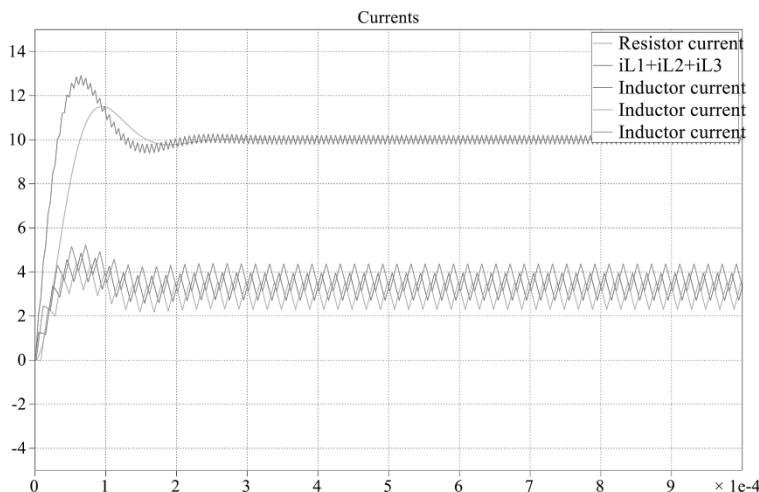
For example, an interleaved buck converter such as the one in Figure 3.4(a) can be drawn in a more compact form using the star-connection blocks and a vectorized control signal generator or modulator that will be described later. Such an implementation is shown in Figure 3.4(b). The number of cells is set to three in the “initialization” part of the “simulation parameters” menu to obtain the same waveforms as those of the left circuit, but this value can be directly changed to obtain waveforms corresponding to a different number of interleaved phases.

The corresponding current waveforms are displayed in Figure 3.5. It can be seen that the current ripple in the three inductors is phase-shifted, which produces a sum with a much smaller ripple and three times the average value of

each inductor current. It should also be noted that although this simulation starts from a balanced state (all currents are zero), the three currents do not reach the same average value. This will be explained and addressed in section 4.2 in which a specialized modulator is described.



**Figure 3.4.** Interleaved converter a) three-phase,  
b) corresponding resizable version

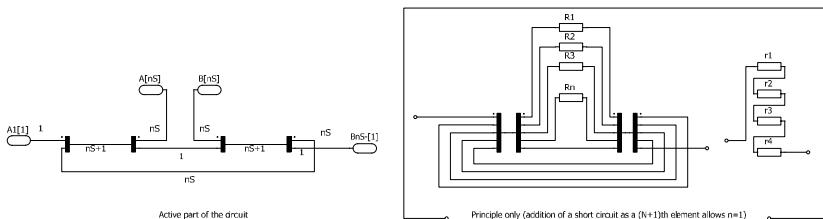


**Figure 3.5.** Current waveforms of a three-phase interleaved converter. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

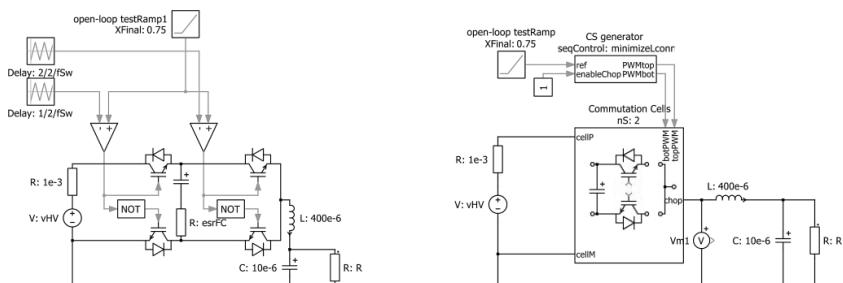
### 3.3. Series connection block and series multicell converter

The same principles of vectorization can be applied to generate a series-connection block that will be convenient to build series-multicell converters. This block must be designed in such a way that no vector of zero or negative length is created in the wire multiplexer, even when  $n = 1$ . Such a block is shown in Figure 3.6.

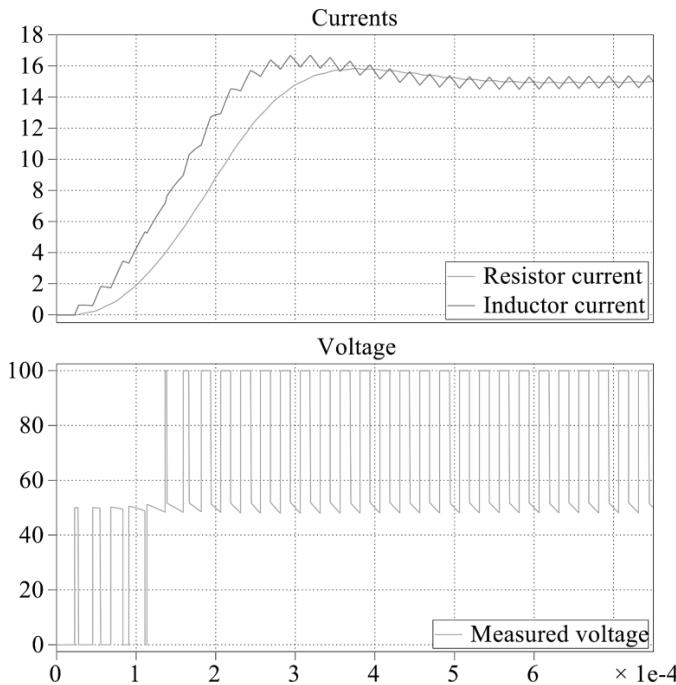
This block can be used to build a resizable “flying capacitor” series multicell converter, an example of which is given in Figure 3.7. The number of cells in series  $ns$  can be defined in the initialization menu; and when it is set to 2, the two circuits give the same waveforms (Figure 3.8).



**Figure 3.6.** Resizable series connection block



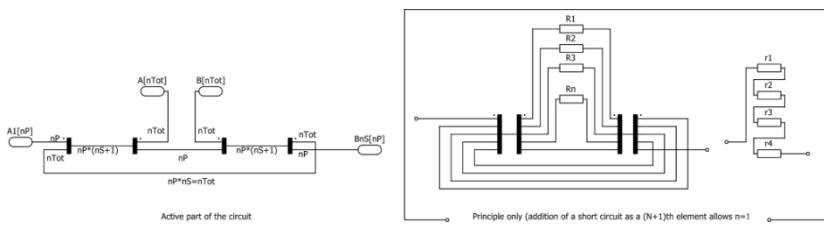
**Figure 3.7.** “Flying capacitor” series multicell converter  
a) 2-cell, b) corresponding resizable version



**Figure 3.8.** Waveforms of a two-cell flying capacitor converter. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

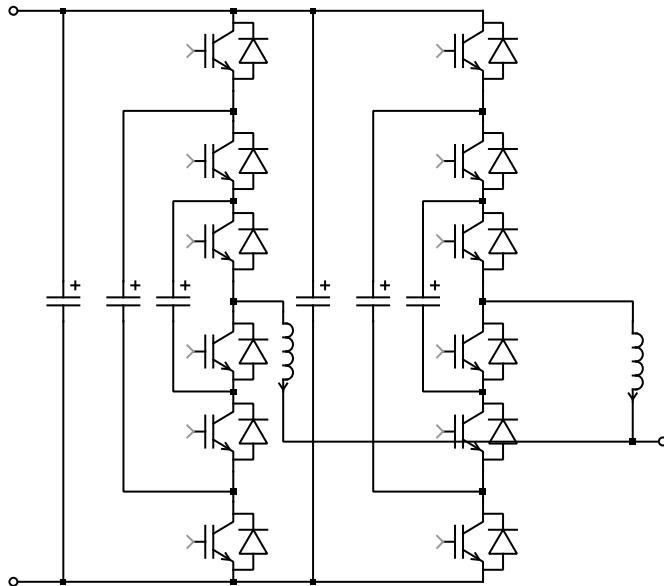
### 3.4. Generalized multicell commutation cell

To make the series-connection block really useful, it should be able to series-connect subgroups of cells, and to allow these subgroups to be parallelized to create a generalized series-parallel commutation cell. The principle of the more general series-connection block is the same as the previous one, but the size of the vectors must be adapted (Figure 3.9). The block now has two input parameters which are  $n_P$  and  $n_S$ ; it involves  $n_{tot} = n_P \cdot n_S$  components between terminals A and B, and gives access to the  $n_P$  A-nodes of the first element of each line, and to the  $n_P$  B-nodes of the last element of each line.



**Figure 3.9.** Resizable series connection block with parallelizing ability

With this generalized series connection block, we can build a macro-commutation block facilitating parallelization of series-multicell commutation cells such as the one in Figure 3.10 corresponding to the particular case of paralleling two three-cell flying capacitor legs.



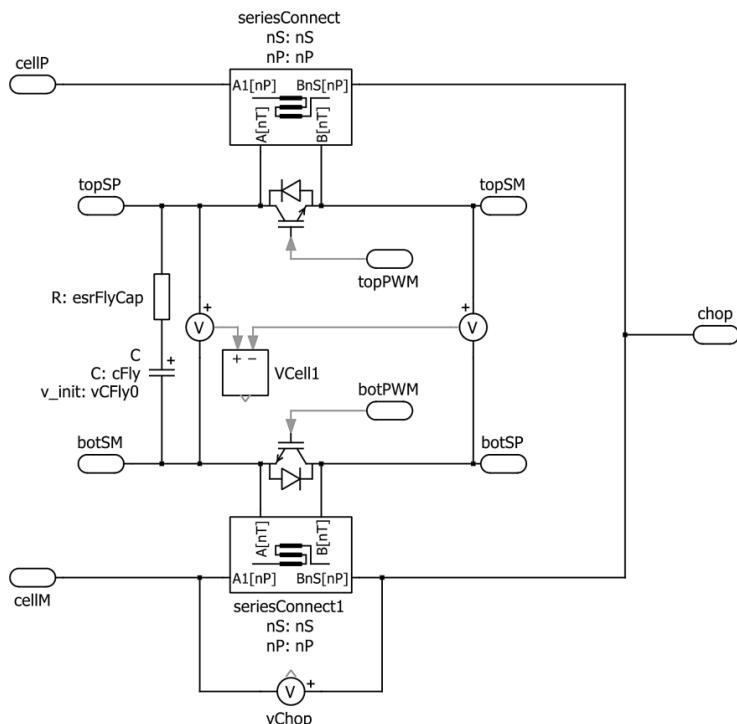
**Figure 3.10.** Combining series and multicell principles

The building block of a flying capacitor multicell converter (Figure 3.11) is composed of one capacitor and two switches

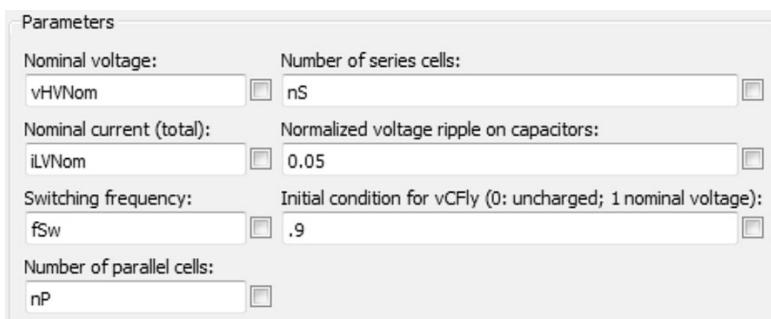
controlled with complementary signals. The top semiconductors of all cells are connected in series which is done using a first series connection block. The bottom semiconductors of all cells are connected in series using a second series-connection block. Terminals  $cellP$ ,  $cellN$  and  $chop$  are the three power terminals of this macrocell; terminals  $cellP$  and  $cellN$  are the HV side terminals and must be connected to the positive and negative terminals of a voltage source and terminal  $chop$  is the LV-side terminal and must be connected to a current-source. More generally, these terminals are the equivalents of the three terminals of a conventional commutation cell (in fact, they *are* these three terminal when  $ns = np = 1$ ) and can be used wherever standard commutation cells are used.

It should also be noted that cells are numbered from the HV side to the LV side. This is related to an asymmetry of the balancing mechanism: it has been shown [MEY 92] that the response to a DC bus variation will be faster if the cells are sequentially controlled from the HV side to the LV side, and not the other way around. In this presentation, we do not want to study this aspect, but we will adopt this sequence nonetheless by numbering from HV side to LV side.

When  $ns$  and  $np$  are changed, the value of the flying capacitors also need to be adapted to obtain meaningful results. This can be done automatically using the mask of the block (Figure 3.12) to derive the value of capacitors from general specifications ( $v_{HVnom}$ ,  $i_{LVnom}$ ) converter characteristics ( $f_{sw}$ ,  $ns$ ,  $np$ ) and voltage ripple requirement ( $v_{FlyNRip}$ ). The first parameters are transmitted from higher level blocks through the mask and the last parameter has a default value that can be modified by the user. An extra parameter is recommended to define a balanced or unbalanced initial condition of cell voltages to allow visualization of balancing mechanisms.



**Figure 3.11.** Resizable flying capacitor multicell commutation cell as a vectorized PLECS block



**Figure 3.12.** Mask of the resizable flying capacitor multicell commutation cell

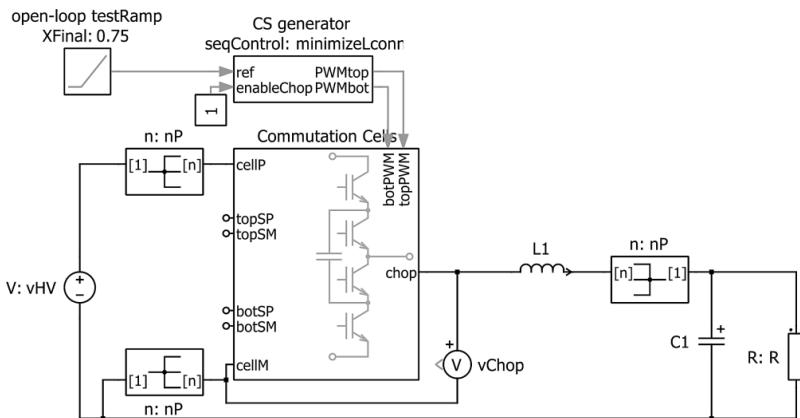
The code included in the mask initialization is as follows:

```
disp('== MacroCell Block =====')
disp('-- flying caps section -----')
vFlyNRip = .05 % pkpk norm. voltage ripple (% cell voltage) across Flying Caps
cFly = iLVNom/nP / (nS*fSw)/ (vFlyNRip*vHVNOM/nS)
esrFlyCap = 1e-3
% Initial conditions : Define initial conditions as a matrix
v0 = vHVNOM / nS * ones(nP,1) * (nS:-1:1);
% make it a line vector
for i = 1 : nS * nP
    vCFly0(i) = v0(i) ;
end
vCFly0 = kInitvCFly * vCFly0;
disp(strcat('vCFly0 = ',num2str(vCFly0)))
```

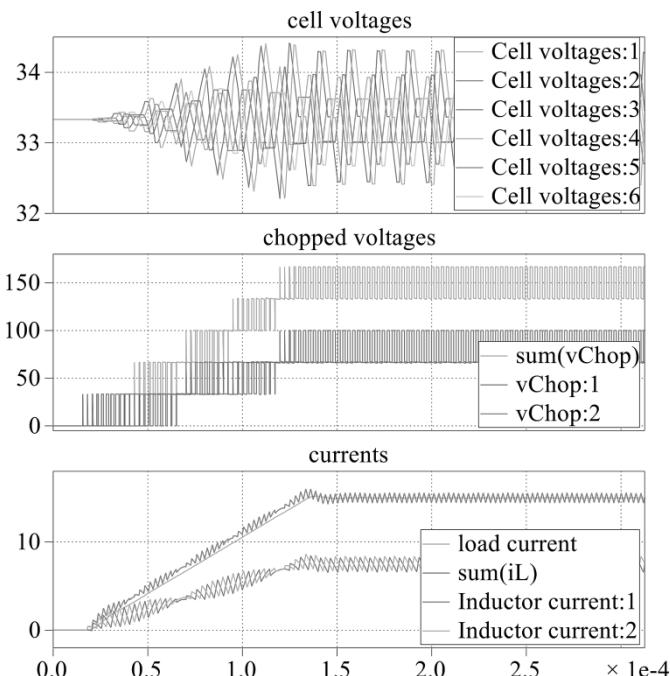
Using this block, a resizable series-parallel buck converter can be constructed (Figure 3.13). As can be seen from the figure, star-connection blocks are required on the HV side and between the inductor and the capacitor of the filter to connect to a single source and a single load.

The waveforms obtained for  $n_s = 3$  and  $n_p = 2$  are given in Figure 3.14.

Such a macrocell block is very interesting, however it is difficult to vary  $n_p$  and  $n_s$  and obtain meaningful simulation results because most of the parameters of the circuit must be adapted when the macro-commutation cell is resized. For this reason, some blocks with masks able to perform an automatic pre-design will be described in the following for the control loops, the filter and the magnetic components.



**Figure 3.13.** Paralleling vectorized series multicell commutation cells



**Figure 3.14.** Waveforms of a series-parallel multicell chopper. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

### 3.5. Practice

#### 3.5.1. How to?

For a better understanding, you should first answer the question, and *then* build the corresponding circuits to see implementation details and get the correct answers.

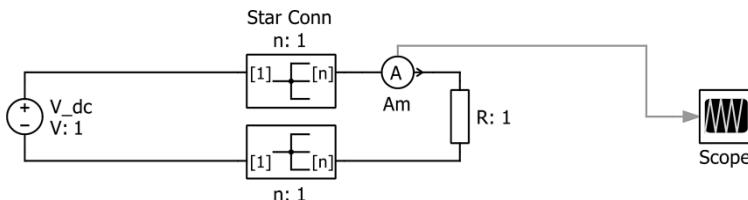
To build the circuits, you can copy/paste the blocks from the file *MacroCell Libray.plecs* but it is more convenient to access elements from the standard *Library* menu in PLECS:

- copy *MacroCell Libray.plecs* in a folder;
- in PLECS, go to *File / Plecs preferences / Libraries*;
- select the path to this folder in the *search path* section;
- point to *MacroCell Libray.plecs* in the *user libraries* section with for example *MacroCell Lib* as a description.

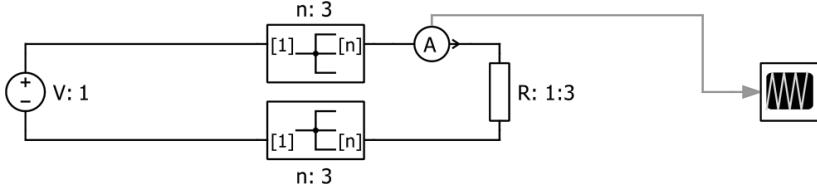
You should now see *MacroCell Lib* at the bottom of your components list in the *PLECS / LibraryBrowser* and access to these blocks by drag and drop.

#### 3.5.2. Basic blocks

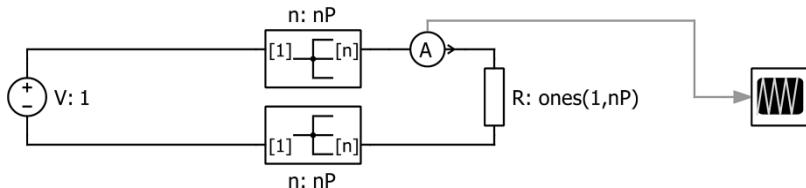
- 1) In the following circuit, how much current shall we visualize in the scope?



2) If the parameters of the star connection blocks and the value of the resistor are changed as shown here, what current shall we get in the scope.



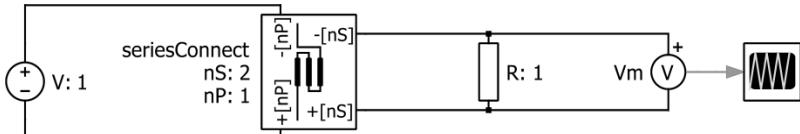
3) In the initialization mask (Ctrl+E, initialization) we define  $n_P = 3$  and modify the parameters of the star connection blocks and the resistance as follows. What currents do we get in the scope?



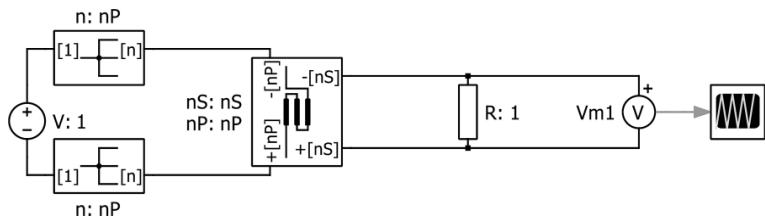
NOTE.— The current in the scope is now blue instead of green, right-click on the waveform and select “spread signals”.

4) How many modifications do we need to simulate 5 resistors of  $1\Omega$  connected in parallel to a 1 V source?

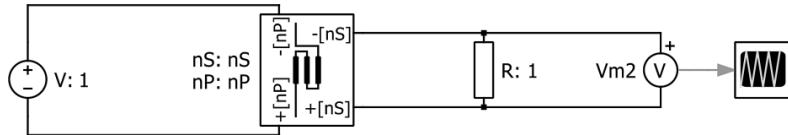
5) What is the following circuit? Which waveforms will we get?



6) What is this circuit, and where should  $n_S$  and  $n_P$  be defined?

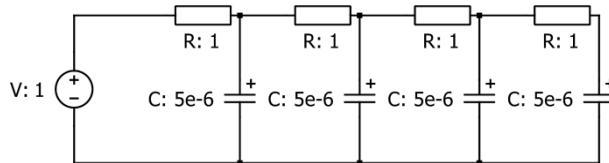


7) What is the difference with this circuit?

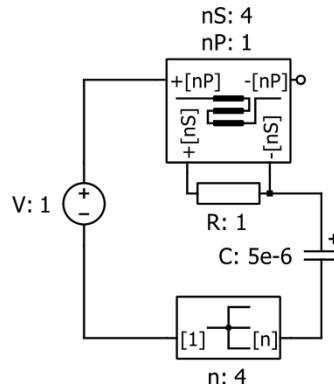


NOTE.— To get the right answer, not only the waveforms in the scope should be considered. For example, the current in the voltage source(s) should be observed.

8) How can the following circuit be vectorized with one star-connection and one series connection block?



Solution:



---

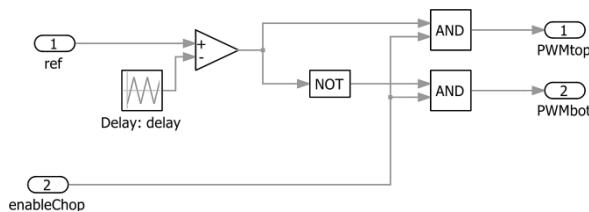
## Vectorized Modulator for Multilevel Choppers

---

### 4.1. General principle

The modulator is a good example to illustrate the power of the concept of vectorization. The diagram shown in Figure 4.1 is exactly the same as the one of a standard two-level converter. There is only a slight difference that cannot be seen in the figure: the parameter delay of the triangular source is, in fact, a vector that is defined in the mask as follows:

$$\text{delay} = \frac{(0 : n_{\text{cell}} - 1)}{n_{\text{cell}} \cdot f_{\text{sw}}} \quad [4.1]$$



**Figure 4.1.** Block diagram of modulator for multicell converter

This makes the whole block vectorized with a size  $n_{\text{cell}}$  that can be defined in the mask by the user or transferred

from a parent block. Of course, other functions, like dead time, for example, can be added if necessary without any special precaution.

## 4.2. xZOH: equalizing multisampler for multilevel choppers

### 4.2.1. *Control as the main source of perturbation*

The voltage and/or current distribution in multilevel choppers is imposed by internal state variables: flying capacitor voltages in series multilevel, inductor or ICT currents in parallel multilevel converters. These variables vary as the integral of the difference of control signals multiplied by:

- $i_{LV}$ , the LV-side current in series converters,
- $v_{HV}$ , the HV-side voltage in parallel converters.

In steady state, these quantities are constant so that maintaining the internal variables to their nominal values and imposing balanced constraints on the commutation cells is theoretically relatively trivial since it involves using equal duty cycles on all cells. However, this condition must be satisfied with a high accuracy since internal components act as quasi-pure integrators and, in practice, this requires a careful design of the modulator, the gate drivers and the switching device itself. Digital modulators, modern drivers and semiconductors match these requirements quite well, but in medium voltage applications, or when the switching frequency is very high, the error on the effective duty cycle can increase.

### 4.2.2. *Handling duty cycle variation*

#### 4.2.2.1. *An exact solution for unmodulated signals*

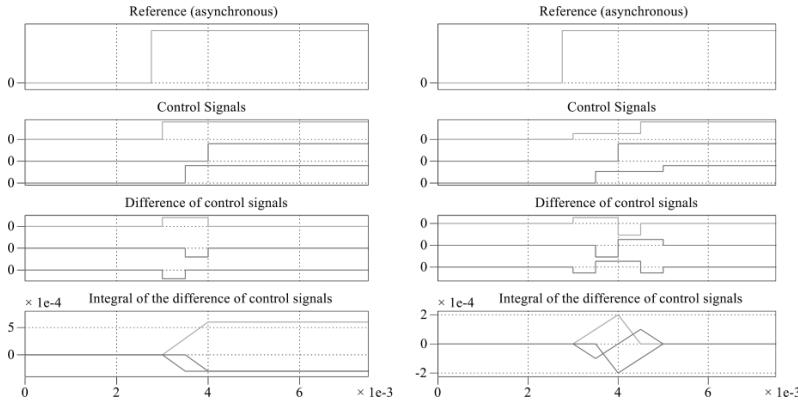
During transients, it is a little more difficult to “always impose equal duty cycles”. The duty cycle can be same for all

cells, but the transformation of this continuous-time reference into a square signal is inherently a discrete-time process. This is even more obvious when this reference is sampled; in this case, it is fundamental to take the sampled values into account at instants where the step cannot create extra switching or very short pulses. In interleaved converters, this means phase-shifted sampling of the common reference to address the different cells. However, this principle means that a step in the reference creates a difference in the integral of the control signals of the different cells, as shown in Figure 4.2 (left). The imbalance resulting from the step depends on the amplitude from the step, and how it impacts the different cells is related to which cell is affected first, i.e. when the step occurs within the switching period. In a real system, such steps will happen at each period, and although their amplitude will be generally very small, their effects will combine through the pure integral action to generate what seems to be an erratic behavior when observed over long time intervals.

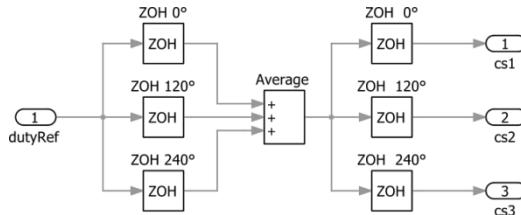
To solve this problem, the first cell that is affected must not apply the positive step at once otherwise the integral of its control signal will inevitably be higher than the others; the same applies to the second cell, and only the third can follow the step immediately. An example of the waveforms to be generated is given in Figure 4.2 (right). The timing of second possible transitions for cells 1 and 2 is imposed by the sampling clocks so that a simple set of equations can be found to determine the amplitudes of the first steps of cells 1 and 2.

However, there is a much simpler method for achieving these conditions that are “naturally” fulfilled by a simple circuit using basically two sampling blocks and a summer (Figure 4.3). The first sampling stage and the averaging block generate partial steps of appropriate amplitude at

appropriate times, and the second sampling distributes these steps to the different cells.



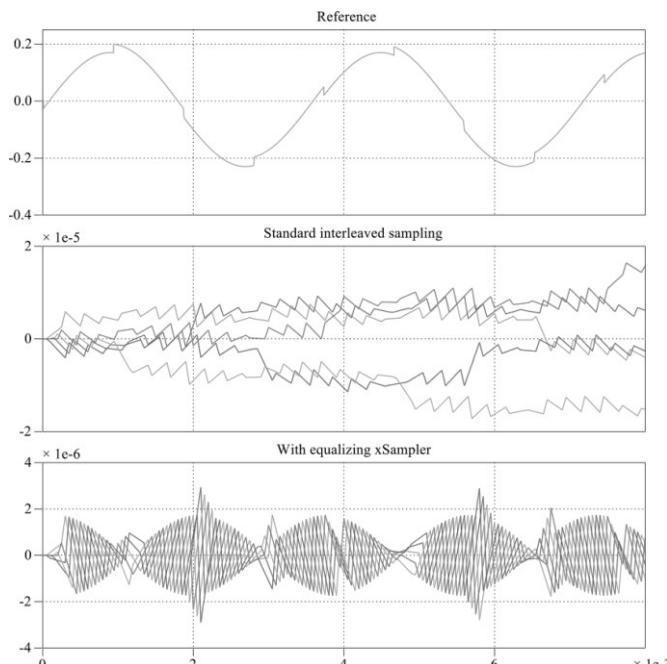
**Figure 4.2.** Influence of delayed sampling of the reference (continuous time). For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)



**Figure 4.3.** Balancing interleaved sampler

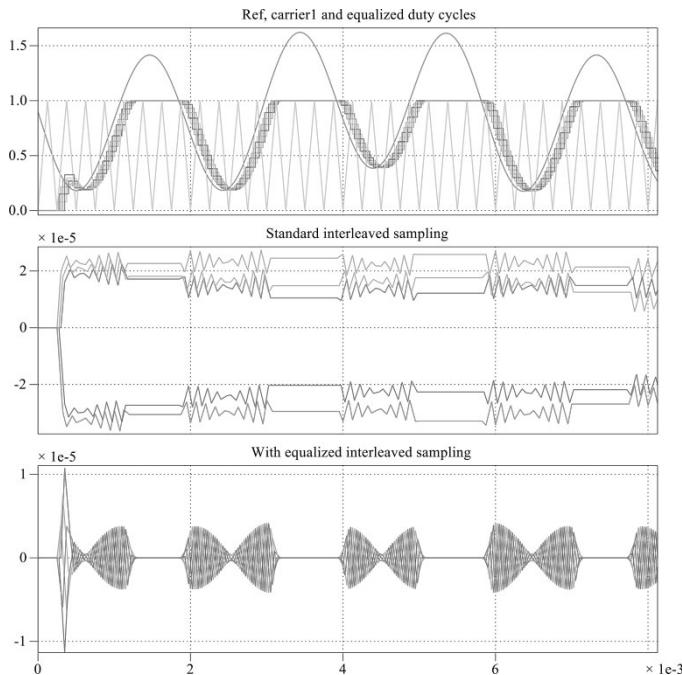
The advantage of this principle is that it can directly be generalized to any number of cells, and in PLECS, it can be vectorized and made resizable. An example with five cells is given in Figure 4.4. The reference signal includes a sinusoidal component that generates many small steps of continuously varying amplitude, and this does not significantly affect balance except for special conditions. But the reference also includes steps at a frequency that is not an integer divider of the switching frequency (which would make it worse by always applying the perturbation on the

same cell), to show how the reference steps affect balance. It can be seen that with a standard control, balance is severely affected on a very short time scale, while equalizing multisampler maintains the system perfectly balanced. Observations over longer time periods confirm this significant difference in behavior. A system with standard interleaving will therefore need extra balancing control loops to operate, and this can even be required at the simulation level if high dynamic conditions are studied. In real-world conditions, there will be slight imperfections of the system and, even with the equalizing multisampler, some imbalance can appear, but this will be a much slower process involving smaller amounts of energy and, as will be shown, certain imperfections of the system tend to rebalance the system. Therefore, open-loop operation is possible in practice.



**Figure 4.4.** Integral of differences in a five-cell system with standard or equalizing multisampler. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

It is also important to check that saturation of the reference does not cause any problems. As can be seen from Figure 4.5, this situation is also naturally handled using the equalizing principle.

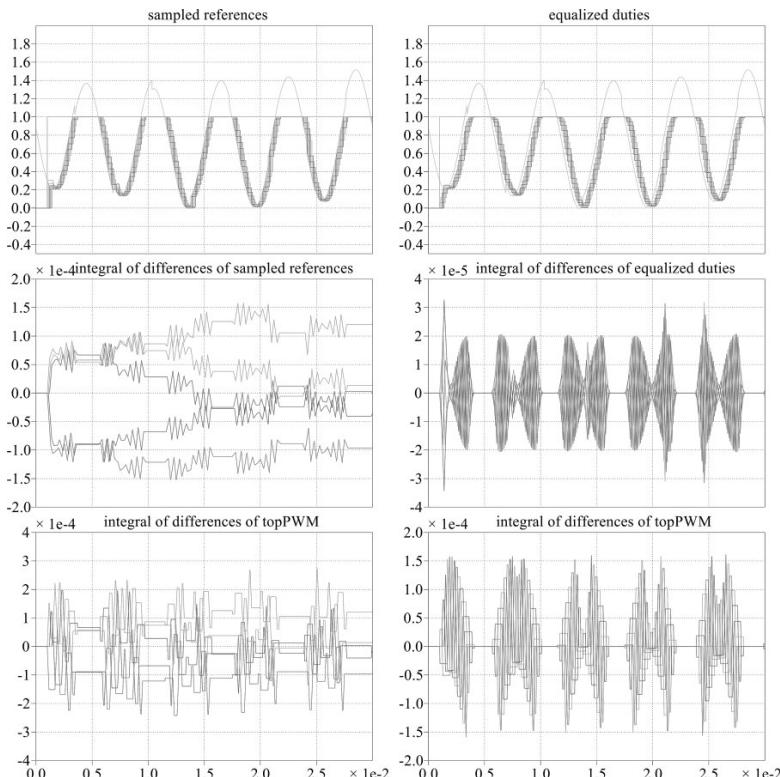


**Figure 4.5.** Integral of differences in a five-cell system in case of a saturated reference. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

#### 4.2.2.2. Accounting for switching

For simplicity reasons, the discussion and even the simulation results presented up to here have involved only the integral of the difference of cell references; the influence of the switching principle itself has not been addressed and we need to check the properties of the integral of the differences of chopped signals. Such verification is exemplified in Figure 4.6 in which the bottom curves are the

integral of the difference of chopped signals. These signals are therefore a direct representation of the voltage across the capacitors of a flying capacitor converter, or the circulation currents of an interleaved converter. Once again, these results show that the equalizing principle maintains the system rigorously balanced (right), while standard interleaving creates uncontrolled waveforms and possible drift over longer time intervals.

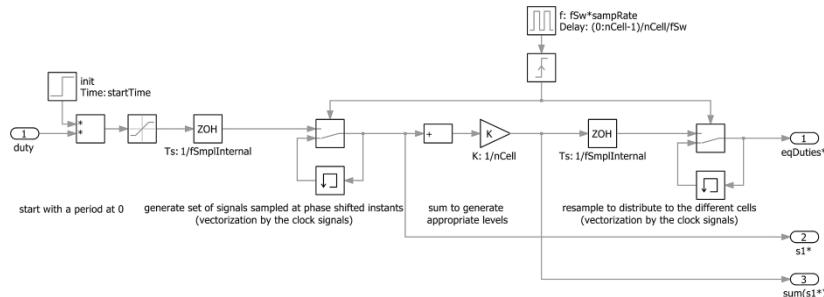


**Figure 4.6.** Equalizing multisampler with chopping and saturated reference. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

These principles can be implemented in a quite simple PLECS block, as shown in Figure 4.7. In this block, *duty* is a

one-dimensional (1D) input and a first vectorization is made by the sampling block on the far left; it is defined as a standard block but the clock provided by the top pulse generator is vectorized by defining its phase as a vector, and by inheritance, this makes the sampling vectorized as well. The averaging block takes the dimension back to 1 and the second sampling block restores the dimension to  $n_{Cell}$ . The output  $s_1^*$  corresponds to standard interleaved signals and is provided to allow easy comparison of these two options. The output  $\text{sum}(s_1^*)$  gives a signal that is an image of the ideal voltage that the multilevel converter should deliver on the LV side, and an image of the current it should impose on the HV side if it is a parallel converter.

It should be noted that this block needs an initialization value to start correctly since it utilizes memory blocks. The initial value of the duty cycle can be defined in the mask of the block. If this initial value is not known, it is also possible to allow an interval of one switching period before starting switching. This time interval is also defined in the mask. Using none of these options may result in unbalanced operation.



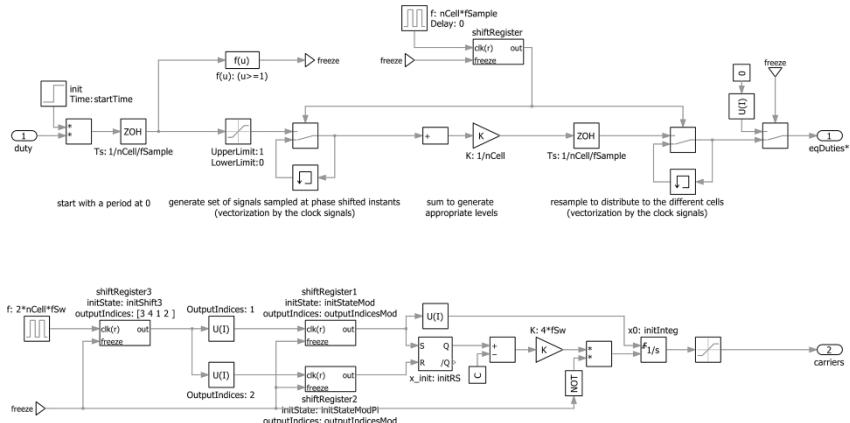
**Figure 4.7.** Vectorized equalizing sampler as a PLECS block

#### 4.2.2.3. Handling fast transients (at the sampling frequency)

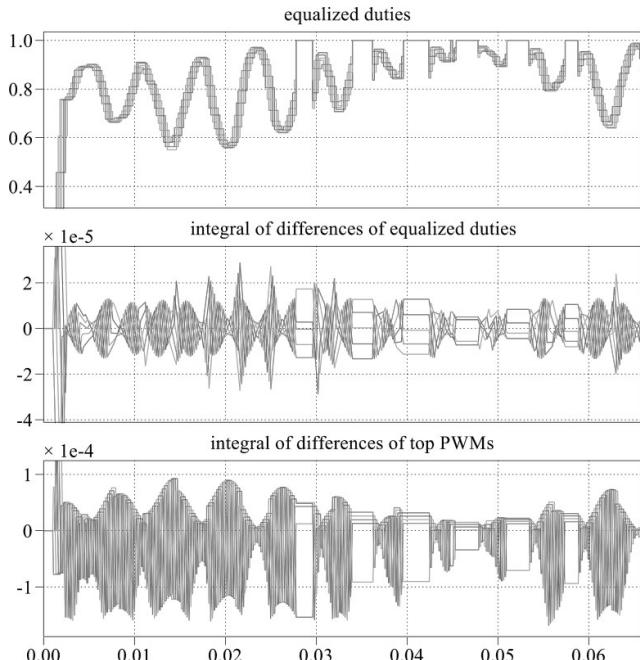
There is, however, one point that needs further development. A real system needs to be protected against

short circuit, voltage overshoot, etc. This is a serious issue especially when multilevel converters allow reducing the amount of energy stored in the filters which makes it more sensitive to outer perturbations. As a consequence, it may be needed to have a faster response in case of emergency, and we may want to saturate the duty cycles of all cells at the same time. This is not done by the previous block which will progressively saturate the different cells over one or two switching periods. It is not really a problem to allow the references of all cells to saturate at the same time. If this is done, the state of the system is “frozen” since all duty cycles are equal and the integrators have zeros as inputs, so no imbalance is created even if saturation lasts. In fact, when the system enters saturation, it is not necessarily balanced but the imbalance is memorized in the sampling blocks and it is ready to be used when getting out of saturation. However, if saturation lasts, the memory is progressively cleared and an imbalance will be generated when switching starts again. Therefore, to handle fast saturation, it is required that the sampling blocks be disabled during saturation.

However, it is not enough to just suppress the clock signals during saturation of the reference in order to avoid generating an imbalance when getting out of saturation. A certain state has been memorized when entering saturation, which corresponds to a normal state at a given time of the switching pattern and when switching again. The system must restart from this point of the switching pattern. Therefore, a daisy-chain clock generator is created and it is the clock of this generator that is disabled during saturation. As a consequence, if saturation has been detected at the clock signal of cell  $k$ , the first clock signal when switching again will be on cell  $k+1$ , independently of the duration of the saturation. The control signals of the different cells must also stay synchronized with reference samples. A freezable carrier generator must be included so that the modulator itself has been included in the same block.



**Figure 4.8.** Vectorized equalizing sampler with fast saturation handling as a PLECS block



**Figure 4.9.** Equalizing multisampler with emergency saturation handling. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

An example of results obtained with this block [TES 14] is given in Figure 4.9. With this control, the chopped voltage can be taken to full saturation within  $1/(n_{cell} \cdot f_{sw})$  if sampling at  $f_{sw}$  or  $1/(2n_{cell} \cdot f_{sw})$  if sampling at  $2f_{sw}$ .

The different parameters required to configure this block are defined in the mask as follows:

```

disp("-- Equalizing_xSampler -----")
if floor(nCell/2) == nCell/2
    parity = "even";
else
    parity = "odd";
end

% xZOH parameters
switch parity
case "even" % nCell even & sampRate=2 => synchronous sampling for
pairs of cells
    fSample = fSw ;
case "odd"
    fSample = sampRate * fSw ;
end

switch sampRate
case 1
    initState      = [ zeros( 1, nCell - 1 ) 1 ];
    outputIndices = [ nCell 1:nCell-1 ];
case 2
    initState = [zeros( 1, floor((nCell+1)/2)-1 ) 1 zeros( 1,floor((nCell+1)/2)-1 )
ones(1,( -1)^nCell + 1 ) / 2 ];
    outputIndices = [ floor((nCell+1)/2):nCell , 1: floor((nCell+1)/2)-1 ];
end

```

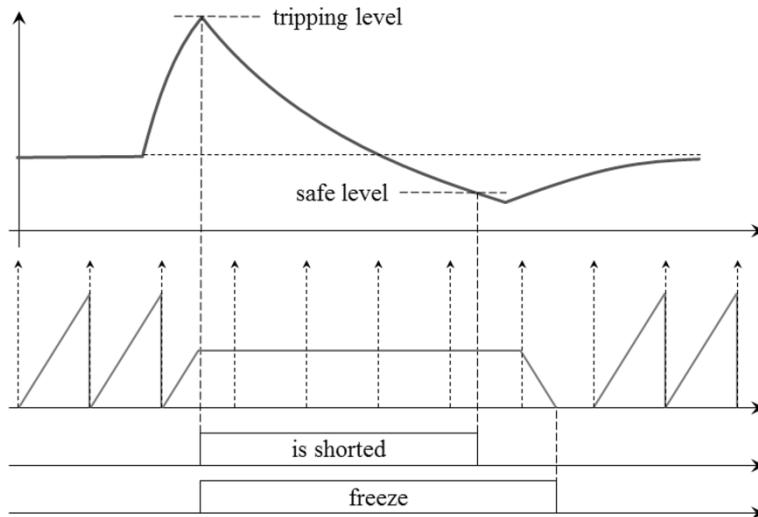
```
% Modulator parameters
outputIndicesMod = [ nCell 1:nCell-1 ];
initStateMod      = [ zeros( 1, nCell - 1 ) 1 ];
initStateModP1    = [ zeros( 1, floor((nCell-1)/2)) , 1 , zeros( 1, floor
(nCell/2) ) ];
initRS           = [ zeros( 1 , floor( (nCell+1) / 2 ) ) , ones( 1 , nCell -
floor( (nCell+1) / 2 ) ) ];
initInteg         = 1 - abs(1 - 2*(0:nCell-1) / nCell );

switch parity
case "even"
    initShift3      = [0 0 1 1] ;
case "odd"
    initShift3      = [0 1 1 0] ;
end
```

#### 4.2.2.4. Handling emergency transients (instantaneous and asynchronous)

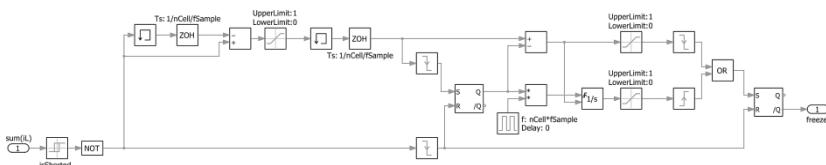
When short circuit is concerned, waiting for the next sampling time is not realistic. So, we describe here how equalized sampling can be adapted to handle asynchronous emergency and restart switching without creating any imbalances.

As soon as the tripping current threshold is exceeded, all top switches must be turned off; this can be done by an additional gate after the sampling stage that will generate an asynchronous event. To avoid generating imbalance when switching again, the fraction of control pattern that has been suppressed needs to be memorized so it can be applied after the current level has significantly decreased. In the example below, this is done after the current is taken to 0; it can be done earlier, for example when the current has become less than the current reference, but the risk of reaching the tripping current a second time would be higher.



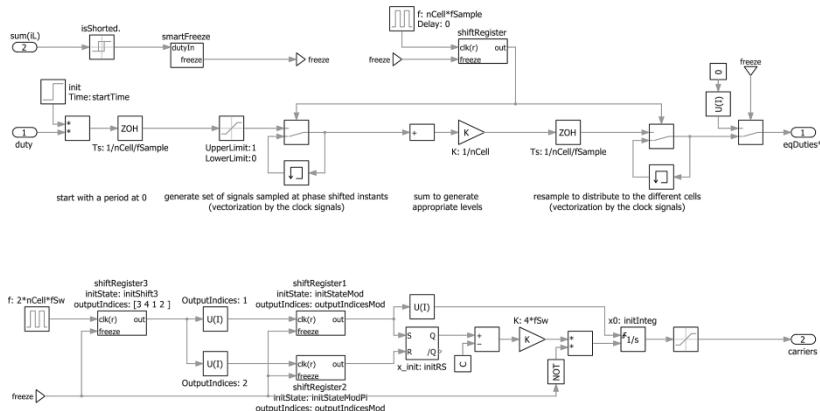
**Figure 4.10.** Asynchronous freezing and equalizing restarting

As can be seen in Figure 4.10, the idea is to use a resettable integrator that in normal operation integrates a permanent 1 and generates a saw-tooth signal synchronized with sampling. When tripping occurs, it is frozen (0 input and no more resetting pulses) so that the time interval between the last sampling time and tripping time is memorized in the form of a DC level. When entering the safe zone, a -1 is imposed at the input of the integrator, which will ramp down and reach 0 after the same time as the fraction of period already played. Triggering restart of switching at this time will therefore allow restarting without any imbalance.



**Figure 4.11.** Smart freeze circuit

The circuit used to generate such a *freeze* signal is shown in Figure 4.11. This signal will then be used to freeze both the equalizing multisampler and the daisy-chain block of the carrier generator (Figure 4.12). Finally, the circuit is not very different from the former one, except that the freezing signal is now an asynchronous signal based on the current measurement.



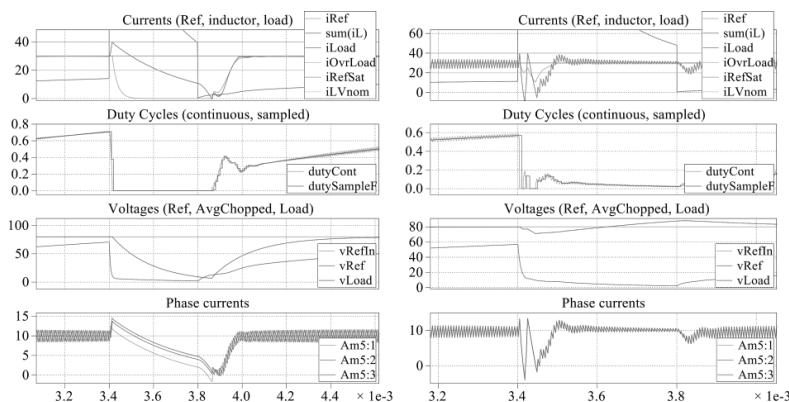
**Figure 4.12.** Vectorized equalizing sampler with emergency saturation handling as a PLECS block

An example of a result obtained with this control is given in Figure 4.13 (left) for a circuit using three cells in parallel and uncoupled inductors. It can be seen that the duty cycle is not taken to zero in a single step; however, the first decrease occurs before the tripping level is reached; this is just the reaction of the current loop. During the freezing phase, the currents are not balanced in the three phases, but when switching restarts the interleaved currents are perfectly balanced again. In Figure 4.13 (right), the same converter is used except that a monolithic ICT is used instead of the inductors. It is thus possible to use a much smaller total inductance. After the first trip, when the current returns to zero and switching restarts by

finishing the uncompleted period with the last non-zero duty cycle, the  $dI/dt$  is so high that it causes a second trip of the protection. Multiple trips have two main causes:

- except for the freezing principle, the variation of the duty cycle from one period to the other is limited so the duty cycle cannot go to zero fast enough;
- if only steady-state requirements are used to design the inductor, a very low value of inductance can be selected when the number of cells increases, especially when ICTs are used.

In some cases, more than two successive trips can be observed, which can be a severe limitation.

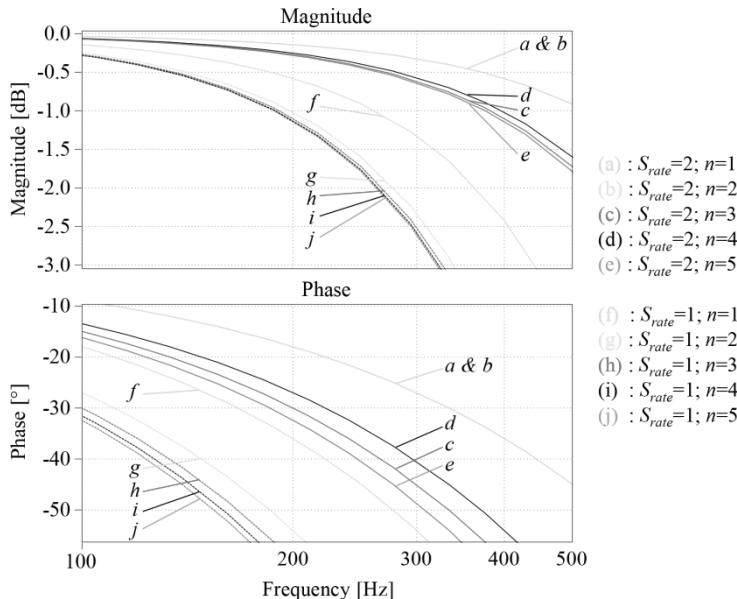


**Figure 4.13.** Example of short-circuit handling without any current imbalance. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

#### 4.2.3. Frequency response of the equalizing sampler and modulator

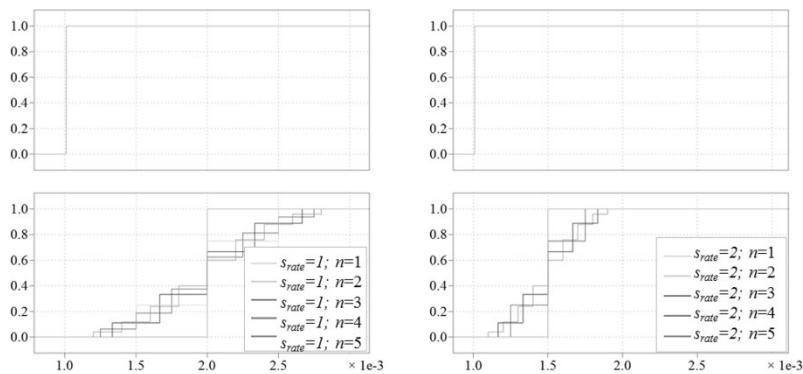
The equalizing multisampling block will be part of the most studied circuits and it has a major influence on the overall open-loop transfer function. Therefore, it is important to characterize the transfer function of these blocks to allow appropriate design of the regulators. These transfer

functions can be plotted using the AC sweep analysis and the results are given in Figure 4.14.



**Figure 4.14.** Transfer function of the equalizing multi-sampler for different parameters ( $f_{sw} = 1 \text{ kHz}$ ). For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

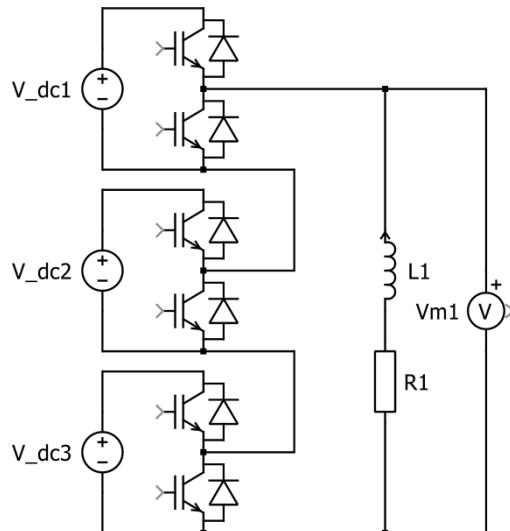
It can be seen that the most influential parameter is the sampling rate, not the number of cells. This is also illustrated in the time domain by the response to a step occurring just after the 1 ms sampling time in a commutation cell switching at 1 kHz. In particular, it can be seen that the “volt.second” product error is typically equal to  $V/f_{sw}$  for a sampling rate of 1 and  $V/f_{sw}/2$  for a sampling rate of 2. This consideration will be, for example, useful for choosing an inductor limiting the current overshoot in case of short circuit on LV side or in case of HV side voltage variation.



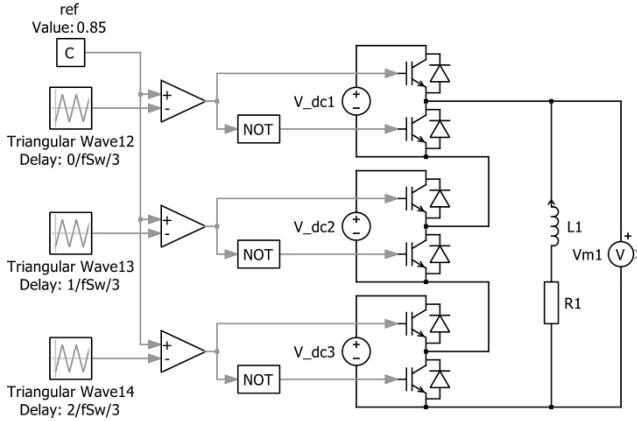
**Figure 4.15.** Step response of the equalizing multisampler for different cell numbers and sampling rate (step just after the 1 ms sample,  $f_{sw} = 1 \text{ kHz}$ ). For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

### 4.3. Practice

- 1) Build a vectorized version of this circuit using a series connection block:

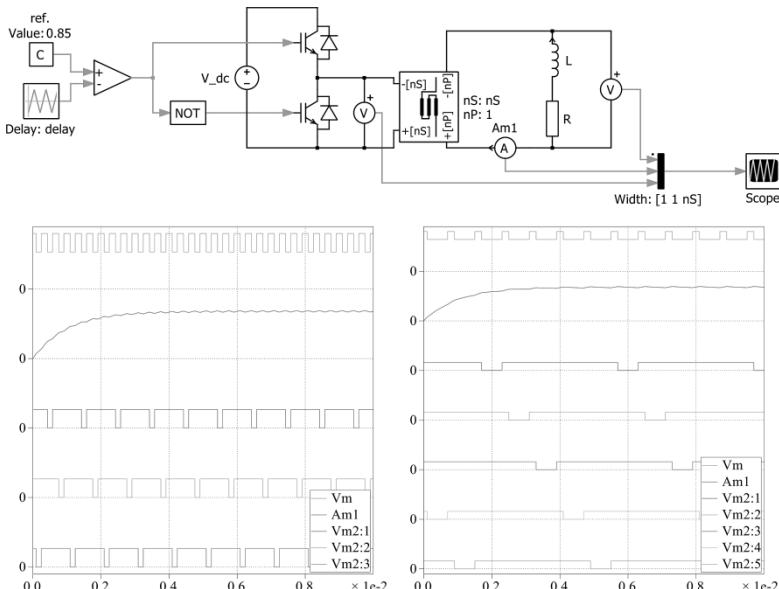


2) Vectorize the control section to match this schematic:



3) Change the number of cells of both the control and the power circuit by a single action and check the different waveforms.

Solution:



The parameters are defined in the *Simulation Parameters* menu as follows:

```
fSw      = 1e3  
nS       = 5  
delay   = (0:nS-1)*1/fSw/nS
```

N.B.: See in the figure the correct syntax to define the width of the multiplexer at the scope input.



## Voltage Balance in Series Multilevel Converters

---

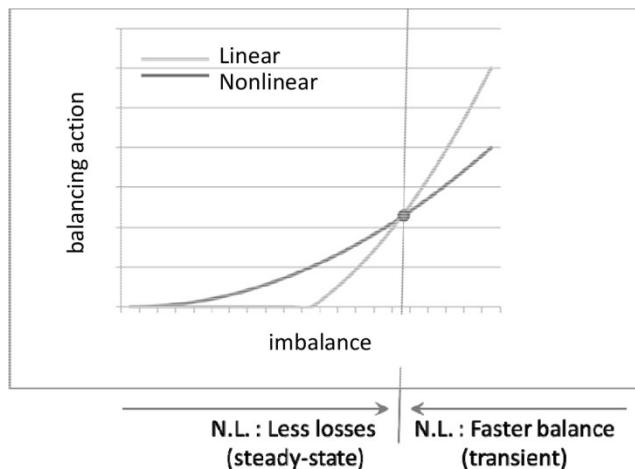
### 5.1. Basic principles

There are basically two ways to balance the cell voltages with passive components.

The most obvious principle involves passive components connected to each cell and generating losses that increase with the cell voltage; the capacitors with the higher values will supply more energy and tend to decrease until their voltage is equal to the others. In its simplest form, this is obtained with pure resistances, but other types can be used.

There is another mechanism that is slightly more subtle and has been described as “natural balance” [MEY 97], since it already exists in the circuit without any extra components. It involves AC current harmonics of all ranks except the multiples of  $ns$ , the convolution of these harmonics with the harmonics of the chopping signals creating DC currents in the flying capacitors. However, this mechanism can be too weak and different types of “balance boosters” may need to be added to reinforce this effect.

It is not straightforward to select the right solution for a given application, and it is therefore interesting to have general models of these devices to allow fast comparison. But all these devices also share common features; there is a trade-off between balancing strength and power consumption, and of course, the faster, the more losses. Therefore, the trade-off can be improved with nonlinear variants: designed for the same balancing strength at a certain level of imbalance, a nonlinear circuit should have a stronger effect for higher imbalance, and in the meantime less losses for lower imbalance (Figure 5.1).



**Figure 5.1.** Motivation for using nonlinear balance boosters

## 5.2. Linear circuits

### 5.2.1. Internal balancers

Cell losses increasing with the cell voltage have a balancing effect. We can use *voltage-induced losses*, e.g. parallel resistors  $R_{level}^{int}$  across all switches, so that at any time one of the resistances of each cell has a voltage equal to the cell voltage and the other resistance has a zero voltage

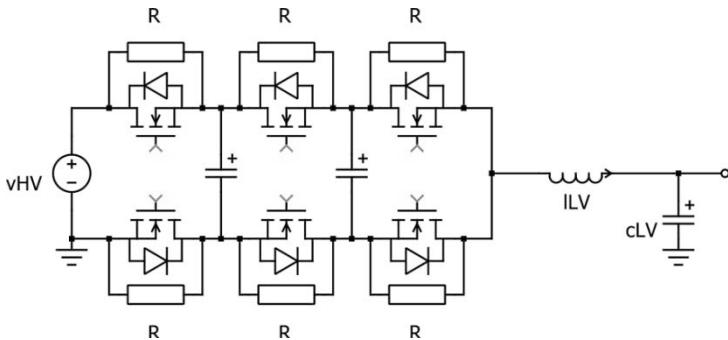
(Figure 5.2). But, we can also rely on *transition-induced losses*, e.g. resistance–capacitance networks  $R_{trans}^{\text{int}} C_{trans}^{\text{int}}$  connected across switches. The average power taken from a cell is, in the first case:

$$P_{level}^{\text{int}} = v_{cell}^2 / R_{level}^{\text{int}} \quad [5.1]$$

and in the second case, provided that  $R_{trans} \cdot C_{trans} \ll T_{OFF}$ , it can be approximated as:

$$P_{trans}^{\text{int}} = 2C_{trans}^{\text{int}} \cdot v_{cell}^2 \cdot f_{sw} \quad [5.2]$$

So, if  $R_{level}^{\text{int}} = 2C_{trans}^{\text{int}} \cdot f_{sw}$  the balancing performance of the two systems can be similar. However, when the converter is under voltage but not operating, or when it is operating but with a saturated duty cycle (0 or 100%), the transition-induced losses disappear and only the level-induced losses will allow balancing the system.



**Figure 5.2.** Internal balancer using level-induced losses

### 5.2.2. External balance boosters

Balance boost can be obtained by lowering the impedance on the current source of the commutation cell (LV side) at frequencies between  $f_{sw}, \dots, (n_S - 1)f_{sw}$ . Under ideally balanced conditions, no voltage harmonics are generated by

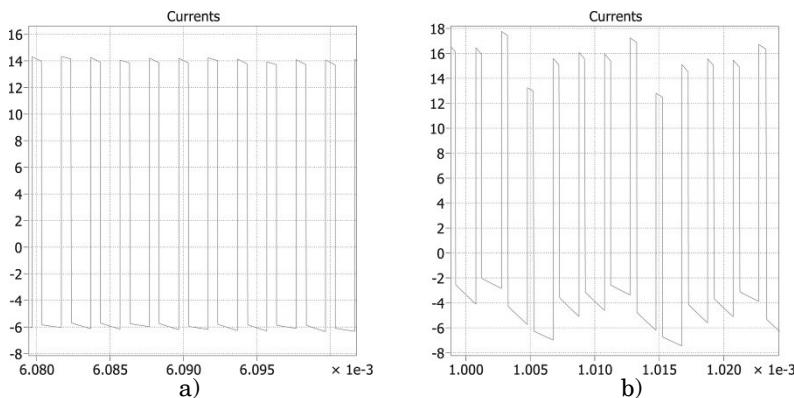
the commutation cell in this band of frequency, so that the low impedance is transparent. But in the presence of unbalanced voltages, voltage harmonics are generated and current harmonics of significant amplitude are allowed to flow and rebalance “naturally” the flying capacitor voltages as described in [MEY 97]. This natural balance is fast when *high current harmonics in phase* with the chopped voltage are generated, which means:

- low LV-side impedance *module* at  $f_{sw}, \dots, (n_s-1)f_{sw}$ ;
- low LV-side impedance *phase* at  $f_{sw}, \dots, (n_s-1)f_{sw}$ .

One way to obtain an impedance that is very low for frequencies less than  $n_s.f_{sw}$  is to use one or several resonant filters tuned at the multiples of  $f_{sw}$ . This can be a good solution for two-cell or three-cell converters since in both cases one filter is enough to ensure balance, but for higher numbers of cells several circuits are needed, which is a serious drawback of this solution ( $n/2$  circuits as explained in [DAV 97a, DAV 97b] and [DAV 95] for the case of parallel multicell converters). When the number of cells increases, another option is to allow currents to bypass the filtering inductor through a low impedance and ideally to block harmonics at  $n_s.f_{sw}$  to suppress permanent current circulation under balanced conditions. This could be done with a resistance in series with a parallel inductor-capacitor (LC) network tuned at  $n_s.f_{sw}$ . Such a solution involves relatively small components because of the high frequency, and only one network irrespective of the number of cells. However, adding inductance is generally considered too expensive and tuned circuit can be a manufacturing challenge; therefore, this solution is not described here.

With a balanced system, the voltage across the inductor is a square voltage waveform with an amplitude equal to  $v_{HV}/n_s$ , a frequency  $n_s.f_{sw}$  and a duty cycle equal to  $\text{mod}(n_s.D,1)$ . An example of such a waveform is given in

Figure 5.3(a) for a five-cell converter with  $V_{HV} = 100$  V and  $f_{sw} = 100$  kHz. A slight difference in the ripple of the top and bottom levels of the waveforms can be noted; it is related to the voltage ripple which involves, in general, two flying capacitors, but only one for the first and last cells. We can check that the peak-peak amplitude is 20 V, and if we neglect the small difference of voltage ripples, the period is 2  $\mu$ s. In Figure 5.3(b), an example of waveform obtained with the same converter with unbalanced voltages is given. It can be seen that the voltage levels are different and the period of the signal is now 10  $\mu$ s.

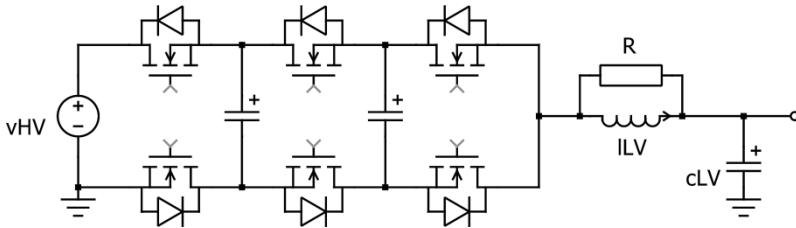


**Figure 5.3.** Waveforms of the voltage across the LV-side magnetic device of a five-cell chopper a) balanced conditions and b) unbalanced conditions

An intuitive understanding of the balancing mechanism is provided by saying that any circuit that consumes more energy when fed by the unbalanced voltage instead of the balanced voltage tends to rebalance the system.

A pure resistor is the simplest way to achieve this (Figure 5.4), but it should be noted that core losses are often modeled as a resistance in parallel with the winding, so in practice core losses help balancing, and they can have a

very significant influence. Of course, depending on the material and specific speed requirements of a given application, it is possible to increase this effect with an extra resistance.



**Figure 5.4.** External balancer using level-induced losses

Calling  $R_{level}^{ext}$  the resistance equivalent to the parallel connection the resistance representing core losses and the external resistor, the worst-case ( $D_{eq} = 50\%$ ) average power dissipated in balanced conditions is:

$$P_{level}^{ext} = \frac{1}{R_{level}^{ext}} \cdot \left( \frac{V_{HW}}{2n_S} \right)^2 \quad [5.3]$$

Like for external balancers, it is also possible to rely on losses induced by the voltage transitions instead of those induced by the voltage level; this can be done by using a resistor-capacitor (RC) network instead of a pure resistance. This may be motivated by the intuition that using the transition only will reduce the power consumption. It may not be so because balancing is mainly caused by current harmonics with ranks 1 to  $n_S - 1$ , and steady-state losses by rank  $n_S$ ; therefore, it would probably be wiser to use a series inductor (higher low rank currents) to improve the speed/loss trade-off, but we may not want to add an inductor at this

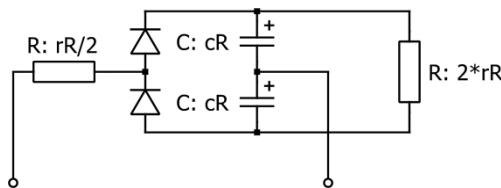
point to limit cost and dimensions. In the end, it is not so easy to know which solution is the best because the speed of balancing depends on many factors, such as phase of the current harmonics, number of cells and duty cycle; in this chapter, the aim is to provide models allowing a case-by-case study. In the case of an RC network in parallel with the smoothing inductor, the power consumption is:

$$P_{trans}^{ext} = C_{trans}^{ext} \cdot \left( \frac{V_{HV}}{n_S} \right)^2 \cdot n_S f_{sw} \quad [5.4]$$

The RC circuit basically works on the transitions of the chopped voltage, and to better understand how it works and how it could be improved, we will describe a simple case of operation and assume that only one cell has a higher than normal voltage. This case is easier to study than the general case, but in fact it is a case of high practical interest because this is what happens if the system is balanced and  $V_{HV}$  increases suddenly: at the beginning, the increase of  $V_{HV}$  is fully applied to the HV-side cell. Under such circumstances, the transitions generated by the cell with the highest voltage will generate a higher current in the balance booster, which means that the flying capacitors connected to this cell will evolve toward values giving a better balance: one is charging and the other is discharging. The neighbor cell will then see its voltage increase and generate more current in the balance booster. The voltage increase will thus propagate from the first cell to the others until balance is reached. If the number of cells is high, it will take some time for the last cell to even begin to charge; this is not the optimal balancing mechanism.

Another option is to use a balance booster that somehow treats all the cells with lower voltage in the same way and allows them to increase all together. One way to go

in this direction is to take only power from the highest and lowest levels which can somewhat be done with some storage and a rectifier. In the example of Figure 5.5, a series resistor is provided to limit the amplitude of current pulses and the values of these resistors are defined so that each absorbs half of the losses in balanced steady state. There are of course many possible variants of such a circuit.



**Figure 5.5.** Example of rectifier-based external balance booster

### 5.2.3. Pros and cons of internal/external balance boosters

Independently of the speed/losses trade-off that can be evaluated by simulation, the different principles described above differ in terms of operating range and complexity of implementation.

The advantage of using level-induced losses of the internal balance booster is that it is totally independent of the switching action and will still act under operating conditions where the balancing effect provided by the LV-side impedance vanishes:

- converter under voltage but not running;
- converter running with saturated duty cycles (0 or 100%);
- converter running at a particular duty cycle where natural balance vanishes (e.g.  $D = 50\%$  with  $n_s = 4$ ).

From the point of view of implementation, the internal balance booster should be made as simple as possible because the chosen schematic is replicated for each cell and even each switch; that includes many components and components typically in proximity of the switching devices, i.e. a point of the circuit where there are many constraints: commutation loop stray inductances must be minimized, driver should not be far, close connection to two capacitors, etc. An external balance booster has less constraints because there is only one and its connection to the inductor can generally be longer which gives more freedom for the design layout.

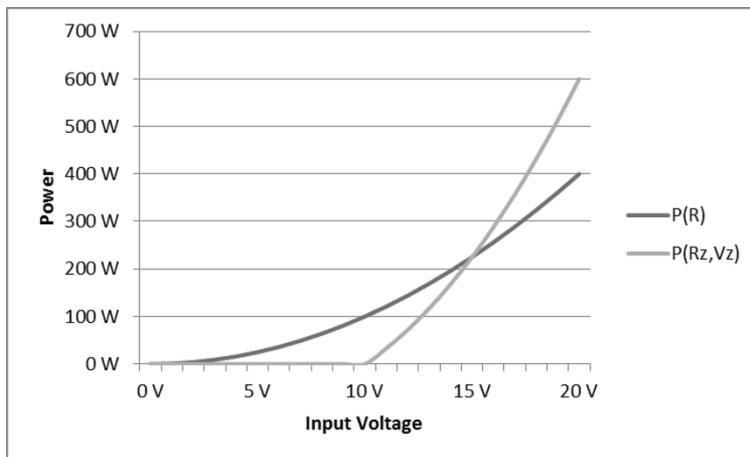
### 5.3. Nonlinear variants

#### 5.3.1. Internal balance boosters

The simplest nonlinear variant of level-based internal balance booster is obtained by using a Zener diode or any power circuit emulating its behavior. If the Zener voltage is  $V_Z$  and its series resistance is  $R_Z$ , the power taken from the cell is:

$$P_{level}^{int\ N.L.} = \max\left(0 ; v_{cell} \cdot \left(\frac{v_{cell} - V_Z}{R_Z}\right)\right) \quad [5.5]$$

Of course, assuming  $V_Z = 0$  takes us back to the linear circuit; therefore, this expression can be used for both linear and nonlinear circuits. An example of these characteristics is given in Figure 5.6. It can be seen that if these circuits were used for a converter with a nominal voltage of 12 V, for example, the nonlinear circuit would have roughly half the steady-state losses of the linear circuit, but in case of strong imbalance, the reaction of the nonlinear circuit will be much stronger.



**Figure 5.6.** Power losses vs. voltage for a linear and nonlinear level-based internal balance booster. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

When an RC circuit is used, a similar behavior can be obtained by connecting two back-to-back Zener diodes in series with the RC network. If such a circuit is connected to a cell generating a square voltage source with a peak-peak amplitude  $v_{cell} > V_Z$  at a frequency  $f$  such that  $RC \ll 1/f$ , the quantity of electricity taken from the source at each cycle will be  $C.(V - V_Z)$  and the power will be:

$$P_{trans}^{\text{int}} = v_{cell} \cdot C \cdot (v_{cell} - V_Z) \cdot f \quad [5.6]$$

### 5.3.2. External balance boosters

If a Zener diode is inserted in series with the resistance of an external balance booster, the worst-case ( $D_{eq} = 50\%$ ) average power consumed under balanced conditions is:

$$P_{level}^{\text{ext}} = \frac{V_{HV}}{2n_S \cdot R_{level}^{\text{ext}}} \cdot \left( \frac{V_{HV}}{2n_S} - V_Z \right) \quad [5.7]$$

In case of an RC network with back-to-back Zeners, we get:

$$P_{trans}^{ext} = \frac{V_{HV}}{n_S} C_{trans}^{ext} \cdot \left( \frac{V_{HV}}{n_S} - 2V_Z \right) \cdot n_S f_{sw} \quad [5.8]$$

For the rectifier-based circuit, we have:

$$Loss_{rect} = \frac{\frac{V_{HVnom}}{n_S} \left( \frac{V_{HVnom}}{n_S} - v_{Z_{rect}}^{ext} \right)}{4 \cdot r_{rect}^{ext}} \quad [5.9]$$

## 5.4. Loss-based design

### 5.4.1. Introduction

Since the performance of balance booster is mainly a matter of trade-off between losses and speed, and speed is quite difficult to predict by calculation, it is sensible to use losses as an input parameter for the design of the different types of balance boosters so that we can, for example, impose the same level of power consumption for all types and compare their balancing behavior and speed over a given mission profile.

This design is now described for an  $n_S n_P$  series-parallel converter in which the steady-state cell voltages are:

$$v_{cell} = \frac{V_{HV}}{n_S} \quad [5.10]$$

and the level of losses for each of the  $n_P$  phases is equal to the total losses divided by  $n_P$ . A coefficient  $K_{NL}$  is introduced to select the sharpness of the nonlinearity; setting this coefficient to 0 gives a linear system, and when it tends to 1 the nonlinearity becomes infinitely sharp.

### 5.4.2. Internal balance boosters

For a level-based internal balance booster, we can derive the circuit parameters from the steady-state losses using equations [5.1] and [5.5], and we get:

$$\left\{ \begin{array}{l} v_{Z_{level}}^{\text{int}} = K_{NL} \cdot \frac{V_{HVnom}}{n_S} \\ r_{level}^{\text{int}} = \frac{n_P \cdot V_{HVnom} \cdot \left( \frac{V_{HVnom}}{n_S} - v_{Z_{level}}^{\text{int}} \right)}{Loss_{level}} \end{array} \right. \quad [5.11]$$

Using a similar approach, we can derive the parameters of the transition-based version:

$$\left\{ \begin{array}{l} v_{Z_{trans}}^{\text{int}} = K_{NL} \cdot \frac{V_{HVnom}}{n_S} \\ c_{trans}^{\text{int}} = \frac{Loss_{trans}}{2n_P \cdot V_{HVnom} \cdot \left( \frac{V_{HVnom}}{n_S} - v_{Z_{trans}}^{\text{int}} \right) \cdot f_{sw}} \\ r_{trans}^{\text{int}} = \frac{1}{10n_S \cdot c_{trans}^{\text{int}} \cdot f_{sw}} \end{array} \right. \quad [5.12]$$

### 5.4.3. External balance boosters

In the case of external balance booster, we get the following design equations for the level-based version:

$$\left\{ \begin{array}{l} v_{Z_{level}}^{\text{ext}} = K_{NL} \cdot \frac{V_{HVnom}}{2n_S} \\ r_{level}^{\text{ext}} = \frac{n_P \cdot \frac{V_{HVnom}}{2n_S} \cdot \left( \frac{V_{HVnom}}{2n_S} - v_{Z_{level}}^{\text{ext}} \right)}{Loss_{level}} \end{array} \right. \quad [5.13]$$

for the transition-based version:

$$\left\{ \begin{array}{l} v_{Z_{trans}}^{ext} = K_{NL} \cdot \frac{V_{HVnom}}{2n_S} \\ c_{trans}^{ext} = \frac{Loss_{trans}}{2n_P \cdot \frac{V_{HVnom}}{2n_S} \left( \frac{V_{HVnom}}{2n_S} - v_{Z_{trans}}^{ext} \right) \cdot 2n_S f_{sw}} \\ r_{trans}^{ext} = \frac{1}{10n_S \cdot c_{trans}^{ext} \cdot f_{sw}} \end{array} \right. \quad [5.14]$$

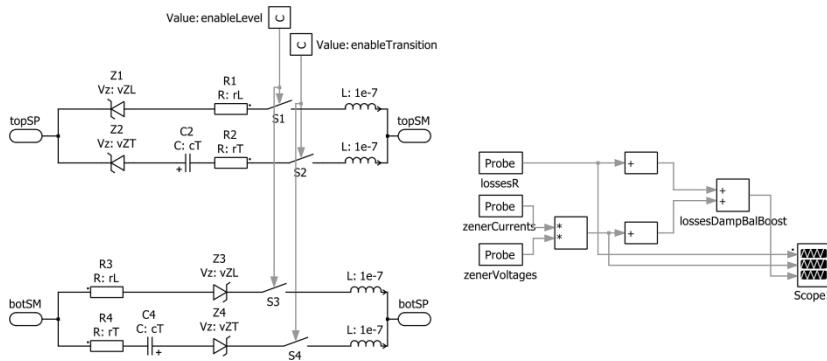
and for the rectifier-based version:

$$\left\{ \begin{array}{l} v_{Z_{rect}}^{ext} = K_{NL} \cdot \frac{V_{HVnom}}{n_S} \\ r_{rect}^{ext} = \frac{n_P \cdot \frac{V_{HVnom}}{n_S} \left( \frac{V_{HVnom}}{n_S} - v_{Z_{rect}}^{ext} \right)}{4 \cdot Loss_{rect}} \\ c_{rect}^{ext} = \frac{1}{n_S \cdot r_{rect}^{ext} \cdot f_{sw}} \end{array} \right. \quad [5.15]$$

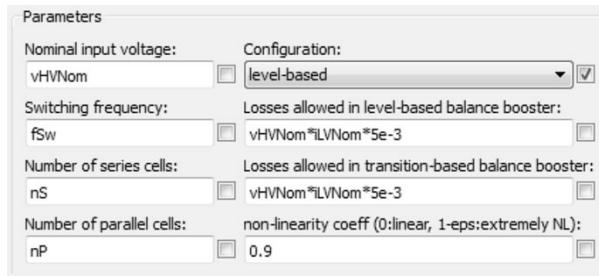
## 5.5. Vectorized models of balance boosters

Taking into account the previous calculation simulation models of both internal and external balance boosters, a design-oriented mask that is scalable for any number of cells can be developed. As suggested earlier, the user will select a permissible value of steady-state losses and the topology and values of the components in the balance boosters will be calculated automatically.

The different variants of internal balance boosters are included in the same model (Figure 5.7). Mask parameter options (Figure 5.8) facilitate using them separately or together with the level of losses in each of them adjusted separately. On the right-hand part of the circuit, the losses in this balance booster are evaluated to allow visualization and checking of results.



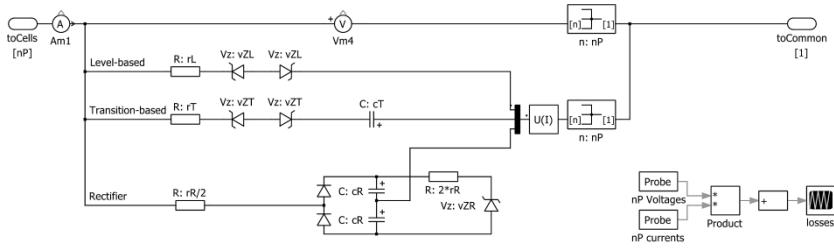
**Figure 5.7.** Model of the vectorized internal balance booster



**Figure 5.8.** Mask parameters of the vectorized internal balance booster

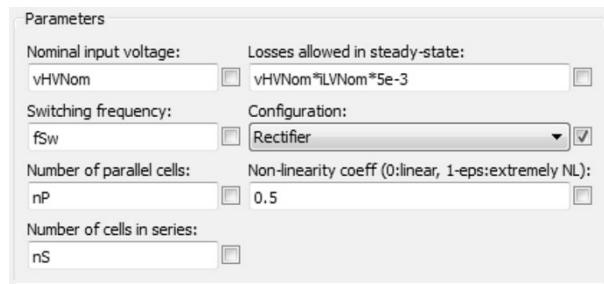
The model of the external balance booster (Figure 5.9) is vectorized with respect to  $n_P$  only, since by principle there is a single circuit for  $n_S$  series cells. The three variants are included in the same model, and the mask (Figure 5.10)

allows selecting the variant to be used, the level of steady-state losses allowed as well as the nonlinearity coefficient.



Author : TM

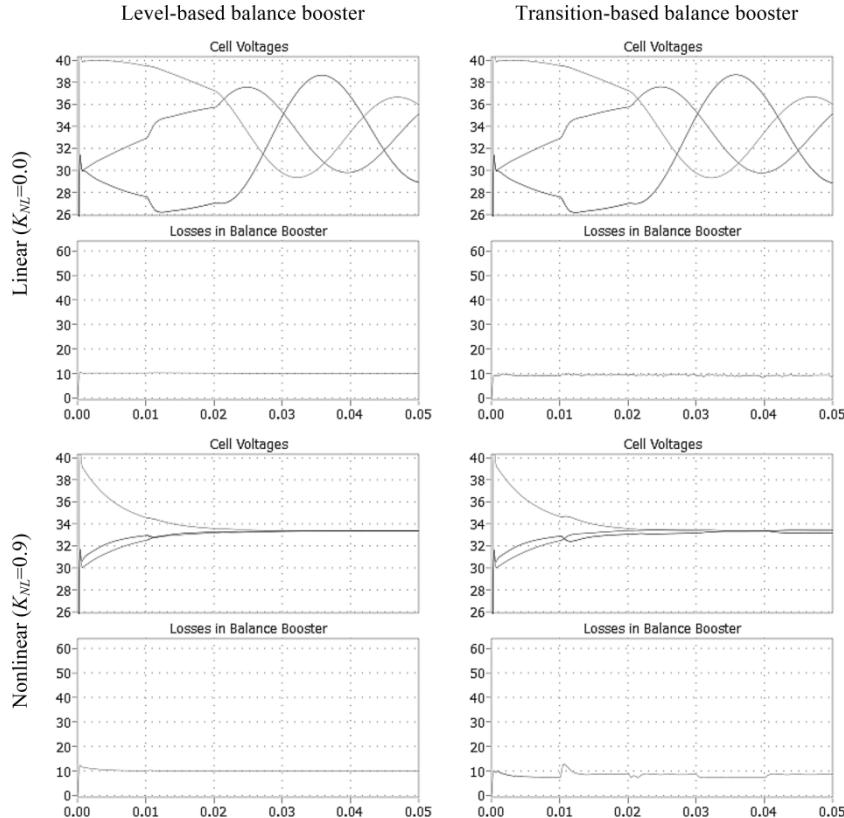
**Figure 5.9.** Model of the external balance booster



**Figure 5.10.** Mask parameters of the external balance booster

The results obtained with four different configurations of internal balance booster of a three-cell converter for the same initial conditions, control profile, load profile and level of steady-state losses are shown in Figure 5.11. It can be seen that the nonlinear variants give a much faster rebalance and a non-oscillatory response. The responses of the level-based and transition-based versions are very similar, but the first response is simpler and has the decisive advantage of working at all duty cycles. The only disadvantage of this solution is that if the nonlinearity is obtained with a Zener or an equivalent device with a fixed voltage, the response will be different when the HV-side

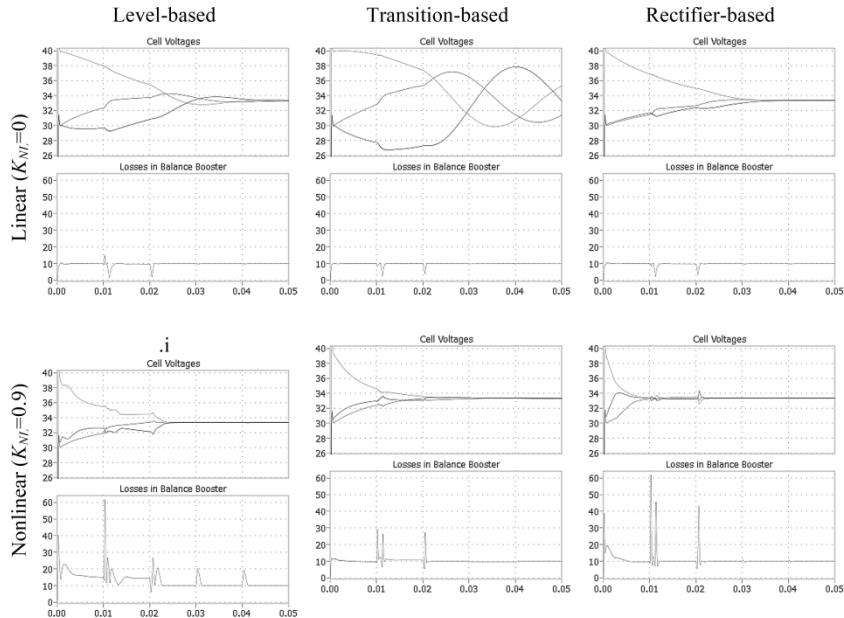
voltage is varied. This means that the behavior of the balancing mechanism should be checked over a voltage range and not only at the nominal voltage.



**Figure 5.11.** Balancing waveforms for different configurations of internal balance boosters. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

Using the same converter and control/load profile, the different configurations of external balance booster are also evaluated and the results are given in Figure 5.12. In this case also, the general conclusion is that nonlinear versions improve significantly the behavior. The best response is obtained with the nonlinear version of the rectifier-based

variant, but it can be seen that some easier-to-implement options can also perform quite well.



**Figure 5.12.** Balancing behavior with different designs of external balance boosters. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

In practice, it is often beneficial to use both internal and external balance mechanisms. The internal mechanism is always compulsory because it is this mechanism that will act when not switching. The external mechanism will be involved with almost any design because of core losses; it may be reinforced with a possibly more sophisticated circuit since it is shared by all cells. For example, the nonlinearity can be controlled to follow the variations of the HV-side voltage, and there are a number of ways to do this with circuits that can even be regenerative.



---

## Filter Design

---

### 6.1. Requirements

#### 6.1.1. Steady state: current ripple, voltage ripple and standards

The first function of the filters is to provide high-quality waveforms to the external world: source and load. This is challenging because loads and lines accept only high-quality signals, whereas a two-level communication cell delivers more noise than signal (noise is a square of amplitude 1, and signal can be adjusted somewhere between 0 and 1). This requirement is sometimes formulated as a constraint on the pk-pk ripple; so we need the expression of current and voltage ripples. The current ripple can be directly derived from the usual equations of a two-level converter and account for  $n_P$  and  $n_S$ :

$$\Delta I_{LV}^{pkpk} = \frac{\left( \frac{V_{HV}}{n_P \cdot n_S} \right)}{4 \cdot L_{LV} (n_P \cdot n_S \cdot f_{sw})} \quad [6.1]$$

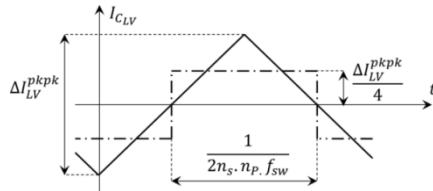
By looking at the capacitor current waveform in Figure 6.1, we can see that the voltage ripple caused by the triangular current is the same as that created by the fictive square current (dashed line); so we get the following formula for the voltage ripple:

$$\Delta V_{LV}^{pkpk} = \frac{\frac{\Delta I_{LV}^{pkpk}}{4} \left( \frac{1}{2n_p \cdot n_s \cdot f_{sw}} \right)}{C_{LV}} \quad [6.2]$$

Combining these equations, we get the following criteria on the inductance-capacitance product (LC) to match the voltage ripple requirement:

$$L_{LV} C_{LV} \geq \frac{V_{HV}}{16 \Delta V_{LV}^{pkpk} (n_p \cdot n_s)^3 f_{sw}^2} \quad [6.3]$$

As can be seen from this formula, when the switching frequency or the number of cells increases, a given voltage ripple requirement can be met with a much smaller LC value.

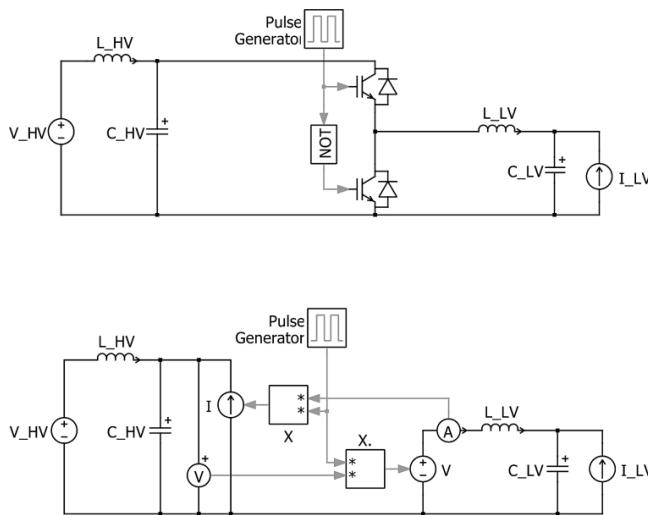


**Figure 6.1.** Current waveform in the LV-side capacitor

However, peak-peak ripple is only one of the requirements and the Electromagnetic Compatibility (EMC) standards are mainly expressed in the frequency domain, which gives a quite different formulation and behavior. Subsequently, we will show how the requirements on low frequency components of conducted emissions of EMC can be taken into account in the filter design.

If the converter is a chopper with a duty cycle  $D$ , the harmonics of rank  $r$  of these two sources can be easily calculated as:

$$\begin{cases} I_{r,f_{sw}}^{chop} = \frac{2I_{LV}}{r\pi} \cdot \sin(r\pi D) \\ V_{r,f_{sw}}^{chop} = \frac{2V_{HV}}{r\pi} \cdot \sin(r\pi D) \end{cases} \quad \text{for } r = 1, \dots, \infty \quad [6.4]$$



**Figure 6.2.** Commutation cell and its model

Because the standard must be respected for all points of operation, the reduction brought by the duty cycle can be omitted and the envelope of the spectra can be used to determine the filter requirements on both sides of the commutation cell. With the same kind of simplification in mind, the asymptotic response of the filter can be assumed, which means that for a second-order filter with a natural frequency lower than the fundamental frequency the envelopes of the spectra after filtering are:

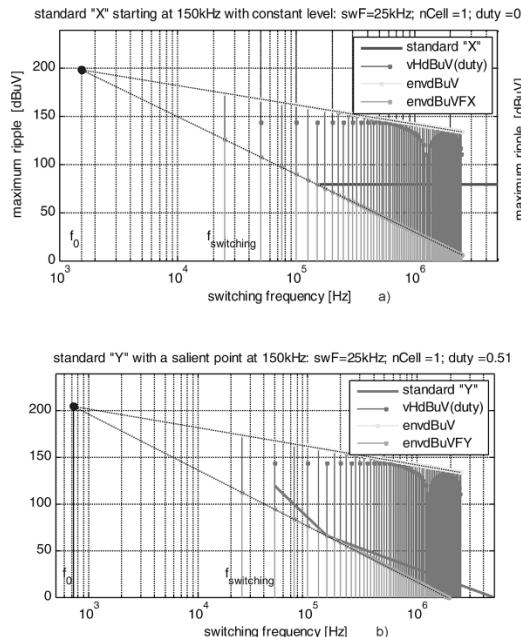
$$\begin{cases} \hat{I}_{r,f_{sw}}^{HV} = \left( \frac{f_0^{HV}}{r \cdot f_{sw}} \right)^2 \frac{2I_{LV}}{r\pi} & \text{for } r = 1, \dots, \infty \\ \hat{V}_{r,f_{sw}}^{LV} = \left( \frac{f_0^{LV}}{r \cdot f_{sw}} \right)^2 \frac{2V_{HV}}{r\pi} \end{cases} \quad [6.5]$$

As explained previously (Figure 1.3), interleaving  $n$  PWM signals makes possible cancelling all harmonics with a rank that is not a multiple of  $n$  and does not modify harmonics

with a rank multiple of  $n$  (sum of  $n$  vectors of amplitude  $1/n$ ). When the commutation cell is a parallel assembly of  $n_P$  blocks of  $n_S$  cells in series, parallel connection affects the spectrum on both sides, but series connection influences only the LV side; therefore, the previous expression of the harmonics is still valid except that it must be applied only for:

–  $r = n_P, 2.n_P, \dots, \infty$  for the current harmonics on the HV side;

–  $r = n_P.n_S, 2.n_P.n_S, \dots, \infty$  for the voltage harmonics on the LV side.



**Figure 6.3.** Envelopes of spectra before and after filtering versus EMC standard profiles (frequency of first non-zero harmonic  $< f_{\text{salient}}$ ). For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

From these equations, we get that the envelopes of spectra after filtering have a slope of  $-60 \text{ dB/dcde}$  so that

there is generally only one harmonic that governs the choice of the cutoff frequency of the filter. This harmonic corresponds to a salient point in the limit of the standard. This point is sometimes the starting point of the limit, i.e. no requirement before 150 kHz like in Figure 6.3(a), or it is a point of the limit such that the slope is less than  $-60 \text{ dB/dcde}$  before this point and greater than  $-60 \text{ dB/dcde}$  after this point (Figure 6.3(b)). Because of the relative slopes, making the filtered harmonic at this point equal to the max value allowed by the standard is sufficient, and allows maximizing the cutoff frequency of the filter. In these examples, the salient point is at 150 kHz, but this value is not a random example, it is frequently encountered; so in many cases, a reasonable first estimate of the filter requirements is obtained by evaluating the 150 kHz harmonic only.

When the switching frequency is high, the situation can be different. If the first non-zero harmonic is at a frequency higher than the salient frequency, it is this harmonic that needs to be tracked. As explained in more detail in [MEY 13], these two situations give a quite different behavior:

- if the frequency of the first non-zero harmonic is higher than the frequency of the salient point, the design is governed by rank 1, and substituting for  $r = 1$  in [6.5] gives:

$$\begin{cases} \frac{f_0^{HV}}{f_{sw}} = \sqrt{\frac{\pi \hat{J}_{f_{sw}}^{HV}}{2I_{LV}}} \\ \frac{f_0^{LV}}{f_{sw}} = \sqrt{\frac{\pi \hat{V}_{f_{sw}}^{LV}}{2V_{HV}}} \end{cases} \quad [6.6]$$

so we can see that in this region, increasing the switching frequency facilitates increasing the cutoff frequency of the filter;

– if the frequency of the first non-zero harmonic is less than the frequency of the salient point, the design is governed by the harmonic at the frequency of the salient point; so we must now substitute for  $r = f_{salient}/f_{sw}$ :

$$\begin{cases} \left(f_0^{HV}\right)^2 f_{sw} = \frac{\pi \hat{I}_{r,f_{sw}}^{HV} f_{salient}^3}{2I_{LV}} \\ \left(f_0^{LV}\right)^2 f_{sw} = \frac{\pi \hat{V}_{r,f_{sw}}^{LV} f_{salient}^3}{2V_{HV}} \end{cases} \quad [6.7]$$

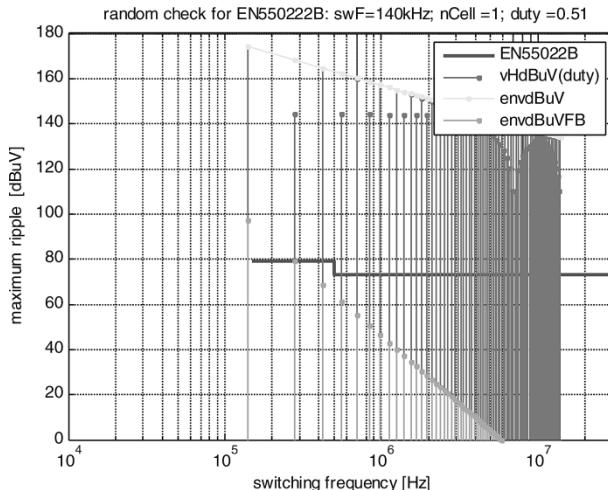
and we can see that in this region the switching frequency must be decreased to increase the cutoff frequency of the filter and minimize its size.

In conclusion, we can see that in many cases the filter can be made smaller by reducing the switching frequency, and this goes against many common statements.

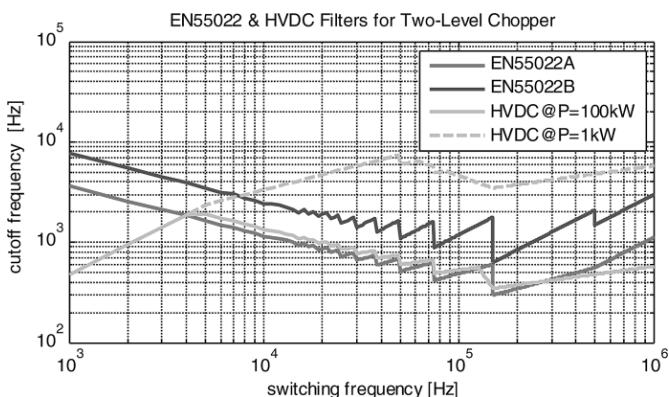
In the previous equation, the discrete nature of the spectrum has not been taken into account. In some cases, especially when the standard starts at the salient frequency, it is the opportunity for the designer to use a filter such that the envelope exceeds the standard but the real spectrum complies. Such an example is given in Figure 6.4; the first non-zero harmonic is at 140 kHz and out of the scope of the standard; so the design of the filter is governed by the harmonic at 280 kHz, with the same level allowed at this frequency than at 150 kHz in this example. In this case, switching at 150 kHz would roughly require dividing the cutoff frequency by 2.

With this approach, we can plot the evolution of the cutoff frequency required for a two-level converter for a given standard versus the switching frequency (Figure 6.5). In this graph, the saw-tooth is related to the discrete nature of the spectrum as discussed above, but we can see that, as

explained earlier, the general trend is a decrease in the cutoff frequency when switching frequency increases up to 150 kHz (the starting frequency of the standards), and an increase beyond.

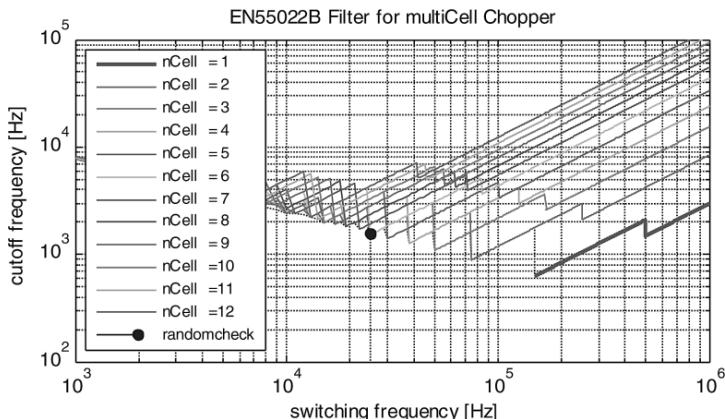


**Figure 6.4.** Filter design taking advantage of the discrete nature of the spectrum. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)



**Figure 6.5.** Evolution of cutoff frequency vs. switching frequency (two-level converter). For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

When considering multilevel converters, similar principles apply but give quite different results. For very low switching frequencies, the curve is almost the same as for two-level converters because cancelling harmonics 1 to  $n - 1$  has no effect (these harmonics are in a region not covered by the standards) and cancelling harmonics of higher ranks modifies the density of the spectrum but not the envelope that governs the choice of the cutoff frequency. But for higher and more realistic values of the switching frequency, the required cutoff frequency starts increasing as soon as  $n$  times the switching frequency exceeds 150 kHz (Figure 6.6). As a result, it can be seen that a 10-cell converter at 100 kHz can use a filter with a cutoff frequency that is 10 times higher than the cutoff frequency required for a two-level converter switching at the same frequency.



**Figure 6.6.** Evolution of cutoff frequency vs. switching frequency (multicell converter). For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

This is, however, only a partial conclusion related to standard compliance, and as we try to show in this chapter, filter design is a combination of several factors and this is just one of the constraints applied on the LC product.

### 6.1.2. Transients

Dynamic response depends on the control loops and regulators, and the parameters of the regulator are derived from the values of the elements in the filter, so a full description is difficult. However, assuming an infinitely fast response of the control, we can see that the filter imposes physical limits to the response time and overshoots when the output of the regulator saturates.

For example, the control loop of a converter with  $n_P$  cells in parallel cannot do any better than saturate immediately the duty cycle to 0 in case of full-load to no-load step in order to reduce voltage overshoot that will be in this case:

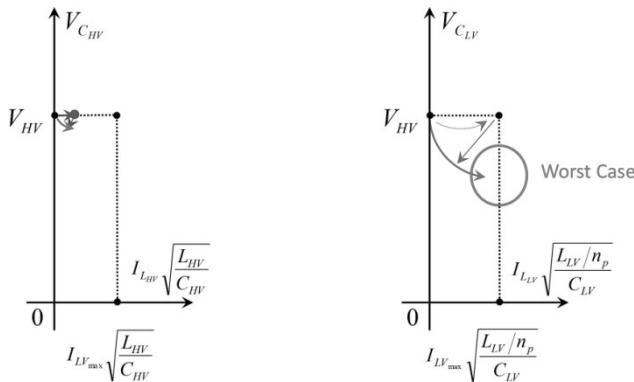
$$V_{overshoot} = I_{LV}^{nom} \cdot \sqrt{\frac{L_{LV} / n_P}{C_{LV}}} \quad [6.8]$$

The control loop cannot do better than saturate the duty cycle to 100% in case of no-load to full-load, which will give a worst-case voltage dip of the same value as the voltage overshoot. So, the tolerance on the LV-side voltage in case of transient gives a minimal value of the  $L_{LV}/C_{LV}$  ratio that can be directly derived from [6.8].

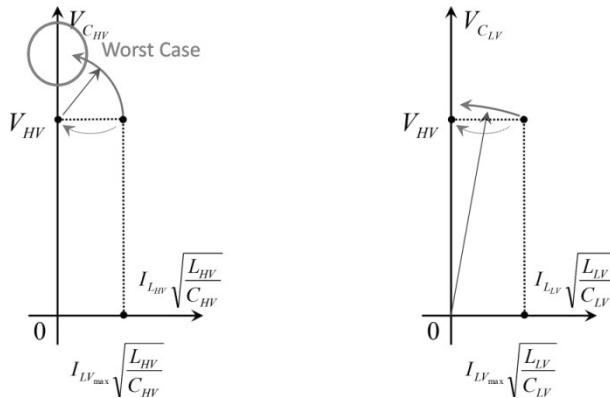
Concerning the HV side, a similar analysis shows that the worst case corresponds to the full-load to no-load case and gives the following requirement on the  $L_{HV}/C_{HV}$  ratio:

$$\sqrt{\frac{L_{HV}}{C_{HV}}} = \frac{V_{HV}^{overshoot}}{I_{LV}^{\max}} \quad [6.9]$$

Taking load step into consideration, we have constraints on the L/C ratio of both filters, so when combined with steady-state transients we already have a deterministic system. If we want to minimize the inductors and the capacitors, there is already one solution. However, other requirements may need to be taken into account, and minimizing L and C is not always the best thing to do.



**Figure 6.7.** State-plane analysis of the response to a no-load to full-load step



**Figure 6.8.** State-plane analysis of the response to a full-load to no-load step

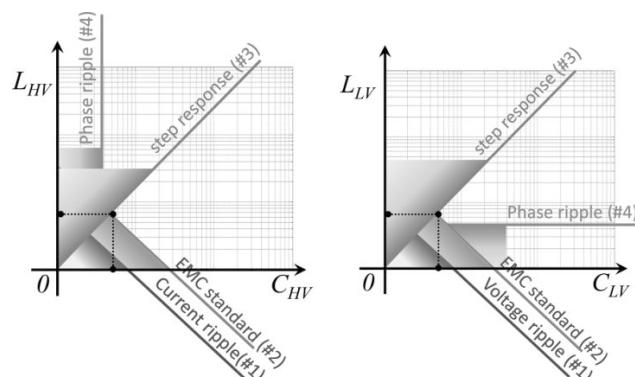
### 6.1.3. Extra design constraints

Starting the design of an LV-side filter by imposing the value of the current is certainly not the best way to optimize the filter because this current ripple is one of the degrees of freedom available to the designer; it is purely internal and cannot be directly known from the load or source point of view; therefore, it cannot be imposed by any standard.

However, leaving this value totally free and conducting design using only LC and L/C can give impractical results with current ripples of several 100%, especially in the case of multicell converters. If the design involves weight or volume and the model of inductor is not purely basic, the result should never use such low value/high ripple inductors, because high ripple gives a weight/volume penalty that will prevent optimization to go in this direction. However, when simple models are used, it is safer to limit phase current ripples, still allowing quite high values like a little more than 200%, for example, which is the limit of Zero Voltage Switching (ZVS).

## 6.2. Design process

From a mathematical point of view, these different criteria generate inequalities that combine differently depending on the application; some criteria may become “transparent” because one criterion imposes a more severe constraint that masks the first criterion. This can be represented in a log-log diagram in which LC and L/C requirements are straight lines. An example is given in Figure 6.9 for both the HV-side and LV-side filters.



**Figure 6.9.** Filter requirements in  $(L, C)$  planes. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

The points indicated on these graphs satisfy all criteria and may seem to be the optimal design, but it is not always true. The clear advantage of these points is that they give the minimal value of the capacitors. However, in practice, capacitors have a much higher energy density than magnetic components, a lower density and lower cost; so it may be interesting to increase the value of the capacitor to optimize the overall volume of the filter. To match the criteria, the first idea is, in the configuration illustrated in Figure 6.9, to test other designs along the EMC standard requirement to lower the value of the inductance. However, especially in the case of the LV-side inductor, reducing the value of the inductance does not always bring a volume reduction since it may correspond to high values of current ripple and flux density ripple that generate more losses and require in the end a bigger device. In the end, designs along the step response requirement, corresponding to higher values of inductance *and* capacitance, must not be systematically ignored.

The main part of the corresponding code to be included in the mask is given here:

```
% Find ILV and cLV
lMin = vHVNOM / fSw / (iMax/nP); % phase inductance to limit deltaI
for 1/fSw with no duty change
switch LVmagType
case {1,2} % uncoupled inductors
    lRipple = vHVNOM/4/(iLVnRip*iLVNom/nP)/fSw / nS^2; % phase
    inductance to limit worst case phase ripple
case {3,4,5,6} % interCell transformer
    lRipple = vHVNOM/4/(iLVnRip*iLVNom/nP)/fSw / nS^2 / nP^2; % phase
    inductance to limit worst case phase ripple
end
ILV = max(lRipple,lMin); % phase inductance
cRipple = (iLVnRip*iLVNom/nP/nP/4) * (1/2/nP/nS/fSw) /
(vLVnRip*vHVNOM);
cStandard = 1/(2*pi*f0LVstandard)^2 / ILV;
```

```
cTransient = ILV/nP * (iLVNom/vLVTransN/vHVNOM)^2 * 0.6 ; % coeff  
0.6 if 4C+sqrt(L/C) in // with C  
cLV = max(cRipple,cStandard); cLV = max(cLV,cTransient) ;  
f0 = 1/2/pi/sqrt(ILV/nP*cLV); ratioF = fSw/f0 ;
```



## Design of Magnetic Components for Multilevel Choppers

---

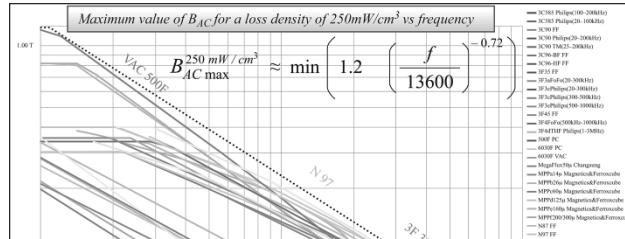
### 7.1. Requirements and problem formulation

The size of magnetic components correlates to material limits, such as flux density saturation and maximum operating temperature (magnetic, conductors and insulators). The approach proposed here is simplified to avoid entering the complex field of thermal modeling; it is based on the assumption that we are able to determine appropriate magnetic and conductor loss densities that make operating conditions compatible with standard material limits. For example, we can impose loss densities of 250, 500 or 750 mW/cm<sup>3</sup>; this choice depends on thermal conditions (ventilation and ambient temperature) and on the size of the object (lower loss densities are allowed for big objects since losses are proportional to the cube of dimensions and the exchange surface is proportional to the square of dimensions).

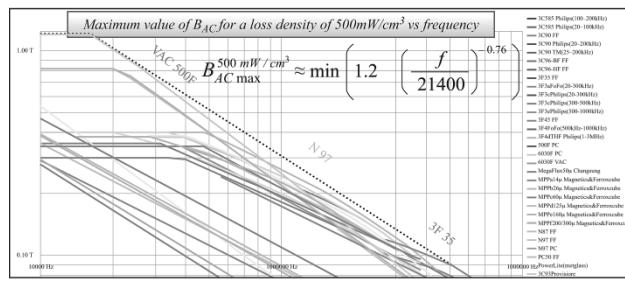
These loss densities translate to RMS current densities and flux densities but the exact relationship depends on the material and the frequency. Here, we will also allow a simpler formulation by studying the material properties independently of the design process itself. As shown in Figure 7.1, we can identify a simple equation representing the

best performance at any frequency. The equation shown in the figures corresponds to quite an optimistic approach, and for the design, we use more realistic values that are as follows:

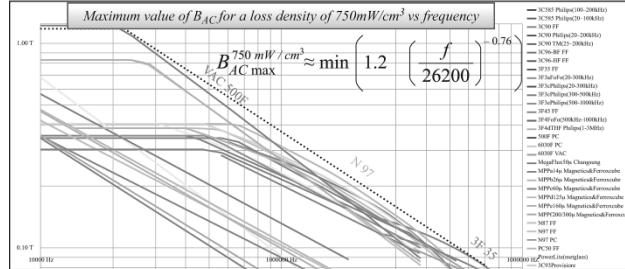
$$B_{AC\ max}^{250\ mW/cm^3} \approx \min \left( 1.2 \left( \frac{f}{10,000} \right)^{-0.72} \right) \quad [7.1]$$



a)



b)



c)

**Figure 7.1.** Maximum AC flux densities versus frequency for different materials: a)  $250\text{ W/cm}^3$ , b)  $500\text{ W/cm}^3$  and c)  $750\text{ W/cm}^3$ .

For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

$$B_{AC\max}^{500mW/cm^3} \approx \min \left( 1.2 \left( \frac{f}{15,000} \right)^{-0.76} \right) \quad [7.2]$$

$$B_{AC\max}^{750mW/cm^3} \approx \min \left( 1.2 \left( \frac{f}{18,500} \right)^{-0.76} \right) \quad [7.3]$$

A similar approach is used for conductors and gives the following table valid for DC currents.

	250 W/cm <sup>3</sup>	500 W/cm <sup>3</sup>	750 W/cm <sup>3</sup>
Copper	3.3 A/mm <sup>2</sup>	4.7 A/mm <sup>2</sup>	5.8 A/mm <sup>2</sup>
Aluminum	2.6 A/mm <sup>2</sup>	3.7 A/mm <sup>2</sup>	4.5 A/mm <sup>2</sup>

**Table 7.1.** Current densities for different loss densities

AC currents do not flow evenly in a conductor, which increases the losses, and this is generally interpreted as an increase in AC resistance. In the case of a single conductor, this is called the skin effect and gives an equivalent resistance that varies with the square root of the frequency. In a winding, the different conductors influence each other and result in a complex behavior that involves geometry, 3D effects, etc. In practice, for a realistic winding geometry, this increase in the resistance can be very high (10 is not rare and even higher values can be found). In a filtering device for a DC/DC converter, the current is the sum of a DC current and a triangular current, and to account for increased AC resistance, the losses can be estimated using an equivalent RMS current calculated as:

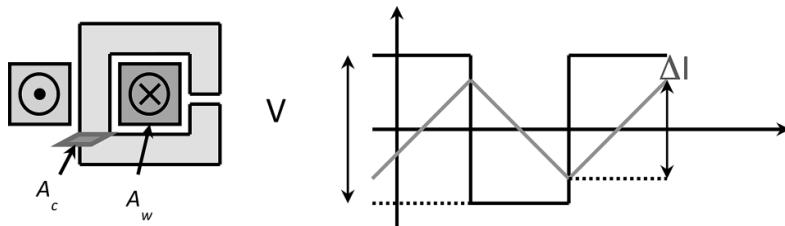
$$I_{RMSeq} = I_{DC} \cdot \sqrt{1 + \frac{R_{AC}}{R_{DC}} \frac{1}{12} \left( \frac{\Delta I}{I_{DC}} \right)^2} \quad [7.4]$$

Because of the quotient 12 and the limited values of  $\Delta I/I_{DC}$  used in practice, the influence of  $R_{AC}/R_{DC}$  is not as dramatic as it first seems. We need to take it into account but we will allow a simplified formulation, inspired by the behavior resulting from the skin effect:

$$\frac{R_{AC}(f)}{R_{DC}} = \sqrt{1 + \frac{f}{f_{skin}}} \quad [7.5]$$

NOTE.– As will be shown further on, this formula must be applied with  $f = f_{sw}$  for inductors and  $f = n_{Cell}.f_{sw}$  for InterCell Transformers (ICT).

We will now show how these equations can be combined and used to limit conductor loss densities to the user-defined value.



**Figure 7.2.** Definition of sections  $A_w$  and  $A_c$ , voltage  $V$  and current ripple  $\Delta I$  (pk-pk)

## 7.2. Area product

### 7.2.1. Low frequency – low ripple formulation for filtering inductors

In low-frequency applications and assuming linear behavior right to the point of saturation, the flux density limit is related to the saturation of the material:

$$B_{sat} = \frac{L\hat{I}}{n_t \cdot A_c} \quad [7.6]$$

and the current density in the winding must be limited to limit Joule loss density:

$$j_{RMS} = \frac{n_t \cdot I_{RMSeq}}{k_w \cdot A_w} \quad [7.7]$$

These two equations combine to form an area product that is independent of the number of turns and is generally used to determine directly if a core is appropriate for the target application:

$$A_w \cdot A_c = L \cdot \hat{I} \cdot \frac{I_{RMSeq}}{B_{sat} k_w j_{RMS}} \quad [7.8]$$

However, when chopper filtering is the application, inductance, peak and RMS currents are linked and this product can be rewritten as a function of the normalized current ripple, which is one of the degrees of freedom available to the designer:

$$L = \frac{V}{4\Delta I \cdot f_{sw}} \quad [7.9]$$

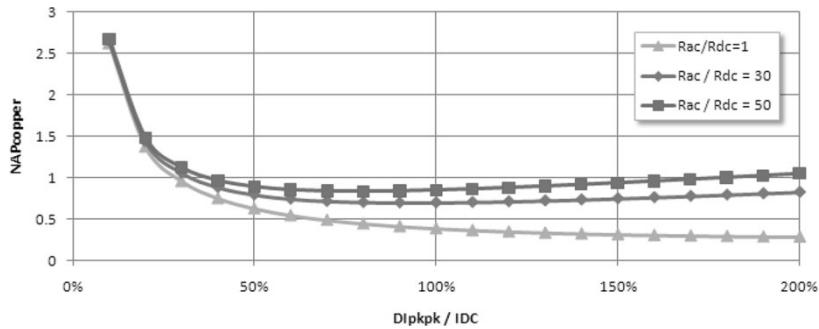
$$\hat{I} = I_{DC} \cdot \left( 1 + \frac{\Delta I}{2I_{DC}} \right) \quad [7.10]$$

Combining equations [7.4] and [7.6]–[7.10], we obtain:

$$A_w \cdot A_c = \frac{V \cdot I_{DC} \cdot \left( 1 + \frac{\Delta I}{2I_{DC}} \right) \cdot \sqrt{1 + \frac{R_{AC}(f_{sw})}{R_{DC}} \frac{1}{12} \left( \frac{\Delta I}{I_{DC}} \right)^2}}{4(\Delta I / I_{DC}) \cdot f_{sw} \cdot B_{sat} \cdot k_w \cdot j_{RMS}} \quad [7.11]$$

or in a normalized form that enables plotting (Figure 7.3):

$$\begin{aligned} NAP^{copper} &= \frac{A_c \cdot A_w \cdot B_{sat} \cdot f_{sw} \cdot k_w \cdot j_{RMS}}{V \cdot I_{DC}} \\ &= \frac{1}{8} \left( 1 + \frac{2}{\Delta I / I_{DC}} \right) \cdot \sqrt{1 + \frac{R_{AC}(f_{sw})}{R_{DC}} \frac{1}{12} \left( \frac{\Delta I}{I_{DC}} \right)^2} \end{aligned} \quad [7.12]$$



**Figure 7.3.** Normalized area product versus  $pk-pk$  current ripple  $\Delta I$ . For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

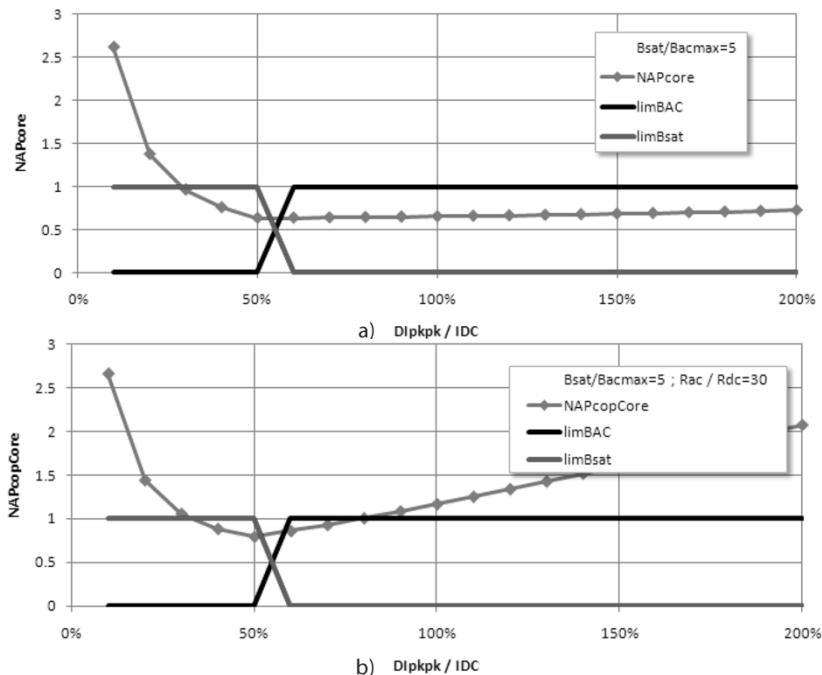
### 7.2.2. General formulation for filtering inductors

When the switching frequency or the current ripple is increased, the AC induction must be limited to maintain core losses at an acceptable level. AC flux density is indeed a function of the normalized current ripple:

$$B_{AC} = \frac{\Phi_{AC}}{\Phi_{AC} + \Phi_{DC}} \cdot \hat{B} = \frac{\hat{B}}{1 + \Phi_{DC}/\Phi_{AC}} = \frac{\hat{B}}{1 + \frac{2}{\Delta I/I_{DC}}} \quad [7.13]$$

The resulting constraint can be introduced in the previous formulation using a *max* function that includes both saturation and loss limits and makes it applicable for design at any frequency:

$$\begin{aligned} NAP_{core}^{cond} &= \frac{A_c \cdot A_w \cdot B_{sat} \cdot f_{sw} \cdot k_w \cdot j_{RMS}}{V \cdot I_{DC}} \\ &= \frac{1}{8} \max \left( 1 + \frac{2}{\Delta I/I_{DC}}; \frac{B_{sat}}{B_{AC \max(f)}} \right) \cdot \sqrt{1 + \frac{R_{AC}(f_{sw})}{R_{DC}} \frac{1}{12} \left( \frac{\Delta I}{I_{DC}} \right)^2} \quad [7.14] \end{aligned}$$



**Figure 7.4.** Normalized area product driven by saturation a) or losses b). For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

### 7.2.3. Application to inductors for interleaved converters

When interleaved converters are considered, the main concern is the total current ripple which is the combination of interleaved current ripples; this AC current is injected in the capacitor and governs the output voltage ripple. The total current ripple of  $n_P$  current ripples phase-shifted by  $360^\circ/n_P$  is divided by  $n_P$ :

$$\Delta I_{tot} = \frac{\Delta I_{ind}}{n_p} \quad [7.15]$$

The DC currents add up:

$$I_{DCtot} = n_p \cdot I_{DCind} \quad [7.16]$$

So, the individual and total relative current ripple are related as:

$$\Rightarrow \frac{\Delta I_{ind}}{I_{DCind}} = \frac{n_p \Delta I_{tot}}{I_{DCtot}/n_p} = \frac{n_p^2 \Delta I_{tot}}{I_{DCtot}} \quad [7.17]$$

Expressing  $A_w \cdot A_c$  as a function of the total current ripple, we obtain:

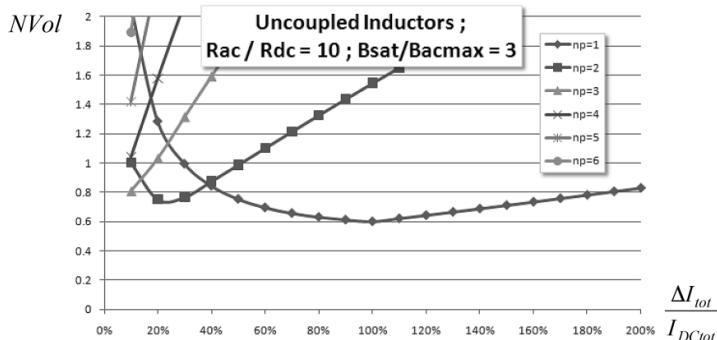
$$A_c \cdot A_w = \frac{V \cdot \frac{I_{DCtot}}{n_p} \cdot \left( \max \left( 1 + \frac{2I_{DCtot}}{n_p^2 \Delta I_{tot}}, \frac{B_{sat}}{B_{AC\max}} \right) \right) \sqrt{1 + \frac{R_{AC}(f_{sw})}{R_{DC}} \frac{1}{12} \left( \frac{n_p^2 \Delta I_{tot}}{I_{DCtot}} \right)^2}}{8B_{sat} \cdot f_{sw} \cdot k_w \cdot j_{RMS}} \quad [7.18]$$

Given that  $A_w \cdot A_c$  is a function of power 4 of the dimensions while volume is a cubic function of these same dimensions, an image of the volume of the  $n_p$  inductors can be obtained for scaled cores:

$$Vol_{tot} = n_p \cdot K_{shape} \left( \frac{V \cdot \frac{I_{DCtot}}{n_p} \cdot \max \left( 1 + \frac{2I_{DCtot}}{n_p^2 \Delta I_{tot}}, \frac{B_{sat}}{B_{AC\max}} \right) \sqrt{1 + \frac{R_{AC}(f_{sw})}{R_{DC}} \frac{1}{12} \left( \frac{n_p^2 \Delta I_{tot}}{I_{DCtot}} \right)^2}}{8B_{sat} \cdot f_{sw} \cdot k_w \cdot j_{RMS}} \right)^{3/4} \quad [7.19]$$

and a normalized expression can be built to plot a dimensionless curve (Figure 7.5):

$$\begin{aligned} NVol_L &= \frac{Vol_{tot}}{K_{shape}} \cdot \left( \frac{B_{sat} \cdot f_{sw} \cdot k_w \cdot j_{RMS}}{V \cdot I_{DCtot}} \right)^{3/4} \\ &= n_p \cdot \left( \frac{1}{8n_p} \cdot \max \left( 1 + \frac{2I_{DCtot}}{n_p^2 \Delta I_{tot}}, \frac{B_{sat}}{B_{AC\max}} \right) \sqrt{1 + \frac{R_{AC}(f_{sw})}{R_{DC}} \frac{1}{12} \left( \frac{n_p^2 \Delta I_{tot}}{I_{DCtot}} \right)^2} \right)^{3/4} \end{aligned} \quad [7.20]$$



**Figure 7.5.** Normalized total volume of filtering inductors for interleaved converters. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

As can be seen from this figure, interleaved converters should be designed with a low total current ripple to minimize the volume of magnetic components. However, it means that a substantial amount of energy is stored in magnetics, and this will be a burden if we want to optimize dynamic performances.

#### 7.2.4. Extension to InterCell Transformers

The operation and design of ICTs is not very different from those of inductors for interleaved converters, except that the currents are coupled, so their ripple is at  $n_p$  times the switching frequency, in phase and add up. As a result, the relation between individual and total current ripple is modified as follows:

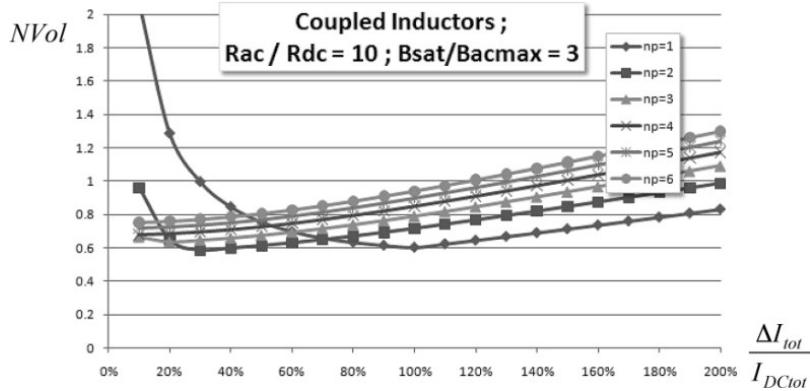
$$\Delta I_{tot} = n_p \Delta I_{ind} \quad [7.21]$$

$$I_{DCtot} = n_p \cdot I_{DCind} \quad [7.22]$$

$$\Rightarrow \frac{\Delta I_{ind}}{I_{DCind}} = \frac{n_p \Delta I_{tot}}{n_p \cdot I_{DCtot}} = \frac{\Delta I_{tot}}{I_{DCtot}} \quad [7.23]$$

The area product, volume and normalized volume are derived in the same way as for inductors:

$$A_c \cdot A_w = \frac{V \cdot \frac{I_{DCtot}}{n_p} \cdot \left( \max \left( 1 + \frac{2I_{DCtot}}{n_p^2 \Delta I_{tot}}; \frac{B_{sat}}{B_{ACmax}} \right) \right) \sqrt{1 + \frac{R_{AC}(n_p f_{sw})}{R_{DC}} \frac{1}{12} \left( \frac{\Delta I_{tot}}{I_{DCtot}} \right)^2}}{8B_{sat} f_{sw} k_w j_{RMS}} \quad [7.24]$$



**Figure 7.6.** Normalized total volume of ICTs for interleaved converters. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

$$Vol_{tot} = n_p \cdot K_{shape} \left( \frac{V \cdot \frac{I_{DCtot}}{n_p} \cdot \max \left( 1 + \frac{2I_{DCtot}}{n_p^2 \Delta I_{tot}}; \frac{B_{sat}}{B_{ACmax}} \right) \sqrt{1 + \frac{R_{AC}(n_p f_{sw})}{R_{DC}} \frac{1}{12} \left( \frac{\Delta I_{tot}}{I_{DCtot}} \right)^2}}{8B_{sat} f_{sw} k_w j_{RMS}} \right)^{3/4} \quad [7.25]$$

$$\begin{aligned} NVol_{ICT} &= \frac{Vol_{tot}}{K_{shape}} \cdot \left( \frac{B_{sat} f_{sw} k_w j_{RMS}}{V I_{DCtot}} \right)^{3/4} \\ &= n_p \cdot \left( \frac{1}{8n_p} \cdot \max \left( 1 + \frac{2I_{DCtot}}{n_p^2 \Delta I_{tot}}; \frac{B_{sat}}{B_{ACmax}} \right) \sqrt{1 + \frac{R_{AC}(n_p f_{sw})}{R_{DC}} \frac{1}{12} \left( \frac{\Delta I_{tot}}{I_{DCtot}} \right)^2} \right)^{3/4} \end{aligned} \quad [7.26]$$

### 7.3. Optimal area product of magnetic components for interleaved converters

#### 7.3.1. Optimal area product for inductors

The volume of [7.25] can be rewritten as:

$$\text{volume}_{LV}^L = K_1 \left( \max \left( 1 + \frac{a}{\chi}, b \right) \cdot \sqrt{1 + c \chi^2} \right)^{3/4}$$

with  $\begin{cases} K_1 = n_p K_{shape}^L \left( \frac{V_{HV} \cdot I_{DC}^{LV}}{8n_s^2 \cdot n_p \cdot f_{sw} \cdot B_{sat} \cdot k_w \cdot j_{eff}} \right)^{3/4} \\ \chi = \frac{\Delta I_{LV}^{pkpk}}{I_{DC}^{LV}} \quad a = \frac{2}{n_p^2} \quad b = \frac{B_{sat}}{B_{AC \max}} \quad c = \frac{R_{AC @ n_s f_{sw}}}{12 R_{DC}} n_p^4 \end{cases}$  [7.27]

From this expression, it can be seen that finding the current ripple resulting in the smallest volume amounts to finding the minimum of:

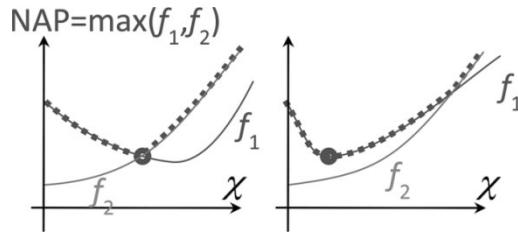
$$\begin{aligned} f(\chi) &= \max \left( 1 + \frac{a}{\chi}; b \right) \sqrt{1 + c \chi^2} \\ &= \max \left( \left( 1 + \frac{a}{\chi} \right) \sqrt{1 + c \chi^2}; b \sqrt{1 + c \chi^2} \right) = \max(f_1(\chi); f_2(\chi)) \end{aligned} \quad [7.28]$$

–  $f_1(\chi)$  tends to  $+\infty$  when  $\chi$  tends to  $0_+$  and tends to  $+\infty$  when  $\chi$  tends to  $+\infty$ , so it has a minimum;

–  $f_2(\chi)$  is monotonously increasing.

So, we have two cases as shown in Figure 7.7 and we can see that  $\max(f_1(\chi), f_2(\chi))$  has a minimum at:

$$\chi_{\min(f)} = \min \left( \chi_{\min(f_1)}, \chi_{\text{Xing}(f_1, f_2)} \right) \quad [7.29]$$



**Figure 7.7.** Two cases for  $f_1$  and  $f_2$ . For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

The derivative of  $f_1$  is:

$$\begin{aligned} \frac{df_1}{d\chi} &= \left(1 + \frac{a}{\chi}\right) \cdot \frac{1}{2} 2c\chi \cdot \frac{1}{\sqrt{1+c.\chi^2}} - \frac{a}{\chi^2} \sqrt{1+c.\chi^2} \\ &= \frac{c\chi + ca}{\sqrt{1+c.\chi^2}} - \frac{a}{\chi^2} \sqrt{1+c.\chi^2} = \frac{c\chi^3 + ca\chi^2 - a - ac\chi^2}{\chi^2 \sqrt{1+c.\chi^2}} = \frac{c\chi^3 - a}{\chi^2 \sqrt{1+c.\chi^2}} \end{aligned} \quad [7.30]$$

So, the minimum of  $f_1$  is at:

$$\chi_{\min(f_1)} = \sqrt[3]{\frac{a}{c}} \quad [7.31]$$

The crossing of  $f_1$  and  $f_2$  is found as follows:

$$\left(1 + \frac{a}{\chi}\right) \sqrt{1+c.\chi^2} = b \sqrt{1+c.\chi^2} \Leftrightarrow \chi_{Xing(f_1,f_2)} = \frac{a}{b-1} \quad [7.32]$$

Finally, the equation of the current ripple giving the minimum volume of inductors is:

$$\chi_{\min Vol} = \min \left( \frac{1}{n_P^2} \sqrt[3]{\frac{24}{R_{AC@n_s f_{sw}} / R_{DC}}} ; \frac{2}{n_P^2} \frac{1}{\frac{B_{sat}}{B_{AC \max}} - 1} \right) \quad [7.33]$$

### 7.3.2. Optimal area product for InterCell Transformers

The expression of the total volume of an ICT is of the same form with only coefficient  $K_1$  and  $c$  changed for  $K'_1$  and  $c'$  respectively:

$$\text{Volume } V_{ICT} = K'_1 \left( \max \left( 1 + \frac{a}{\chi}, b \right) \cdot \sqrt{1 + c' \chi^2} \right)^{3/4} \text{ with } \begin{cases} K'_1 = K_1 \cdot \frac{K_{shape}^{ICT}}{K_{shape}^L} \\ c' = \frac{R_{AC} @ n_s n_p f_{sw}}{12 R_{DC}} \end{cases} \quad [7.34]$$

Following the same process, we obtain the current ripple giving the minimum volume of an ICT:

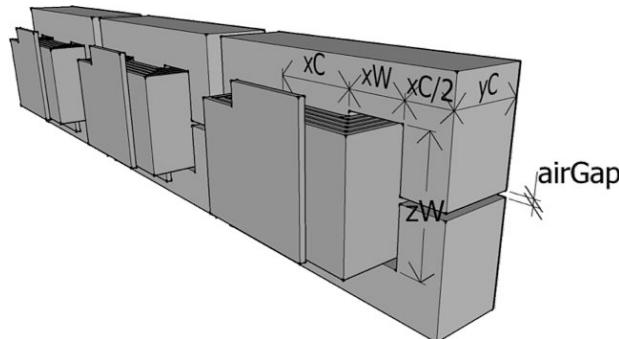
$$\chi_{minVolICT} = \min \left( \frac{1}{n_P^{2/3}} \sqrt[3]{\frac{24}{R_{AC} n_s n_p f_{sw} / R_{DC}}} ; \frac{2}{n_P^2} \frac{1}{\frac{B_{sat}}{B_{AC \max}} - 1} \right) \quad [7.35]$$

## 7.4. Weight-optimal dimensions for a given area product

### 7.4.1. For inductors

When the area product is defined, there are still multiple degrees of freedom to design magnetic components. When using scaled cores, most degrees of freedoms are lost; the area product directly imposes the winding area which, combined with the current density, imposes the number of turns. The air gap is left as the sole remaining degree of freedom that allows tuning the inductor to the specified value (this tuning giving implicitly the appropriate flux density). The following design process shows how the degrees of freedom can be used independently to minimize the weight of the component. It should be noted that this process can be applied irrespective of the way the area product has been

determined; even, and it is probably more important in this case, if the area product has not been minimized (e.g. a certain value of inductance was imposed by considerations other than minimization of magnetics weight), it can be interesting to choose dimensions that minimize the weight *for this given non-optimal area product.*



**Figure 7.8.** Definition of characteristic dimensions. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

The weight of the magnetic device is:

$$\begin{aligned} \text{weight} = & ((2x_C + 2x_W) \cdot y_C \cdot (z_W + x_C) - 2x_W \cdot y_C \cdot z_W) \cdot \rho_{mag} \\ & + ((x_C + 2x_W) \cdot (y_C + 2x_W) \cdot z_W - x_C \cdot y_C \cdot z_W) \cdot k_W \cdot \rho_{cond} \end{aligned} \quad [7.36]$$

Using symbolic calculation in Matlab, we find analytic expression for  $x_C$  and  $x_W$  that minimize weight [WEI 14]:

$$x_W = \sqrt{\frac{A_W \cdot A_C \cdot \rho_{mag}}{2 \cdot k_W \cdot \rho_{cond} \cdot A_W^2 + A_W \cdot A_C \cdot \rho_{mag}}} \quad [7.37]$$

$$x_C = \sqrt{\frac{A_W \cdot A_C \cdot k_W \cdot \rho_{cond}}{k_W \cdot \rho_{cond} \cdot A_W^2 + A_W \cdot A_C \cdot \rho_{mag}}} \quad [7.38]$$

This permits us to eliminate 2 of the 3 degrees of freedom (four dimensions with imposed product) but searching for an analytic expression for the last degree of freedom fails. With only one degree of freedom left, it is however possible to plot the evolution of the weight versus the last degree of freedom. This is done in Figure 7.9 using  $A_w$  as the last degree of freedom ( $x$ -axis); a family of curves corresponding to different density ratios are plotted to show that the minimum weight is obtained for different values of  $A_w$ . The interpretation of this is easily understandable: when the conductors' density is smaller,  $A_w$  should be made smaller (smaller number of turns), and vice versa.

Processing these data, it is possible to locate the minimum of each curve numerically. The corresponding  $A_w^{opt}$  is plotted in Figure 7.10 together with an obvious fit (it is suspected that the values  $A_w^{opt}$  align perfectly in log-log space and that deviations are only due to numerical errors):

$$A_w^{opt} = 0.83\sqrt{A_w \cdot A_C} \cdot \left( \frac{\rho_{mag}}{k_w \cdot \rho_{cond}} \right)^{0.46} \quad [7.39]$$

Combining this numerical fit of  $A_w^{opt}$  with the analytic expressions of  $x_C^{opt}$  and  $x_W^{opt}$ , we can get analytic expressions of the optimal values of all dimensions, but plotting the optimal dimensions in log-log coordinates shows that a simple curve fit is probably more convenient and very accurate (Figure 7.11).

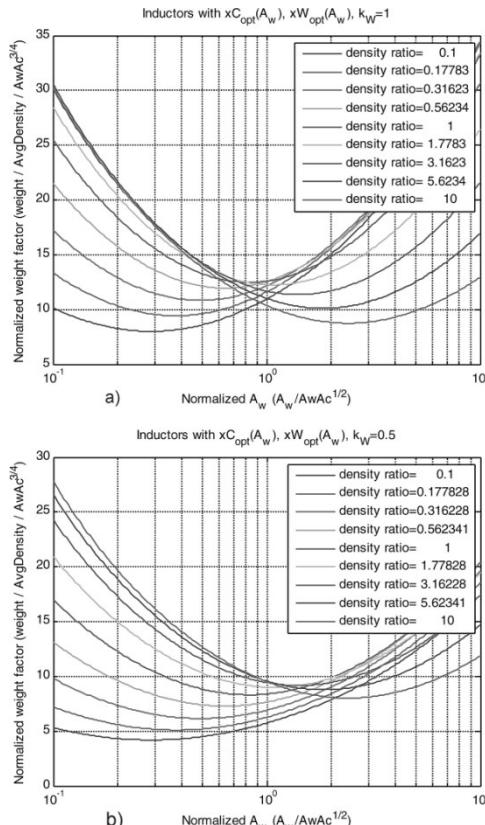
As a result, the optimal dimensions are as follows:

$$x_C = 0.69947 \cdot \sqrt[4]{A_w A_C} \cdot \left( \frac{\rho_{mag}}{k_w \cdot \rho_{cond}} \right)^{-0.2539} \quad [7.40]$$

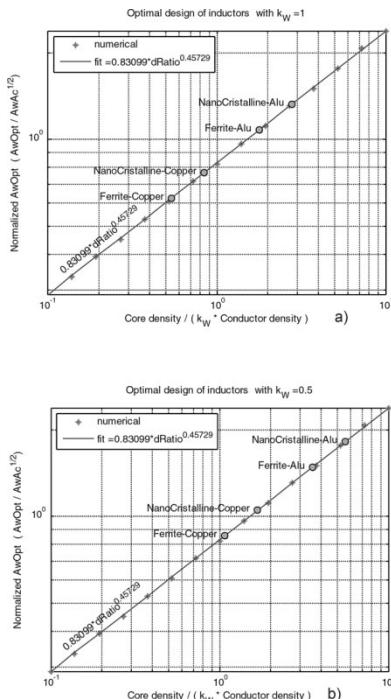
$$y_C = 1.7204 \cdot \sqrt[4]{A_W A_C} \cdot \left( \frac{\rho_{mag}}{k_W \cdot \rho_{cond}} \right)^{-0.20339} \quad [7.41]$$

$$x_W = 0.58937 \cdot \sqrt[4]{A_W A_C} \cdot \left( \frac{\rho_{mag}}{k_W \cdot \rho_{cond}} \right)^{0.25341} \quad [7.42]$$

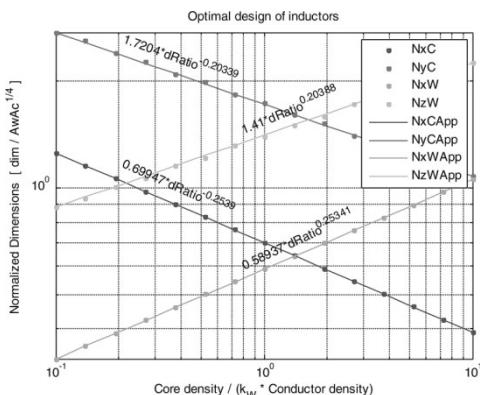
$$z_W = 1.41 \cdot \sqrt[4]{A_W A_C} \cdot \left( \frac{\rho_{mag}}{k_W \cdot \rho_{cond}} \right)^{0.20388} \quad [7.43]$$



**Figure 7.9.** Weight versus winding area at different density ratios: a)  $k_W = 1.0$  and b)  $k_W = 0.5$ . For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

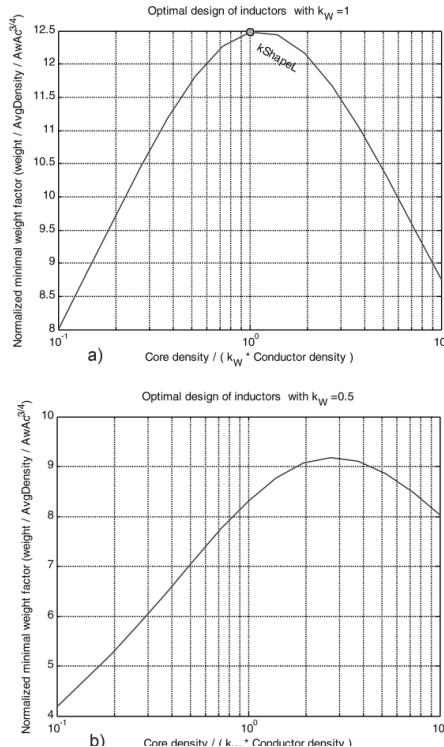


**Figure 7.10.** Normalized optimal winding area of filtering inductors:  
a)  $k_W = 1.0$  and b)  $k_W = 0.5$ . For a color version of the figure, see  
[www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)



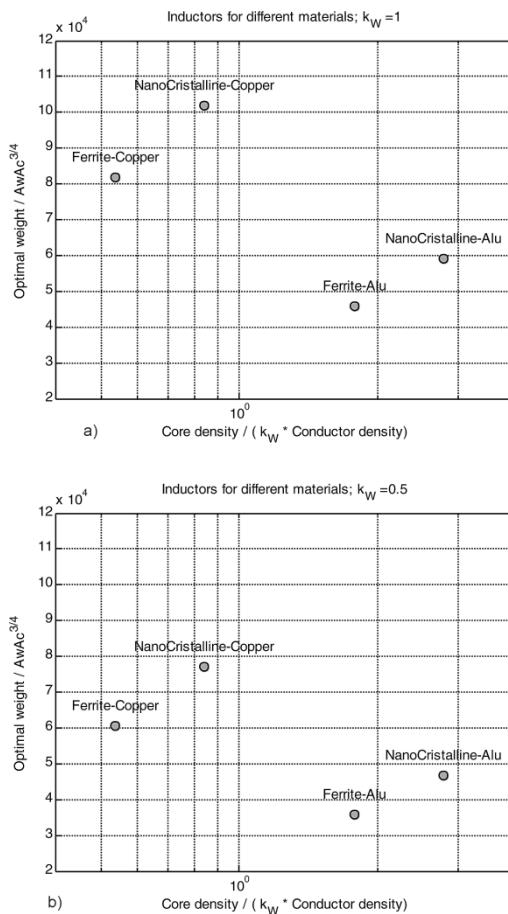
**Figure 7.11.** Normalized optimal dimensions of filtering inductors. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

It is also interesting to plot the evolution of the optimal weight as a function of the ratio of densities *for a constant sum of the densities*. This is done in Figure 7.12 and shows that it is better to have materials with different densities to modify the proportion of magnetic and conducting materials and take advantage of the lightest material.



**Figure 7.12.** Normalized optimal weight versus density ratio: a)  $k_W = 1.0$  and b)  $k_W = 0.5$

With this approach, we can also represent the influence of the choice of several couples of existing materials (Figure 7.13); the normalized minimal weight factor of these couples is a consequence of the density of each material, but as said previously, it is also influenced by the difference of these densities.



**Figure 7.13.** Weight coefficient for different combinations of materials: a)  $k_W = 1.0$  and b)  $k_W = 0.5$

#### 7.4.2. For InterCell Transformers

In terms of weight for a given  $A_{uw}A_c$ , the difference between inductors and ICTs is that the optimal section of the return leg can be reduced or even taken to zero and, to a lesser extent, that the optimal section of horizontal legs may be slightly modified. Exact answers to both these questions are complicated because they involve not only flux

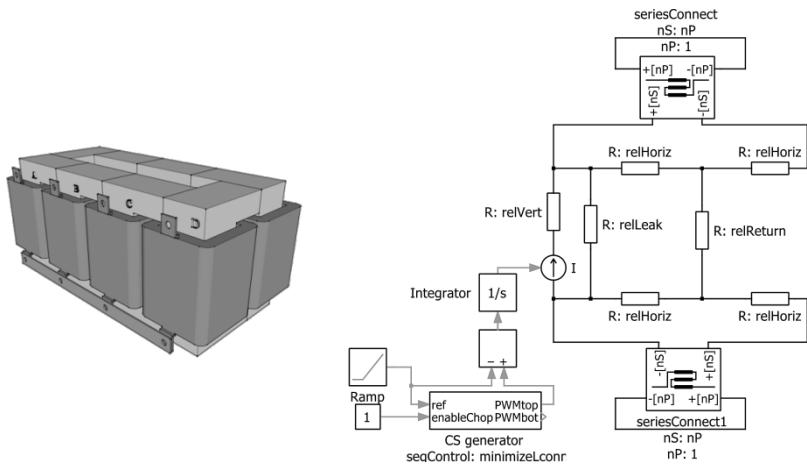
combinations resulting from optimal phase sequence (different expressions for numbers of phases that are odd, even non-multiples of 4 or even and multiples of 4, particular cases for two and four phases, etc.), but also from leakage reluctances corresponding to fluxes distributed in the air, and proportion of reluctances of vertical and horizontal legs.

Since our aim is to provide engineering insight and obtain a relatively simple design process, we will briefly discuss the particular cases and look for simplified expressions that can be used for design.

#### 7.4.2.1. *Flux and section of horizontal legs*

Fluxes in horizontal legs have been studied in [FOR 07] and an optimal phase sequence has been proposed to minimize the amplitude of the fundamental of these fluxes. We will show here how this translates in terms of peak and peak-peak values in the practical case of triangular fluxes in the windings.

As explained in this chapter, in steady state, the DC voltage across each winding is zero and a square AC voltage is imposed by the external circuit so that each winding behaves as a triangular flux source. These flux sources are interconnected via a reluctance network such as the one in Figure 7.14. In practice, the distribution of the fluxes in this meshed network is almost independent of the values of the reluctances; core reluctances and air reluctances can be several orders of magnitude apart, and it can be assumed that the sum of the forced winding fluxes distributes evenly among the air return paths, which directly imposes the fluxes in all core legs. In the following developments, we will use this assumption, but the PLECS models [FLU 14a, FLU 14b] used in this section to quantify horizontal fluxes can also be tuned to account for imbalance or the influence of core reluctances if needed.



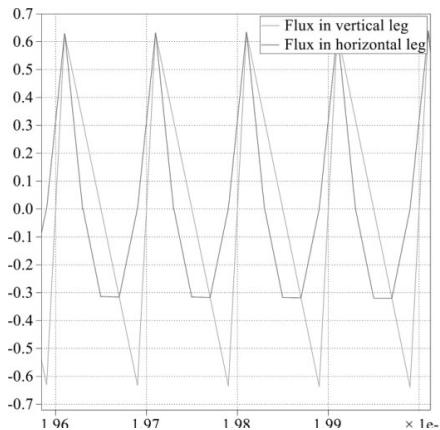
**Figure 7.14.** Monolithic ICT and its vectorized reluctance model

A preliminary remark must be made concerning the waveforms of horizontal fluxes. Despite the symmetry of winding fluxes (in particular, maximum and minimum symmetrical with respect to the average value), the horizontal fluxes can be asymmetric as shown in Figure 7.15; it can be seen that the positive and negative extrema of the horizontal flux are not opposite although the average value is zero. For this reason, we need to characterize the evolution of two quantities that are not trivially related: the peak value which is needed with respect to saturation and the peak-peak value which is related to the loss density.

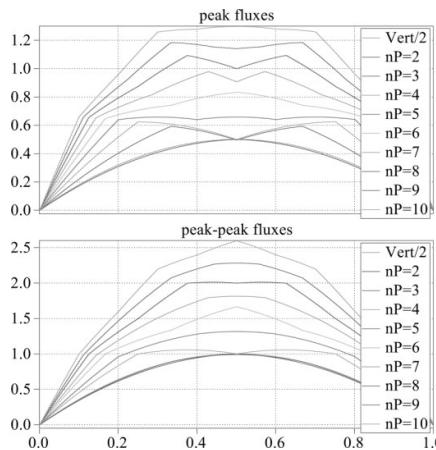
We will first study the case of a standard phase sequence:  $0^\circ$ ,  $360^\circ/n_P$ ,  $2*360^\circ/n_P$ , etc.

In Figure 7.16, the evolution of the ratio of horizontal to vertical flux is given for a standard phase sequence  $0^\circ$ ,  $360^\circ/n_P$ ,  $2*360^\circ/n_P$ , etc. In both graphs, the lowest curve is the superposition of half the value of the vertical flux (directly forced by the winding) and the curve corresponding to  $n_P = 2$ ; and then we can see that the curves corresponding to increasing values of  $n_P$  are sequentially disposed with a

general tendency to increase. As will be shown later, these values strongly influence the section needed for the horizontal legs, and having maximal values for  $n_P = 10$  as high as 2.5 times that of  $n_P = 2$  shows that the standard sequence is incompatible with high numbers of cells.

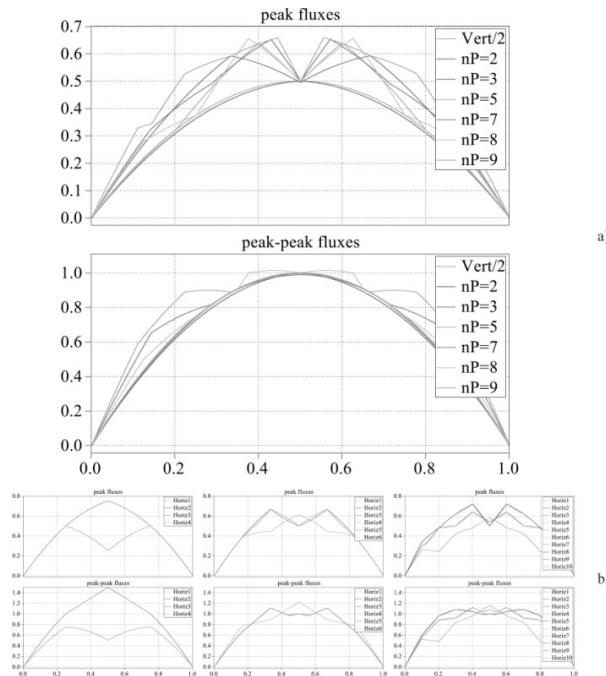


**Figure 7.15.** Example of flux waveforms in a five-cell IGBT. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)



**Figure 7.16.** Evolution of normalized peak and peak-peak fluxes in horizontal legs versus duty cycle (standard phase sequence). For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

In Figure 7.17, the curves corresponding to the optimal sequence are given. Because of arithmetic properties, when  $n_P = 4$  or any even number non-multiple of 4, we have  $n$  couples of neighbor windings, each couple has a phase difference between its two windings, these  $n$  differences cannot all be the same and the horizontal fluxes in different legs can be different. Compared to previous values, there is a clear reduction of both values for  $n_P \geq 5$ , the benefit increasing with  $n_P$ . However, for  $n_P = 2$  or 3, there is no improvement because the sequence cannot be changed, and when  $n_P = 4$ , there is no clear gain; because of disparities, the optimal sequence would require a special core with horizontal legs of different sections, and even then no clear advantage can be claimed.



**Figure 7.17.** Evolution of normalized peak and peak-peak fluxes in horizontal legs versus duty cycle (optimal phase sequence):  
a)  $n_P = 2, 3, 5, 7, 9$  and b)  $n_P = 4, 6, 10$ . For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

$n_P$	2	3	4	5	6	7	8	9	10
<b>Standard sequence</b>	<b>1.000</b>	<b>1.186</b>	<b>1.25</b>	<b>1.316</b>	<b>1.666</b>	<b>1.958</b>	<b>2.186</b>	<b>2.37</b>	<b>2.598</b>
<b>Optimal sequence</b>	<b>1.000</b>	<b>1.186</b>	<b>1.50 (2x)</b> <b>1.00 (2x)</b>	<b>1.28</b>	<b>1.334 (4x)</b> <b>1.222 (2x)</b>	<b>1.306</b>	<b>1.312</b>	<b>1.318</b>	<b>1.44 (4x)</b> <b>1.28 (4x)</b> <b>1.16 (2x)</b>

**Table 7.2.** Normalized horizontal peak flux versus duty cycle

$n_P$	2	3	4	5	6	7	8	9	10
<b>Standard Sequence</b>	<b>1.000</b>	<b>1.000</b>	<b>1.056</b>	<b>1.316</b>	<b>1.665</b>	<b>1.81</b>	<b>2.012</b>	<b>2.281</b>	<b>2.596</b>
<b>Optimal sequence</b>	<b>1.000</b>	<b>1.000</b>	<b>1.500 (2x)</b> <b>0.750 (2x)</b>	<b>1.000</b>	<b>1.221 (2x)</b> <b>1.111 (4x)</b>	<b>1.00</b>	<b>1.000</b>	<b>1.000</b>	<b>1.159 (2x)</b> <b>1.119 (4x)</b> <b>1.075 (2x)</b> <b>1.065 (2x)</b>

**Table 7.3.** Normalized horizontal peak-peak flux versus duty cycle

Knowing how vertical AC fluxes translate to horizontal fluxes, we can determine the sections of the horizontal and

return legs and optimize the weight of the ICT as follows. Because of the definition of  $\chi$ , the (DC|pk|pkpk) proportion of flux density in the return legs is  $(1|\chi/2|\chi)$ , and due to interleaving in the vertical legs, it will be  $(1|\chi n_p^2/2|\chi n_p^2)$ . Saturation and loss limits can thus be expressed as:

$$\left\{ \begin{array}{l} B_{sat} \geq K \cdot \frac{1 + \frac{\chi}{2} \cdot n_p^2}{a_{vert}} \\ B_{AC\max} \geq K \cdot \frac{\chi \cdot n_p^2}{a_{vert}} \end{array} \right. \quad [7.44]$$

where  $K$  is a constant that does not need to be expressed to derive the following requirement fulfilled by  $a_{vert}$ :

$$\begin{aligned} a_{vert} &= K \cdot \max \left( \frac{1 + \frac{\chi}{2} \cdot n_p^2}{B_{sat}}, \frac{\chi \cdot n_p^2}{B_{AC\max}} \right) \\ &= \frac{K}{B_{sat}} \max \left( 1 + \frac{\chi}{2} \cdot n_p^2, \chi \cdot n_p^2 \cdot \frac{B_{sat}}{B_{AC\max}} \right) \end{aligned} \quad [7.45]$$

Using the same representation, the flux components in the horizontal legs are  $(1/2 | k_{pk}\chi n_p^2 / 4 | k_{pkpk}\chi n_p^2 / 2)$ , with  $k_{pk}$  and  $k_{pkpk}$ , the values in Tables 7.2 and 7.3, respectively. And since the horizontal leg is made up of the same material as the vertical, we can derive from the previous equation the requirement for  $a_{horiz}$ , the section of horizontal legs:

$$a_{horiz} = \frac{K}{B_{sat}} \max \left( \frac{1}{2} + k_{pk} \cdot \frac{\chi}{4} \cdot n_p^2, k_{pkpk} \cdot \frac{\chi}{2} \cdot n_p^2 \cdot \frac{B_{sat}}{B_{AC\max}} \right) \quad [7.46]$$

Now, substituting for  $K/B_{sat}$ , we get the section of the horizontal leg:

$$a_{horiz} = a_{vert} \frac{\max\left(\frac{1}{2} + k_{pk} \cdot \frac{\chi}{4} \cdot n_p^2, k_{pkpk} \cdot \frac{\chi}{2} \cdot n_p^2 \cdot \frac{B_{sat}}{B_{AC\max}}\right)}{\max\left(1 + \frac{\chi}{2} \cdot n_p^2, \chi \cdot n_p^2 \cdot \frac{B_{sat}}{B_{AC\max}}\right)} \quad [7.47]$$

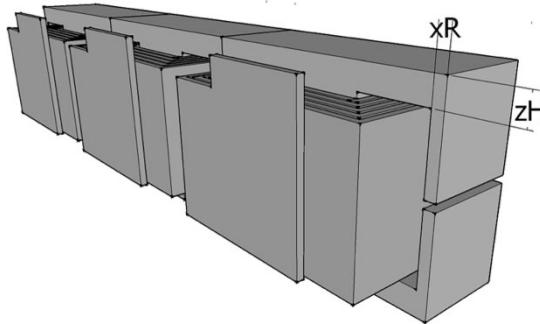
As stated previously, the flux components in return legs are  $(1 | \chi/2 | \chi)$ , so we can write directly the expression of  $a_{return}$ , their section:

$$a_{return} = a_{vert} \cdot \frac{\max\left(1 + \frac{\chi}{2}, \chi \cdot \frac{B_{sat}}{B_{AC\max}}\right)}{\max\left(1 + \frac{\chi}{2} \cdot n_p^2, \chi \cdot n_p^2 \cdot \frac{B_{sat}}{B_{AC\max}}\right)} \quad [7.48]$$

In high-frequency applications, the design is mainly governed by core losses, so we can see that  $a_{return}$  would in this case be divided by  $n_p^2$  and this without taking leakage flux into account. Under such circumstances, removing the return legs can be an option to consider as soon as  $n_p$  is greater than or equal to 5, for example, but to check the viability of this option, a good estimate of the leakage flux is required, which is not an easy problem.

#### 7.4.2.2. Determination of optimal dimensions

It has been shown in the previous section that the sections of horizontal and return legs can be expressed as functions of design parameters, and considering the shape of the ICT, we now have a 3D geometry defined by the same four quantities as for the inductors ( $x_c$ ,  $y_c$ ,  $x_w$  and  $z_w$  defined in Figure 7.8) plus two new parameters  $z_H$  and  $x_R$  defined in Figure 7.18.



**Figure 7.18.** Extra parameters for the definition of ICT geometry

Respecting this geometry and section ratios defined by [7.47] and [7.48], it can be seen that  $z_H$  and  $x_R$  are related to  $x_C$  by means of two constants  $K_{z_H}$  and  $K_{x_R}$  which are imposed by the design parameters:

$$z_H = x_C \frac{\max\left(\frac{1}{2} + k_{pk} \cdot \frac{\chi}{4} \cdot n_p^2 - k_{pkpk} \cdot \frac{\chi}{2} \cdot n_p^2 \cdot \frac{B_{sat}}{B_{AC\max}}\right)}{\max\left(1 + \frac{\chi}{2} \cdot n_p^2 - \chi \cdot n_p^2 \cdot \frac{B_{sat}}{B_{AC\max}}\right)} = K_{z_H} \cdot x_C \quad [7.49]$$

$$x_R = x_C \cdot \frac{\max\left(1 + \frac{\chi}{2} - \chi \cdot \frac{B_{sat}}{B_{AC\max}}\right)}{\max\left(1 + \frac{\chi}{2} \cdot n_p^2 - \chi \cdot n_p^2 \cdot \frac{B_{sat}}{B_{AC\max}}\right)} = K_{x_R} \cdot x_C \quad [7.50]$$

The per phase weight of the magnetic device is now given by:

$$\begin{aligned} weight = & \left( \left( x_C \cdot \left( 1 + K_{x_R} \right) + 2x_w \right) \cdot y_C \cdot \left( z_w + 2K_{z_H} x_C \right) - 2x_w \cdot y_C \cdot z_w \right) \cdot \rho_{mag} \\ & + \left( \left( x_C + 2x_w \right) \cdot \left( y_C + 2x_w \right) z_w - x_C \cdot y_C \cdot z_w \right) k_w \cdot \rho_{cond} \end{aligned} \quad [7.51]$$

Using symbolic calculation in Matlab, analytic expressions for  $x_C$  and  $x_W$  that minimize the weight of the ICT can be found [WEI 14]:

$$x_W = \sqrt{\frac{A_W \cdot A_W \cdot A_C \cdot (K_{x_R} + 1) \cdot \rho_{mag}}{4(A_W^2 \cdot k_W \cdot \rho_{cond} + K_{z_H} \cdot A_W \cdot A_C \cdot \rho_{mag})}} \quad [7.52]$$

$$x_C = \sqrt{\frac{A_W \cdot A_W \cdot A_C \cdot k_W \cdot \rho_{cond}}{A_W^2 \cdot k_W \cdot \rho_{cond} + A_W \cdot A_C \cdot K_{z_H} \cdot (K_{x_R} + 1) \cdot \rho_{mag}}} \quad [7.53]$$

These expressions are general and allow us to describe the case of the inductor by taking  $K_{x_R} = 1$  and  $K_{z_H} = 1/2$ . In the case of ICTs, we may need to use slightly higher values for  $K_{z_H}$  (slightly thicker horizontal legs) and lower values for  $K_{x_R}$  (hopefully, no return leg at all), and the exact values are directly derived from [7.49] and [7.50]:

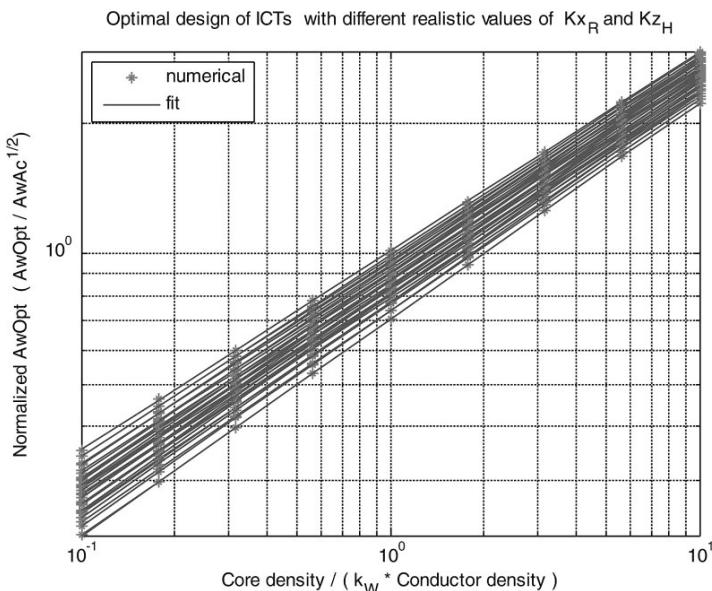
$$K_{z_H} = \frac{\max\left(\frac{1}{2} + k_{pk} \cdot \frac{\chi}{4} \cdot n_P^2, k_{pkpk} \cdot \frac{\chi}{2} \cdot n_P^2 \cdot \frac{B_{sat}}{B_{AC\max}}\right)}{\max\left(1 + \frac{\chi}{2} \cdot n_P^2, \chi \cdot n_P^2 \cdot \frac{B_{sat}}{B_{AC\max}}\right)} \quad [7.54]$$

and

$$K_{x_R} = \frac{\max\left(1 + \frac{\chi}{2}, \chi \cdot \frac{B_{sat}}{B_{AC\max}}\right)}{\max\left(1 + \frac{\chi}{2} \cdot n_P^2, \chi \cdot n_P^2 \cdot \frac{B_{sat}}{B_{AC\max}}\right)} \quad [7.55]$$

However, no analytic formula has been found for  $A_w$ , so we have to handle the last degree of freedom numerically. A parametric sweep on the relative densities of magnetic and conductor materials can be made to observe the evolution of

the four characteristic dimensions of the ICT; this is shown in Figure 7.19 for different values of parameters  $K_{z_H}$  and  $K_{x_R}$ . It can be seen that the winding area evolves on straight lines in a log-log scale which remain almost parallel when  $K_{z_H}$  and  $K_{x_R}$  vary, which suggests a fitting of the form  $kX^\alpha$  with  $\alpha$  almost constant.



**Figure 7.19.** Optimal winding area of an ICT. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

Empirical expressions of the form  $k.X^\alpha$  are automatically found for the optimal curve of each set of parameters  $(K_{z_H}, K_{x_R})$ . Coefficients  $k$  and  $\alpha$  are then related to  $K_{z_H}$  and  $K_{x_R}$  by simple fits and intermediate results of this process are shown in Figure 7.20. Two approximations of the optimal value of  $Aw$  are then proposed, the first one, simpler with accuracy  $\xi$  better than 2.5%, the second, more complicated

with accuracy better than 0.8% (accuracy defined as worst error on  $A_W^{opt}$  over the full range of parameters  $(k_w, K_{z_H}, K_{x_R}) \in [0.5; 1] \times [0.5; 0.75] \times [0; 1]$ ):

$$\xi < 2.5\% \Rightarrow \begin{cases} k_{A_W} = 0.361 + 0.695.K_{z_H} + 0.136K_{x_R} \\ \alpha_{A_W} = 0.498 - 0.0398.K_{x_R} \end{cases} \quad [7.56]$$

$$\xi < 0.8\% \Rightarrow \begin{cases} k_{A_W} = 0.389 + 0.640.K_{z_H} + 0.114K_{x_R} + 0.110.K_{z_H}.K_{x_R} \\ \alpha_{A_W} = 0.500 - 0.0539.K_{x_R} + 0.0141.K_{x_R}^2 \end{cases} \quad [7.57]$$

These parameters can then be used to derive the optimal winding area:

$$A_W^{opt} = k_{A_W} \cdot (A_W A_C)^{1/4} \left( \frac{\rho_{mag}}{k_w \cdot \rho_{cond}} \right)^{\alpha_{A_W}} \quad [7.58]$$

When  $A_W^{opt}$  is known, the analytic expression of the optima [7.52] and [7.53] can be used to obtain  $x_C^{opt}$  and  $x_W^{opt}$ , and the full geometry is then known since:

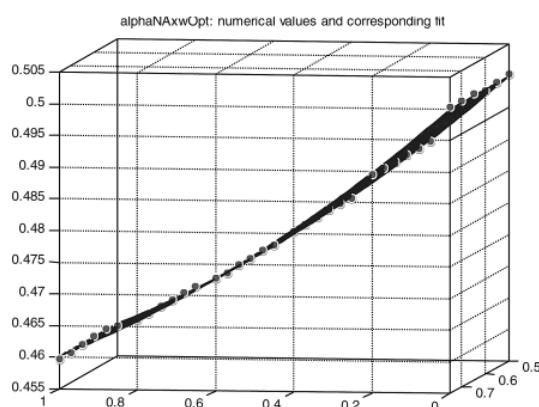
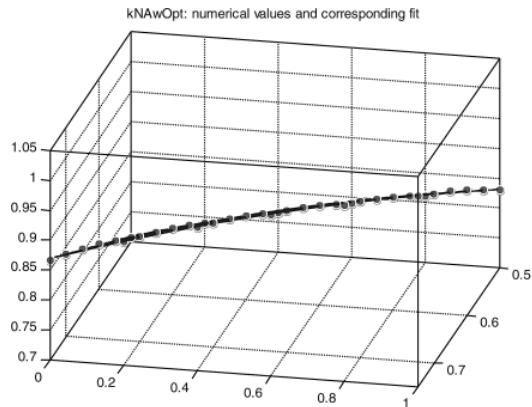
$$\begin{cases} z_W^{opt} = \frac{A_W^{opt}}{x_W^{opt}} \\ y_C^{opt} = \frac{A_C^{opt}}{x_C^{opt}} = \frac{A_W A_C}{A_C^{opt} x_C^{opt}} \end{cases} \quad [7.59]$$

## 7.5. Volume-optimal dimensions for a given area product

It should be noted that the weight optimization described in this section translates into a volume optimization process by using fictitious densities of 1 for both materials' densities.

For example, we can see in Figure 7.12 that the optimal volume of inductors for interleaved converters can be expressed as:

$$Vol_{opt} \approx 12.5 \cdot (A_W \cdot A_C)^{3/4} \quad [7.60]$$



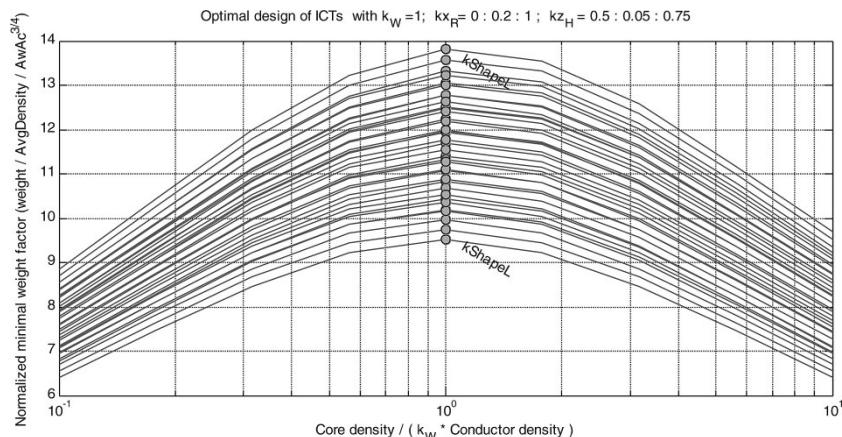
**Figure 7.20.** The three different types of fits used for the parameters

And in Figure 7.21, it can be seen that for an ICT, the optimal volume involves a variable coefficient related to the

extra shape parameters so that the optimal volume of ICTs for interleaved converters can be bounded as:

$$9.5 \cdot (A_w \cdot A_c)^{3/4} \leq Vol_{opt} \leq 14 \cdot (A_w \cdot A_c)^{3/4} \quad [7.61]$$

These last two equations should not be used to jump to too rapid conclusions, since the  $A_w A_c$  product is different for inductors and ICTs.



**Figure 7.21.** Optimal normalized weight and volume factor with different  $K_{xR}$  and  $K_{zH}$

## 7.6. Number of turns and air gap

When the core dimensions are known, the number of turns can be derived directly from the current densities and winding area using [7.4] and [7.5]:

$$n_t = \frac{j_{RMS} k_w \cdot A_w}{\frac{I_{DC}}{n_p} \cdot \sqrt{1 + \frac{R_{AC}}{R_{DC}} \frac{1}{12} \left( \frac{\Delta I}{I_{DC}} \right)^2}} \quad [7.62]$$

Then, we have to determine the air gap to obtain the targeted inductance and flux density, but because ICTs use leakage flux to filter the current ripple, we will account for the influence of direct leakage in the design process. This should be negligible for low numbers of cells, but we know that, in practice, with six cells and more, it is often possible to get rid of the return legs because with the improvement of waveforms induced by interleaving, direct leakage flux is enough to filter the current. Accounting for direct leakage, we also see that there is an extra degree of freedom; if the flux flowing in the air is not negligible, it is possible to reduce the section of the return legs and we should observe that when the number of phases of an ICT increases, the section of the return leg reduces up to a number of cells where they can be removed.

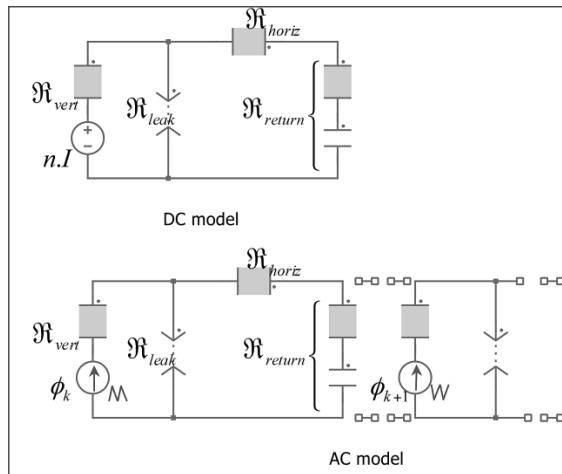
Unfortunately, the evaluation of the flux returning directly in the air is a difficult task, and at this point, this will be represented in a very simple way that is only able to reveal some trends. In future work, a better estimate could be included, such as that proposed in [LEB 58], but for the time being, we will only show how to account for such an inductance in the design process.

The selected area product and subsequent determination of core dimensions give core section and winding sections that are compatible with the specifications; so, we need to define the section and the air gap in the return leg so that when combined with the other parameters already selected (characteristic dimensions and number of turns), we get an overall reluctance giving the specified inductance. The reluctance corresponding to these requirements is:

$$\mathfrak{R}_{total}^{required} = \frac{n_p^2}{l_{LV}} = \mathfrak{R}_{vert} + \frac{1}{\frac{1}{\mathfrak{R}_{leak}} + \frac{1}{\mathfrak{R}_{horiz} + \mathfrak{R}_{return}^{required}}} \quad [7.63]$$

$$\mathfrak{R}_{return}^{required} = \frac{\mathfrak{R}_{leak} \cdot (\mathfrak{R}_{total}^{required} - \mathfrak{R}_{vert})}{\mathfrak{R}_{leak} - \mathfrak{R}_{total}^{required} + \mathfrak{R}_{vert}} - \mathfrak{R}_{horiz} \quad [7.64]$$

The DC flux in the return leg is easily expressed as a function of the DC flux in the vertical leg and the divider formed by the core reluctances on the one hand, and the leakage reluctance on the other hand. For the AC flux, it is a little more complicated since those coming from all vertical legs add up, and if the reluctances of the horizontal legs are neglected, the sum, which is  $n_P$  times smaller than the individual fluxes, distributes evenly over the  $n_P$  return legs; so, the AC flux in each return leg is  $n_p^2$  times smaller than in the vertical legs.



**Figure 7.22.** Reluctance models for IGBTs

Hence, the section of the return leg can be calculated as:

$$a_{return} = a_{vert} \cdot \frac{1}{\frac{\mathfrak{R}_{horiz} + \mathfrak{R}_{return}}{\mathfrak{R}_{leak} - \mathfrak{R}_{total}^{required} + \mathfrak{R}_{vert}}} \cdot \frac{1 + \frac{\chi}{2}}{1 + \frac{\chi}{2} \cdot n_p^2} \quad [7.65]$$

and the air gap can be adjusted to give the required reluctance:

$$\text{airgap} = (\mu_0 \cdot \mu_r \cdot a_{\text{return}} \cdot \mathfrak{R}_{\text{return}}^{\text{required}} - l_{\text{return}}) / (\mu_r - 1) \quad [7.66]$$

## 7.7. Accounting for current overload

The main goal of the design process of magnetics described previously is to respect the thermal limits of the materials, and it implicitly assumes steady-state operation. In most applications, current overload must be possible, either for very short times (line or load transients), or for a more significant duration (time needed to blow a fuse or allow a protection to trip, or even longer durations such as motor start-up, etc.). In none of these cases are the magnetics allowed to saturate; however, the prescribed current density could be exceeded by a factor that is basically inversely proportional to the duration. A simple way to account for such a requirement is to apply the design process described previously with the following substitutions:

$$I_{DCtot} \Rightarrow k_{\text{overLoad}} I_{DCtot} \quad [7.67]$$

$$j_{RMS} \Rightarrow k'_{\text{overLoad}} j_{RMS} \quad [7.68]$$

where  $k_{\text{overLoad}}$  is the ratio of the absolute max current to the nominal current, and  $k'_{\text{overLoad}}$  is chosen between 0 (long overload) and  $k_{\text{overLoad}}$  (short overload).

This substitution must be made from the start of the process, in particular before selecting the area product.

## 7.8. Optimal phase sequence for InterCell Transformers

The LV-side magnetics of interleaved converters are connected, on the one side, to the commutation cells that

behave as square voltage sources, and, on the other side, to the filtering capacitor. As a consequence, each winding behaves as a triangular flux source, and in case of ICTs, these fluxes combine in the core legs (horizontal in our drawings) that interconnect winding legs (vertical legs in our drawings). Depending on the phase shift of fluxes in neighbor windings, we get different amplitudes of fluxes in the linking legs, the minimum being obtained when the phase shift is  $180^\circ$ . However, to optimize the output voltage, phases are imposed to be  $0^\circ$ ,  $360^\circ/n_P$ ,  $2*360^\circ/n_P$ , etc., so the problem is to find a phase sequence using these  $n_P$  values such that the phase shift between two succeeding phases is as close to  $180^\circ$  as possible, the condition also applying to the phase shift between the last and the first.

It has been shown in [FOR 07, MEY 91] that the optimal phase sequence can be found, provided that two cases are distinguished:

–  $n_P$  is odd or even and multiple of 4 :

$$\phi_{k+1} - \phi_k = 360^\circ \text{ floor}\left(\frac{n_P}{2}\right) \cdot \frac{360^\circ}{n_P} \quad k = 1, \dots, n_P \quad [7.69]$$

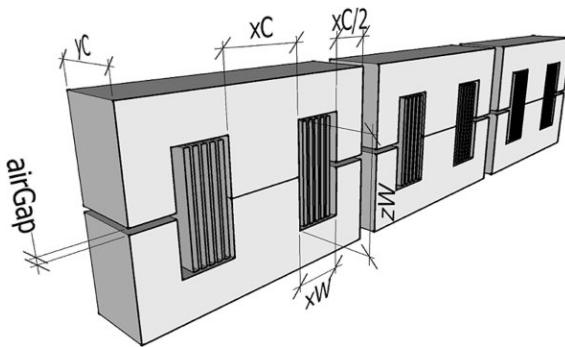
–  $n_P$  is even and multiple of 4:

$$\begin{cases} \phi_{k+1} - \phi_k = \left(\frac{n_P}{2} - 1\right) \cdot \frac{360^\circ}{n_P} & k = 1, \dots, n_P \quad k \neq n_P/2; k \neq n_P \\ \phi_{k+1} - \phi_k = 180^\circ & k = n_P/2, n_P \end{cases} \quad [7.70]$$

with  $\phi_k$  the phase of phase  $k$ , and by extension to simplify writing  $\phi_{n_P+1} = \phi_1$ .

This phase sequence is trivial for two and three cells, not very interesting for four cells, becomes interesting for five cells and makes a decisive difference for higher numbers of

cells. Analyzing the consequence of this phase sequence on linking fluxes under the assumption of fundamental fluxes at the switching frequency is relatively easy and has been described in [FOR 07]. However, accounting for triangular waveforms and determining the peak values is much more difficult. Of course, evaluation of core losses accounting for these complicated waveforms is even more difficult and that is one of the feats that become possible with the simulation models described here.

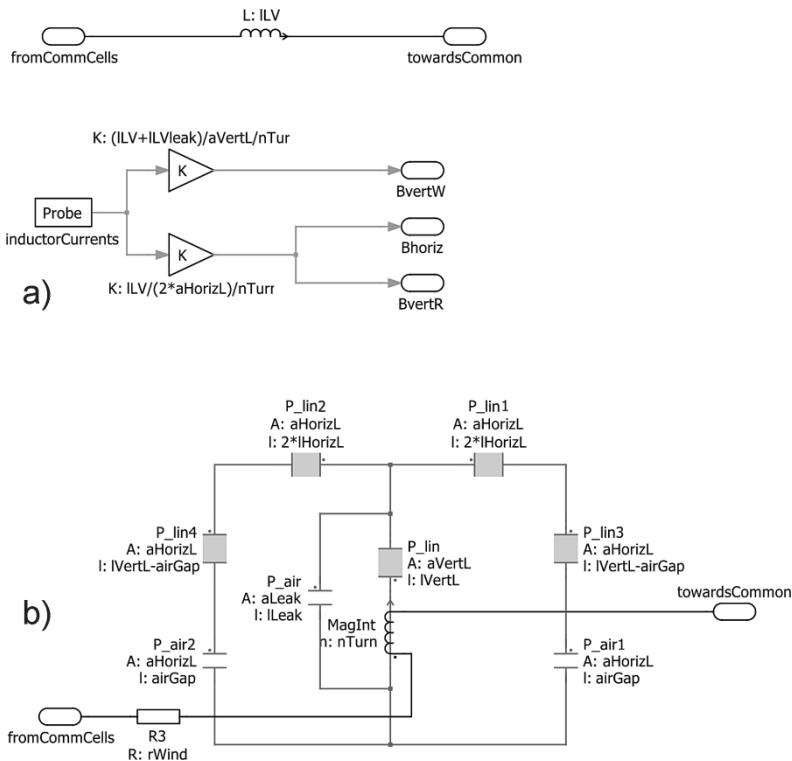


**Figure 7.23.** Inductances: electrical-based (left) and reluctance-based (right)

## 7.9. Vectorized reluctance model of magnetics

### 7.9.1. Inductors

The inductances can be vectorized to allow comparison between different designs, and this can be done with a basic electrical model, or with a reluctance model that allows observing the flux densities in the different parts of the device. In case of inductances, the added value of the reluctance model is not significant because flux densities can easily be derived from current waveforms and dimensions of the object (Figure 7.23, left). However, this is a convenient preliminary step before studying the ICTs.



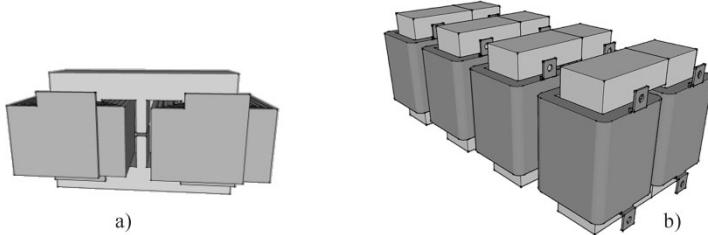
**Figure 7.24.** Vectorized models of inductances:  
electrical-based a) and reluctance-based b)

### 7.9.2. Cyclic cascade InterCell Transformers

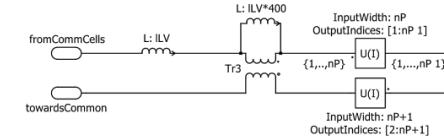
Cyclic cascade ICTs are two-winding transformers, each of these windings coupling the current flowing in one phase to that of the next phase (Figure 7.25).

This can be elegantly implemented using two wire-selector blocks as shown in Figure 7.26 and this applies in the same way for both the electrical and the magnetic model. It should be noted that the first wire is duplicated in the first wire-selector block to make this function compatible with  $n_P = 1$ ; this is not exactly an interleaved converter, but it is

very convenient to be able to compare two-level and interleaved converters with the same schematic.

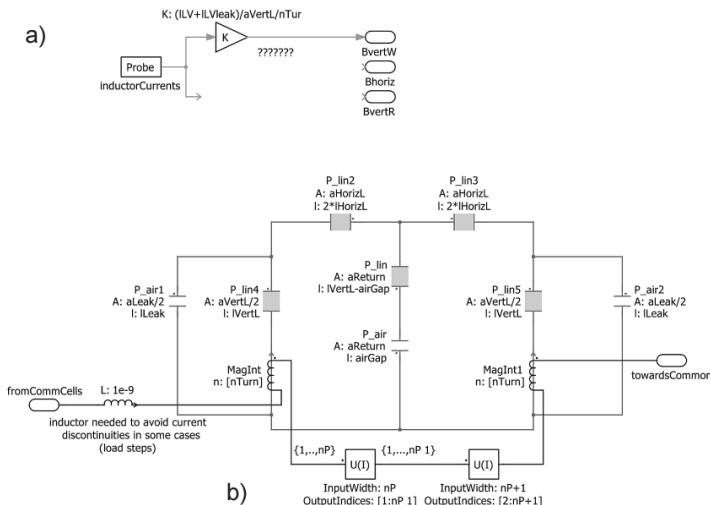


**Figure 7.25.** Cyclic cascade ICT: building block a) and eight-phase assembly b)



The first connexion is added to generate a vector of  $n+1$  connections that can be processed to generate permutation without using any vector of size 1, which allows operation with  $n=1$  (a simpler implementation is possible using  $n=1$ , but will fail with  $n=1$ )

Author : TM

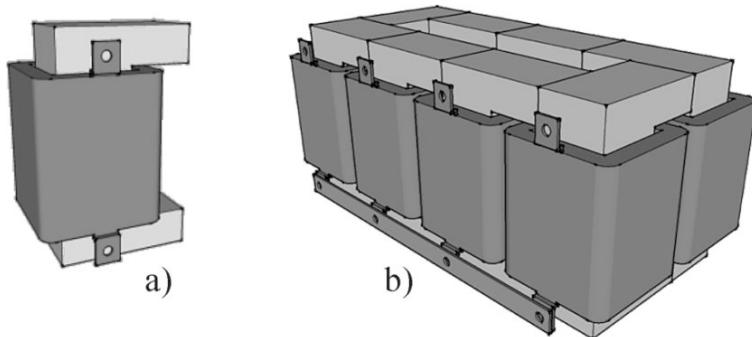


**Figure 7.26.** Vectorized models of cyclic-cascade ICT: electrical-based a) and reluctance-based b)

In this case, the reluctance model is better justified since it is quite complicated to evaluate the flux densities in the return legs case of the electrical model.

### 7.9.3. *Monolithic InterCell Transformers*

Ideal monolithic ICTs would theoretically consist of a single core with  $n_P$  windings coupled symmetrically to single return leg or air path flowing the leakage flux (DC and  $n_P f_{sw}$ ). Such a concept is not easily built and it can even be shown that purely geometric considerations do not allow such an object to be drawn. A more practical configuration of a monolithic ICT is shown in Figure 7.27(b); it is not strictly speaking symmetrical (symmetry would require a circular or polygonal design) but it can easily be built for any even number of cells using the type of "C" core shown in Figure 7.27(a).

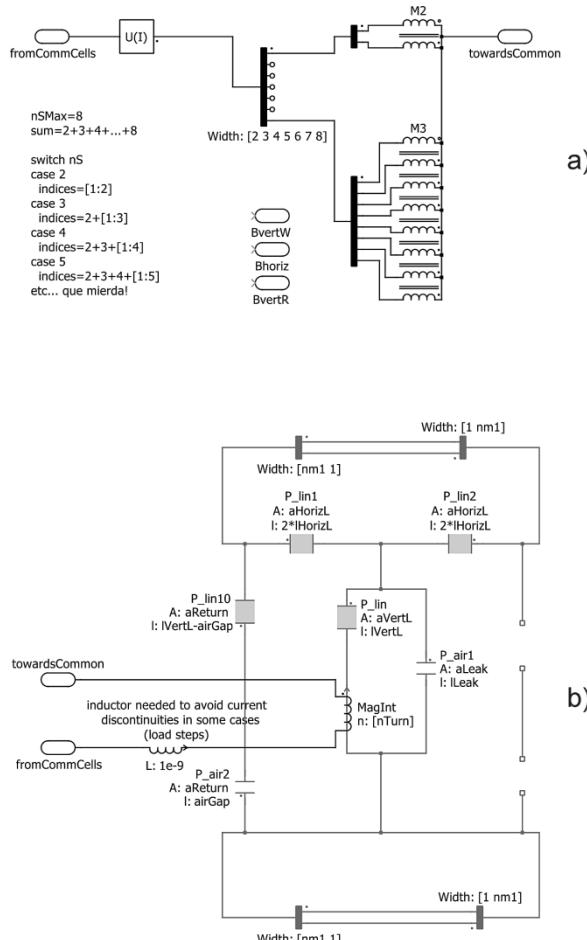


**Figure 7.27.** Monolithic ICT: a) building block;  
b) eight-phase assembly

In PLECS, we have models of  $n_P$ -phase coupled inductors with parameters defined as an L-M matrix including self-inductances and all coupling between all winding pairs, but this model is not resizable (Figure 7.28(a)).

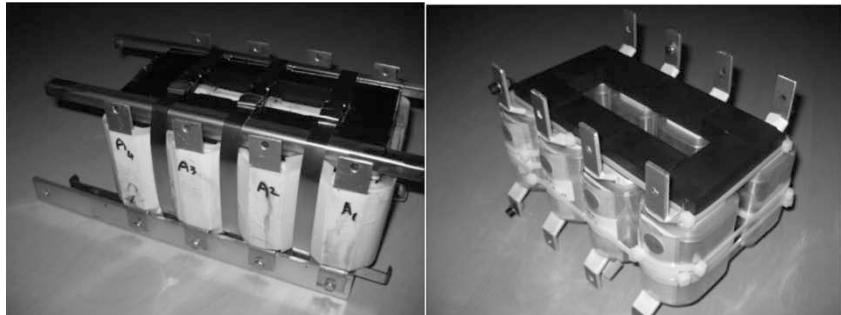
In any case, using electrical components is generally impractical because it is not so easy to derive the L-M matrix from geometrical parameters.

On the other hand, it is very easy to build the reluctance model of such a device (Figure 7.28(b)) and this gives access to flux densities in all branches of the core.



**Figure 7.28.** Vectorized models of monolithic ICTs: a) electrical; b) reluctance-based

Examples of such monolithic ICTs for a high-power application [FOR 14] are given in Figure 7.29.



**Figure 7.29.** Examples of practical monolithic ICTs

## 7.10. Design process

When the simulation models and masks described previously or developed by the user to match specific requirements are sufficiently tested and validated, it is possible to collect the pieces of code included in the different masks and assemble them in a single file to build an automated design routine. This routine, which calculates, for example, dimensions and weight of magnetic components for filters complying with steady-state and dynamic requirements for converters with different numbers of cells, can be used to explore different solutions without performing any simulation. This can be done in Matlab or Octave, for example. After this pre-design phase, it is possible to go back to simulation for a detailed analysis of a reduced set of candidate solutions.

---

## Closed-Loop Control of Multilevel DC/DC Converters

---

### 8.1. Principle

The values of the elements in the filter have been calculated using different assumptions that need to be validated by closed-loop simulations, and because of these assumptions, we know that the design criteria may not always be 100% satisfied:

- an infinitely fast response of the control in the presence of large signal load steps has been assumed to impose minimum values for capacitors  $C_{LV}$  and  $C_{HV}$ , but in the end the voltage overshoot and dip will also depend on the control;
- sampling may prevent the control to react within the switching period that follows a step; so a minimal value of  $L_{LV}$  has been imposed to limit current variation within this time interval.

The interactions between filter design and control design could be handled in a global way to better describe the interactions of these two blocks, but it would then be difficult to build independent blocks that can be reused independently which this is the option chosen here.

So the aim here is to design regulators that demonstrate the dynamic performances that can be reached with a given configuration. Considering that the numbers of series cells ( $n_s$ ) and parallel commutation cells ( $n_p$ ) are known and that the filters have been designed to match steady-state and transient specifications, the Integral Proportional (IP) regulators of cascaded voltage and current loops will be designed to obtain, in closed-loop, a damped second-order response. In order to compare the dynamic ability of different designs, we will use the same design rules for all configurations:

- identify the closed-loop system to a second-order filter with specified damping [GAT 10];
- maximize the frequency of the response within the limits imposed by saturation in response to large-signal load steps.

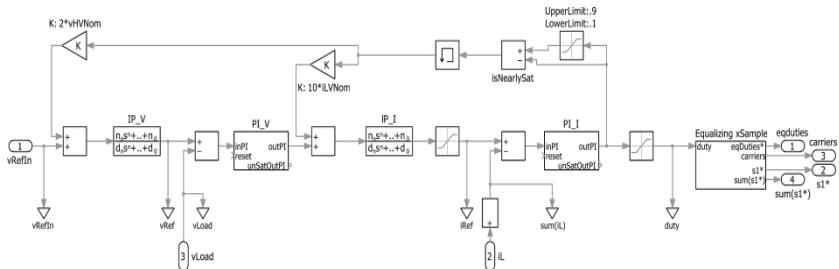
However, because the modulator generally includes a sampling block, the frequency of the response cannot be increased indefinitely; it is well-known that for a conventional 2-level converter the sampling frequency is a hard limit that causes the phase of the open-loop transfer function to tend towards  $-\infty$  and a certain margin must be taken with respect to this frequency. When multicell converters are considered, the modulator may include several sampling blocks that can be arranged in different ways as described in Chapter 4. Each type of sampling gives a different open-loop transfer function (Figure 4.14) and this must be taken into account when calculating the maximum frequency response of the system. As a consequence, the type of sampling selected by the user is taken into account via an empirical look-up table to limit the response frequency to a fraction of the sampling frequency:

	Natural	Synchronous	Equalizing	Phase-shifted
$f_{sw}$	3/5	1/5	0.5/5	1/5
$2f_{sw}$	6/5	2/5	1/5	2/5

**Table 8.1.** Ratio of closed-loop response frequency to the switching frequency for different types of sampling

The remaining design process is equivalent to what would be done with a two-level converter, the specific features of multicell converters being indirectly included in the filter values and the transfer function of the modulator:

- a first target pulsation is calculated to guarantee the stability;
- a second target pulsation is calculated to match the saturation level according to a user-selected parameter;
- the final pulsation is selected as the minimum of the two previous values;
- appropriate damping is imposed and proportional and integral gains are calculated;
- a similar process is applied for voltage loop also.



**Figure 8.1.** Cascaded current–voltage loops with IP regulators

## 8.2. Corresponding PLECS block

A regulator PLECS block with self-adjusting parameters can be constructed according to the design rules described above. The input parameters of its mask are as follows:

Converter [vHVNOM iLVNom fSw nS nP ILV cLV v...]	converter
Sampling type	sampType
Duty cycle saturation coefficient(>0,<1)	allowedSat
Max current variation for vHV/fSw (V.us applied)	k_iMax
Current reference saturation coefficient	k_iRefSat

with the list of supported sampling type being:

- 1) Natural
- 2) Synchronous@ $f_{sw}$
- 3) Synchronous@ $2f_{sw}$
- 4) Equalizing@ $f_{sw}$
- 5) Equalizing@ $2f_{sw}$
- 6) PhaseShifted@ $f_{sw}$
- 7) PhaseShifted@ $2f_{sw}$

'Natural' means no sampling, 'Synchronous@ $f_{sw}$ ' refers to sampling at the zeros of the first carrier, 'Synchronous@ $2f_{sw}$ ' means sampling at the zeros and ones of the first carrier, 'Equalizing' describes sampling as described in Chapter 4, and 'Phase Shifted' means that each comparator samples the duty cycle reference at the zeros and/or ones of the corresponding carrier.

```
disp('== xCascadedIV_IP=====')
vHVNOM      = converter(1)    % Nominal voltage on HV side
iLVNom      = converter(2)    % Nominal current on LV side (total)
fSw         = converter(3)    % Switching frequency
nS          = converter(4)    % Number of cells in series
nP          = converter(5)    % Number of cells in parallel
ILV         = converter(6)    % Per phase inductance
cLV         = converter(7)    % Capacitance on LV side (total)
vcLV0       = converter(8)    % Initial condition on filter capacitor

disp('-- current limits section -----')
iRefSat     = k_iRefSat * iLVNom
% saturation value of current ref
iMax        = k_iMax * iLVNom
% max variation of current if duty cycle maintained for 1 period
```

```

kSat           = 1+allowedSat;

disp('-- sampling section -----')

% Vector of normalized equivalent sampling frequency vs sampling type
nEqSampF_     = [3 1 1 0.5 0.5 1 1];

% Vector of sampling rate vs sampling type
sampRate_     = [1 1 2 1 2 1 2];

% Vector of index for duty selector
iSamp_         = [1 2 2 3 3 4 4];

% Normalized equivalent sampling frequency
nEqSampF      = nEqSampF_(sampType)

% Sampling rate
sampRate       = sampRate_(sampType)

% Index for duty selector
iSamp          = iSamp_(sampType);

nCell          = nP*nS;
onesNCell      = ones(1,nP*nS);

%% Regulator design assuming chopped voltage is sampled at fSw

disp('-- current IP section -----')

wnI_ZOH       = 2*pi * fSw * sampRate * nEqSampF / 5
% fZOH=fSw/5 =>phase@fSw=36° => stable

wnI_sat = kSat* pi * vHVNOM / (lLV/nP) / iRefSat
% sat.lim :vHVNOM=(lLV/nP)*(iRefSat-0)*(fResponseI * 2) )

wnI       = min(wnI_ZOH , wnI_sat)
% desired pulsation of the response

xiI       = sqrt(2)/2
% desired damping of the response

```

```
KiI      = ILV/nP * wnI^2 / vHVNom    % Integral gain (current loop)
KpI      = 2*xiI * KiI / wnI          % Proportional gain (current loop)

disp('-- voltage IP section -----')

wnV_ZOH      = wnI * nEqSampF/ 2.5
% desired pulsation of the response

wnV_sat      = kSat* pi * iRefSat / cLV / vHVNom
% desired pulsation of the response

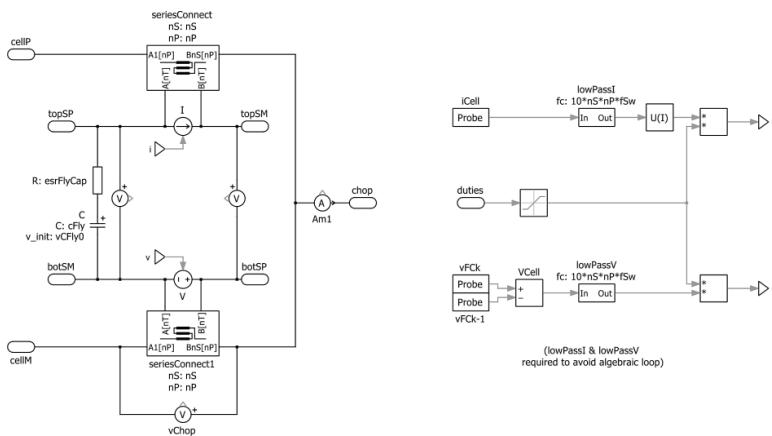
wnV          = min(wnV_ZOH, wnV_sat)
% desired pulsation of the response

xiV          = sqrt(2)/2
% desired damping of the response

KiV      = cLV * wnV^2                % Integral gain (voltage loop)
KpV      = 2*xiV * KiV / wnV          % Proportional gain (voltage loop)
```

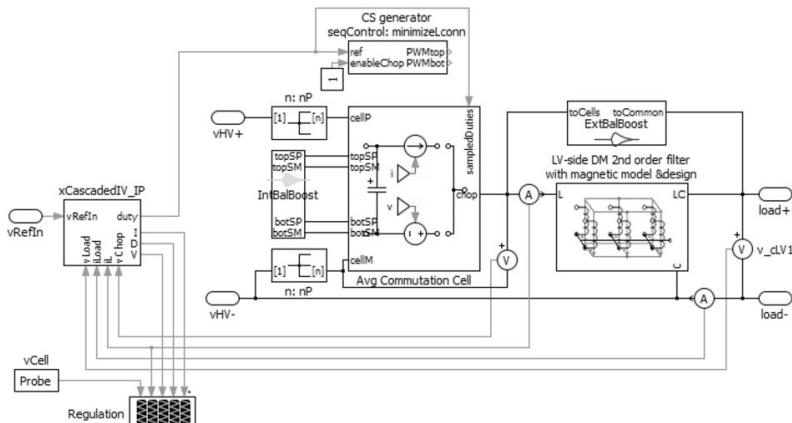
### 8.3. Average model of the macro-commutation cell for transient studies

When studying the dynamic response or checking the design of regulators, faster simulations with most relevant phenomena can be obtained using an average model of the commutation cell. In this model, in each individual cell, one of the switches is replaced by a voltage source controlled by the duty cycle times the cell voltage and the other switch is replaced by a current source controlled by the duty cycle times the cell current (Figure 8.2). When  $n_S = n_P = 1$ , this gives the standard average model of a two-level commutation cell. Low-pass filters are needed to avoid creating an algebraic loop, but their cutoff frequency should not significantly affect the result provided that it is much greater than  $n_S.n_P.f_{sw}$ .



**Figure 8.2.** Average model of the macro-commutation cell

This model can be used instead of the normal commutation cell block using the vector of sampled duties as an input (Figure 8.3). Such simulations are faster than those that use the normal model, and because dynamic performances are mainly influenced by sampling, filters and regulator parameters, they should allow checking the design and obtaining relevant information on overall performances.

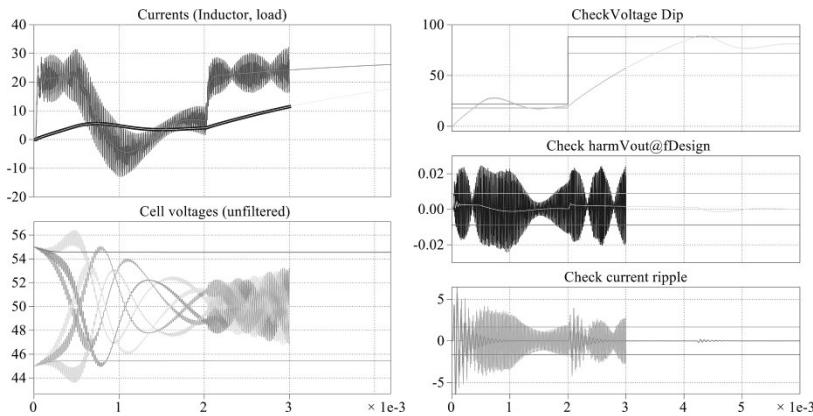


**Figure 8.3.** Using the average model of the commutation cell

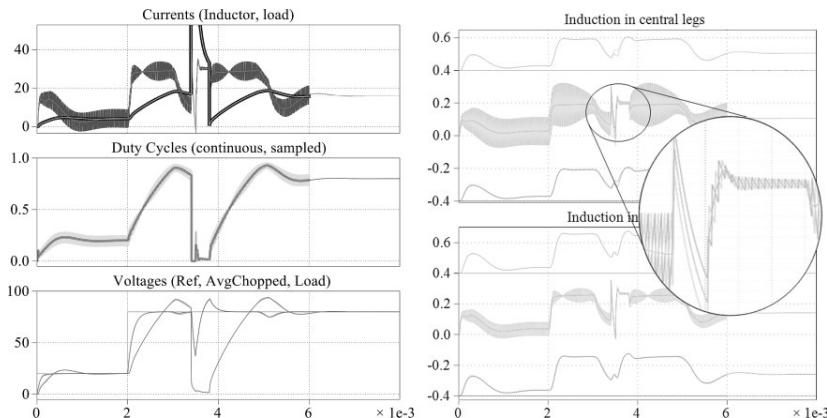
In Figure 8.4, simulations for a converter with  $n_S = 2$  and  $n_P = 3$  with the normal and average models are superimposed to show the matching of the two models. The simulation with the instantaneous model is stopped at  $t = 3$  ms to better identify the different curves.

From the left-side diagrams, it can be seen that average currents are accurately estimated by the average model, but, with no surprise, the cell voltages are less well represented. We know that there are balancing mechanisms related to switching (transition-based internal balance boosters) and switching harmonics (LV side impedance and external balance boosters); none of these phenomena is taken into account with the average model. The only balancing mechanism in the average model is the level-based internal booster; its influence can be seen at the beginning of the simulation, but after roughly 300  $\mu$ s its influence becomes zero because it is the nonlinear version that stops acting under a certain level of imbalance. It should be noted that the error on the cell voltage does not affect the accuracy of the current waveforms because the average voltage delivered by the commutation cell is equal to the duty cycle multiplied by the sum of the cell voltages and the sum of the cell voltages cannot be wrong (the sum of cell voltages is inherently equal to the DC bus voltage).

On the right-hand side of the same figure, the “Check Voltage Dip” diagram shows that the output voltage transient is correctly represented by the average model that can be used to check the design of control loops with much faster simulations. This model is, of course, of no interest as far as output voltage harmonics or current ripple are concerned; for these quantities, the instantaneous model is required and it can be seen that the relatively small imbalance of cell voltages present in this simulation causes these requirements to be unmatched.



**Figure 8.4.** Waveforms with instantaneous and average models compared (plain: instantaneous model; dashed, average model). For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)



**Figure 8.5.** Instantaneous and average models compared in case of short-circuit. For a color version of the figure, see [www.iste.co.uk/meynard/vectorized.zip](http://www.iste.co.uk/meynard/vectorized.zip)

Figure 8.5 shows results obtained in the case of a two-cell parallel converter with a short-circuit occurring around 3.5 ms. It can be seen in the left part that during short-circuit the average model gives a slightly different response

(especially visible on waveforms *AverageChoppedVoltage* and *LoadVoltage*), but the general behavior and reaction to this short-circuit is still very honest. The waveforms on the right are those of the flux densities in the windings (top) and in the return legs (bottom). It can be seen that even during and after short-circuit the flux densities are very well balanced, which is related to the phase currents balance but with a much stronger accuracy requirement; if no or little air gap is present in the ICT, which is the case here, a 1% current imbalance may easily generate 10% or even 100% of flux density imbalance.

## 8.4. Conclusion

The self-adjusting regulators described in this chapter allow running simulation with a regulation of the LV side current and LV side voltage. The internal variables (cell voltages in series connected cells, differences of phase currents in magnetic components in case of commutation cells in parallel) need not be actively regulated in these simulations:

- the currents are initially set to zero and will stay balanced when the equalizing sampling blocks are used;
- the voltages can be initially unbalanced; they will tend to rebalance because of the action of internal and external balance boosters, and balance will not be affected by the variations of duty cycle when the equalizing sampling blocks are used.

When only the output performances are considered, faster simulations can be run using the average model of the commutation cell.

---

## Bibliography

---

- [BEN 02] BEN ABDELGHANI A., MARTINS C.A., ROBOAM X., *et al.*, “Use of extra degrees of freedom in multilevel drives”, *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 965–977, October 2002.
- [DAV 95] DAVANCENS P., MEYNARD T.A., “Current balance in paralleled commutation cells”, *Conference on Power Conversion & Intelligent Motion*, 20–22 June 1995.
- [DAV 97a] DAVANCENS P., MEYNARD T.A., “Etude des convertisseurs multicellulaires parallèles. Première partie: Modélisation”, *Journal de Physique III*, vol. 7, no. 1, pp. 143–160, January 1997.
- [DAV 97b] DAVANCENS P., MEYNARD T.A., “Etude des convertisseurs multicellulaires parallèles. Deuxième partie: Analyse du modèle”, *Journal de Physique III*, vol. 7, no. 1, pp. 161–177, January 1997.
- [FOR 07] FOREST F., MEYNARD T.A., LABOURE E., *et al.*, “Optimization of the supply voltage system in interleaved converters using intercell transformers”, *IEEE Transactions on Power Electronics*, vol. 22, no. 3, pp. 934–942, May 2007.
- [FOR 14] FOREST F., MEYNARD T.A., HUSELSTEIN J.-J., *et al.*, “Design and characterization of an eight-phase-137-kW intercell transformer dedicated to multicell DC–DC stages in a modular UPS”, *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 45–55, January 2014.

- [FLU 14a] FLUXDISTRIBUTIONSTANDARDSEQUENCE, *PLECS model*, available at <http://www.doi.org/10.13143/vectorized-multicell>, 2014.
- [FLU 14b] FLUXDISTRIBUTIONOPTIMALSEQUENCE, *PLECS model*, available at <http://www.doi.org/10.13143/vectorized-multicell>, 2014.
- [GAT 10] GATEAU G., RÉGNIER J., LLOR A., “VHDL code generation for FPGA implementation of digital control with co-simulation step”, *IEEE International Conference on Industrial Technology (ICIT)*, pp. 850–855, 14–17 March 2010.
- [GAT 02] GATEAU G., FADEL M., MAUSSION P., et al., “Multicell converters: active control and observation of flying-capacitor voltages”, *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 998–1008, October 2002.
- [LEB 58] LEBEDEV V.K., “Calculation of the short-circuit resistance of welding transformers with yoke leakage (russ.)”, *Conference on Automatic Welding [Avtomaticheskaja Svarka]* Kiev, vol. 11, no. 4, pp. 37–44, 1958.
- [LEF 01a] LEFEUVRE E., MEYNARD T.A., “Fast line voltage conditioners using new PWM AC chopper topologies”, *European Power Electronics Conference*, Graz, 27–29 August 2001.
- [LEF 01b] LEFEUVRE E., MEYNARD T.A., “Multilevel AC/AC choppers”, *European Power Electronics Conference*, Graz, 27–29 August 2001.
- [MCG 07] MCGRATH B.P., HOLMES, D.G., “Analytical modeling of voltage balance dynamics for a flying capacitor multilevel converter”, *Power Electronics Specialists Conference, PESC 2007, IEEE*, pp. 1810–1816, 17–21 June 2007.
- [MEY 91] MEYNARD T.A., FOCH H., “Dispositif électronique de conversion d'énergie électrique”, French Patent 91.09582, World Patent 1993002501A1, 25 July 1991.
- [MEY 92] MEYNARD T.A., FOCH H., “Multilevel choppers for high voltage applications”, *European Power Electronics Journal*, vol. 2, no. 1, pp. 45–50, March 1992.

- [MEY 93] MEYNARD T.A., FOCH H., "Imbricated cells multilevel voltage-source inverters for high voltage applications", *European Power Electronics Journal*, vol. 3, no. 2, pp. 99–106, June 1993.
- [MEY 97] MEYNARD T.A., FADEL M., AOUDA N., "Modeling of multilevel converters", *IEEE Transactions on Industrial Electronics*, vol. 44, no. 3, pp. 356–364, June 1997.
- [MEY 02a] MEYNARD T.A., FOCH H., THOMAS P., *et al.*, "Multicell converters: basic concepts and industry applications", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 955–964, October 2002.
- [MEY 02b] MEYNARD T.A., FOCH H., FOREST F., *et al.*, "Multicell converters: derived topologies", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 978–987, October 2002.
- [MEY 05] MEYNARD T.A., FOREST F., LABOURE E., *et al.*, "Procédé et dispositif d'alimentation d'un coupleur magnétique", French Patent 0507136, World Patent WO2007006902A3, 5 July 2005.
- [MEY 13] MEYNARD T.A., COUGO B., BRANDELERO J., "Design of differential mode filters for two-level and multicell converters", *IEEE 11th International Workshop of Electronics, Control, Measurement, Signals and their application to Mechatronics (ECMSM)*, pp. 1–6, 24–26 June 2013.
- [TUR 02] TURPIN C., BAUDESSON P., RICHARDEAU F., *et al.*, "Fault management of multicell converters", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 988–997, October 2002.
- [TES 14] TESTEQXSAMPLERWSWITCHING&FASTSATURATION, *PLECS model*, available at <http://www.doi.org/10.13143/vectorized-multicell>, 2014.
- [VID 13] VIDEAU N., MEYNARD T.A., FONTES G., *et al.*, "A non-isolated DC-DC converter with intercell transformer for buck-type or boost-type application requiring high voltage ratio and high efficiency", *International Conference on Power Conversion & Intelligent Motion*, May 2013.
- [WEI 14] WEIGHTOPTIMALICT.M, *Matlab routine*, available at <http://www.doi.org/10.13143/vectorized-multicell>, 2014.



---

# Index

---

## **A, B, C**

- area product, 92–95, 98, 99, 101, 102, 118, 121, 123
- average model, 11, 13, 136, 137–140
- balance booster, 15, 16, 57–59, 63–73, 138, 140
- commutation cell, 2, 3, 6, 9, 11, 21, 28–33, 38, 52, 59, 60, 77, 78, 123, 132, 136–138, 140
- cyclic cascade, 18, 20, 126, 127

## **D, F, I**

- flying capacitor, 11–16, 27–31, 38, 43, 57, 60, 61, 63
- integral proportional (IP), 132, 133
- intercell transformer (ICT), 17, 18, 20, 38, 50, 51, 92, 97, 98, 101, 107–110, 113–130, 140
- interleaved, 2, 4, 5, 11, 14, 15, 17, 25, 26, 39, 40, 43,

- 44, 50, 95, 97–99, 119, 120, 123, 126, 127

## **M, P, R**

- modulator, 1, 25, 26, 37, 38, 45, 48, 51, 132, 133
- monolithic, 18, 20, 50, 109, 128–130
- multilevel
  - waveforms, 2, 3
  - converters, 1, 2, 23, 38, 44, 45, 57, 82
- parallel, 2–4, 7, 14–21, 24, 25, 28, 29, 32, 33, 35, 38, 44, 58, 60–63, 67, 78, 83, 117, 132, 134, 139, 146
- regulator, 19, 20, 51, 83, 132, 133, 135, 136, 137, 140

## **S, V**

- short-circuit, 51, 139, 140
- star-connection, 17, 25, 32, 36



---

Other titles from



in

Electrical Engineering

---

## 2013

GALLOT-LAVALLÉE Olivier  
*Dielectric Materials and Electrostatic*

GLAIZE Christian, GENIES Sylvie  
*Lithium Batteries and Other Electrochemical Storage*

PERA Marie-Cécile, HISSEL Daniel, GUALOUS Hamid, TURPIN Christophe  
*Electrochemical Components*

## 2012

BECKERS Benoit  
*Solar Energy at Urban Scale*

FOULADGAR Javad  
*Electrothermics*

GLAIZE Christian, GENIES Sylvie  
*Lead and Nickel Electrochemical Batteries*

ROBOAM Xavier

*Systemic Design Methodologies for Electrical Energy Systems*

ROBOAM Xavier

*Integrated Design by Optimization of Electrical Energy Systems*

ROBYNS Benoît *et al.*

*Electricity Production from Renewable Energies*

SABONNADIERE Jean-Claude, HADJSOUD Nourédine

*Smart Grids*

## 2011

GAO Fei, BLUNIER Benjamin, MIRAOUI Abdellatif

*Proton Exchange Membrane Fuel Cells Modeling*

SABONNADIERE Jean-Claude, HADJSOUD Nourédine

*Electrical Distribution Networks*

LOUIS Jean-Paul

*Control of Non-conventional Synchronous Motors*

LOUIS Jean-Paul

*Control of Synchronous Motors*

MONMASSON Eric

*Power Electronic Converters: PWM Strategies and Current Control*

MULTON Bernard

*Marine Renewable Energy Handbook*

RAZIK Hubert

*Handbook of Asynchronous Machine with Variable Speed*

TRIGEASSOU Jean-Claude

*Electrical Machines Diagnosis*

ZAIM Mohammed El-Hadi, REZZOUG Abderrezak

*Non-conventional Electrical Machines*

## **2010**

BERETTA Joseph  
*Automotive Electricity / Electric Drive Systems*

BRUNET Yves  
*Energy Storage*

DE FORNEL Bernard, LOUIS Jean-Paul  
*Electrical Actuators / Identification and Observation*

JUFER Marcel  
*Electric Drive / Design Methodology*

LE DOEFF René, ZAÏM Mohammed El-Hadi  
*Rotating Electrical Machines*

MARTINEZ-VEGA Juan  
*Dielectric Materials for Electrical Engineering*

## **2009**

HADJSAÏD Nouredine, SABONNADIÈRE Jean-Claude  
*Power Systems and Restructuring*

HUSSON René  
*Control Methods for Electrical Machines*

MOTTIER Patrick  
*LED for Lighting Applications*

SABONNADIERE Jean-Claude  
*Low Emission Power Generation Technologies and Energy Management*

SABONNADIERE Jean-Claude  
*Renewable Energy Technologies*

## **2008**

CRAPPE Michel  
*Electric Power Systems*

MEUNIER Gérard

*The Finite Element Method for Electromagnetic Modeling*

**2006**

PRÉVÉ Christophe

*Protection of Electrical Networks*