|  | **Pimpri Chinchwad Education Trust’s**  **Pimpri Chinchwad College of Engineering** |
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| **Experiment No. 5**  **Experimentation details** | |

**Department: E&TC Academic Year: 2023-24 Semester-I**

**Class: B.Tech E&TC Course: VLSI Design Lab**

**Name of Student:**

**Div and Batch: A,A1**

**Roll No:**

**Title of the Experiment:**

**Model and verify 8-bit ALU using VHDL and implement on FPGA and evaluate power and timing performance.**

**Software Requirements: Xilinx 14.7 ISE Design Suite**

**Hardware Requirements: Xilinx Spartan-6 XC6SLX45 FPGA**

**VHDL Code for 8-bit ALU**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity alu\_lab8 is

Port (A,B : in STD\_LOGIC\_VECTOR (1 downto 0);

sel : in STD\_LOGIC\_VECTOR (2 downto 0);

Y : out STD\_LOGIC\_VECTOR (1 downto 0));

end alu\_lab8;

architecture Behavioral of alu\_lab8 is

begin

process(A,B,sel)

begin

case sel is

when "000" => Y <=A+B;

when "001" => Y <=A-B;

when "010" => Y <=A AND B;

when "011" => Y <=A NAND B;

when "100" => Y <=A XOR B;

when "101" => Y <=A XNOR B;

when "110" => Y <=A OR B;

when "111" => Y <=A;

when others => Y <="ZZZZZZZZ";

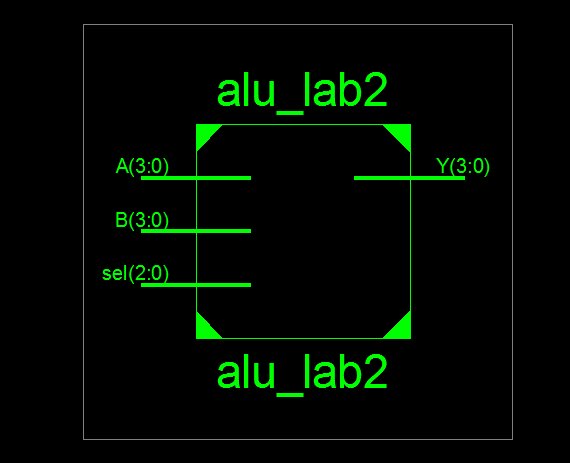
end case;

end process;

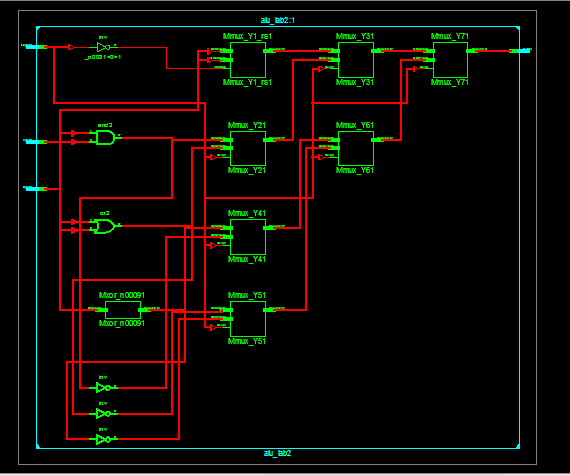
end Behavioral;

**RTL Schematic**

**Block Diagram of Design**



**Detailed Schematic**



**VHDL Test Bench**

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY alu IS

END alu;

ARCHITECTURE behavior OF alu IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT alu\_lab8

PORT(

A : IN std\_logic\_vector(7 downto 0);

B : IN std\_logic\_vector(7 downto 0);

sel : IN std\_logic\_vector(2 downto 0);

Y : OUT std\_logic\_vector(7 downto 0)

);

END COMPONENT;

--Inputs

signal A : std\_logic\_vector(7 downto 0) := (others => '0');

signal B : std\_logic\_vector(7 downto 0) := (others => '0');

signal sel : std\_logic\_vector(2 downto 0) := (others => '0');

--Outputs

signal Y : std\_logic\_vector(7 downto 0);

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: alu\_lab8 PORT MAP (

A => A,

B => B,

sel => sel,

Y => Y

);

PROCESS

BEGIN

B<="01000100";

A<="10110011";

sel<="000";

wait for 20ns;

sel<="001";

wait for 20ns;

sel<="010";

wait for 20ns;

sel<="011";

wait for 20ns;

sel<="100";

wait for 20ns;

sel<="101";

wait for 20ns;

sel<="110";

wait for 20ns;

sel<="111";

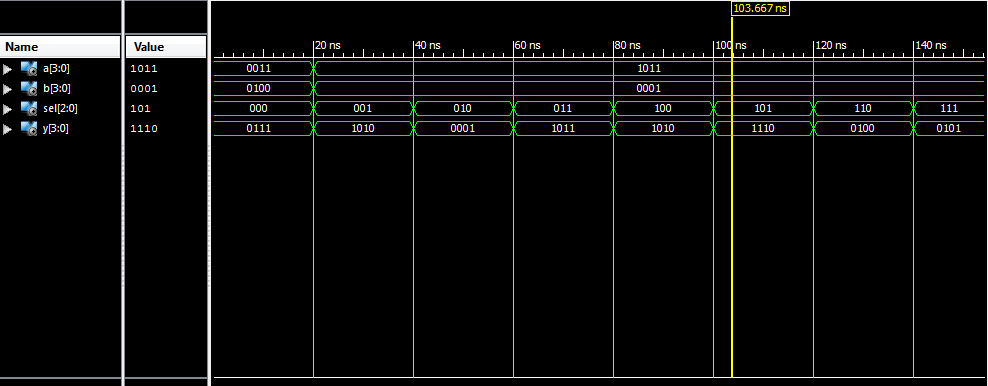
wait;

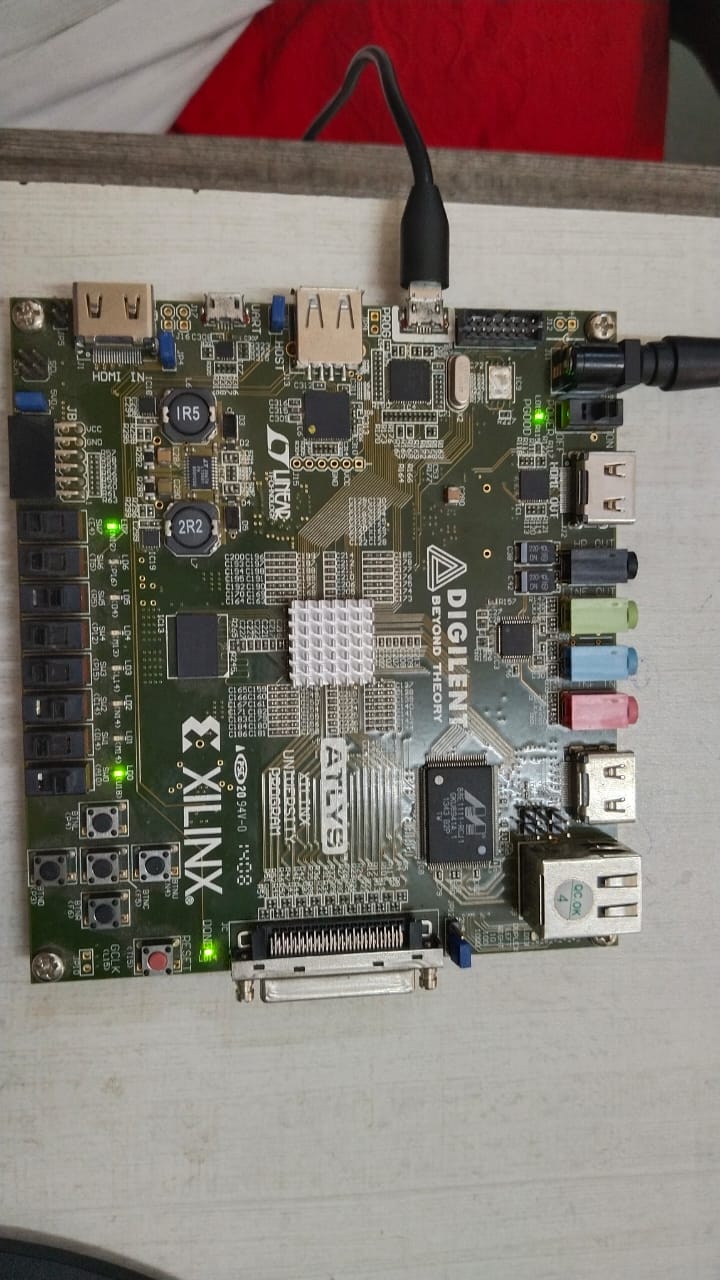
end process;

END;

**Simulation Results**

**8-bit ALU**



**Implementation on Spartan 6**

**2-bit ALU**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity Expt\_1b is

Port ( A : in STD\_LOGIC\_VECTOR**(1 downto 0);**

B : in STD\_LOGIC\_VECTOR**(1 downto 0);**

sel : in STD\_LOGIC\_VECTOR(2 downto 0);

Y : out STD\_LOGIC\_VECTOR**(1 downto 0**));

end Expt\_1b;

architecture Behavioral of Expt\_1b is

begin

process(A,B,sel)

begin

case sel is

when "000" => Y <=A+B;

when "001" => Y <=A-B;

when "010" => Y <=A AND B;

when "011" => Y <=A NAND B;

when "100" => Y <=A XOR B;

when "101" => Y <=A XNOR B;

when "110" => Y <=A OR B;

when "111" => Y <=A;

when others => **Y <="ZZ";**

end case;

end process;

end Behavioral;

**Device Specifications to be selected while implementing:**

Net"A<0>"LOC="A10";

Net"A<1>"LOC="D14";

Net"B<0>"LOC="C14";

Net"B<1>"LOC="P15";

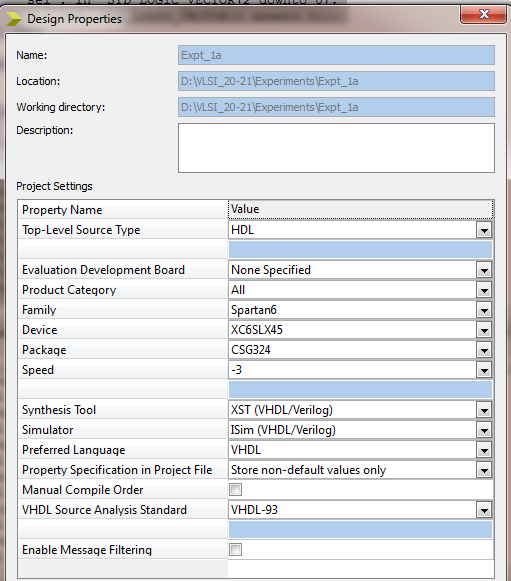
Net"SEL<0>"LOC="P12";

Net"SEL<1>"LOC="R5";

Net"SEL<2>"LOC="T5";

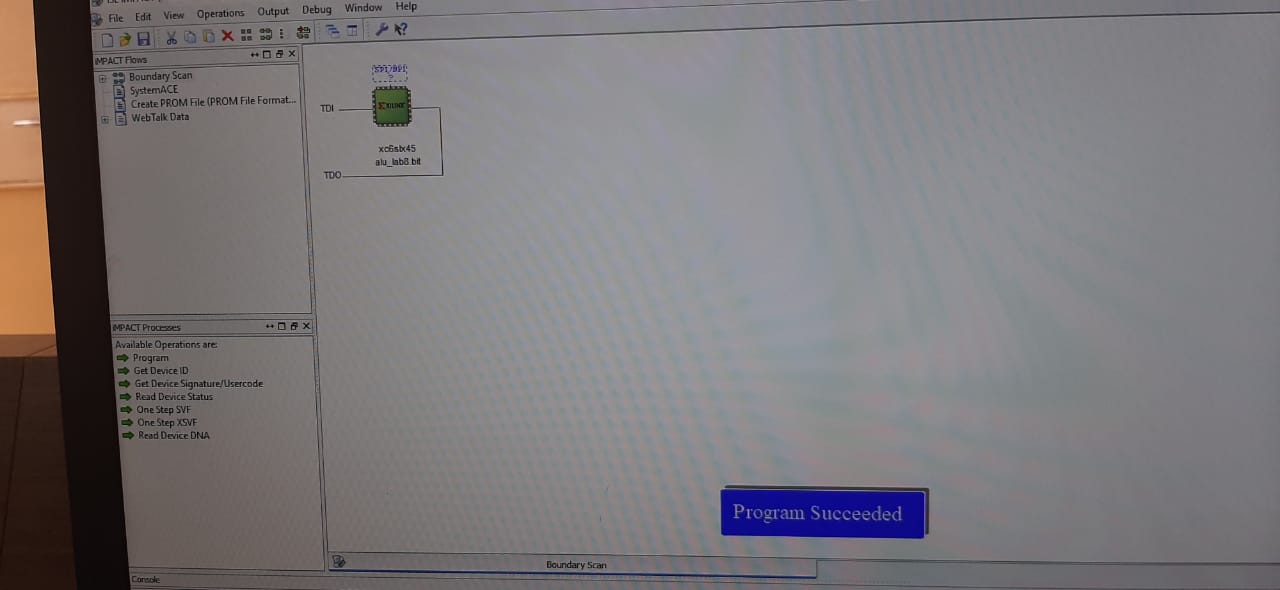
Net"Y<0>"LOC="U18";

Net"Y<1>"LOC="M14";



**Implementation Constraint File**

**Implementation Successful**

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**Hardware Snapshots**

**Digilent ATLYS Spartan 6 FPGA Board**