10.2.2 IDLE MODE

Idle mode has these features:

- The CPU will stop executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 "Selective Peripheral Module Control"**).
- If the WDT or FSCM is enabled, the LPRC will also remain active.

The device will wake from Idle mode on any of these events:

- Any interrupt that is individually enabled.
- Any device Reset.
- A WDT time-out.

On wake-up from Idle, the clock is reapplied to the CPU and instruction execution begins immediately, starting with the instruction following the `PWRSAV` instruction or the first instruction in the ISR.

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSAV` instruction will be held off until entry into Sleep or Idle mode has completed. The device will then wake-up from Sleep or Idle mode.

10.2.4 LOW-VOLTAGE RETENTION REGULATOR

PIC24FJ256GA705 family devices incorporate a second on-chip voltage regulator, designed to provide power to select microcontroller features at 1.2V nominal. This regulator allows features, such as data RAM and the WDT, to be maintained in power-saving modes where they would otherwise be inactive, or maintain them at a lower power than would otherwise be the case.

Retention Sleep uses less power than standard Sleep mode, but takes more time to recover and begin execution. An additional 10-15 µs (typical) is required to charge V_{CAP} from 1.2V to 1.8V and start to execute instructions when exiting Retention Sleep.

The VREGS bit allows control of speed to exit from the Sleep modes (regular and Retention) at the cost of more power. The regulator band gaps are enabled, which increases the current but reduces time to recover from Sleep by ~10 µs.

The low-voltage retention regulator is only available when Sleep mode is invoked. It is controlled by the LPCFG Configuration bit (FPOR[2]) and in firmware by the RETEN bit (RCON[12]). LPCFG must be programmed (= `0`) and the RETEN bit must be set (= `1`) for the regulator to be enabled.

10.2.5 EXITING FROM LOW-VOLTAGE RETENTION SLEEP

All of the methods for exiting from standard Sleep also apply to Retention Sleep ($\overline{MCLR}$, INT0, etc.). However, in order to allow the regulator to switch from 1.8V (operating) to Retention mode (1.2V), there is a hardware 'lockout timer' from the execution of Retention Sleep until Retention Sleep can be exited.

During the 'lockout time', the only method to exit Retention Sleep is a POR or $\overline{MCLR}$. Interrupts that are asserted (such as INT0) during the 'lockout time' are masked. The lockout timer then sets a minimum interval from when the part enters Retention Sleep until it can exit from Retention Sleep. Interrupts are not 'held pending' during lockout; they are masked and in order to exit after the lockout expires, the exiting source must assert after the lockout time.

The lockout timer is derived from the LPRC clock, which has a wide (untrimmed) frequency tolerance.

The lockout time will be one of the following two cases:

- If the LPRC was not running at the time of Retention Sleep, the lockout time is 2 LPRC periods + LPRC wake-up time
- If the LPRC was running at the time of Retention Sleep, the lockout time is 1 LPRC period

Refer to Table 32-20 and Table 32-21 in the AC Electrical Specifications for the LPRC timing.

10.2.6 SUMMARY OF LOW-POWER SLEEP MODES

The RETEN bit and the VREGS bit (RCON[12,8]) allow for four different Sleep modes, which will vary by wake-up time and power consumption. Refer to Table 10-1 for a summary of these modes. Specific information about the current consumption and wake times can be found in **Section 32.0 "Electrical Characteristics"**.

TABLE 10-1: LOW-POWER SLEEP MODES

RETEN	VREGS	MODE	Relative Power
0	**1**	Sleep	**100 µA Range**
0	**0**	Fast Wake-up	**A Few µA Range**
1	**1**	Retention Sleep	**A 1 µA Range**
1	**0**	Fast Retention	**Less than 1 µA**