

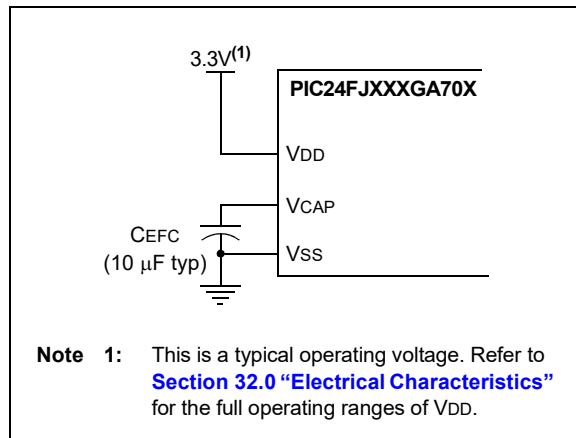
## 29.3 On-Chip Voltage Regulator

All PIC24FJ256GA705 family devices power their core digital logic at a nominal 1.8V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the PIC24FJ256GA705 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

This regulator is always enabled. It provides a constant voltage (1.8V nominal) to the digital core logic, from a VDD of about 2.1V, all the way up to the device's VDDMAX. It does not have the capability to boost VDD levels. In order to prevent "brown-out" conditions when the voltage drops too low for the regulator, the Brown-out Reset occurs. Then, the regulator output follows VDD with a typical voltage drop of 300 mV.

A low-ESR capacitor (such as ceramic) must be connected to the VCAP pin (Figure 29-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor (CEFC) is provided in [Section 32.1 "DC Characteristics"](#).

**FIGURE 29-1: CONNECTIONS FOR THE ON-CHIP REGULATOR**



### 29.3.1 ON-CHIP REGULATOR AND POR

The voltage regulator takes approximately 10 µs for it to generate output. During this time, designated as TVREG, code execution is disabled. TVREG is applied every time the device resumes operation after any power-down, including Sleep mode. TVREG is determined by the status of the VREGS bit (RCON[8]) and the WDTWIN[1:0] Configuration bits (FWDTP[9:8]). Refer to [Section 32.0 "Electrical Characteristics"](#) for more information on TVREG.

**Note:** For more information, see [Section 32.0 "Electrical Characteristics"](#). The information in this data sheet supersedes the information in the FRM.

### 29.3.2 VOLTAGE REGULATOR STANDBY MODE

The on-chip regulator always consumes a small incremental amount of current over IDD/IPD, including when the device is in Sleep mode, even though the core digital logic does not require power. To provide additional savings in applications where power resources are critical, the regulator can be made to enter Standby mode, on its own, whenever the device goes into Sleep mode. This feature is controlled by the VREGS bit (RCON[8]). Clearing the VREGS bit enables the Standby mode. When waking up from Standby mode, the regulator needs to wait for TVREG to expire before wake-up.

### 29.3.3 LOW-VOLTAGE RETENTION REGULATOR

When in Sleep mode, PIC24FJ256GA705 family devices may use a separate low-power, low-voltage retention regulator to power critical circuits. This regulator, which operates at 1.2V nominal, maintains power to data RAM and the RTCC while all other core digital logic is powered down. The low-voltage retention regulator is described in more detail in [Section 10.2.4 "Low-Voltage Retention Regulator"](#).