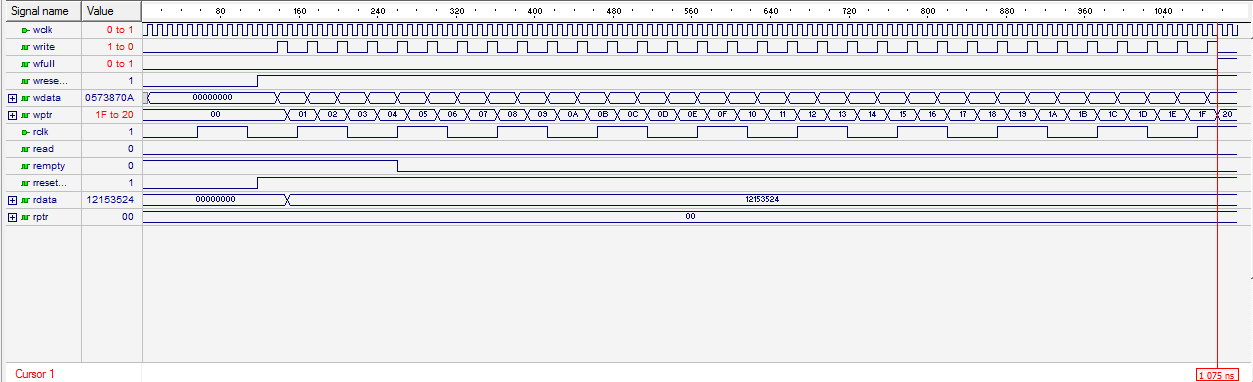
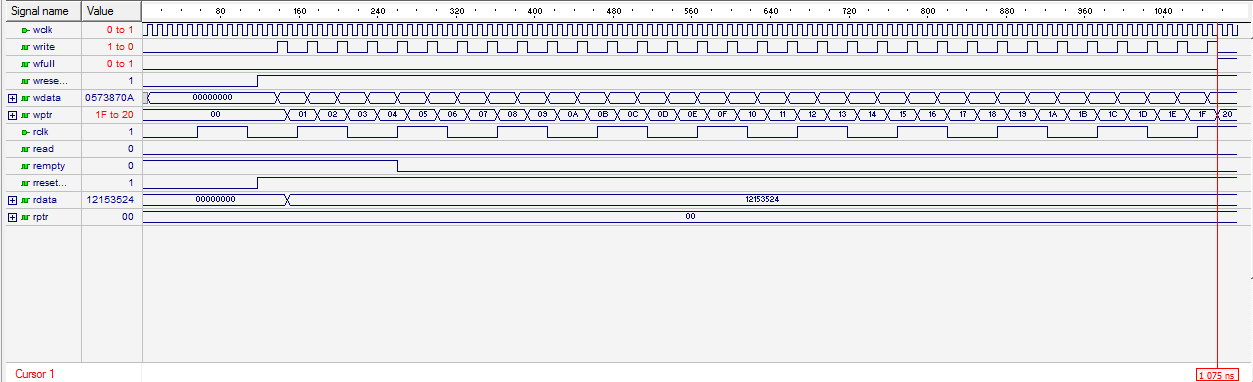
Asynchronous FIFO verification using System Verilog Puneet Nipunage

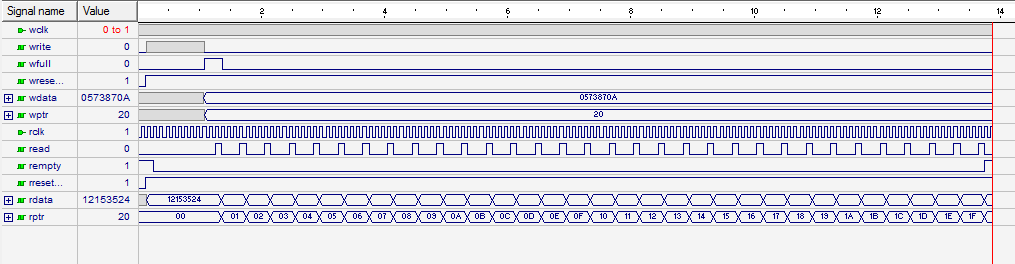
1. Test case 1: FIFO full: Waveform





rptr still points to 0th memory address wptr reaches maximum address and wfull goes high

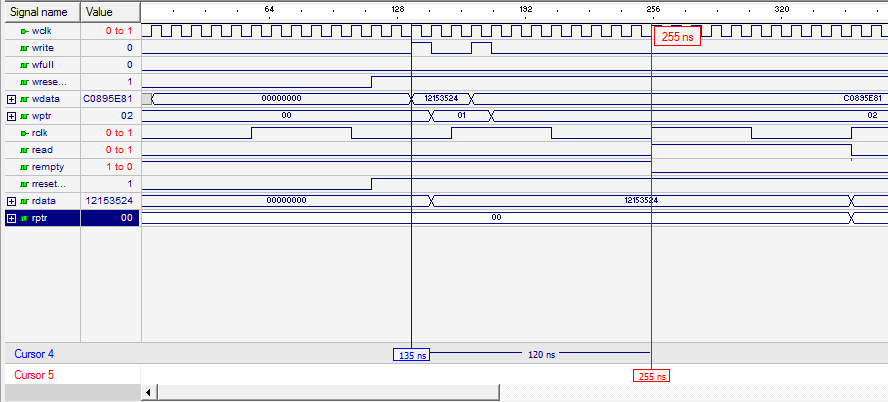
2. Test Case2: FIFO empty: Waveform



FIFO made full

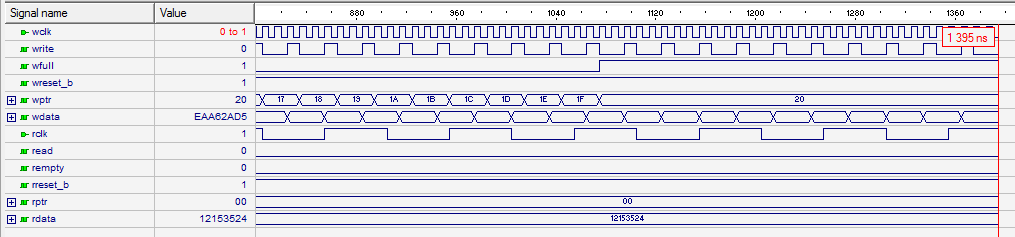
then read = 1 for 32 cycles, and write = 0, which makes rptr == wptr (which means FIFO is empty)

3. Test Case3: Data sent == Data Received



From wavefrom we observe when **write** goes high, data stored at 0th location in memory is **12153524**, and when **read** goes high, data is read from 0th location which is also **12153524**.

4. Test Case4: Data Overflow check:



Here we observe, that though **10** more packets are sent in (observe **wdata**) after the **wfull goes high**, they do not enter the memory, this can be proved from the value of **wptr** which **does not increment beyond h'20 (FIFO full)**.