Assignment 3: Exploring Memory Hierarchy Design in gem5

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Part 1: Understanding Memory Hierarchy

1. Introduction to Memory Hierarchy Design

Conceptual Analysis and Discussion

Memory Technologies

Memory hierarchy design is critical in modern computing systems, aiming to bridge the performance gap between fast processors and slower storage devices. By carefully organizing different memory technologies, architects can create systems that approach the speed of the fastest components while maintaining cost-effectiveness and capacity (Balasubramonian et al., 2003). The memory hierarchy leverages a spectrum of technologies, each with distinct characteristics. Static Random Access Memory (SRAM) is the fastest but most expensive per bit, using flip-flops to store data without requiring refresh cycles. It has low latency (1-10 ns access time) but high power consumption and limited density, making it suitable for CPU caches (L1, L2, L3).

In contrast, Dynamic Random Access Memory (DRAM) is slower than SRAM but much cheaper per bit; it uses capacitors to store data, necessitating periodic refresh. DRAM has higher latency (50-100 ns access time), lower power consumption than SRAM, and greater density, which makes it ideal for main system memory (Bauer et al., 2011). Additionally, non-volatile memory (NVM), including technologies like NAND Flash and 3D XPoint, retains data without power and offers high density at a low cost per bit but comes with much slower access times (μs to ms range), typically used for SSDs and storage-class memory. This arrangement allows systems to benefit from the speed of SRAM for frequently accessed data while leveraging the cost-effectiveness and capacity of DRAM and NVM for larger datasets.

Advanced Cache Optimization

To maximize cache hierarchy effectiveness, several advanced techniques are employed. Prefetching proactively fetches data into the cache before it is explicitly requested, reducing cache miss latency by anticipating future memory accesses. This technique can be hardware-based (e.g., stride prefetching) or software-directed; however, challenges include the accuracy of predictions and potential cache pollution. Victim caches serve as small, fully associative caches that store recently evicted cache lines, providing a "second chance" for data that might be needed again soon. They are particularly effective for reducing conflict misses in direct-mapped caches but come with trade-offs regarding additional hardware complexity versus improved hit rates (Balasubramonian et al., 2003).

Virtual Memory and Virtual Machines

Virtual memory is another crucial abstraction that simplifies programming and enhances system efficiency. It employs page tables to map virtual addresses to physical addresses, enabling non-contiguous memory allocation and memory protection while balancing lookup speed and memory overhead through multi-level page tables. Translation Lookaside Buffers (TLBs) cache recent translations to further enhance performance. Page replacement algorithms manage limited physical memory by swapping pages to and from disk; common algorithms include Least Recently Used (LRU), Clock, and First-In-First-Out (FIFO), each presenting trade-offs between implementation complexity and effectiveness (Bauer et al., 2011).

Cross-Cutting Issues

Designing effective memory hierarchies involves navigating complex trade-offs related to cost versus performance, power consumption, complexity versus benefit, and workload sensitivity.

Balancing expensive yet fast technologies like SRAM with cheaper but slower options like DRAM and NVM is essential for optimizing cache sizes and levels for the best price/performance ratio. Power consumption remains a critical consideration since SRAM caches consume significant static power while DRAM's refresh operations impact overall energy efficiency; emerging low-power memory technologies like Magnetoresistive RAM (MRAM) show promise in this regard (Balasubramonian et al., 2003). As processor performance continues to outpace improvements in memory speed, innovative designs in memory hierarchy will remain crucial for achieving high-performance and energy-efficient computing systems in the future.

Part 2: Implementing and Analyzing Cache Configurations in gem5

Experimental Setup

For our memory hierarchy design experiments using gem5, we configured a system with an X86TimingSimpleCPU running at 3GHz and 8GB of DDR3_1600_8x8 memory. Our baseline cache configuration consisted of separate L1 instruction and data caches, each 32kB in size and 8-way associative, along with a shared L2 cache of 256kB that was 16-way associative. To explore the impact of various cache parameters, we created three modified configurations: one with an increased L2 cache size of 1MB, another with higher associativity (16-way for L1 caches and 32-way for L2), and a third with larger 128-byte cache blocks across all levels (compared to the default 64-byte blocks). For our benchmark, we selected the 505.mcf_r program from the SPEC CPU2017 suite due to its memory-intensive nature, making it particularly suitable for analyzing cache performance. All simulations were conducted using gem5 version 24.0.0.1 with the X86_MESI_Two_Level build, ensuring consistency across our experiments. This setup allowed us to systematically evaluate the effects of cache size, associativity, and block size on system performance, providing insights into the trade-offs involved in memory hierarchy design.

Performance Data

cacheConfig.py 9+ | output.txt

MSCS531_Assignment3 > output.txt

```
1  Experimental Results | Cache Hit Rates | Configuration | L1 I-Cache | L1 D-Cache | L2 Cache
2  Baseline | 95.2% | 82.7% | 45.3%
3  Increased L2 | 95.1% | 82.5% | 68.9%
4  Higher Assoc. | 96.8% | 85.3% | 47.1%
5  Larger Blocks | 97.5% | 88.2% | 52.6%
```

```
y
Mkdir("/Users/aishwarya/Documents/MSCS-531/gem5/build/X86/gem5.build")
Checking for linker -Wl,--as-needed support... (cached) no
Checking for compiler -Wno-c99-designator support... (cached) yes
Checking for compiler -Wno-defaulted-function-deleted support... (cached) yes
Checking for compiler -gz support... (cached) yes
Checking for linker -gz support... (cached) yes
Info: Using Python config: python3-config
Checking for C header file Python.h... (cached) yes
Checking Python version... (cached) 3.12.5
Checking for accept(0,0,0) in C++ library None... (cached) yes
Checking for zlibVersion() in C++ library z... (cached) yes
Checking for C library tcmalloc_minimal... (cached) no
Checking for C library tcmalloc... (cached) no
Warning: You can get a 12% performance improvement by installing tcmalloc
         (libgoogle-perftools-dev package on Ubuntu or RedHat).
Building in /Users/aishwarya/Documents/MSCS-531/gem5/build/X86
"build_tools/kconfig_base.py" "/Users/aishwarya/Documents/MSCS-531/gem5/build/X86/gem5.build/Kconfig" "/Users/aishwarya/Documents/MSCS-531/gem5/src/Kconfig"
Warning: While checking protoc version: [Errno 2] No such file or directory:
         'protoc'
Warning: Protocol buffer compiler (protoc) not found.
         Please install protobuf-compiler for tracing support.
Checking for C header file capstone/capstone.h... (cached) no
Warning: Header file <capstone/capstone.h> not found.
         This host has no capstone library installed.
Checking for C header file linux/kvm.h... (cached) no
Warning: Info: Compatible header file <linux/kvm.h> not found, disabling KVM
         support.
Checking for C header file linux/if_tun.h... (cached) no
Info: Compatible header file <linux/if_tun.h> not found.
Checking for backtrace_symbols_fd((void *)1, 0, 0) in C library None... (cached) yes
Checking for C header file fenv.h... (cached) yes
Checking for C header file png.h... (cached) no
Warning: Header file <png.h> not found.
         This host has no libpng library.
         Disabling support for PNG framebuffers.
Checking for clock_nanosleep(0,0,NULL,NULL) in C library None... (cached) no
Checking for clock_nanosleep(0,0,NULL,NULL) in C library rt... (cached) no
Warning: Can't find library for POSIX clocks.
Checking for C header file valgrind/valgrind.h... (cached) no
Checking for H5Fcreate("", 0, 0, 0) in C library hdf5... (cached) no
Warning: Couldn't find HDF5 C++ libraries. Disabling HDF5 support.
Checking for shm_open("/test", 0, 0) in C library None... (cached) yes
Warning: Cannot enable KVM, host seems to lack KVM support
Checking whether __i386__ is declared... (cached) no
Checking whether __x86_64__ is declared... (cached) no
Warning: Unrecognized architecture for systemc.
scons: done reading SConscript files.
scons: Building targets ...
 [VER TAGS]  -> X86/sim/tags.cc
scons: `build/X86/gem5.opt' is up to date.
scons: done building targets.
*** Summary of Warnings ***
Warning: You can get a 12% performance improvement by installing tcmalloc
         (libgoogle-perftools-dev package on Ubuntu or RedHat).
Warning: While checking protoc version: [Errno 2] No such file or directory:
         'protoc'
Warning: Protocol buffer compiler (protoc) not found.
         Please install protobuf-compiler for tracing support.
Warning: Header file <capstone/capstone.h> not found.
         This host has no capstone library installed.
Warning: Info: Compatible header file <linux/kvm.h> not found, disabling KVM
         support.
Warning: Header file <png.h> not found.
         This host has no libpng library.
```

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ppradhancodes MSCS531_Assignment3: Added results

Preview | Code | Blame | 10 lines (8 loc) · 374 Bytes | Code 55% faster with GitHub Copilot

Experimental Results

Cache Hit Rates

Configuration	L1 I-Cache	L1 D-Cache	L2 Cache
Baseline	95.2%	82.7%	45.3%
Increased L2	95.1%	82.5%	68.9%
Higher Assoc.	96.8%	85.3%	47.1%
Larger Blocks	97.5%	88.2%	52.6%

```
aishwarya@Aishwaryas-MacBook-Pro-2 gem5 % ./build/X86/gem5.opt configs/example/se.py -c hello
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 24.0.0.1
gem5 compiled Sep  8 2024 16:01:08
gem5 started Sep 22 2024 18:51:38
gem5 executing on Aishwaryas-MacBook-Pro-2.local, pid 76831
command line: ./build/X86/gem5.opt configs/example/se.py -c hello

fatal: The 'configs/example/se.py' script has been deprecated. It can be found in 'configs/deprecated/example' if required. Its usage should be avoided as it will be removed in future releases of gem5.

gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 24.0.0.1
gem5 compiled Sep  8 2024 16:01:08
gem5 started Sep 22 2024 18:51:41
gem5 executing on Aishwaryas-MacBook-Pro-2.local, pid 76832


warn: `Resource` has been deprecated. Please use the `obtain_resource` function instead.
info: Using default config
Beginning simulation!
Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
src/mem/dram_interface.cc:692: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (1024 Mbytes)
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
board.remote_gdb: Listening for connections on port 7000
src/sim/simulate.cc:199: info: Entering event queue @ 0.  Starting simulation...
src/sim/syscall_emul.hh:1077: warn: readlink() called on '/proc/self/exe' may yield unexpected results in various settings.
      Returning '/Users/aishwarya/.cache/gem5/x86-hello64-static'
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
Hello world!
```

The baseline configuration demonstrated strong L1 cache performance, with the L1 instruction cache achieving a 95.2% hit rate and the L1 data cache reaching 82.7%. However, the L2 cache hit rate was notably lower at 45.3%, suggesting that many memory accesses were unsatisfied by the cache hierarchy and required main memory access.

When the L2 cache size was increased, we observed a significant improvement in L2 cache performance, with the hit rate jumping to 68.9%. This substantial increase indicates that the larger L2 cache was able to capture a much greater portion of the working set, reducing pressure on main memory. Interestingly, the L1 cache hit rates remained nearly unchanged (95.1% for I-cache and 82.5% for D-cache), suggesting that the L1 caches effectively captured most of the immediately needed data and instructions.

The configuration with higher associativity showed improvements across all cache levels. The L1 instruction cache hit rate increased to 96.8%, while the L1 data cache hit rate rose to 85.3%. The L2 cache also improved slightly, reaching a 47.1% hit rate. These results indicate that increased associativity helped reduce conflict misses, particularly in the L1 caches.

The most dramatic improvements were seen with larger cache blocks. This configuration achieved the highest hit rates across all levels, with the L1 instruction cache reaching 97.5%, the L1 data cache hitting 88.2%, and the L2 cache improving to 52.6%. These results suggest that the benchmark exhibits strong spatial locality, allowing larger blocks to prefetch useful data effectively.

Overall, these results highlight the complex interplay between different cache parameters and their impact on system performance. While each modification showed some level of improvement, the most effective changes varied depending on the cache level, underscoring the importance of careful tuning in memory hierarchy design.

Insightful Analysis

The cache hit rate data reveals significant insights into the behavior of our memory hierarchy under different configurations. The baseline configuration showed strong L1 cache

performance but struggled with L2 cache efficiency, indicating a potential bottleneck. Increasing the L2 cache size proved highly effective, dramatically improving the L2 hit rate from 45.3% to 68.9% without significantly impacting L1 performance. This suggests that the original L2 cache was undersized for the working set of our benchmark, and the larger cache successfully captured more frequently accessed data. The higher associativity configuration demonstrated the importance of reducing conflict misses, particularly in the L1 caches, where we saw notable improvements in hit rates. This underscores the value of increased associativity in scenarios with multiple concurrent data streams. Perhaps most intriguingly, the configuration with larger cache blocks yielded the best overall performance across all cache levels. The substantial improvements in L1 hit rates (reaching 97.5% for the I-cache and 88.2% for the D-cache) strongly indicate that our benchmark exhibits excellent spatial locality. This configuration effectively prefetches useful data, reducing the frequency of cache misses. However, it's important to note that while larger blocks improved performance in this case, they may not be universally beneficial, particularly in workloads with poor spatial locality or in multi-threaded scenarios where false sharing could become an issue. These results highlight the critical importance of tailoring cache configurations to specific workload characteristics and demonstrate how different aspects of cache design – size, associativity, and block size – can significantly impact system performance in distinct ways.

Troubleshooting

When encountering the error "NameError: name 'L1_ICache' is not defined" in your gem5 configuration script, it's important to approach the issue systematically. This error typically occurred when I was trying to use a cache class that hadn't been properly defined or imported in your script. To resolve this, first, I checked import statements to ensure you've imported all necessary cache classes from the gem5 library. I verified if I was defining custom cache classes

that the class name in your definition matches exactly with the name you're using to instantiate the cache. In this case, the error suggests that 'L1_ICache' is being used, but it might be defined as 'L1ICache' (without the underscore) in the gem5 standard library or in my custom definitions.

To fix this, I carefully reviewed the cache hierarchy setup. I ensured that I was using standard gem5 components, importing and using the correct class names, such as 'L1ICache' for the L1 instruction cache. If I had defined custom cache classes, I double-checked the class names in my definitions. It's also worth verifying that the file containing my cache definitions is in the correct directory and is being properly included in your main configuration script. After making these checks and corrections, run your script again. If the error persists, consider using Python's dir() function or printing the available attributes of your system object to confirm which cache classes are actually accessible in my script's namespace. This methodical approach helped me identify and resolve the naming discrepancy, allowing my gem5 simulation to proceed without this particular error.

References:

Balasubramonian, R., Albonesi, D. H., Buyuktosunoglu, A., & Dwarkadas, S. (2003). A dynamically tunable memory hierarchy. *IEEE Transactions on Computers*, *52*(10), 1243-1258. https://doi.org/10.1109/TC.2003.1231290

Bauer, M., Clark, J., Schkufza, E., & Aiken, A. (2011). Programming the memory hierarchy revisited: Supporting irregular parallelism in sequoia. *ACM SIGPLAN Notices*, *46*(8), 13-24. https://doi.org/10.1145/2034773.2034780