National Institute of Technology, Calicut

Computer Science & Engineering Department

CS4032D: Computer Architecture

Assignment-1

Important Instructions

- ➔ This is a group Assignment.
- ➔ Everyone in a group must submit a report (pdf), with all necessary plots and explanations, on EduServer for this assignment. Everyone in the group can have the same report, but the report must include a work distribution section.
- ➔ For all of the tasks, you need to use the **simplescalar** simulator.
- ➔ Each team will be given four specific benchmarks for the experiments which can be found at the link.

Table 1: Baseline System Configuration

Parameter	Value
Core	OoO, Single Core
Frequency	2 GHz
Fetch/Decode/Issue/Commit Width	2
IQ/LSQ size	64/32
ROB size	192
Branch Predictor	Bimodal
BTB/RAS size	4K/32
Cache Block Size	64 Bytes
L1 I-cache	32 KB, 4-way, 3-cycle latency, 32 MSHRs, LRU
L1 D-cache	32 KB, 4-way, 3-cycle latency, 32 MSHRs, LRU
L2 Cache (LLC)	256 KB, 16-way, 9-cycle latency, 32 MSHRs, LRU, Best Offset Prefetcher (BOP)
Main Memory	4 GB, DDR3 1600 MHz

Tasks

1. Analyse and compare the results of two cache replacement policies- LRU and MRU.
2. Identify the best-performing cache replacement policy among them.
3. Provide all necessary plots and a detailed explanation to justify your conclusion.
4. Plots may include the miss rate of cycle time, L1 miss rate.

Evaluation Guidelines

- For the plots, use the LRU as the baseline replacement policy and normalize the parameters for the ***MRU*** replacement policy with respect to the baseline configuration.
- Use absolute values for L1 miss rate comparison.