Expected Deliverables:

- Matlab Simulation Model – System & Bit Level.
- VHDL Simulation & Code.
- Validation in real time on FPGA evaluation board.

RES-URSC 2023-021

Name of ISRO Centre/Unit

U R Rao Satellite Centre, Bengaluru

Title of the research proposal

Development of Indigenous Instruction Set Simulator (ISS) & Profiler for SPARC V8 architecture (UT699 and GR740 processor in particular) for Linux OS

Name of Co PI from ISRO Centre/Unit

Ms. Sowbhagya

Contact Address of Co PI and e-mail id

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Area of Research

Software, SPARC-v8 LEON-3 ISA single core and multicore

Summary of the proposed research and expected deliverables

The aim of this project is to develop an indigenous instruction set simulator for SPARC V8 architecture with all resources as in UT699 and GR740 processor– including caches, memory controller, I/O, load Program Counter, simulate interrupts, CPU reset. Should be able to invoke multiple instances in a single system. The ISA developed has to be available in shared memory which will be accessed by custom application program. Block diagram of proposed ISS based system is as in Fig.

The Profiler will be used during debugging, measure software execution times.

Provision to execute all the above in Real time / Fast simulation provision.

Scope of the Work:

This Instruction set simulator will be the basic building block of Software in Loop Simulator and also it will be used as test bed for onboard software development.

Linkages to Space Programme:

Software in Loop Simulation for NGC system of all satellites.

Testing of onboard software for LEON based systems.

LEON emulation

SPARC-V8 emulation including cache memories, on-chip peripherals and memory controller, cache.
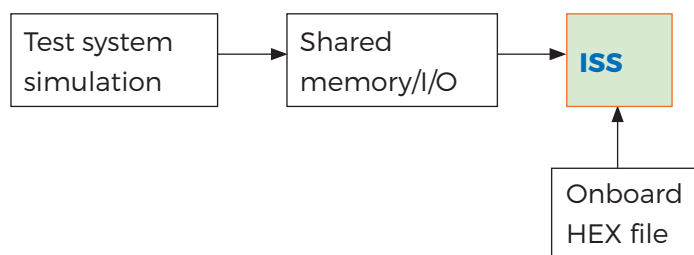
I/O emulation

to simulate user-defined I/O devices. The user can provide a module emulating an I/O device, which

can be loaded at run-time. The I/O module has access to the simulator event queue, interrupts and other internal data structures, allowing for accurate and timing true emulation. The I/O module is typically written in C, and can use any feature of the host operating system. This provides high simulation performance and capability to communicate with external simulator frameworks.

Expected Deliverables:

- C++ based instruction set simulator with source code for Linux based systems which includes:
  - SPARC-v8 LEON-3 processor UT699 ISA.
  - Emulation of Memory & I/O.
  - Caches.
  - Interrupts.
  - CPU reset, Program Counter.
  - Debugger.
- Profiler.

Fig: Block diagram of ISS based system

RES-URSC-2023-022

Name of ISRO Centre/Unit
U R Rao Satellite Centre, Bengaluru

Title of the research proposal
Real Time Anomaly Detection Using AI/ML for Spacecraft NGC applications

Name of Co PI from ISRO Centre/Unit
Ms. Priyanka V

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Area of Research
AI/ML

Summary of the proposed research and expected deliverables
The research work aims at real anomaly identification and its root cause AI/ML techniques. For spacecraft, this is essential for detecting off-nominal situations and responding accordingly. The software should able to classify the parameters to identify the anomaly in real time. A distinction is made between point anomalies, contextual anomalies and collective anomalies. For autonomous systems and anomaly detection, however, a consistent storage all mission data is essential to have a board database for state estimation, pattern recognition and decision-making. Anomaly detection is performed on time-