Chapter3:
Multiplexer, Latch, Buffer

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Objective

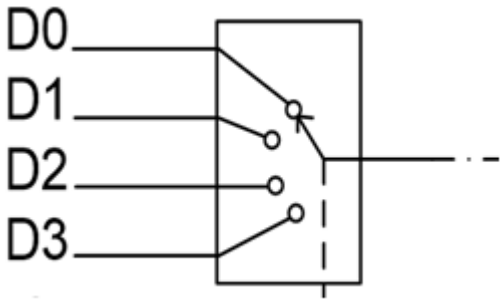
- Describe concept multiplexer and de-multiplexer circuit.
- Compare and contrast latch circuit and buffer circuit.
- Explain truth table of set-reset flipflop.

Topic

- Multiplexer circuit
- Demultiplexer circuit
- Latch circuit
- Buffer circuit
- Set-Reset Flipflop

MULTIPLEXER CIRCUIT

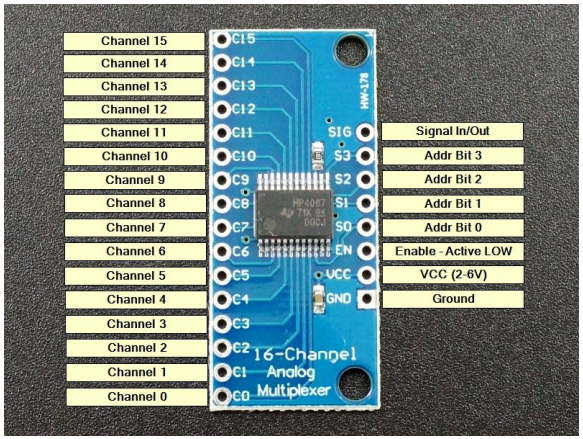
Selector switch

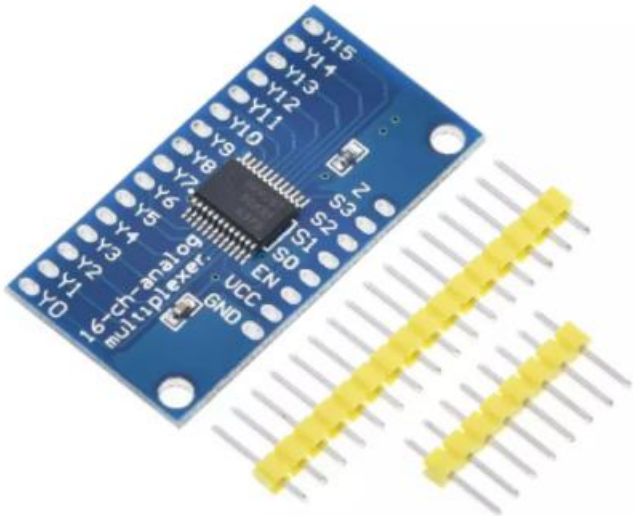


Selector switch is mechanical switch for selecting the signal channels

We found the selector switch in electrical machines, radio event if the car.

Switch -> Multiplexer (MUX)





LazGlobal CD74HC4067 16-Channel Analog Digital Multiplexer Breakout Board Module For Arduino

★★★★★ 1 คะแน

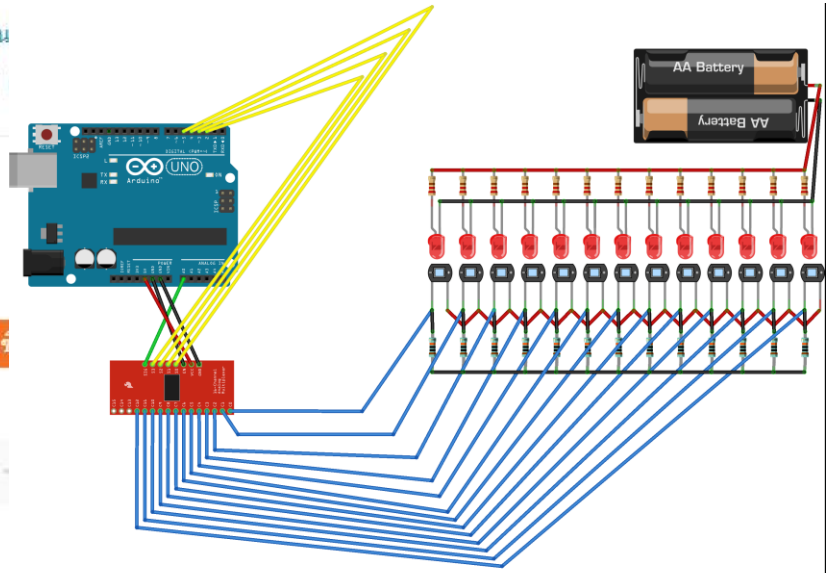
แบรนด์: No Brand |

฿36.00

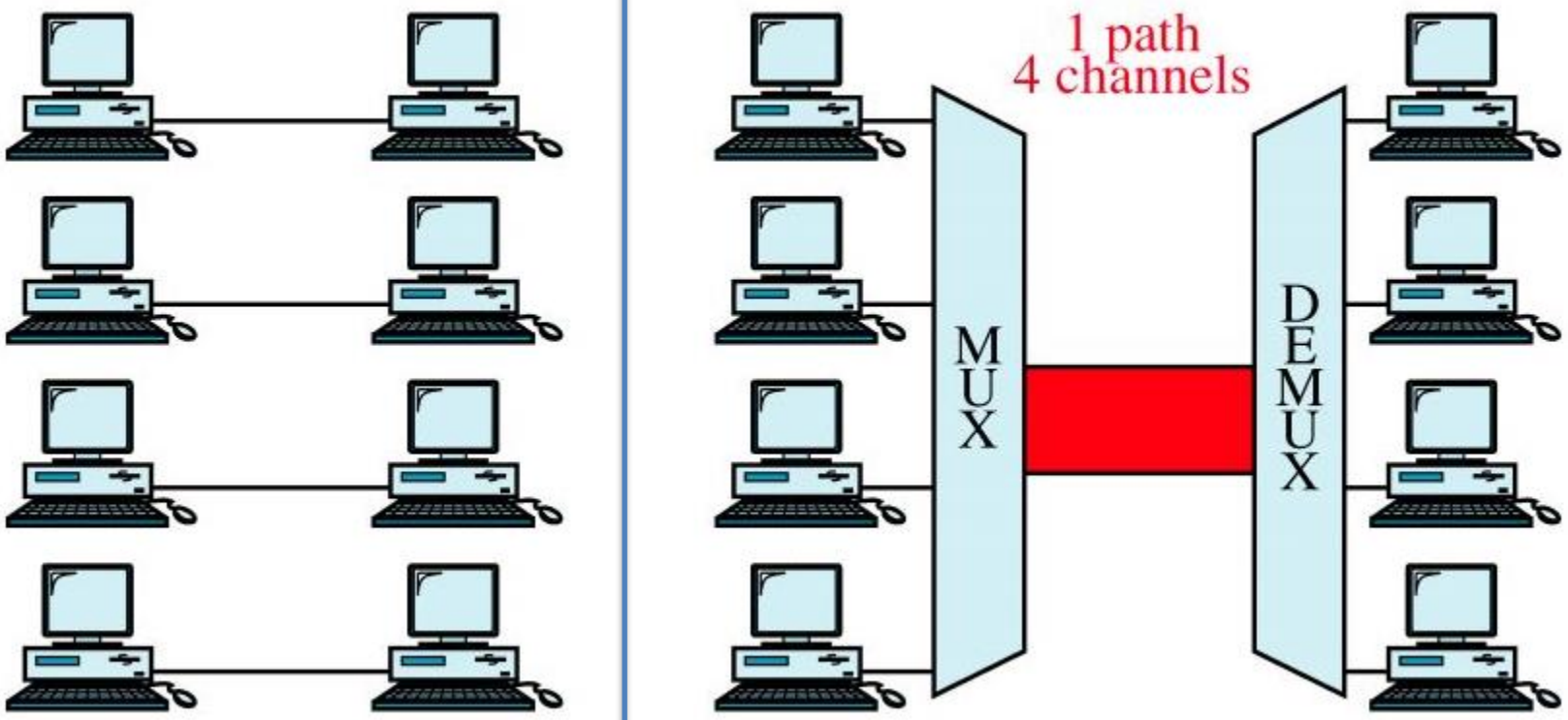
฿50.00 -28%

โปรโมชั่น

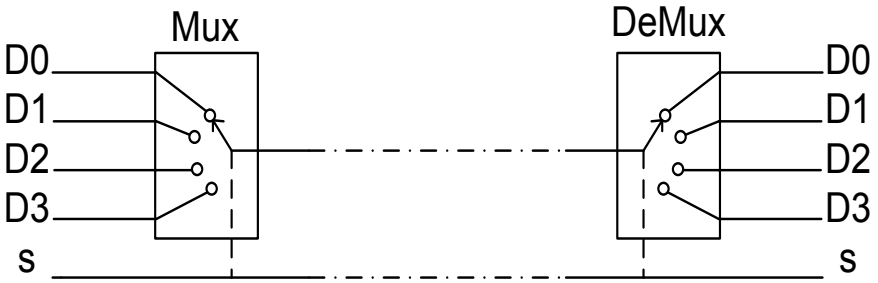
จำนวน

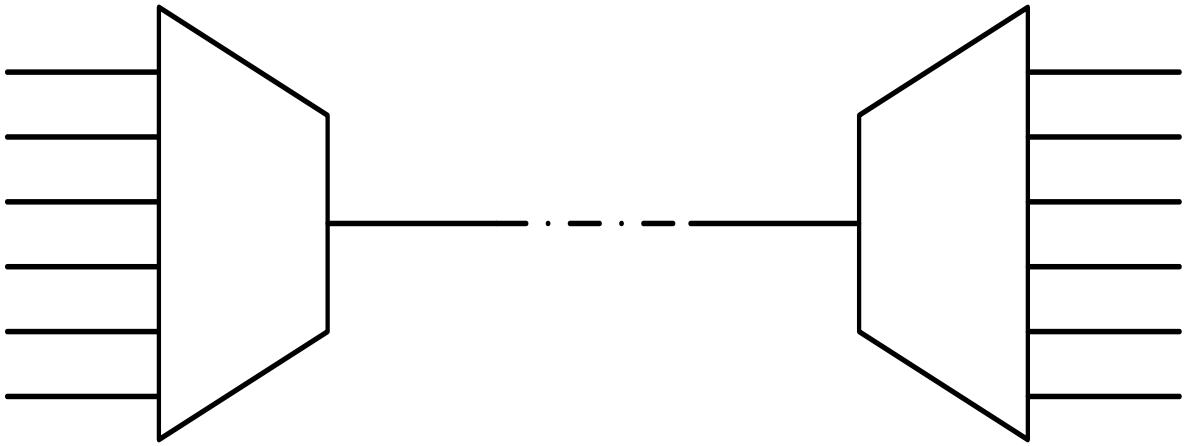


Compare between No MUX and MUX

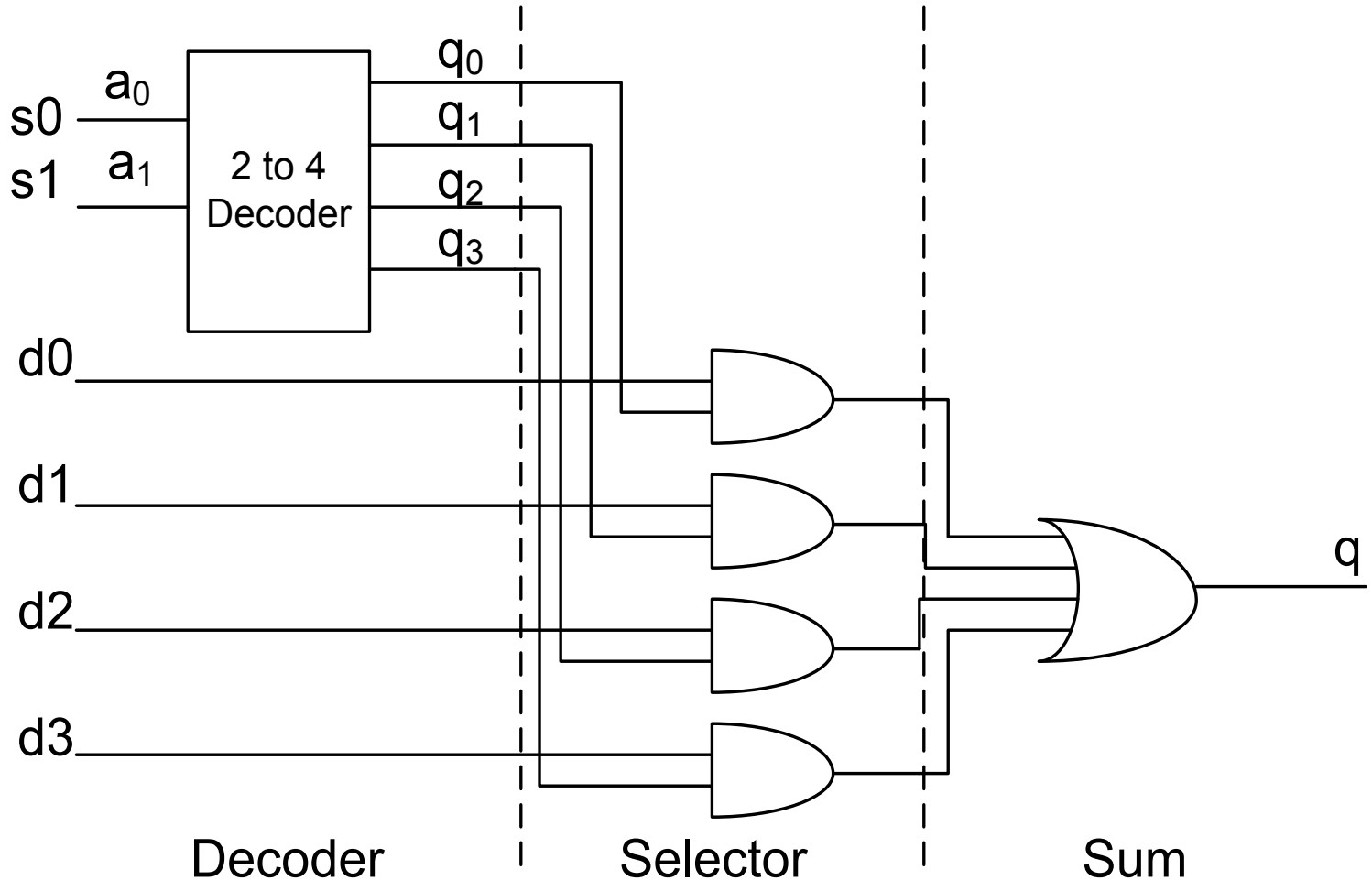


What is circuit inside MUX and DEMUX

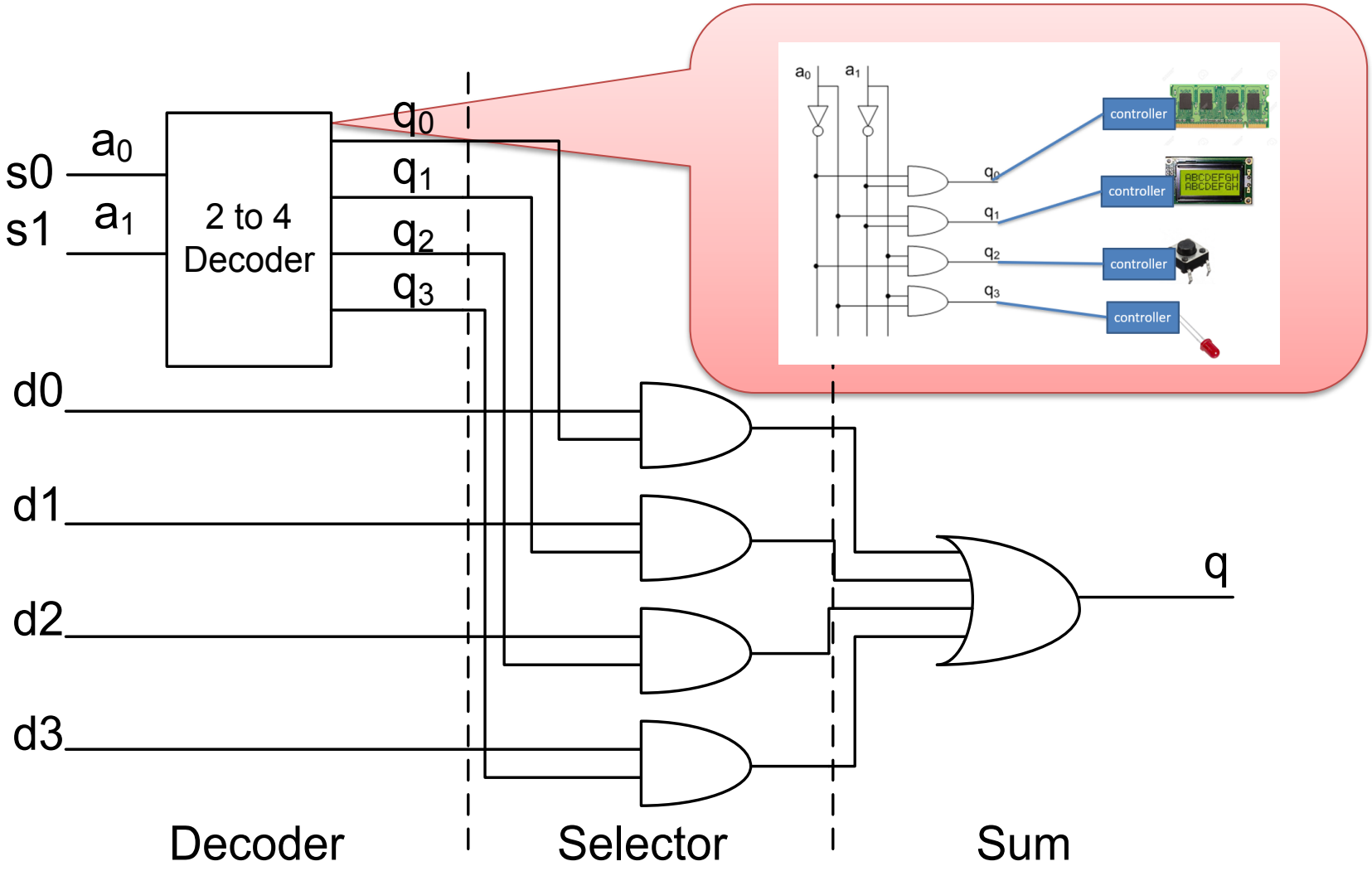




Multiplexer circuit

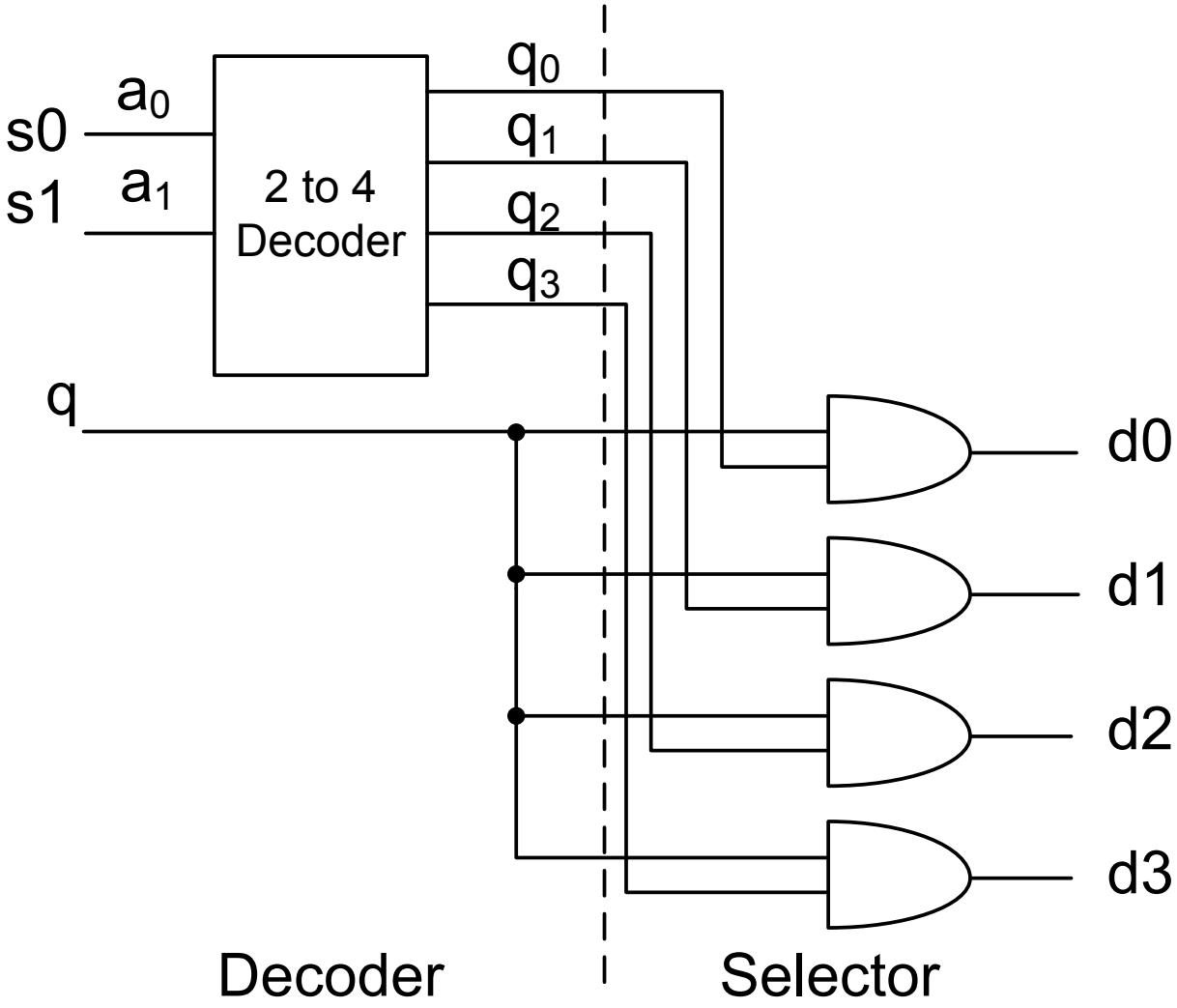


Multiplexer circuit

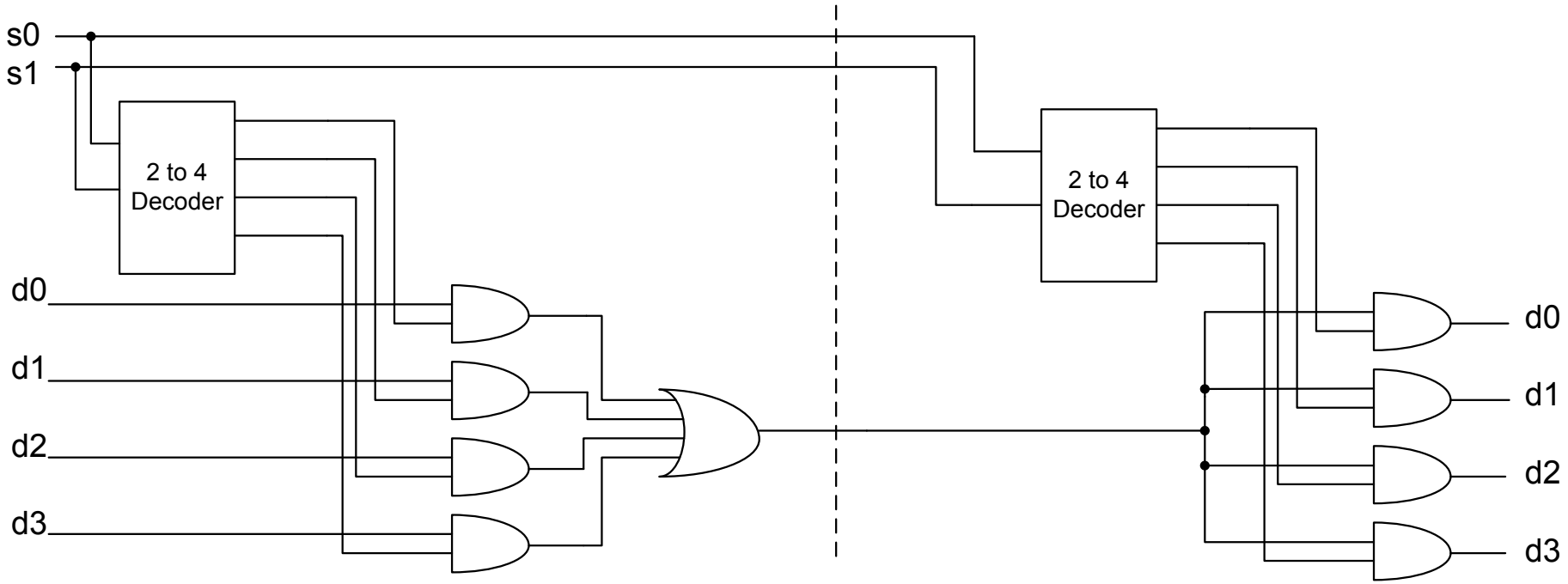


DEMULTIPLEXER CIRCUIT

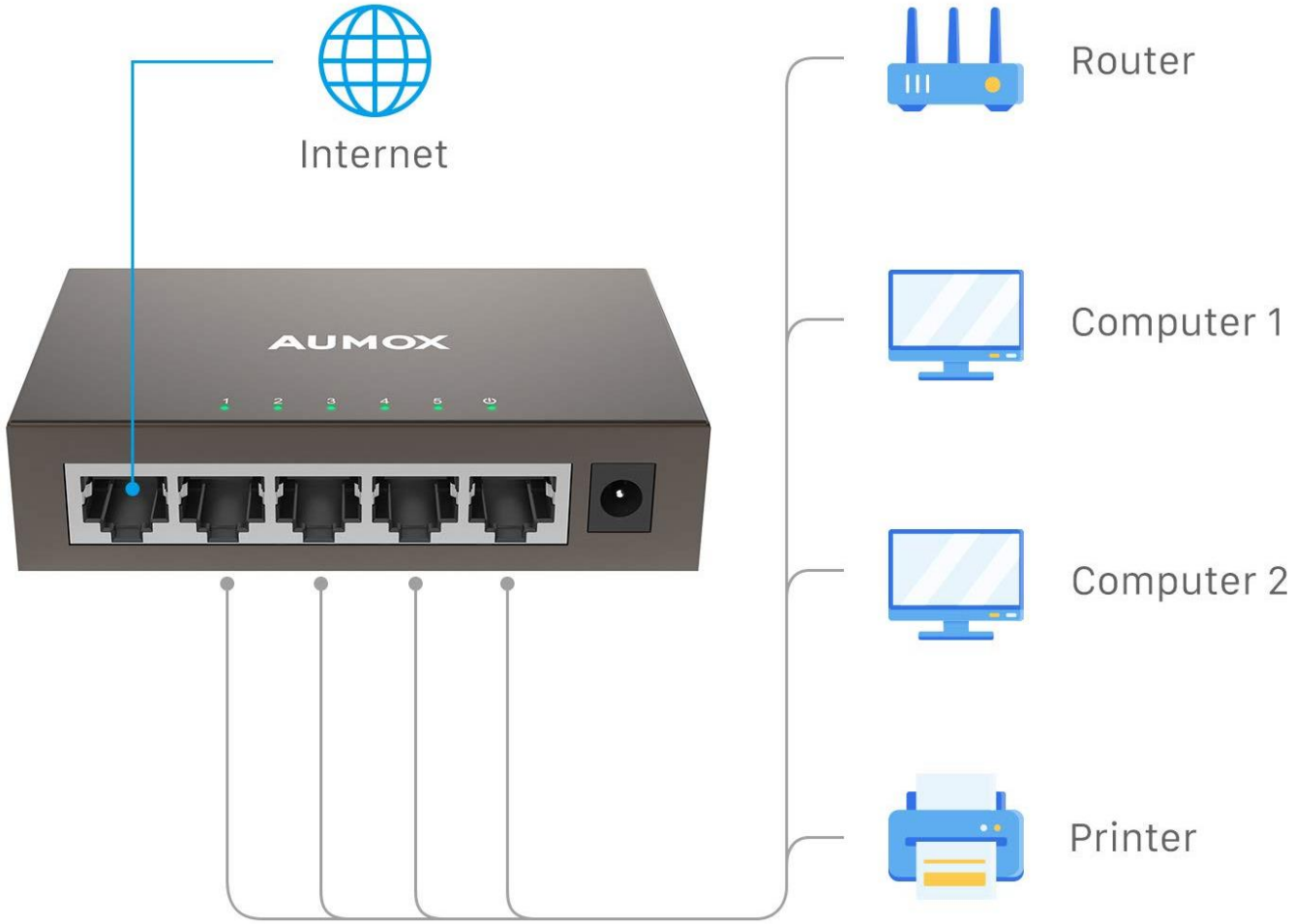
De-multiplexer circuit



MUX + DEMUX



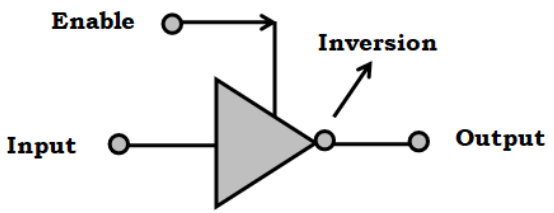
Example devices use MUX/DMUX



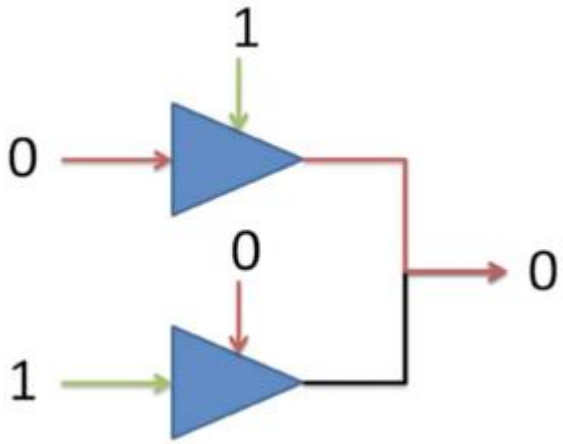
TRISTATE GATE

Tristate gate

- Tristate gate is three logic levels (H/L/Z)
- High impendence (Z) means two junction having high resistance over 1MΩ like open circuit.
- Tristate gate is applied to an output selector from two or more circuit.



Enable	Input	Output
0	0	Hi-Z
0	1	Hi-Z
1	0	1
1	1	0



Tristate gate datasheet and package

SN74LVC1G125 Single Bus Buffer Gate With 3-State Output

1 Features

- Available in the Ultra Small 0.64-mm^2 Package (DPW) With 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V_{CC}
- Max t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Cable Modem Termination System
- High-Speed Data Acquisition and Generation
- Military: Radar and Sonar
- Motor Control: High-Voltage
- Power Line Communication Modem
- SSD: Internal or External
- Video Broadcasting and Infrastructure: Scalable Platform
- Video Broadcasting: IP-Based Multi-Format Transcoder
- Video Communications System

3 Description

This bus buffer gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G125 device is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

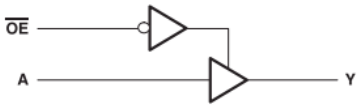
The SN74LVC1G125 device is available in a variety of packages including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

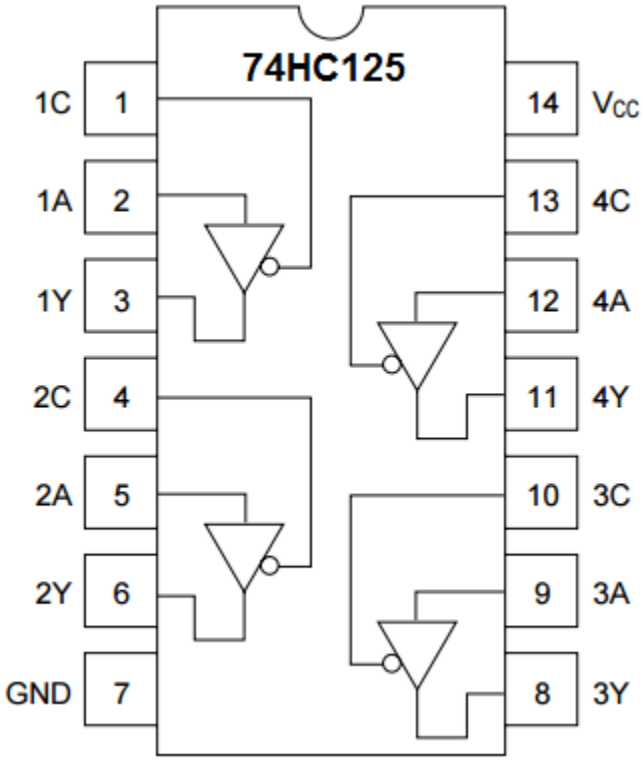
Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
SN74LVC1G125	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
	SON (6)	1.45 mm × 1.00 mm
	DSBGA (5)	1.40 mm × 0.90 mm
	X2SON (4)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic





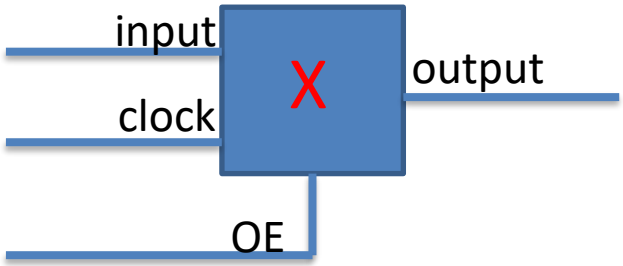
LATCH AND BUFFER

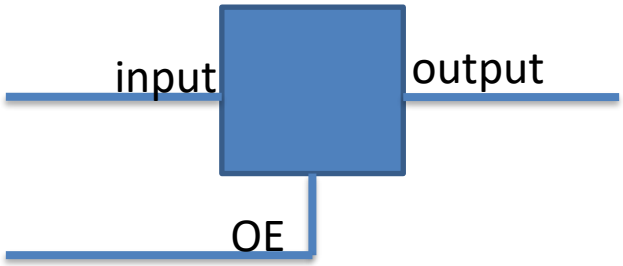
Latch vs Buffer

- Buffers and Latches are different in concepts and usages.
- Latch is in a digital circuit for holding data until a clearing or enable signal send to the latch then the data will be changed.
- Latch is just to hold memory.

- Buffer uses both analog and digital signal
- Buffer is not just to hold memory but also to increase output power or changing output impedance.

Latch/buffer concept





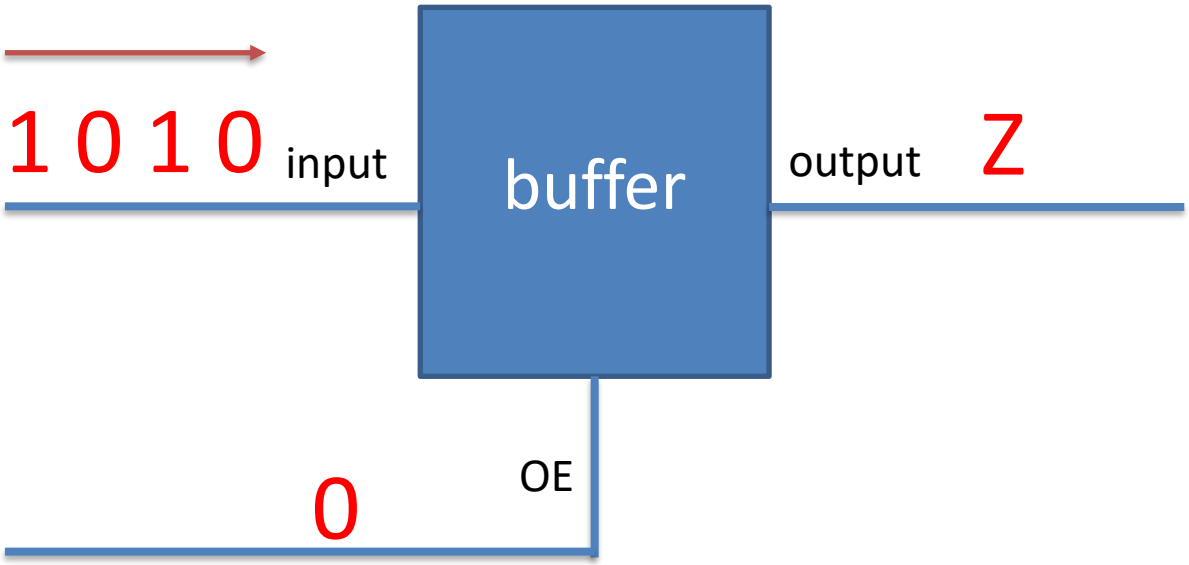
Latch circuit functions

- Hold data from inputs
- Control the data holding with clock/enable pin
- Have an output enable pin to control on/off output signal

Buffer circuit functions

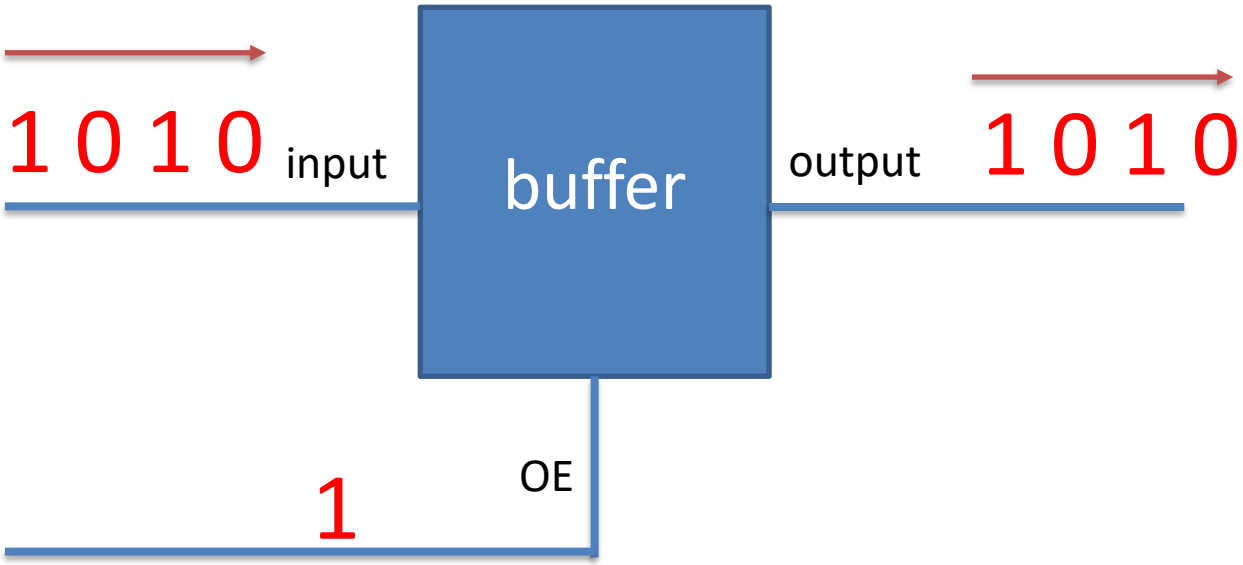
- No hold logic data
- Pass through by amplify the signal
- Some buffer has an enable pin to on/off output signal

Work of the buffer circuit



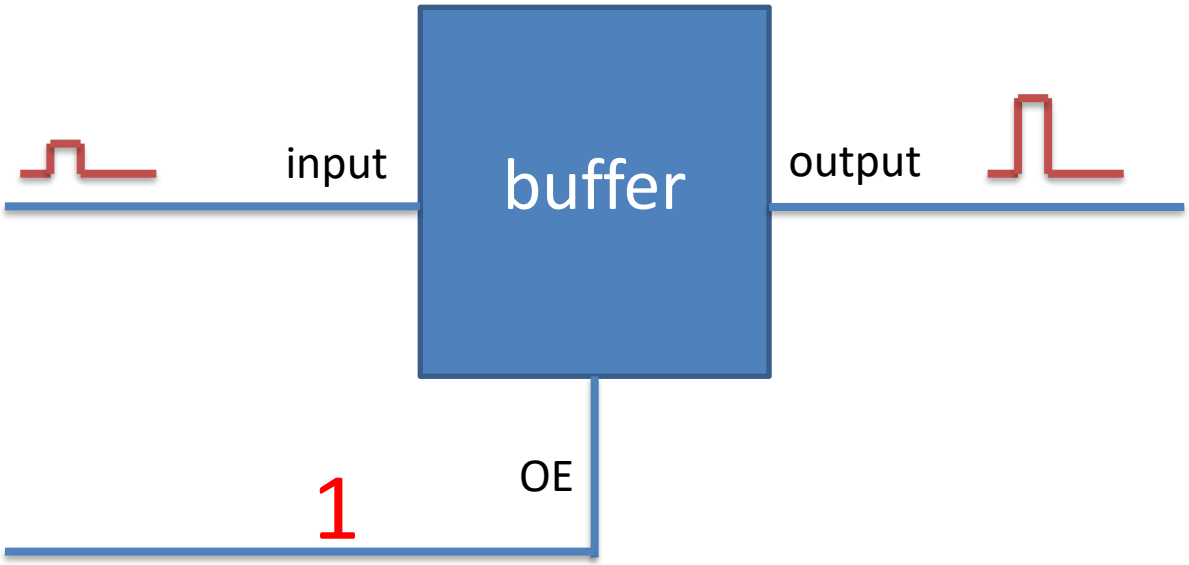
"Z" is a high-impedance state similarly no-connection state.

Work of the buffer circuit



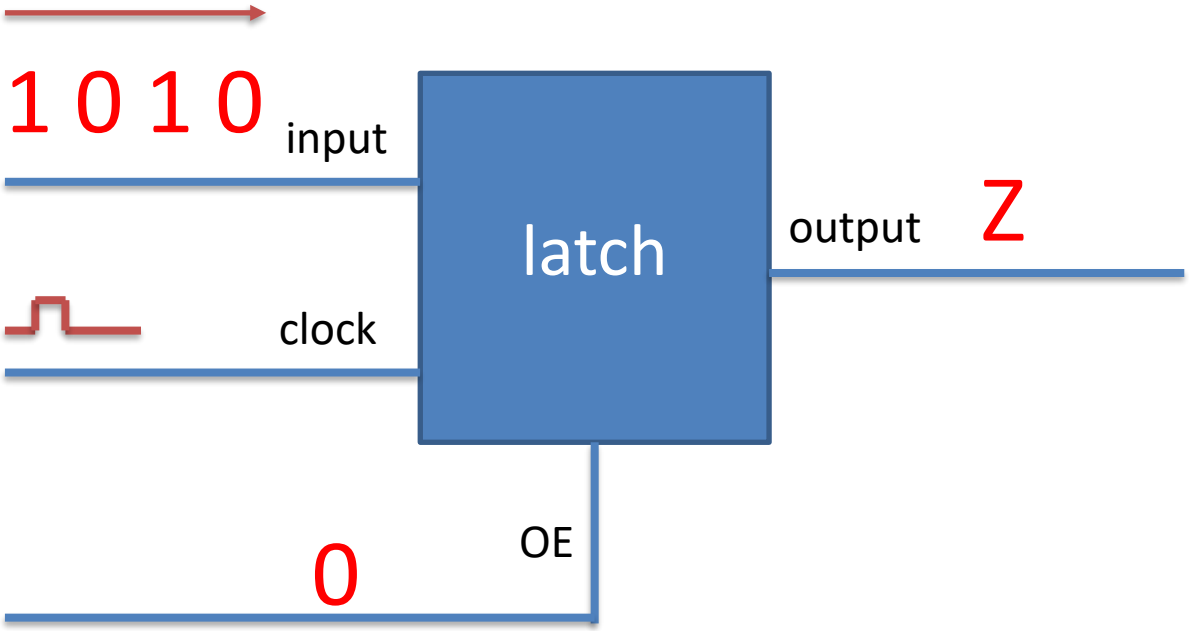
"Z" is a high-impedance state similarly no-connection state.

Work of the buffer circuit



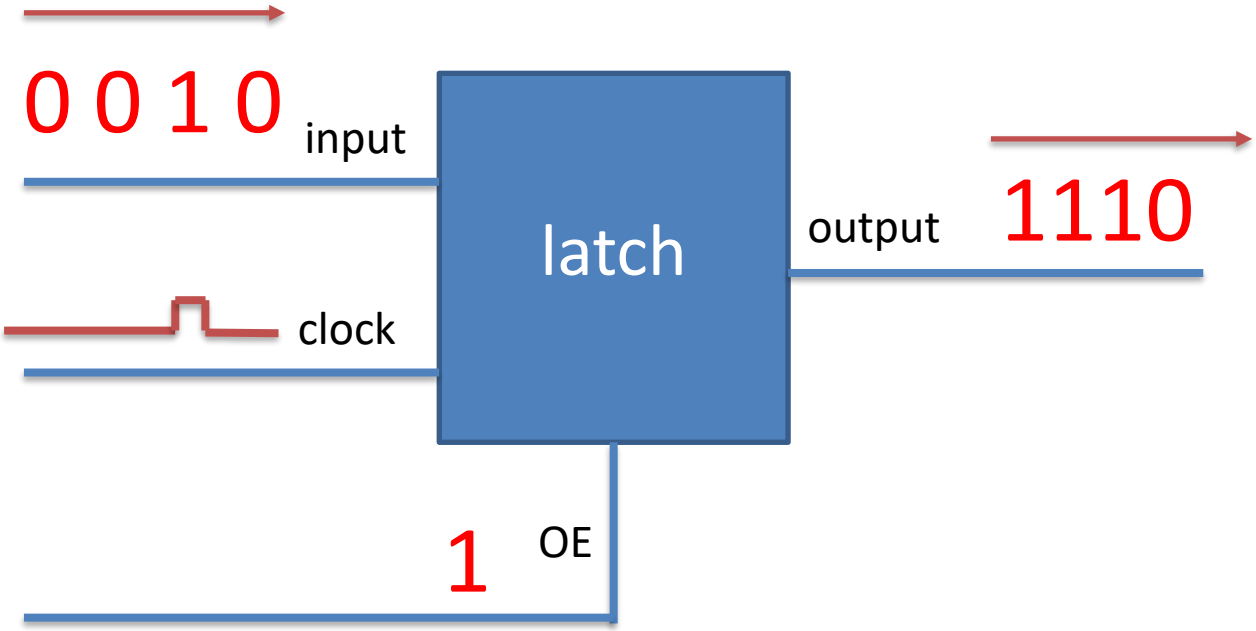
"Z" is a high-impedance state similarly no-connection state.

Work of the latch circuit



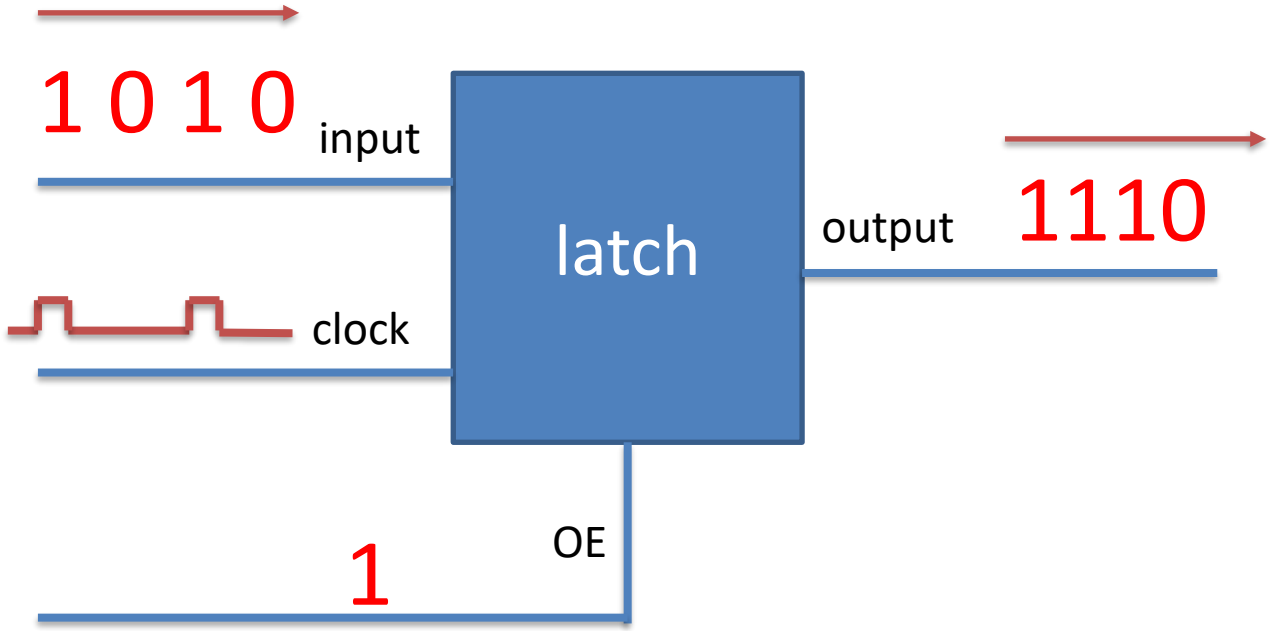
"Z" is a high-impedance state similarly no-connection state.

Work of the latch circuit



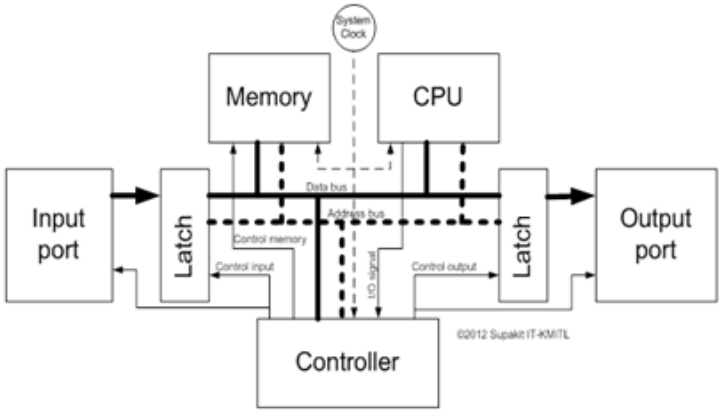
"Z" is a high-impedance state similarly no-connection state.

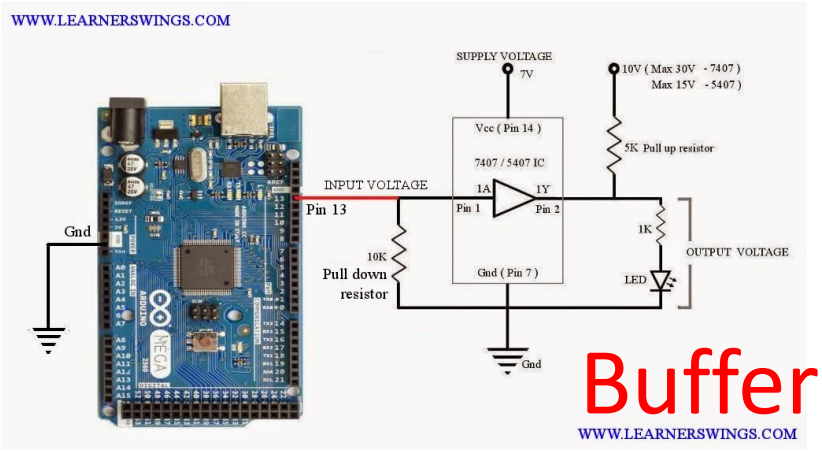
Work of the latch circuit



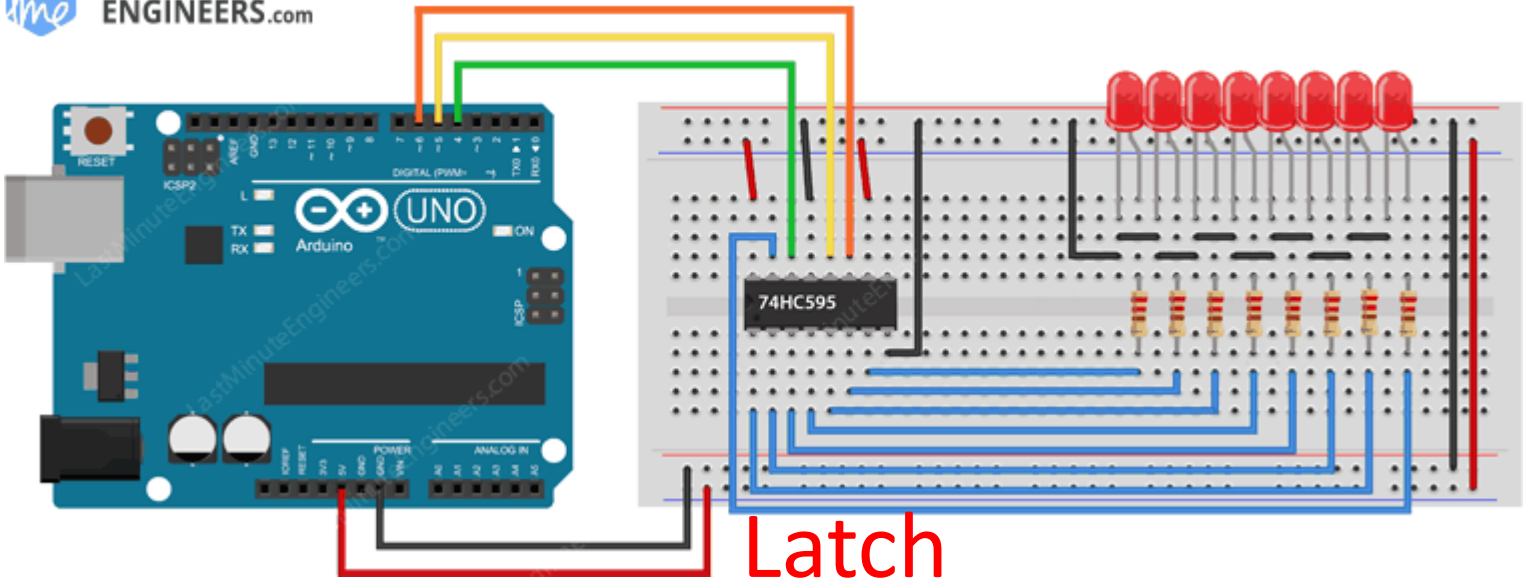
"Z" is a high-impedance state similarly no-connection state.

Latch/buffer in the computer



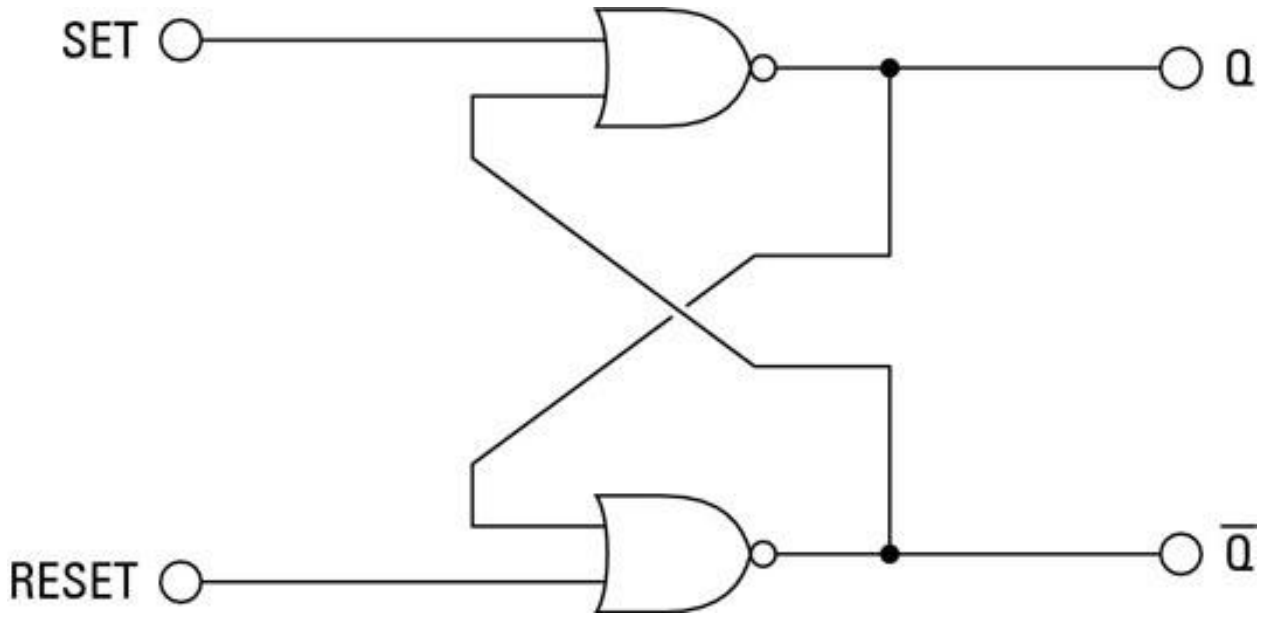


Last Minute ENGINEERS.com



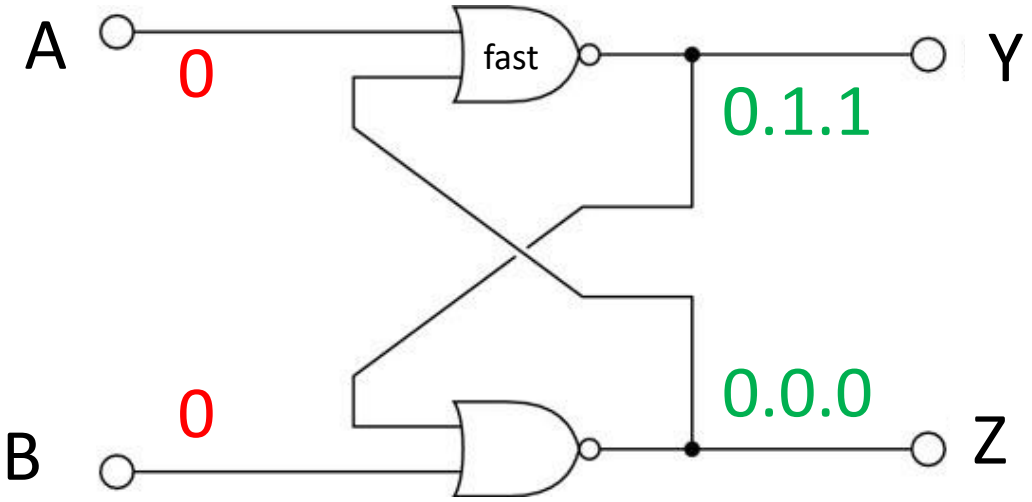
SET-RESET FLIP-FLOP

SR Flip-Flop truth table



S	R	Q	State
0	0	Previous state	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Forbidden

SR Flip-flop analysis



NOR

00 1

01 0

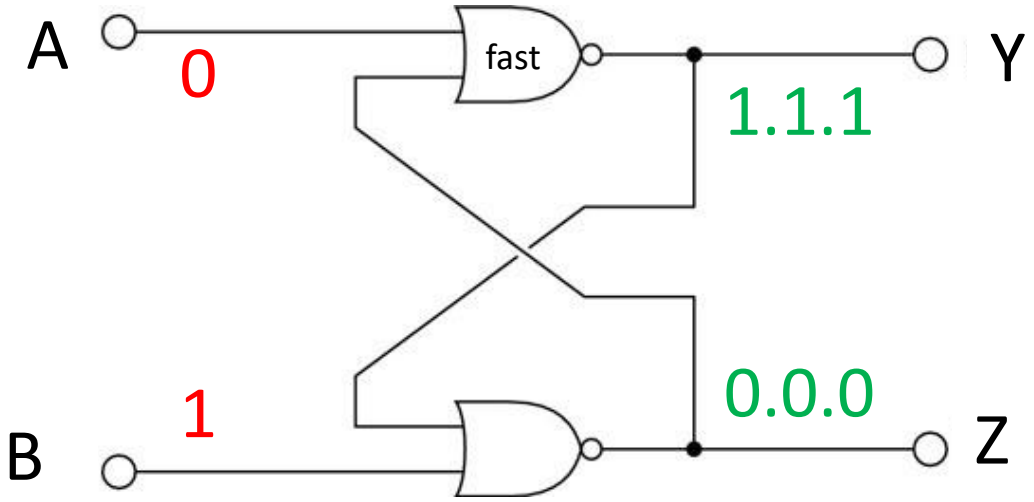
10 0

11 0

Step1

A	B	Y	Z
0	0	1	0
0	1		
0	0		
1	0		
0	0		
0	1		

SR Flip-flop analysis



NOR

00 1

01 0

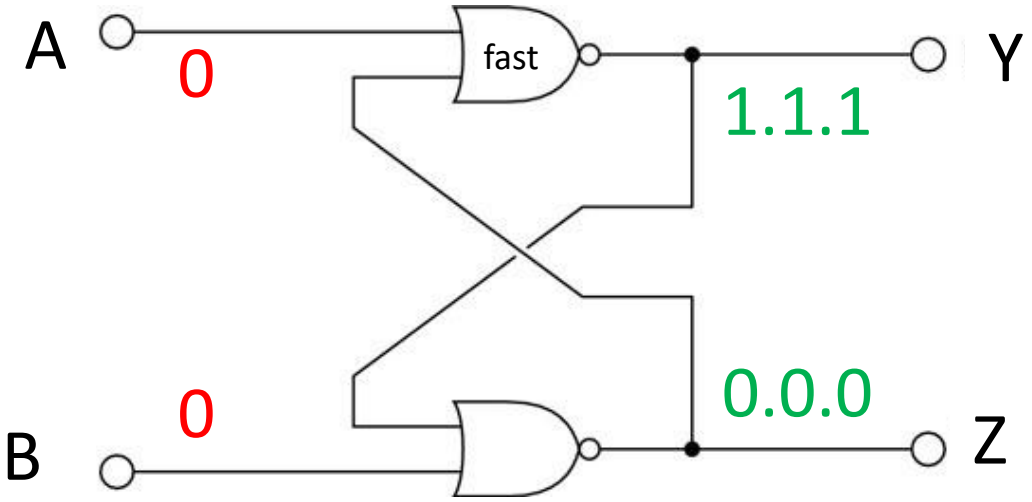
10 0

11 0

Step2

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0		
1	0		
0	0		
0	1		

SR Flip-flop analysis

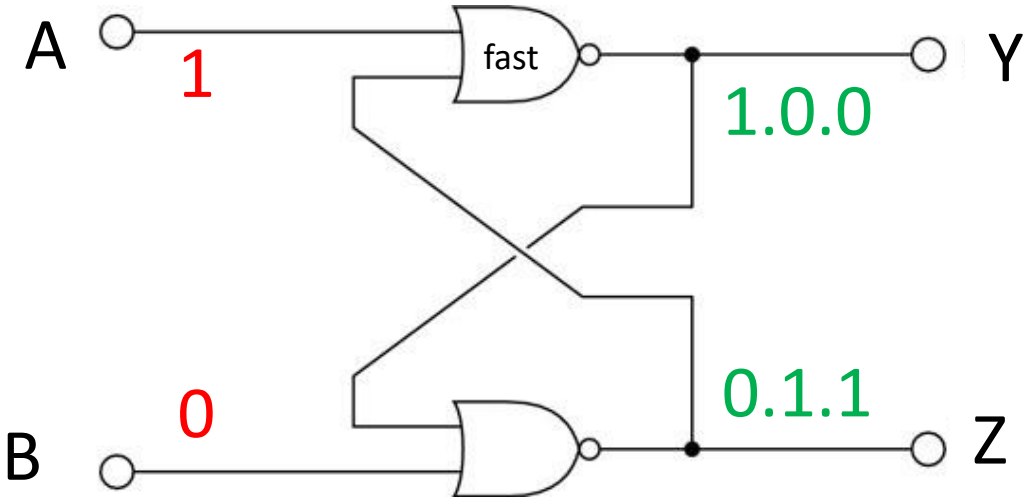


NOR
00 1
01 0
10 0
11 0

Step3

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0	1	0
1	0		
0	0		
0	1		

SR Flip-flop analysis

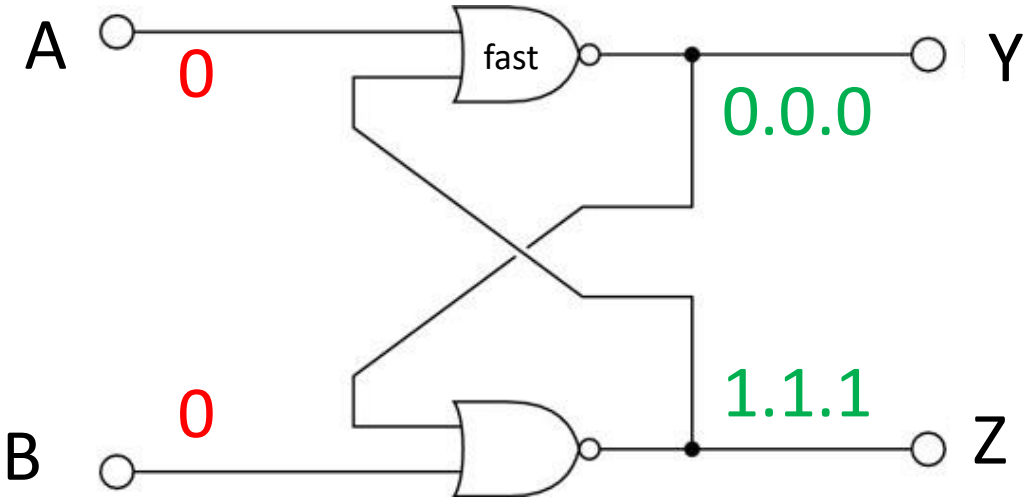


NOR
00 1
01 0
10 0
11 0

Step4

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0	1	0
1	0	0	1
0	0		
0	1		

SR Flip-flop analysis



NOR

00 1

01 0

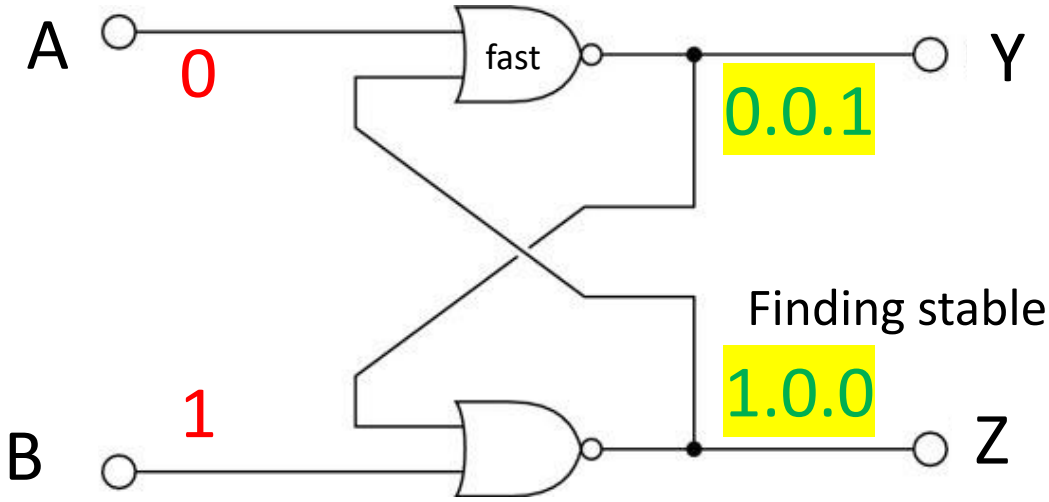
10 0

11 0

Step5

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0	1	0
1	0	0	1
0	0	0	1
0	1		

SR Flip-flop analysis



NOR

00 1

01 0

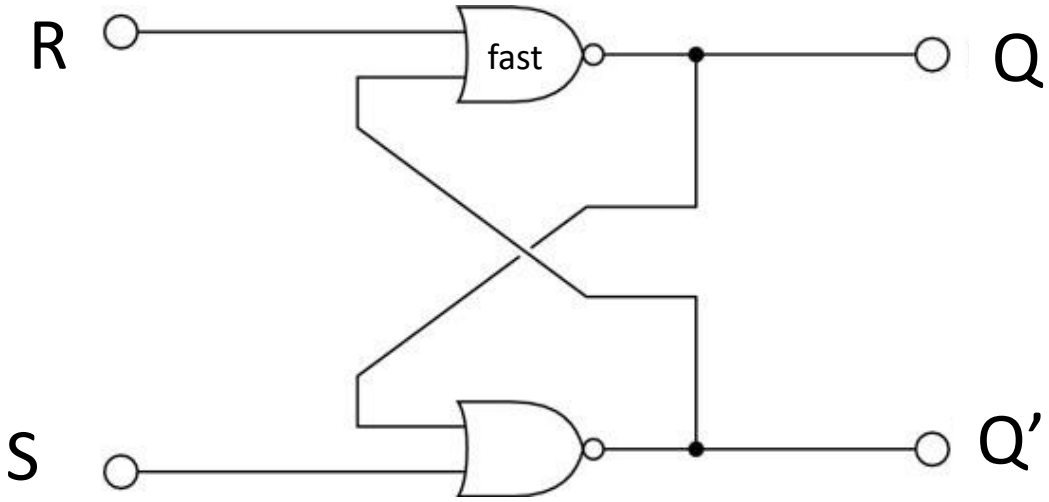
10 0

11 0

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0	1	0
1	0	0	1
0	0	0	1
0	1	1	0

Step6

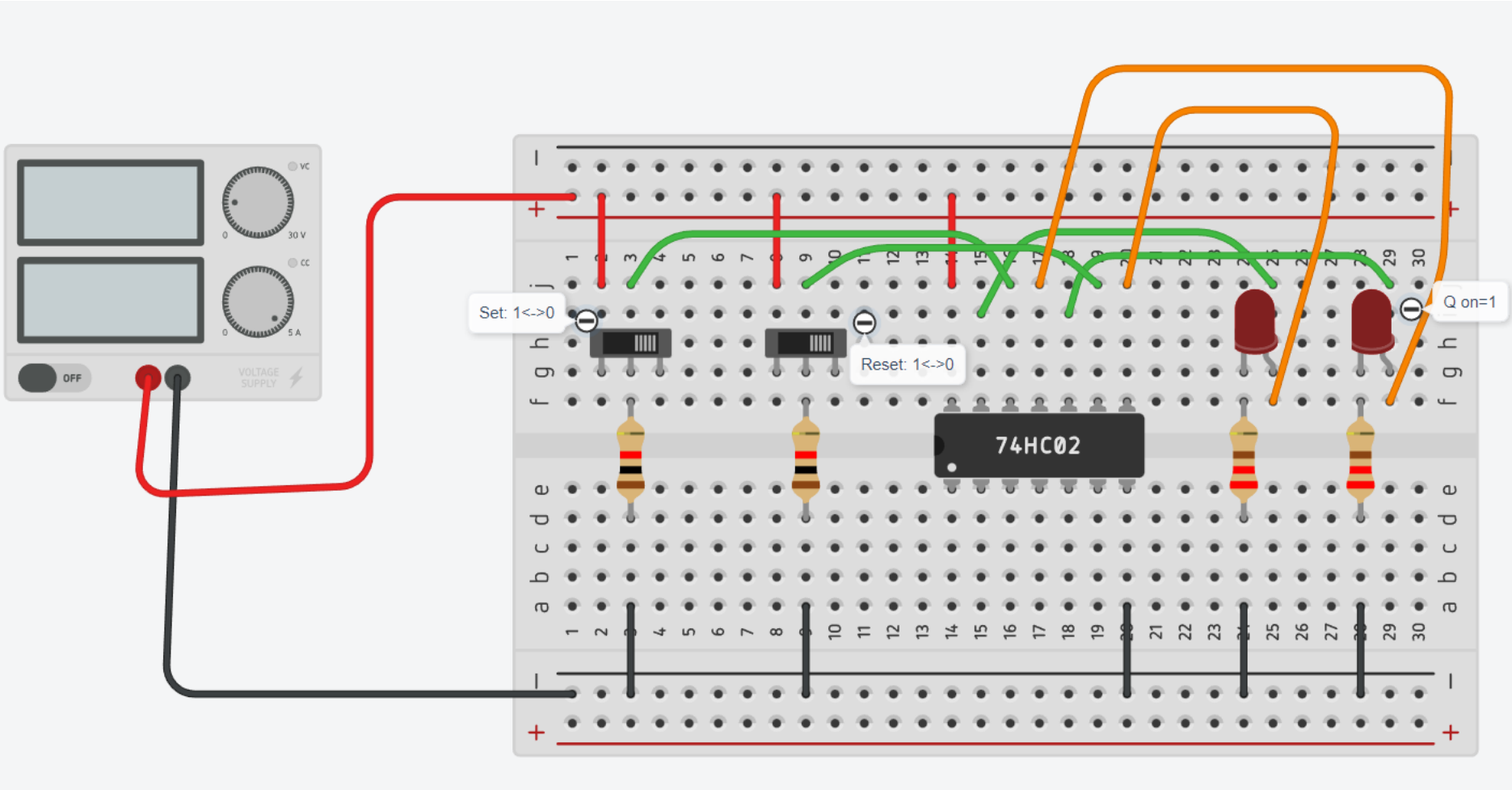
Truth table of SET/RESET – Flip Flop



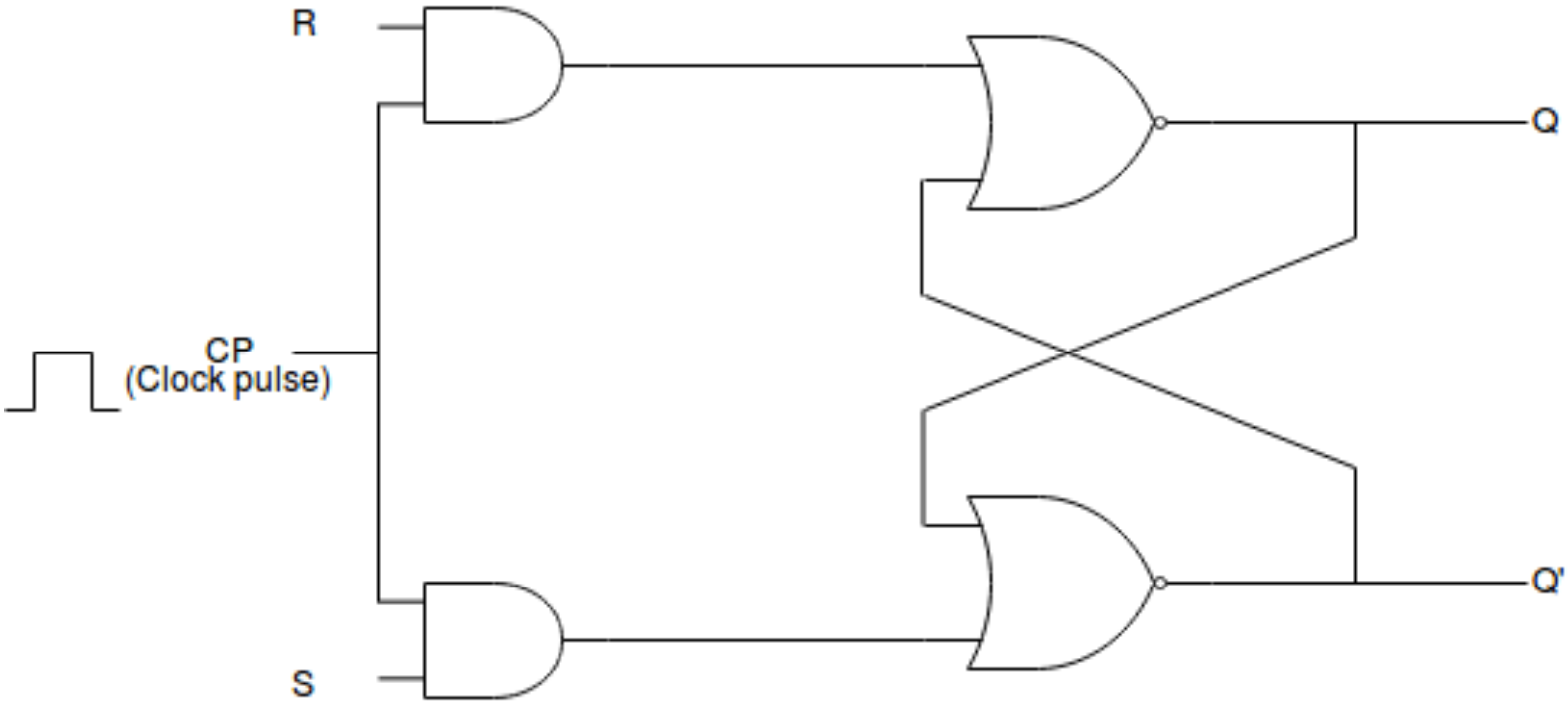
NOR
00 1
01 0
10 0
11 0

Reset	Set	Q	Q'	
0	0	1	0	
0	1	1	0	
0	0	1	0	No change
1	0	0	1	
0	0	0	1	No change
0	1	1	0	

Activity 3.1 Build the SR flipflop on ThinkerCAD



Activity 3.2 Build the SR flipflop with clock on ThinkerCAD



Reference