#### Boolean Minimization

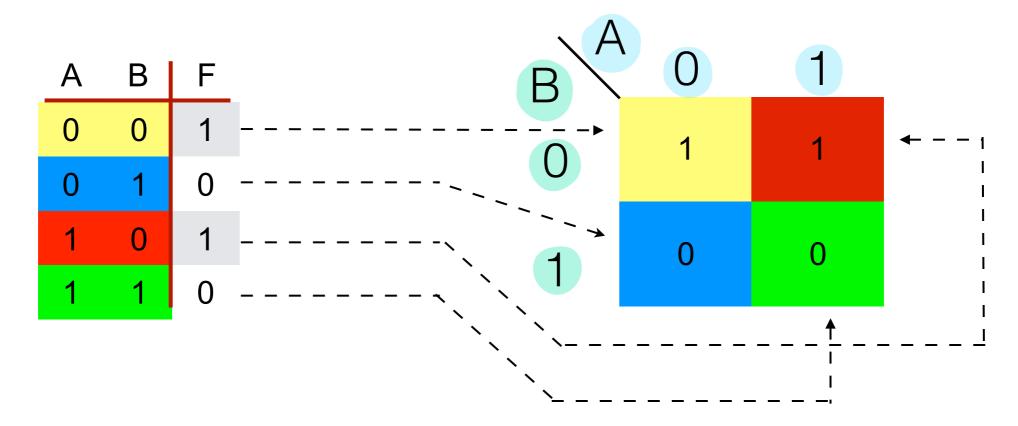
Lecture 4

#### Outline

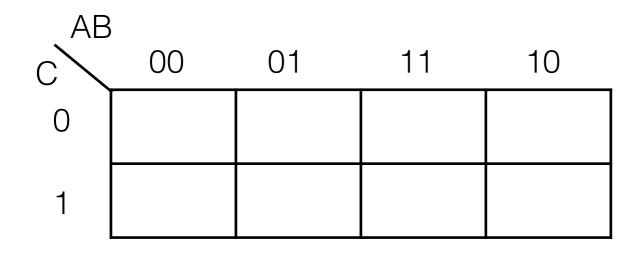
- Karnaugh-map
- Circuit design

## Karnaugh Map

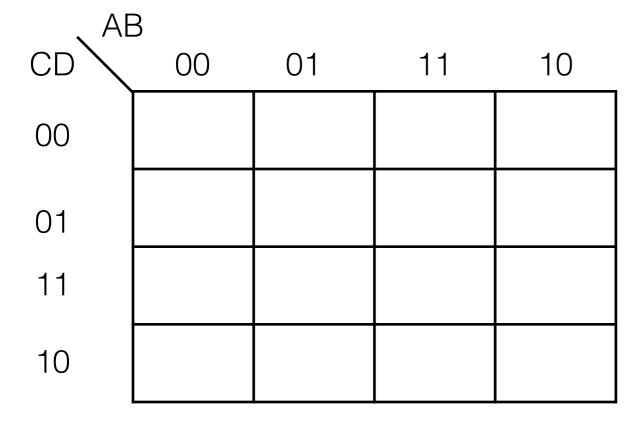
- Karnaugh Map (K-map) อาศัยการจัดเรียงตารางค่าความจริง ในรูปแบบ ใหม่ ซึ่งทำ ให้ สามารถลดรูปโดยอาศัยคุณสมบัติการคอมพลีเมนต์ได้ง่ายขึ้น
- ตัวอย่างของ K-map แบบ 2 ตัวแปร



#### Examples of K-Map



3-variable K-map

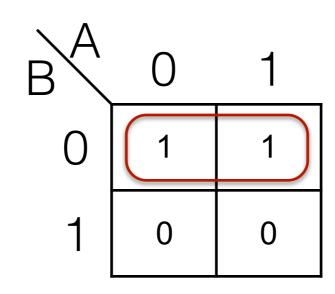


4-variable K-map

# Using K-Map

- หาช่องใน K-map ที่มีลอจิก 1 ติดกัน
- จำนวนช่องที่ ใช้ลดรูปต้องมีขนาด 2, 4, 8, ... เท่านั้น
- ตัวอย่าง

Α	В	F
0	0	1
0	1	0
1	0	1
1	1	0

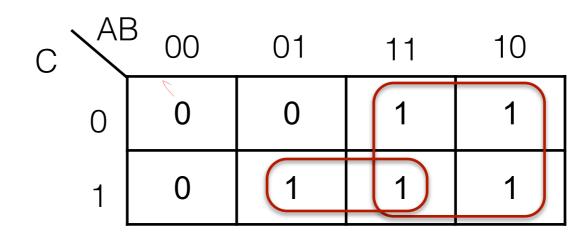


$$F = \overline{B}$$

# Using K-Map (2)

• ตัวอย่าง

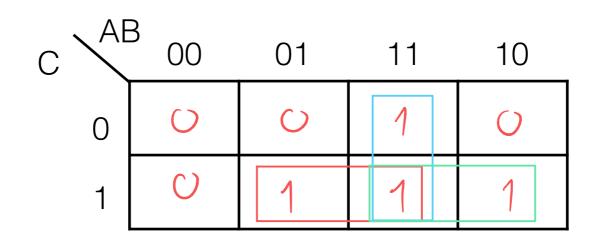
Α	В	С	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



$$F = A + BC$$

### Example

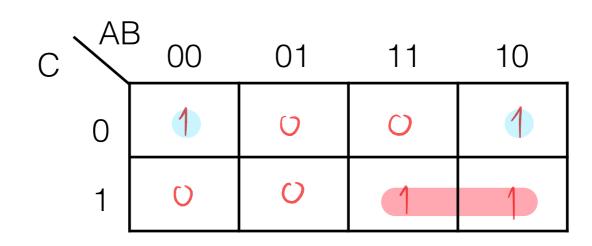
Α	В	С	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



$$F = BC + AB + AC$$

## Example (2)

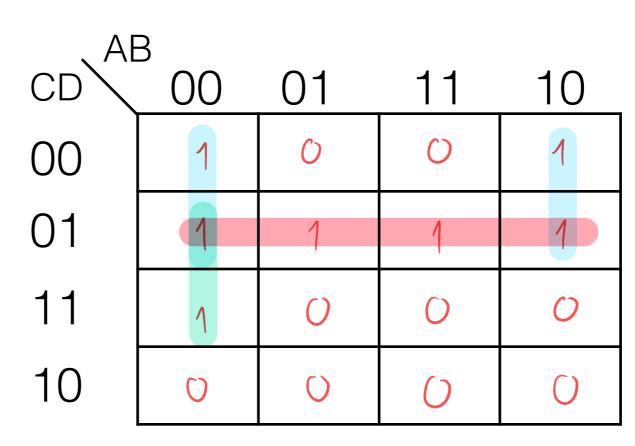
Α	В	С	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



$$F = AC + BC$$

# Example (3)

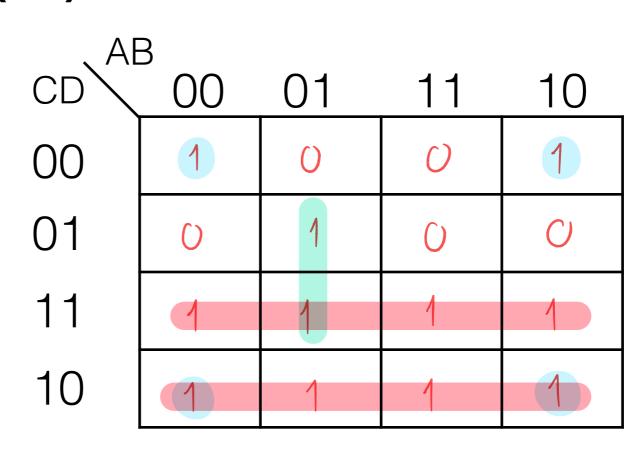
Α	В	С	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



$$F = \overline{CD} + \overline{BC} + \overline{ABD}$$

## Example (4)

Α	В	С	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1



$$F = C + \overline{BD} + \overline{ABD}$$

#### Don't Cares

- การใช้ประโยชน์จาก don't cares
- ตัวอย่าง

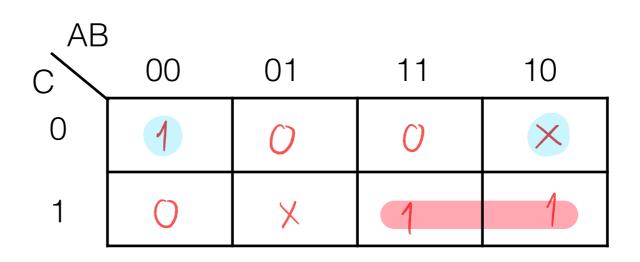
Α	В	С	F	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	1	
1	0	1	0	
1	1	0	X	ما ماء
1	1	1	х	don

$$F = BC + A\overline{C}$$

don't cares

## Example (5)

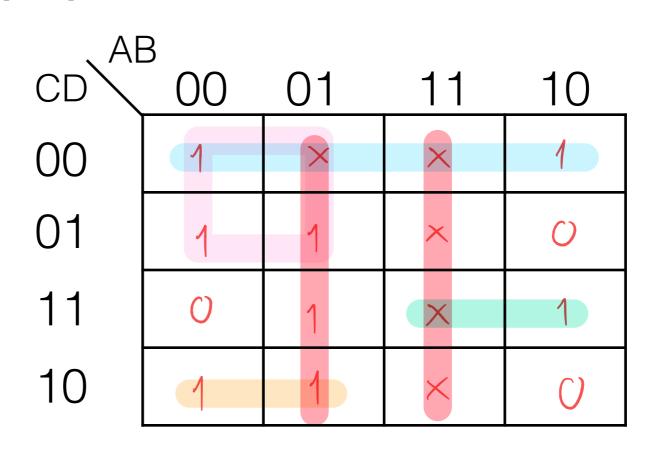
Α	В	С	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	X
1	0	0	X
1	0	1	1
1	1	0	0
1	1	1	1



$$F = AC + \overline{BC}$$

## Example (6)

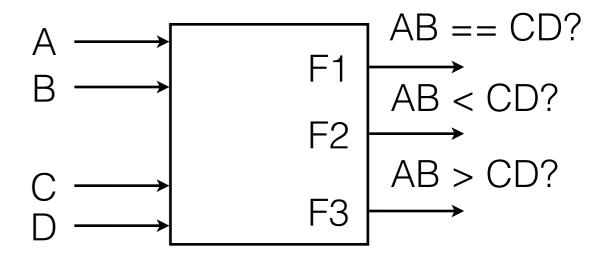
Α	В	С	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	Х
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	Х
1	1	0	1	Х
1	1	1	0	Х
1	1	1	1	Х



$$F = B + \overline{CD} + ACD + \overline{AC} + \overline{AC}$$

## Circuit Design

- ตัวอย่าง: ออกแบบ Two-bit Comparator
- Input Spec:
  - 2-bit input จำนวน 2 ตัว (AB, CD)
- Output Spec:
  - F1 เช็คว่า AB == CD
  - F2 เช็คว่า AB < CD</li>
  - F3 เช็คว่า AB > CD



#### Two-bit Comparator

Α	В	С	D	F1	F2	F3
0	0	0	0	1		
0	0	0	1	0		
0	0	1	0	0		
0	0	1	1	0		
0	1	0	0	0		
0	1	0	1	1		
0	1	1	0	0		
0	1	1	1	0		
1	0	0	0	0		
1	0	0	1	0		
1	0	1	0	1		
1	0	1	1	0		
1	1	0	0	0		
1	1	0	1	0		
1	1	1	0	0		
1	1	1	1	1		

CD\AE	3 00	01	11	10
00	1	O	0	O
01	O	1	O	O
11	0	0	1	0
10	O	O	O	1

$$F_1 = \overline{ABCD} + \overline{ABCD} + \overline{ABCD} + \overline{ABCD}$$

# Two-bit Comparator (2)

Α	В	С	D	F1	F2	F3
0	0	0	0		0	
0	0	0	1		1	
0	0	1	0		1	
0	0	1	1		1	
0	1	0	0		0	
0	1	0	1		0	
0	1	1	0		1	
0	1	1	1		1	
1	0	0	0		0	
1	0	0	1		0	
1	0	1	0		0	
1	0	1	1		1	
1	1	0	0		0	
1	1	0	1		0	
1	1	1	0		O	
1	1	1	1		0	

CD\AE	3 00	01	11	10
00	0	0	0	0
01	1	O	O	O
11	1	1	O	1
10	1	1	O	O

$$F_2 =$$

# Two-bit Comparator (3)

Α	В	С	D	F1	F2	F3
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

CD AE	3 00	01	11	10
00				
01				
11				
10				

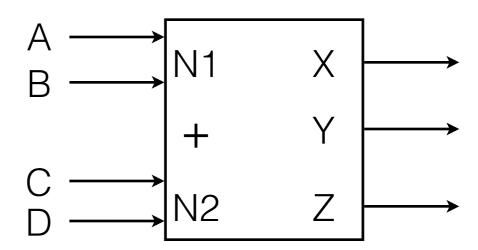
$$F_3 =$$

## Two-Bit Comparator (4)

Schematic Diagram

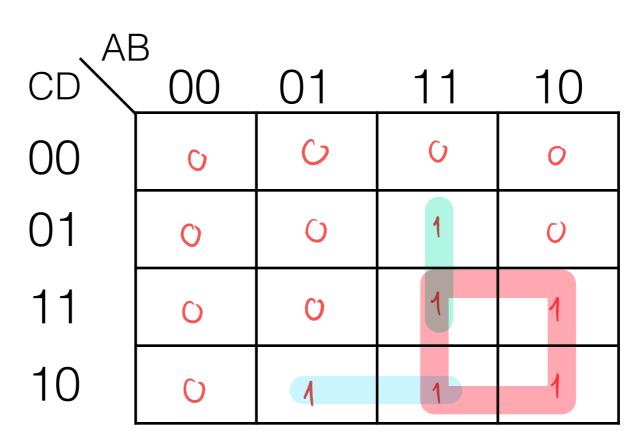
### Two-Bit Binary Adder

- ตัวอย่าง ออกแบบ Two-bit Binary Adder
- Input Spec
  - 2-bit input จำนวน 2 ตัว (AB, CD)
- Output Spec
  - 3-bit binary (XYZ)



# Two-bit Binary Adder (2)

Α	В	С	D	X	Υ	Z
0	0	0	0	0	0	0
0	0	0	1	O	O	1
0	0	1	0	U	1	O
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	O	1	O
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	O	1	0
1	0	0	1	O	1	1
1	0	0	1 0	0	1	1
				1 1	1 0 0	
1	0	1	0	0 1 1 0		0
1	0	1 1	0	O 1 1 O 1	0	0
1 1 1	0 0 1	1 1 0	0 1 0	1 1 0	0	0 1



$$X = AC + ABD + BCD$$

# Two-bit Binary Adder (3)

Α	В	С	D	Χ	Υ	Z
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

CD AE	3 00	01	11	10
00				
01				
11				
10				

$$Y =$$

## Two-bit Binary Adder (4)

Α	В	С	D	Χ	Y	Z
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

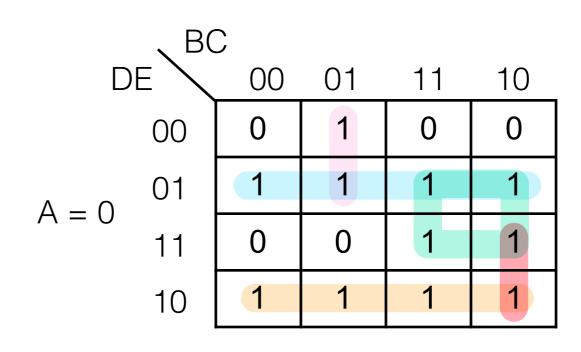
CD\AE	3 00	01	11	10
00				
01				
11				
10				

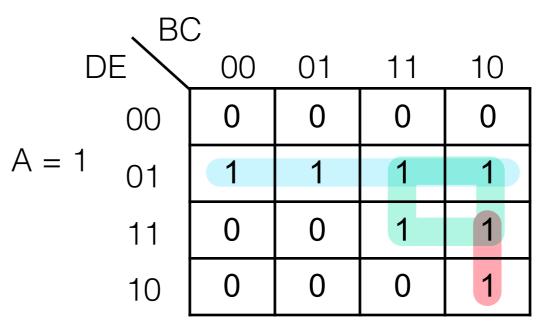
$$Z =$$

#### 5-Variable K-map

A	В	C	D	Е	F	G
0	0	0	0	0	0	1
0	0	0	0	1	1	0
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	1	0	0	1	X
0	0	1	0	1	1	X
0	0	1	1	0	1	1
0	0	1	1	1	0	1
0	1	0	0	0	0	1
0	1	0	0	1	1	0
0	1 1	0	0	1	1 1	0
0	1	0	1	0	1	1
0	1 1	0	1 1	0 1	1 1	1
0 0	1 1	0 0	1 1 0	0 1 0	1 1 0	1 1 x
0 0 0 0	1 1 1 1	0 0 1 1	1 1 0 0	0 1 0 1	1 1 0 1	1 1 x 1

Α	В	С	D	Ε	F	G
1	0	0	0	0	0	1
1	0	0	0	1	1	0
1	0	0	1	0	0	0
1	0	0	1	1	0	1
1	0	1	0	0	0	1
1	0	1	0	1	1	1
1	0	1	1	0	0	1
1	0	1	1	1	0	1
1	1	0	0	0	0	1
1	1	0	0	1	1	1
1	1	0	1	0	1	1
1	1	0	1	1	1	1
1	1	1	0	0	0	Х
1	1	1	0	1	1	1
1	1	1	1	0	0	1
1	1	1	1	1	1	1





## 5-Variable K-map (2)

Α	В	С	D	Е	F	G
0	0	0	0	0	0	1
0	0	0	0	1	1	0
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	1	0	0	1	X
0	0	1	0	1	1	X
0	0	1	1	0	1	1
0	0	1	1	1	0	1
0	1	0	0	0	0	1
0	1	0	0	0	0 1	0
0	1	0	0	1	1	0
0	1	0	0	1 0	1	0
0 0 0	1 1 1	0 0 0	0 1 1	1 0 1	1 1 1	0 1 1
0 0 0	1 1 1	0 0 0	0 1 1 0	1 0 1	1 1 1 0	0 1 1 x

Α	В	С	D	Е	F	G
1	0	0	0	0	0	1
1	0	0	0	1	1	0
1	0	0	1	0	0	0
1	0	0	1	1	0	1
1	0	1	0	0	0	1
1	0	1	0	1	1	1
1	0	1	1	0	0	1
1	0	1	1	1	0	1
1	1	0	0	0	0	1
1	1	0	0	1	1	1
1	1	0	1	0	1	1
1	1	0	1	1	1	1
1	1	1	0	0	0	Χ
1	1	1	0	1	1	1
1	1	1	1	0	0	1
1	1	1	1	1	1	1

