Chapter4:
Counter and
DAC & ADC Part-I

Asst.Prof.Dr.Supakit Nootyaskool

Objective

- Recognize type of flipflops and realize difference between rising edge/falling edge trigger.
- Clarify mechanism inside a counter circuit and express technique of counting up/down.
- Explain and illustrate concept of convert analog signal to digital signal.

Topic

- Combinational logic vs Sequential logic circuit
- Rising/Falling edge trigger
- JK-flipflop
- D-flipflop
- T-flipflop
- Frequency division circuit
- First-in first-out circuit
- Counter circuit
- Analog signal to Digital signal concept

COMBINATIONAL LOGIC CIRCUIT
VS
SEQUENTIAL LOGIC CIRCUIT

World of digital logic circuit

Combinational logic circuit

Sequential logic circuit

Key characteristics

Combinational logic circuit

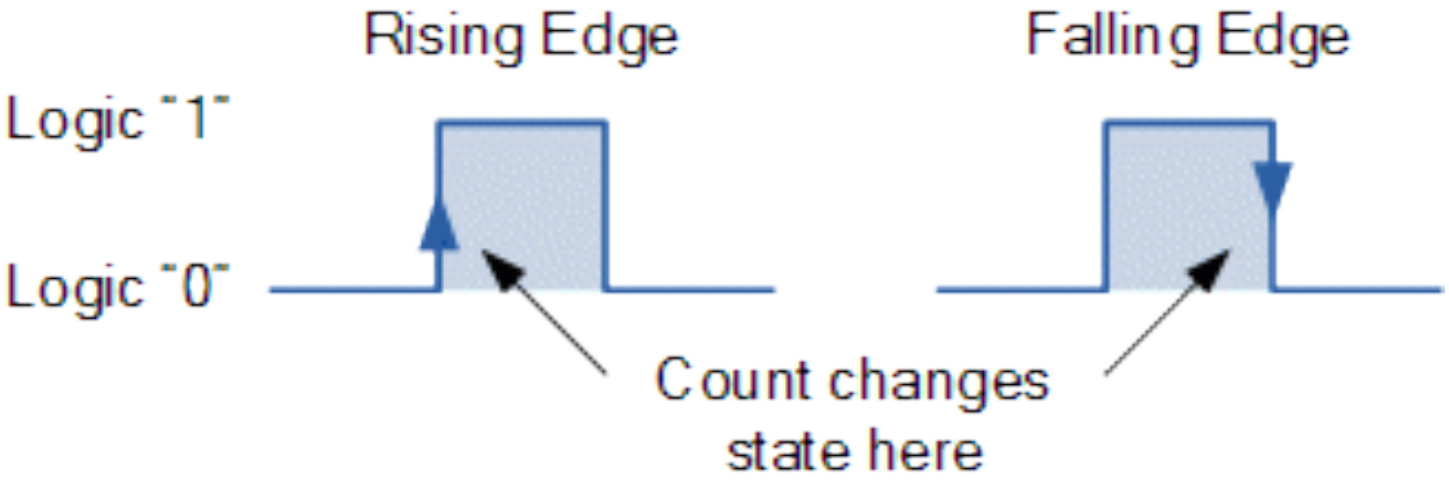
- Memoryless
- Output instant in time
- No clock signal

Sequential logic circuit

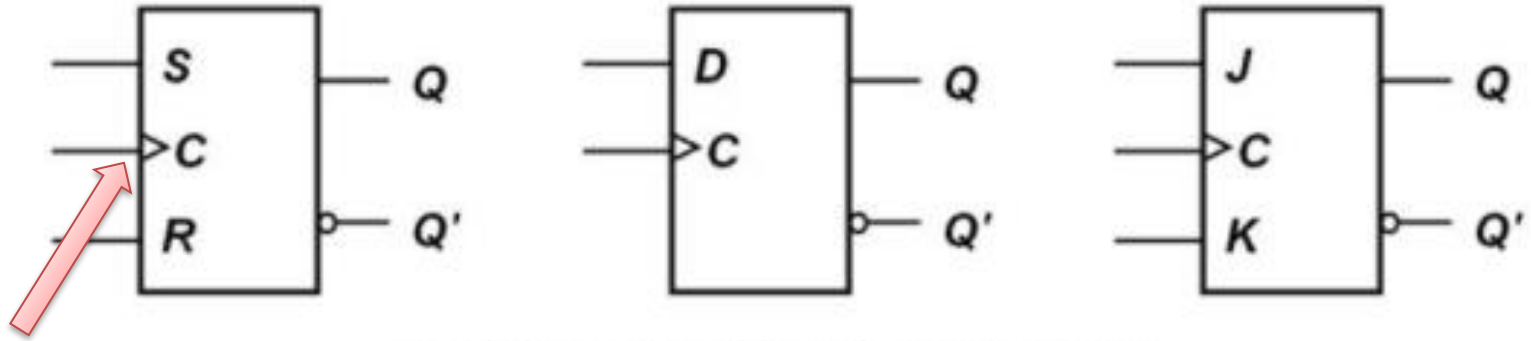
- Memory
- Output depends on previous states
- Related clock signal

RISING AND FALLING EDGE TRIGGER

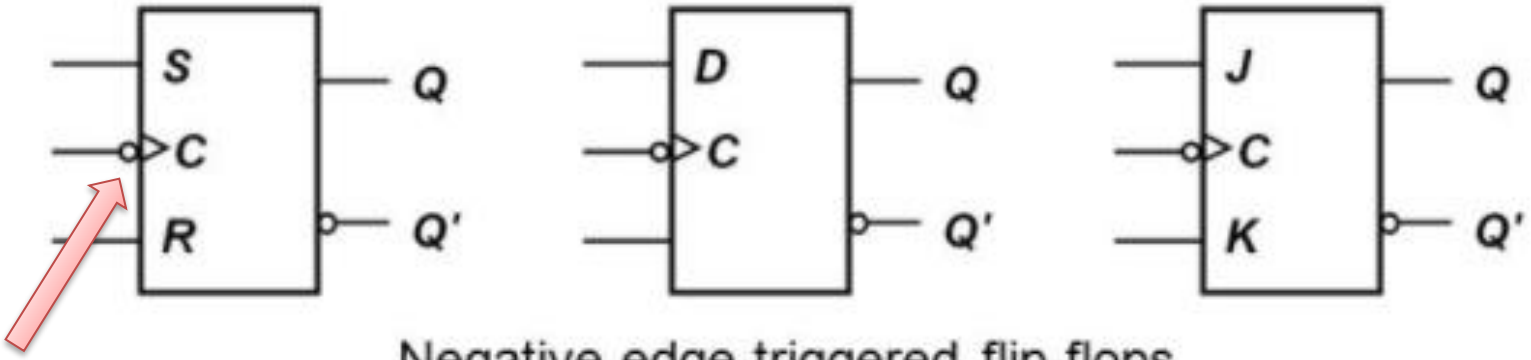
Rising/Falling edge trigger



Flip-flop symbols in rising/falling edge trigger



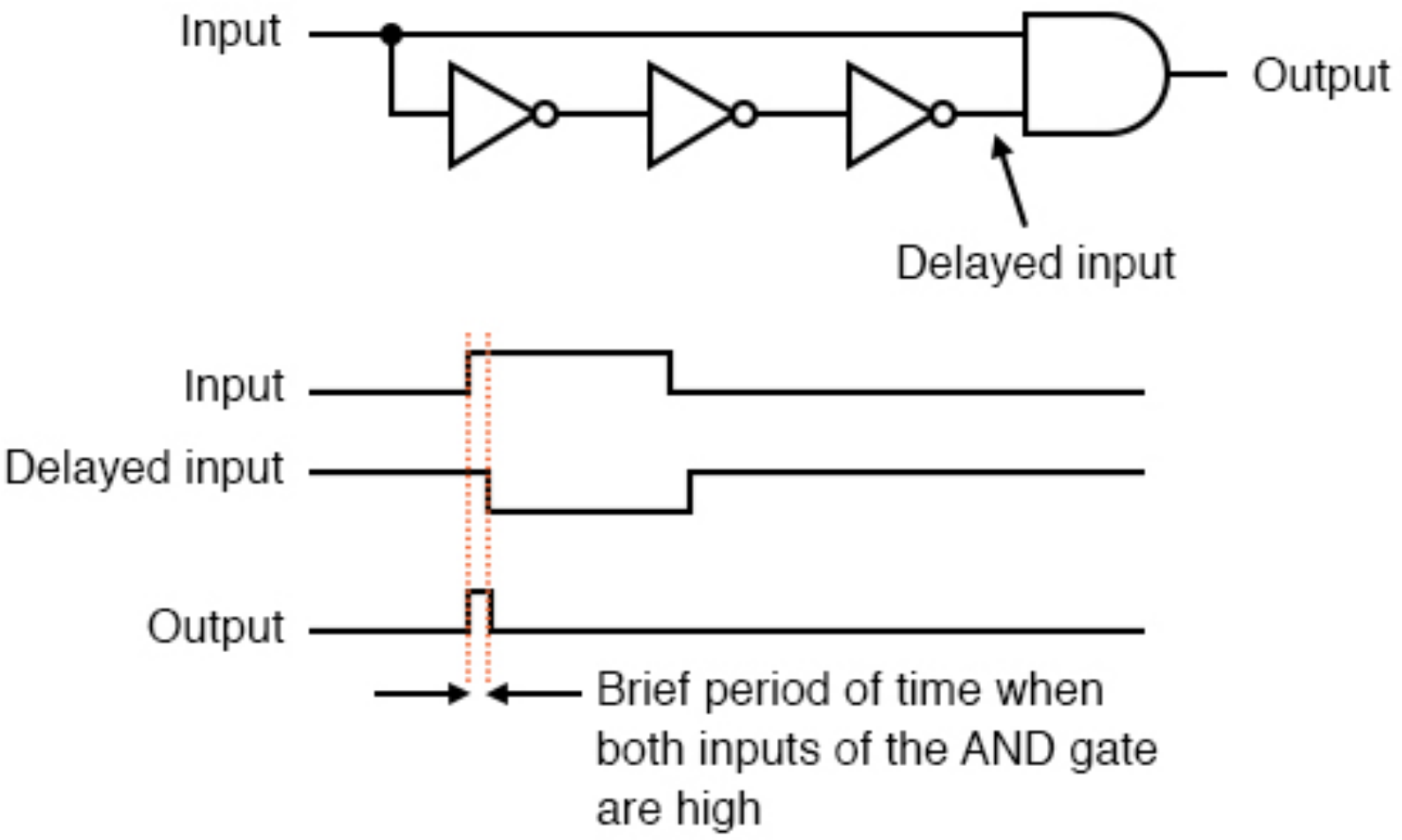
Positive edge-triggered flip-flops



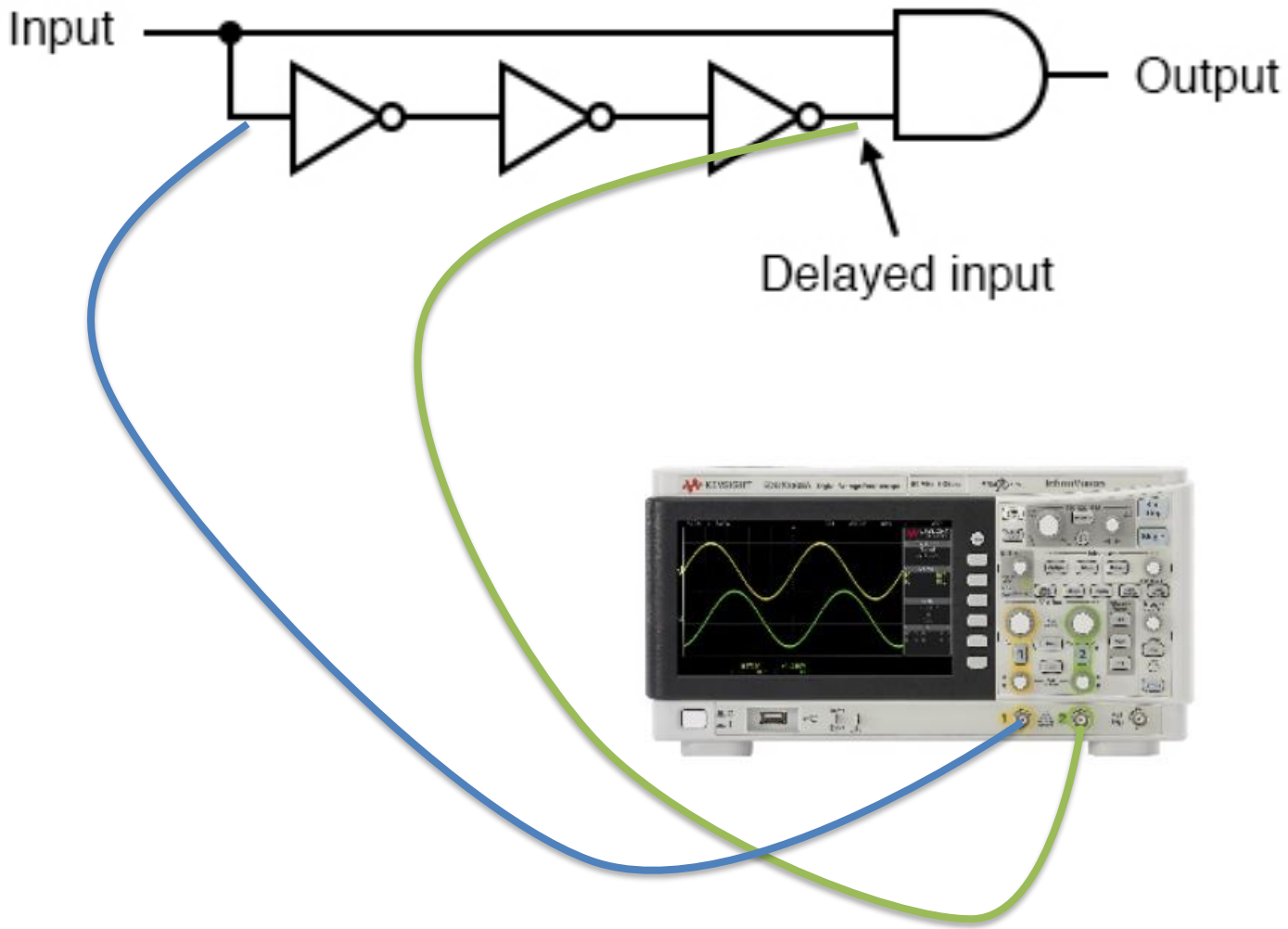
Negative edge-triggered flip-flops

Some textbook for rising/falling edge trigger called positive/negative edge trigger

Circuit detects positive edge trigger



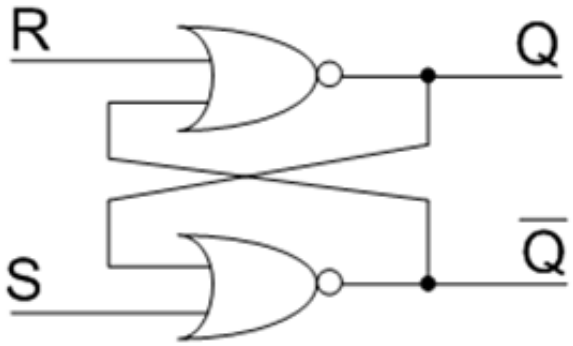
Activity 4.1 Delay time measurement in the positive-edge trigger circuit



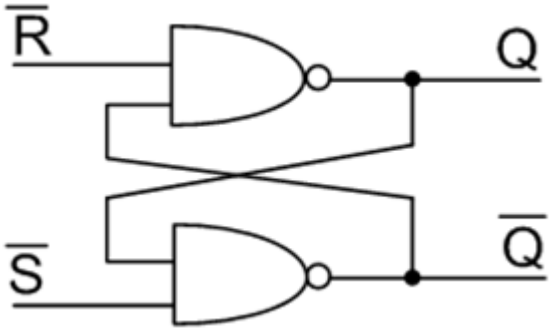
SR FLIP-FLOP

Set-Reset Flip-flop (SR-flipflop)

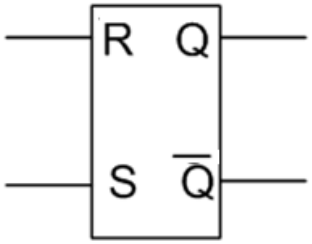
SR flipflop is two types by the structure of logic gate.

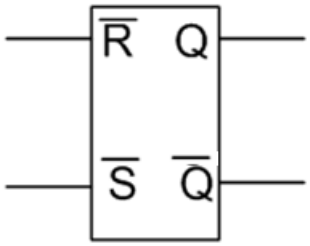


NOR gate SR-flipflop



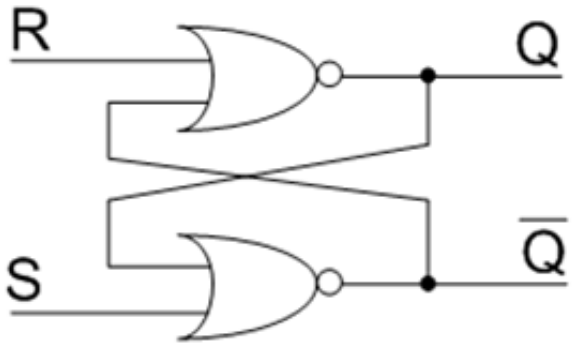
NAND gate SR-flipflop





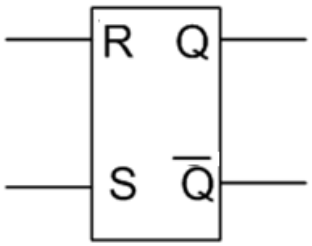
Set-Reset Flip-flop (SR-flipflop)

Truth table



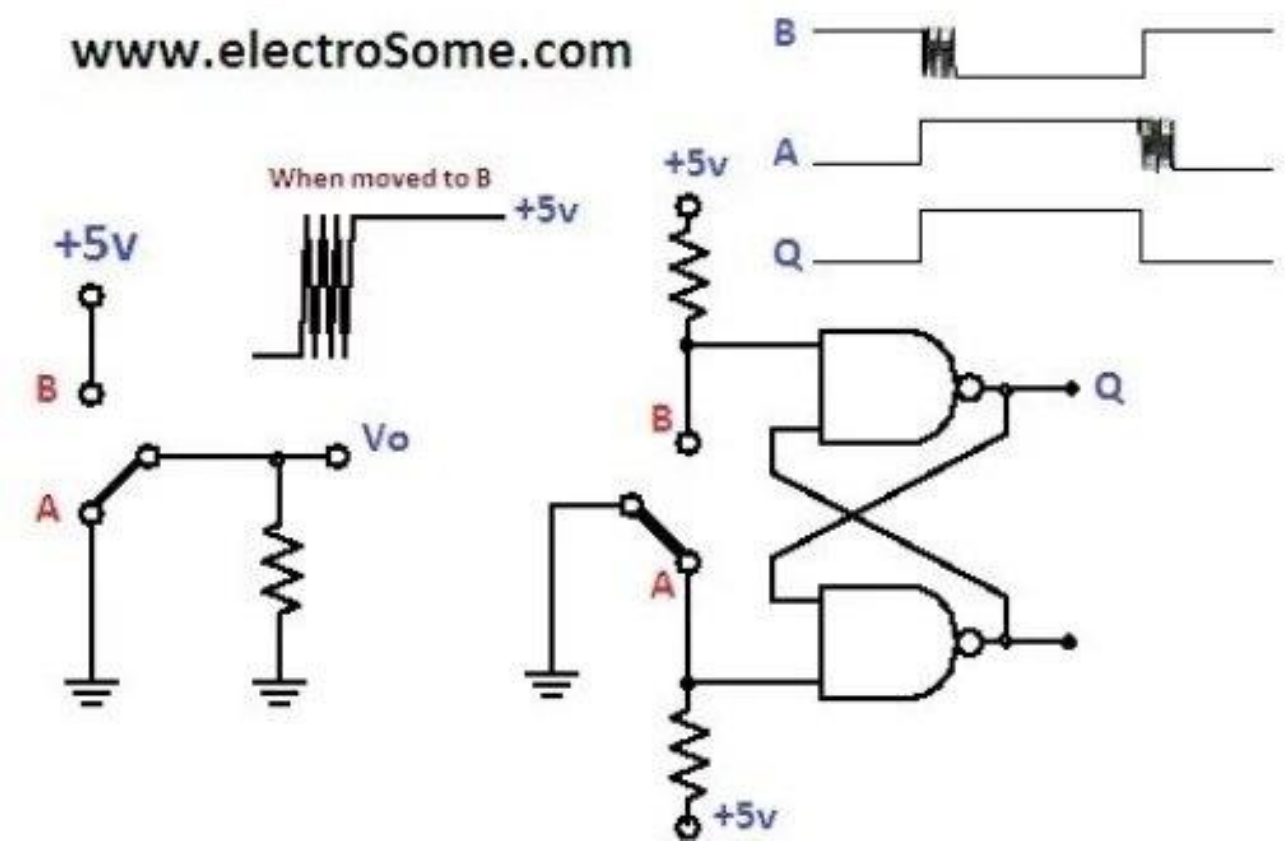
NOR gate SR-flipflop

S	R	Q
0	0	No change
0	1	1 = Set
1	0	0 = Reset
1	1	Restrict Combination



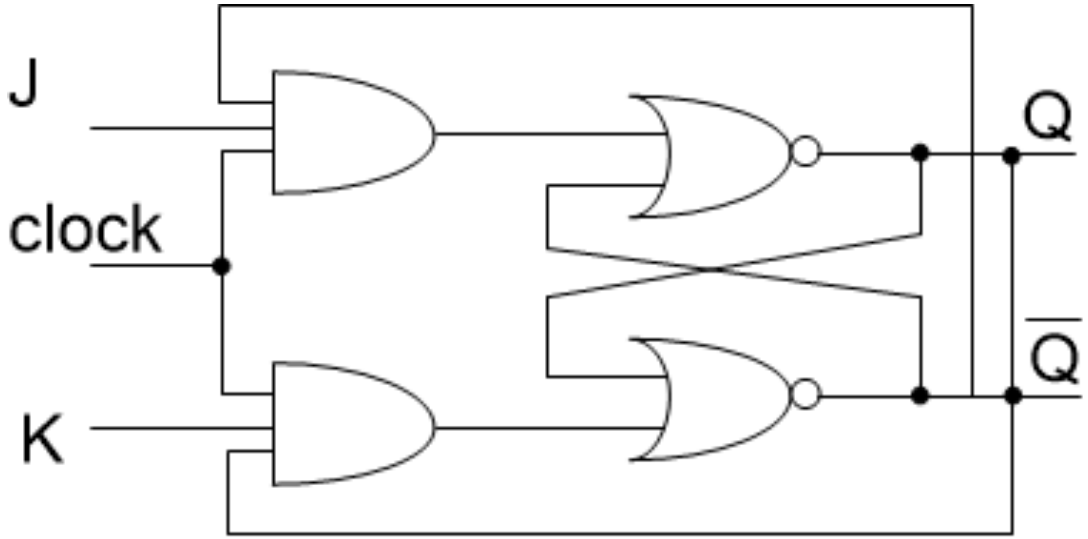
Example application uses SR-flipflop

- Debounced switch



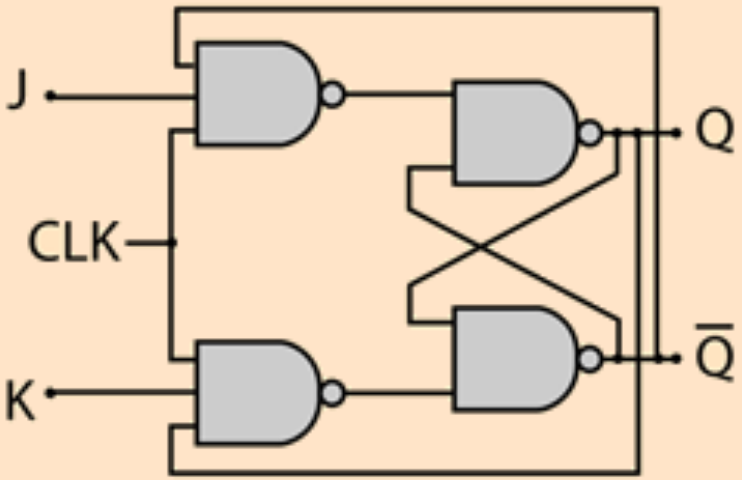
JK FLIP-FLOP

JK Flip-flop

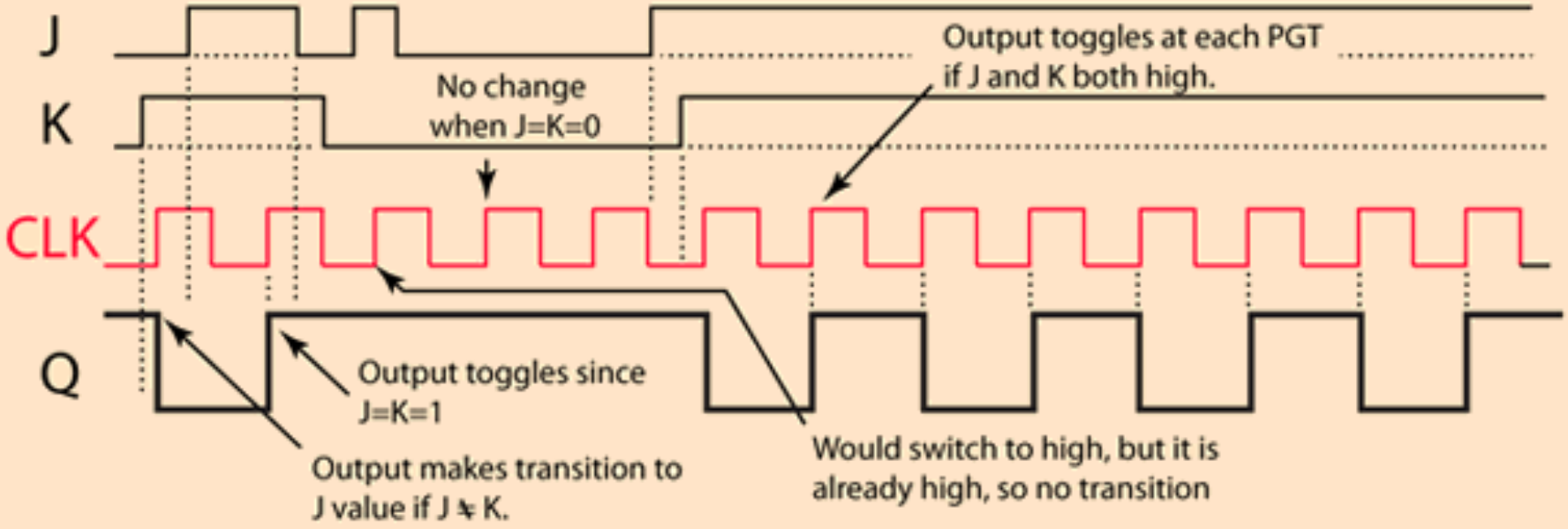


- Invented by Jack Kilby
- The JK flip-flop modified from SR flip-flop by adding a clock input to prevent the invalid output condition that occurs when both S and R are equal to logic “1”.

Switching Example: J-K Flip-Flop



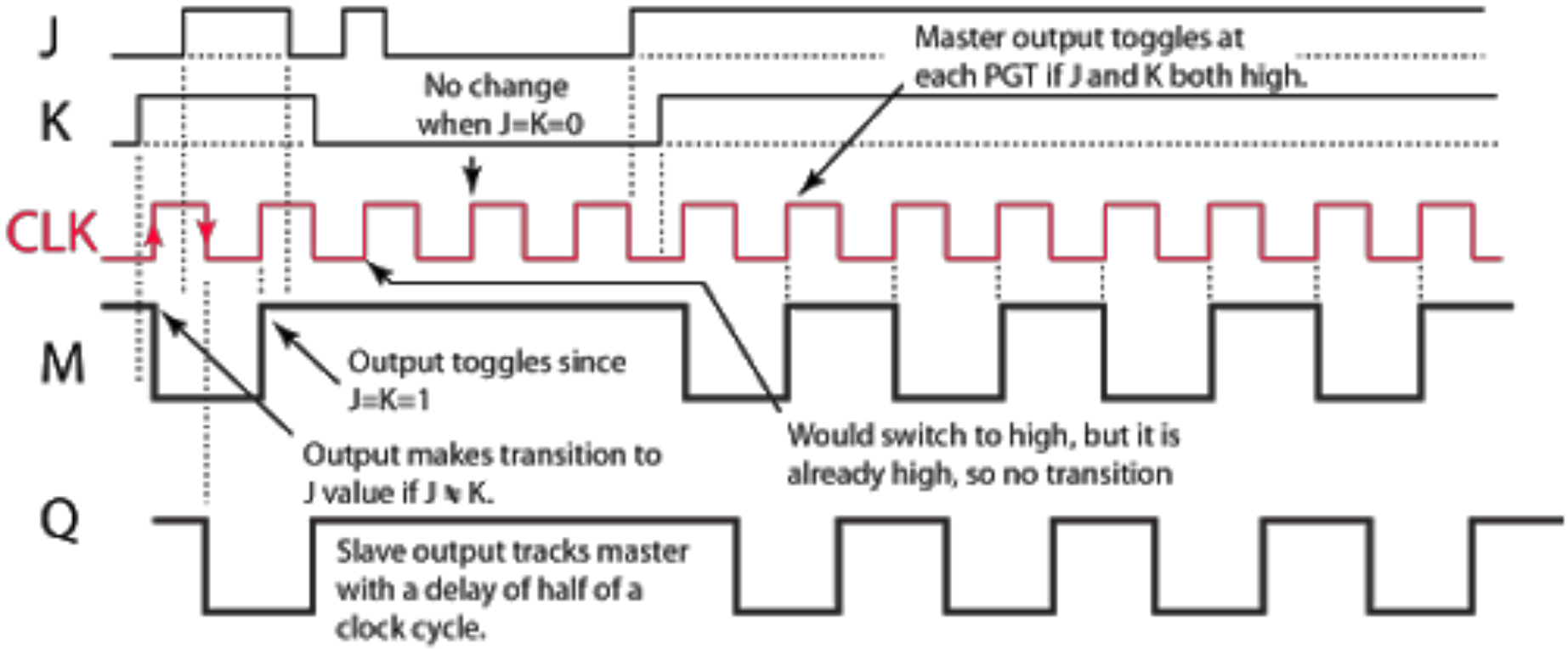
The positive going transition (PGT) of the clock enables the switching of the output Q. The "enable" condition does not persist through the entire positive phase of the clock. The J & K inputs alone cannot cause a transition, but their values at the time of the PGT determine the output according to the truth table. This is an application of the versatile J-K flip-flop.



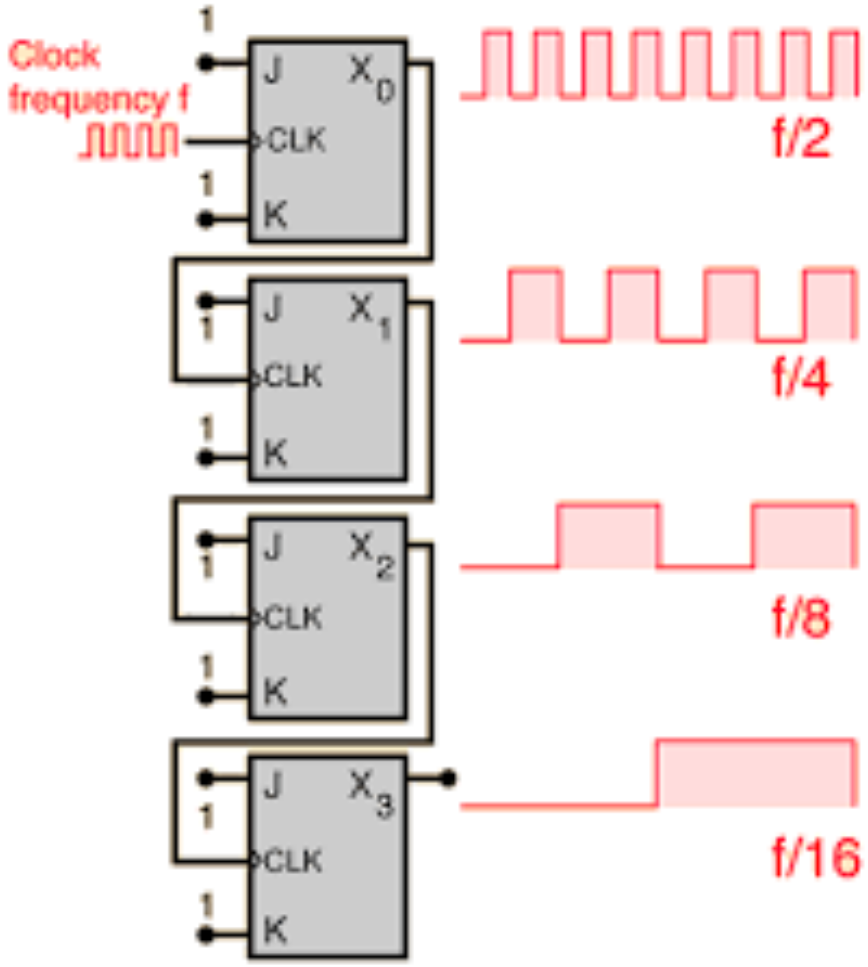
JK Flip-flop Truth table

Clk	J	K	Q	Description
No clock	?	?	?	No change
	0	0	?	No change
	0	1	?->0	Reset
	1	0	?->1	Set
	1	1	0->1 1->0	Toggle

JK flip-flop in timing states

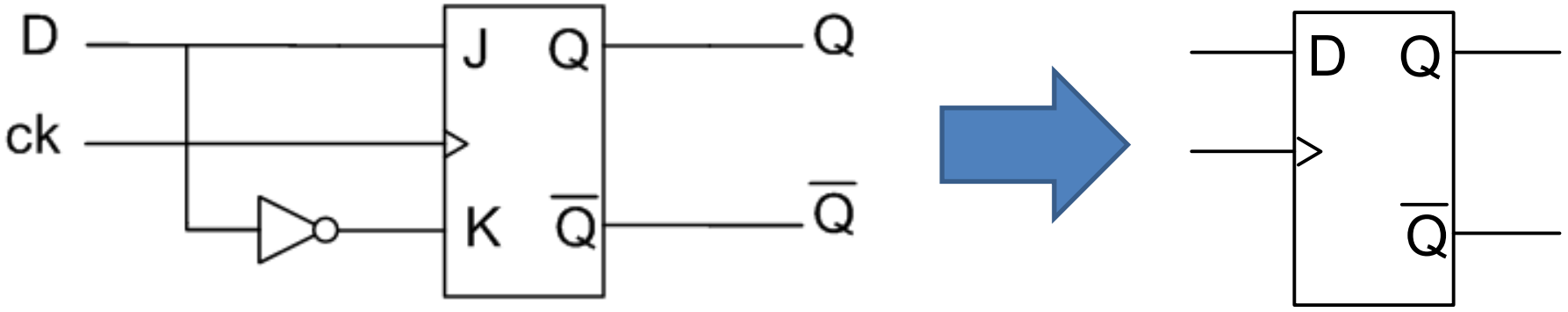


Application used JK flip-flop



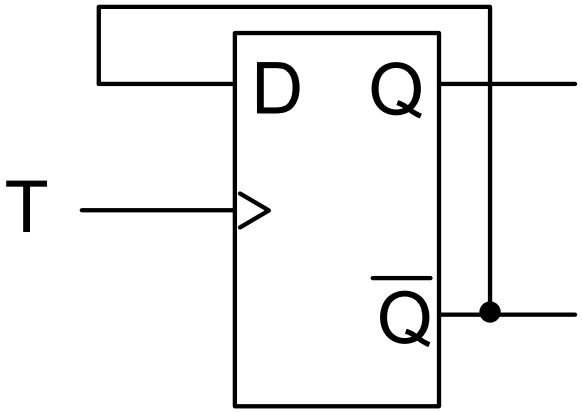
D FLIP-FLOP AND T FLIP-FLOP

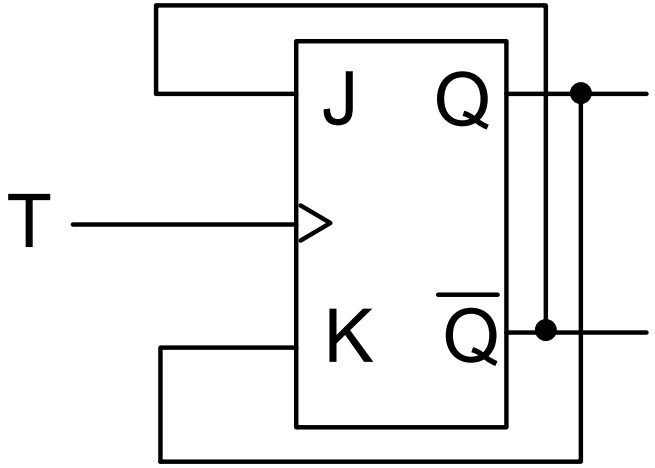
Making D flip-flop from JK



Clk	J	K	Q	Description
No clock	?	?	?	No change
	0	1	?->0	Store “0”
	1	0	?->1	Store “1”

T Flip-flop from D and JK

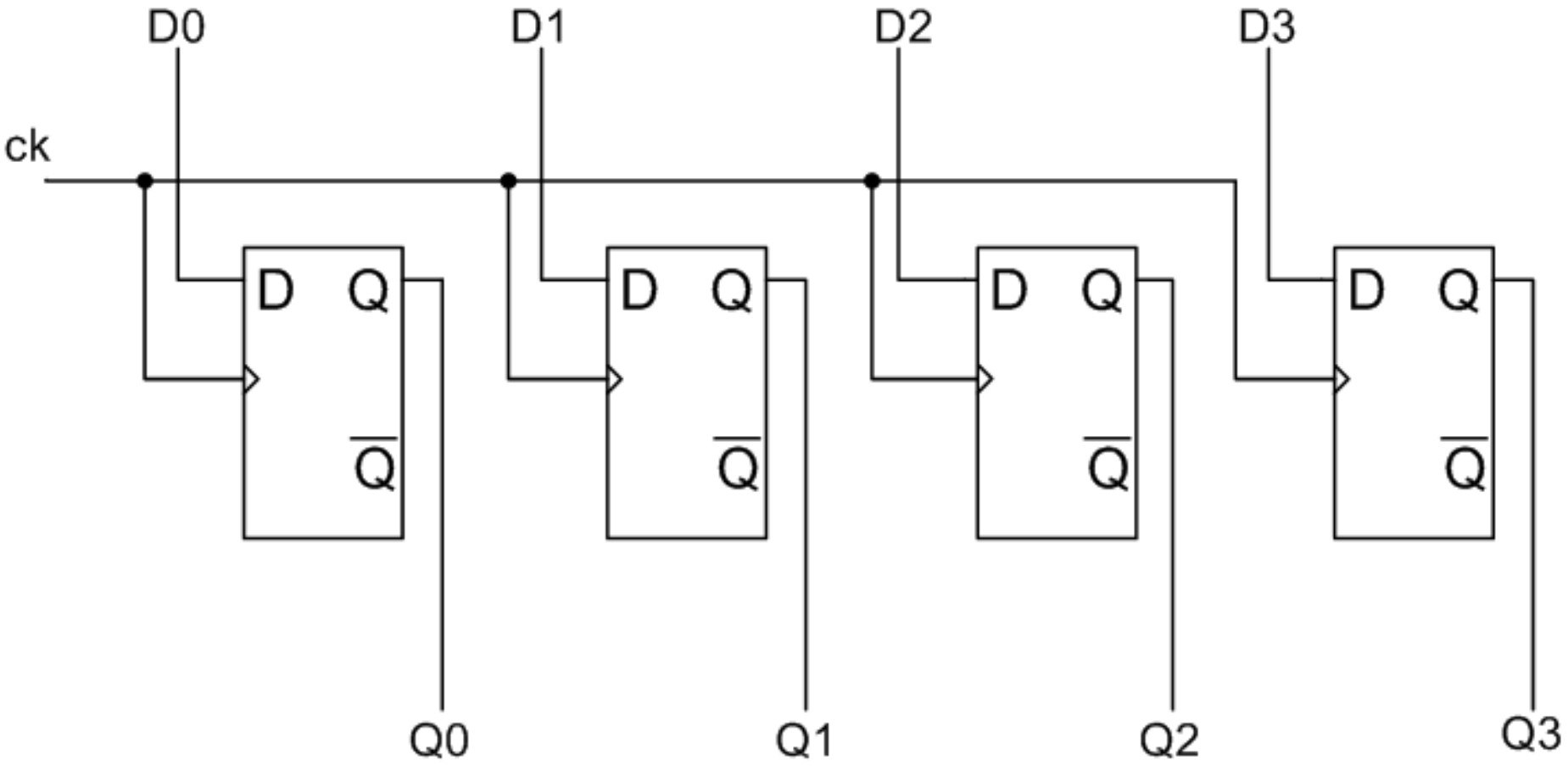




Clk (T)	Q	Description
No clock	?	No change
	?->0 ?->1	Toggle

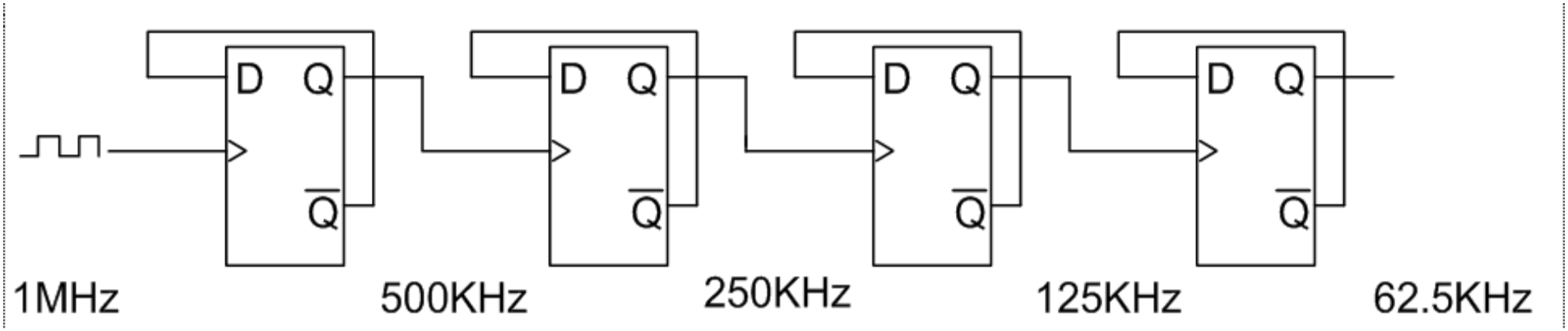
4-BIT LATCH CIRCUIT

4-bit Latch circuit



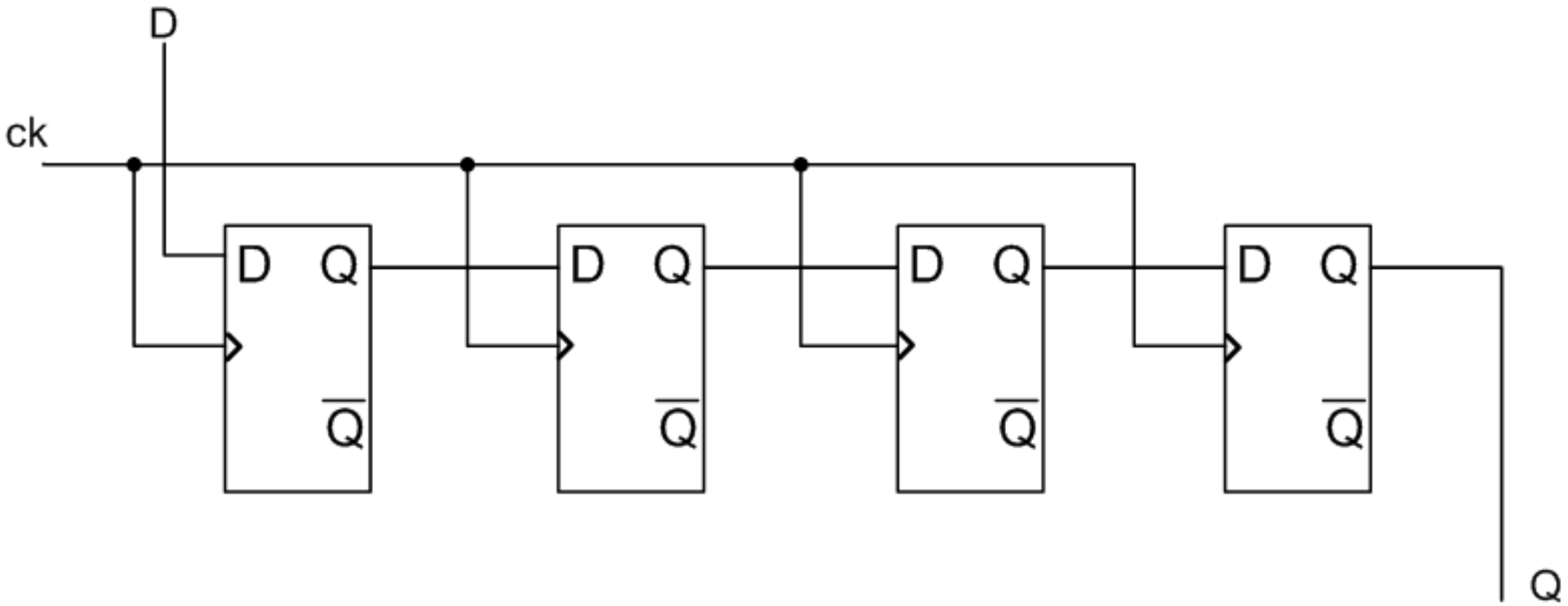
FREQUENCY DIVISION CIRCUIT

Frequency division circuit



4-BIT FIFO CIRCUIT

4-bit First-in First-out (FIFO)



COUNTER

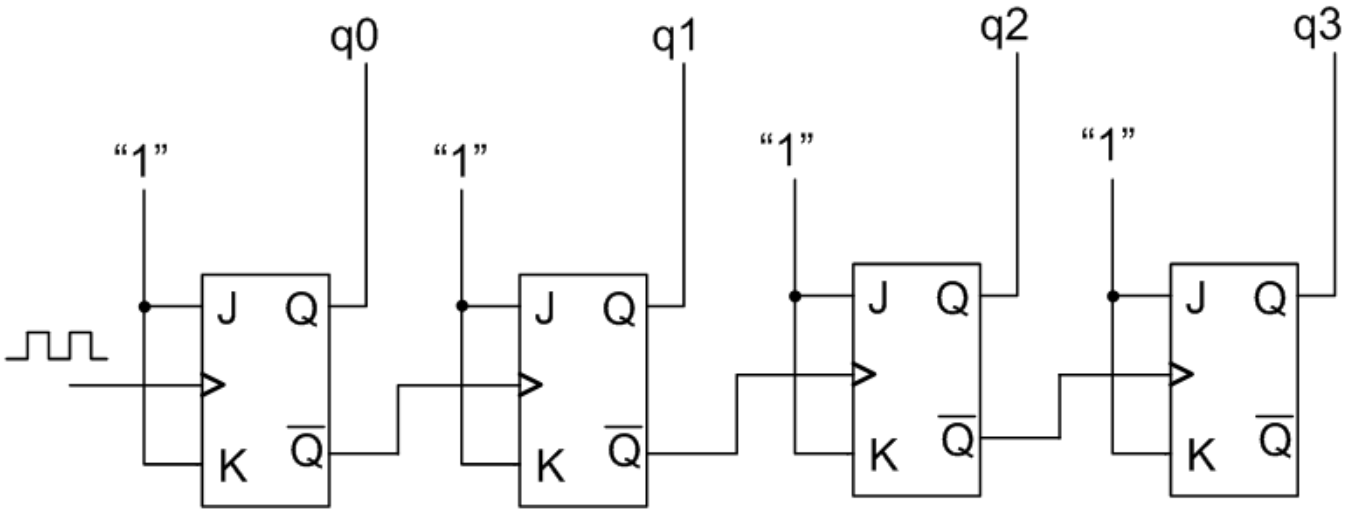
Counter circuit

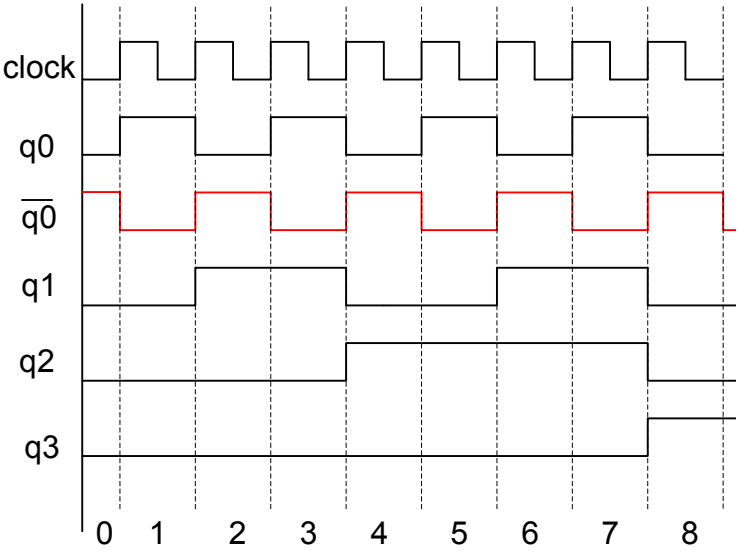
- The digital circuit has divided type of counter circuit by focusing at a characteristic of input clock to the gate in the circuit.

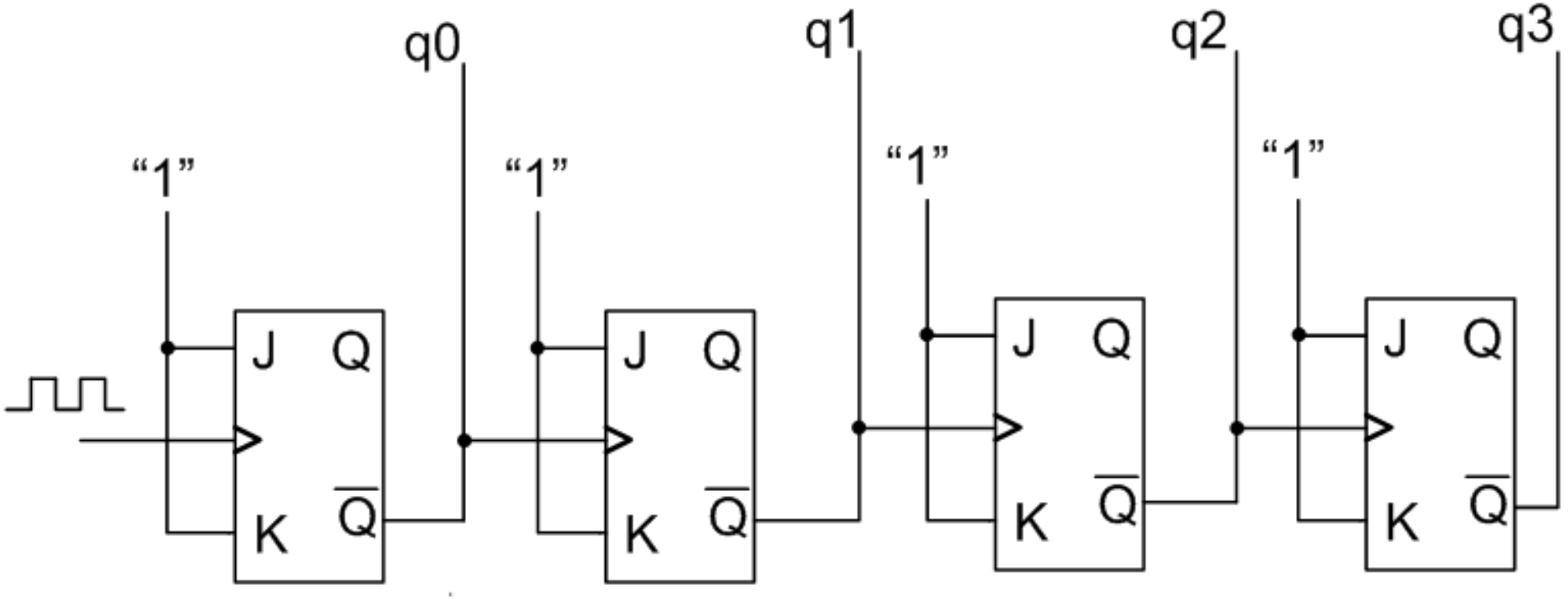
Asynchronous circuit

Synchronous circuit

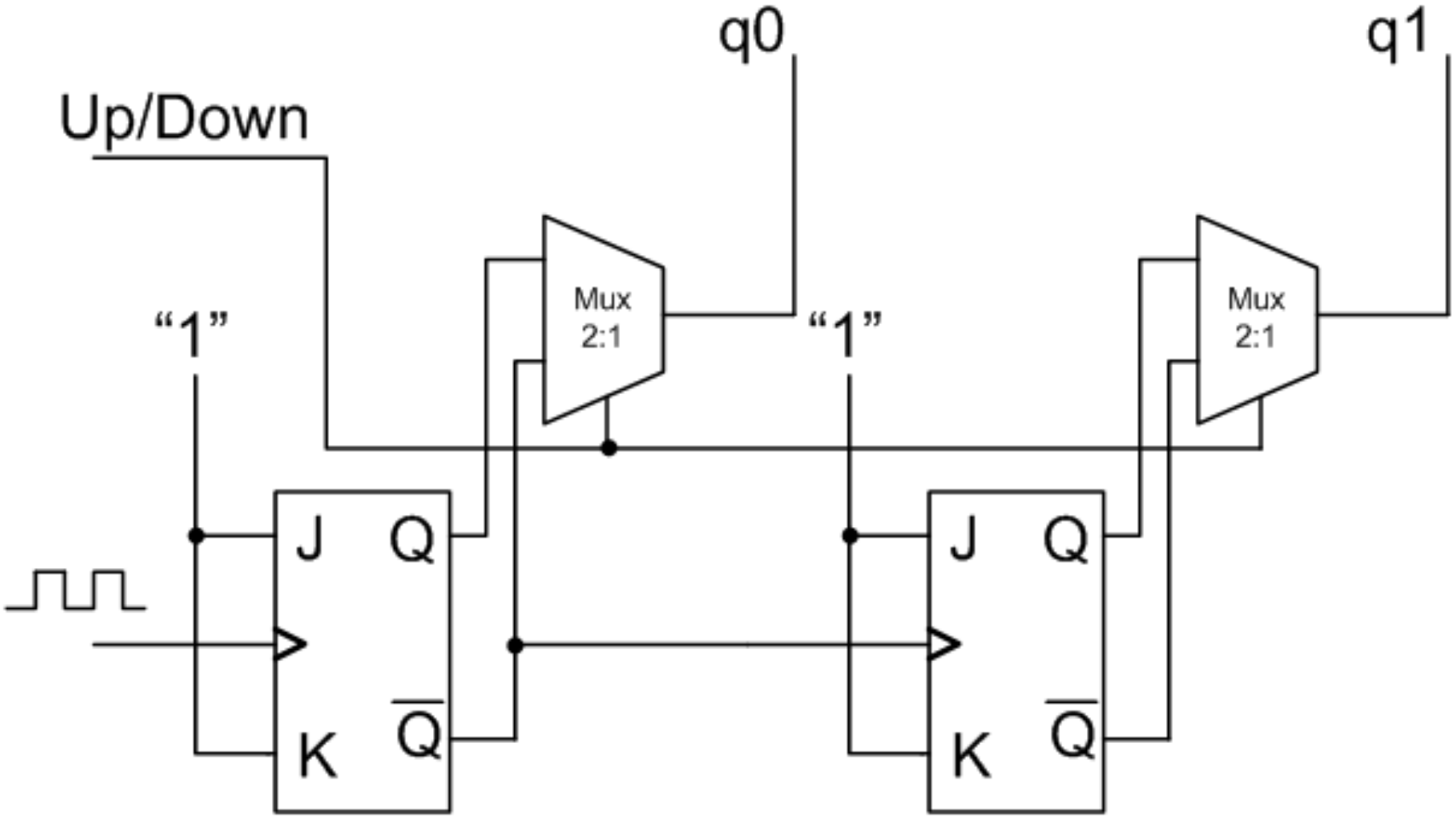
Asynchronous counter



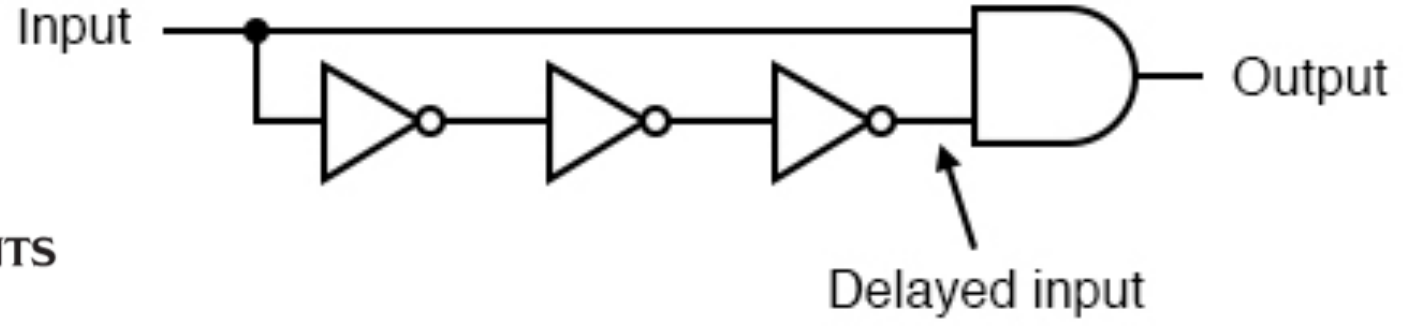



q0
q1
q2
q3
“1”
“1”
“1”
“1”
J
Q
K
Q
J
Q
K
Q
J
Q
K
Q
J
Q
K
Q

2-bit Asynchronous count up/down circuit



Delay-time problem in asynchronous counter circuit

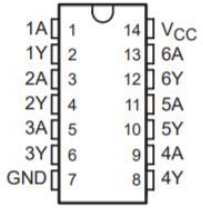


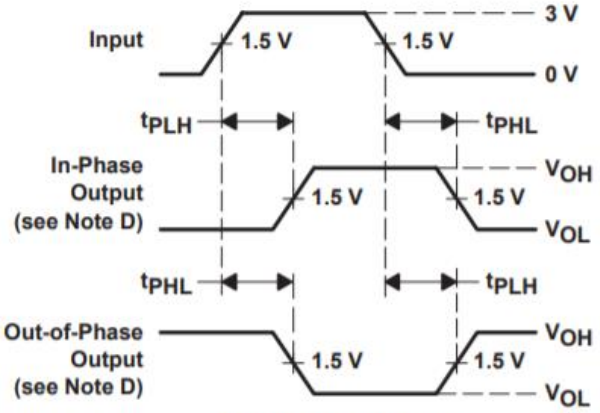
TEXAS INSTRUMENTS

SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS

SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)





VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

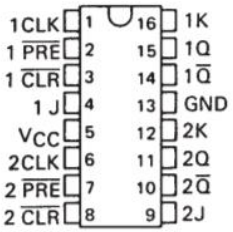
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S04 SN74S04			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 280 Ω, C_L = 15 pF		3	4.5	ns
t_{PHL}					3	5	

Asynchronous counter issue

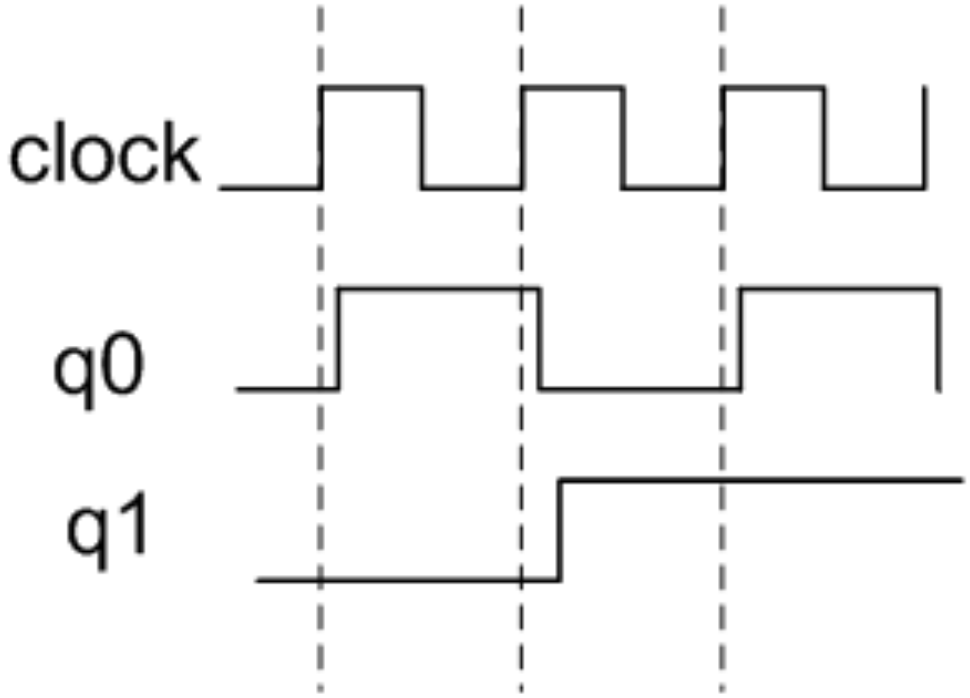
TEXAS INSTRUMENTS

(TOP VIEW)



'76
FUNCTION TABLE

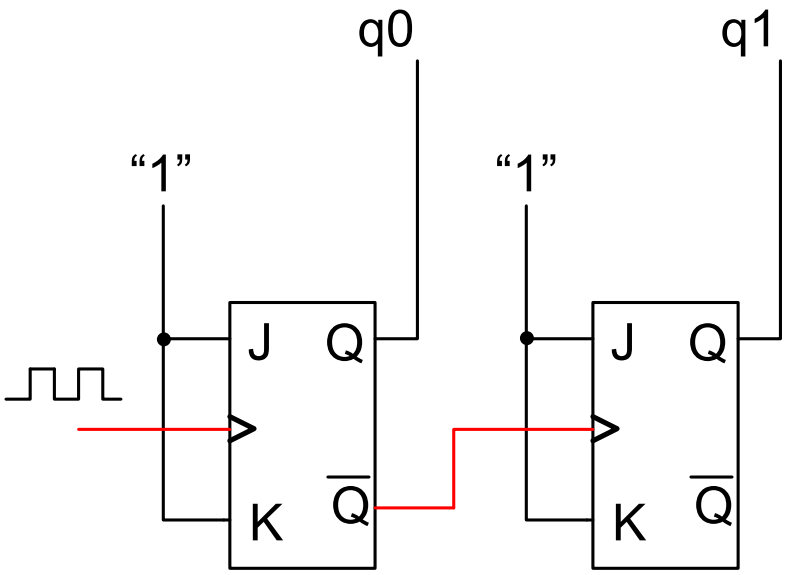
INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	



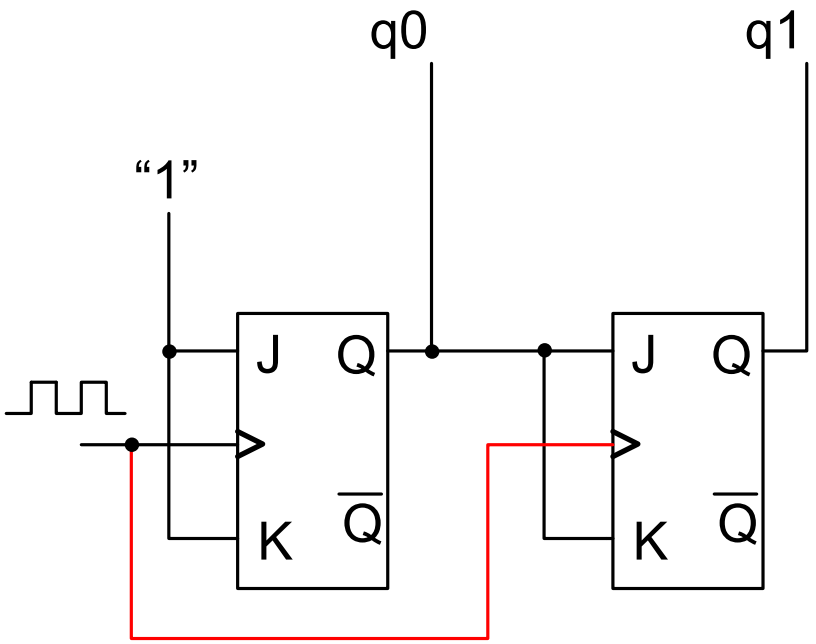
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF	30	45		MHz
t_{PLH}	PRE, CLR or CLK	Q or Q̄			15	20	ns
t_{PHL}					15	20	ns

Asynchronous vs Synchronous counter

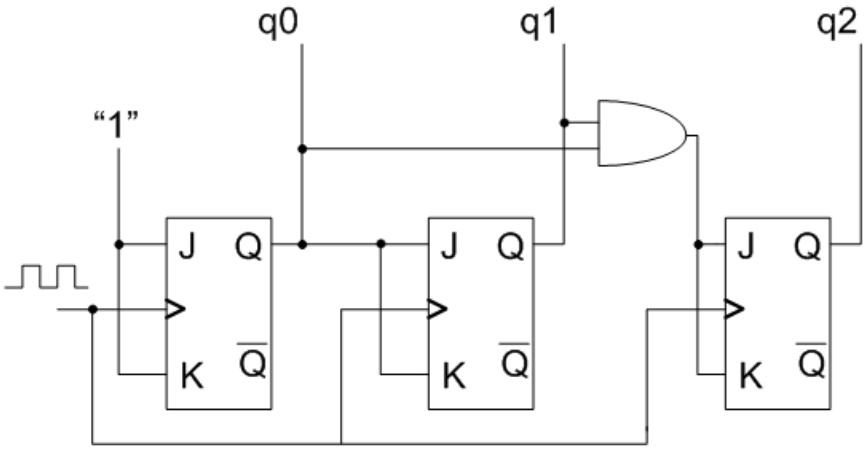


- Clock or control signal getting from previous states
- Easy design the counter circuit.
- Not suitable for a critical time system.



- A clock signal controls all states
- Complexity for design counter circuit.
- Proper for the critical time system

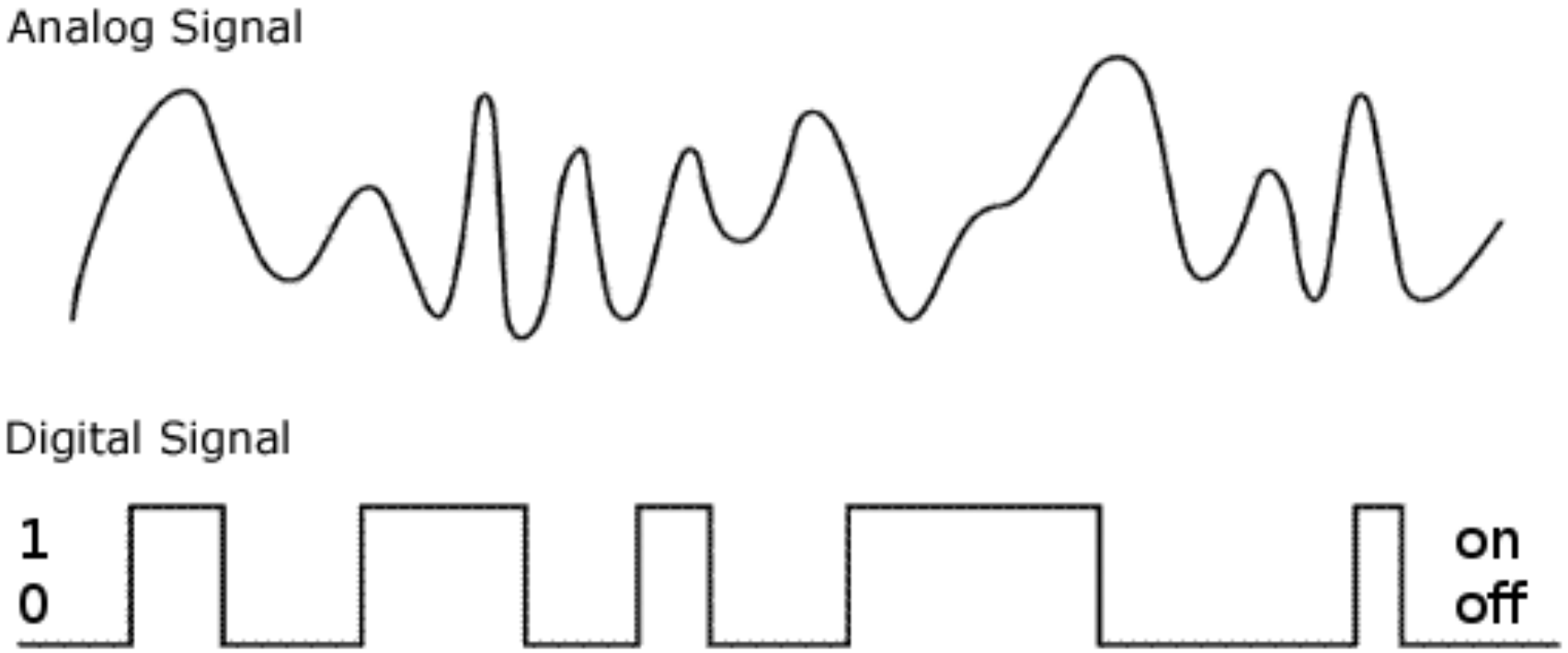
Example 3-bit synchronous counter-up



ลำดับ ck	Q2	Q1	Q0	อธิบาย
1	0	0	0	นับ 0
2	0	0	1	นับ 1
3	0	1	0	นับ 2
4	0	1	1	นับ 3 เอา q0 and q1 = 1
5	1	0	0	นับ 4 เกิด toggle ที่ q2
6	1	0	1	นับ 5
7	1	1	0	นับ 6
8	1	1	1	นับ 7 เอา q0 and q1 =1
9	0	0	0	นับ 0 เกิด toggle ที่ q2

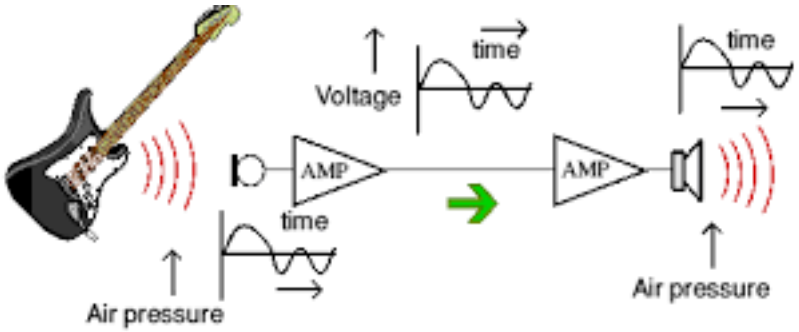
ANALOG SIGNAL AND DIGITAL SIGNAL

Analog signal vs Digital signal

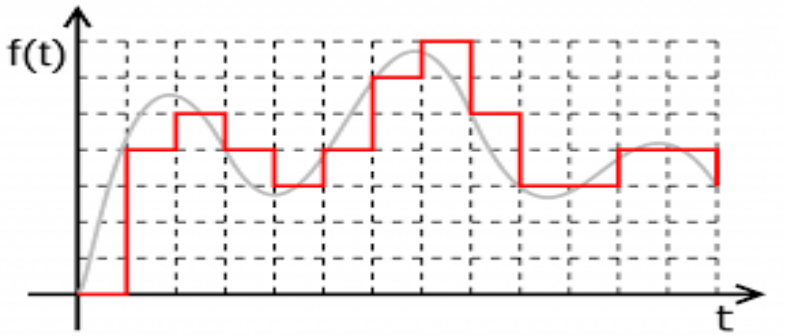


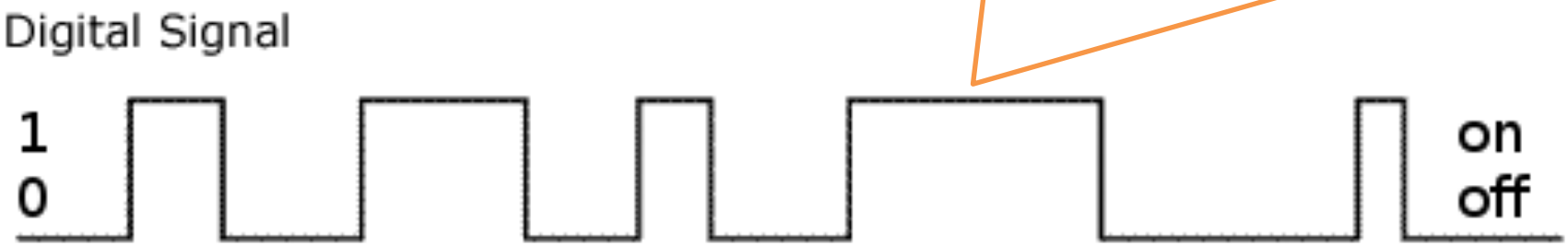
Analog signal vs Digital signal

Analog signals are continuous-time signals changing the wave from continuously.

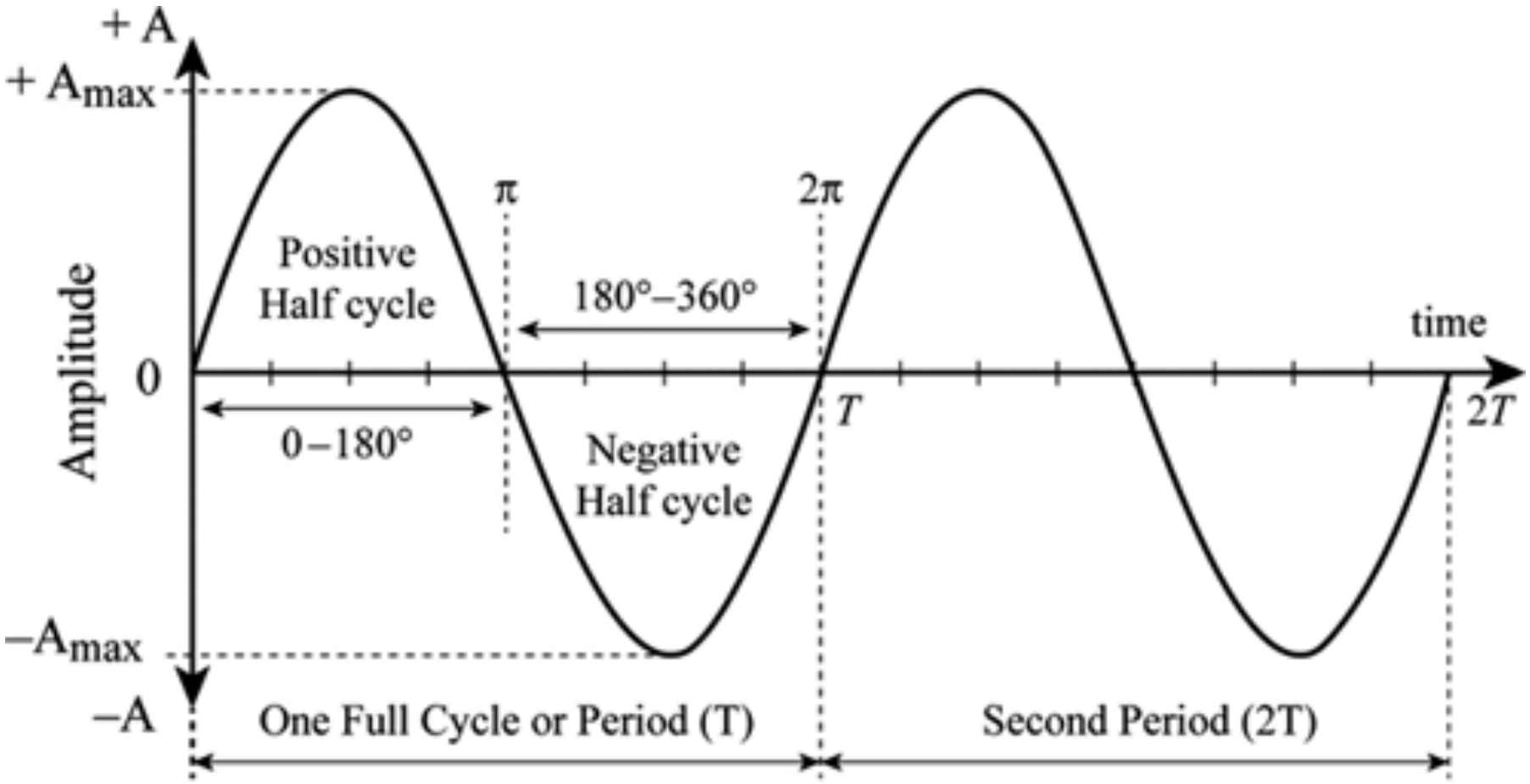


Digital signals are discrete-time signals limited by number of **bits** and the **sampling rate**.

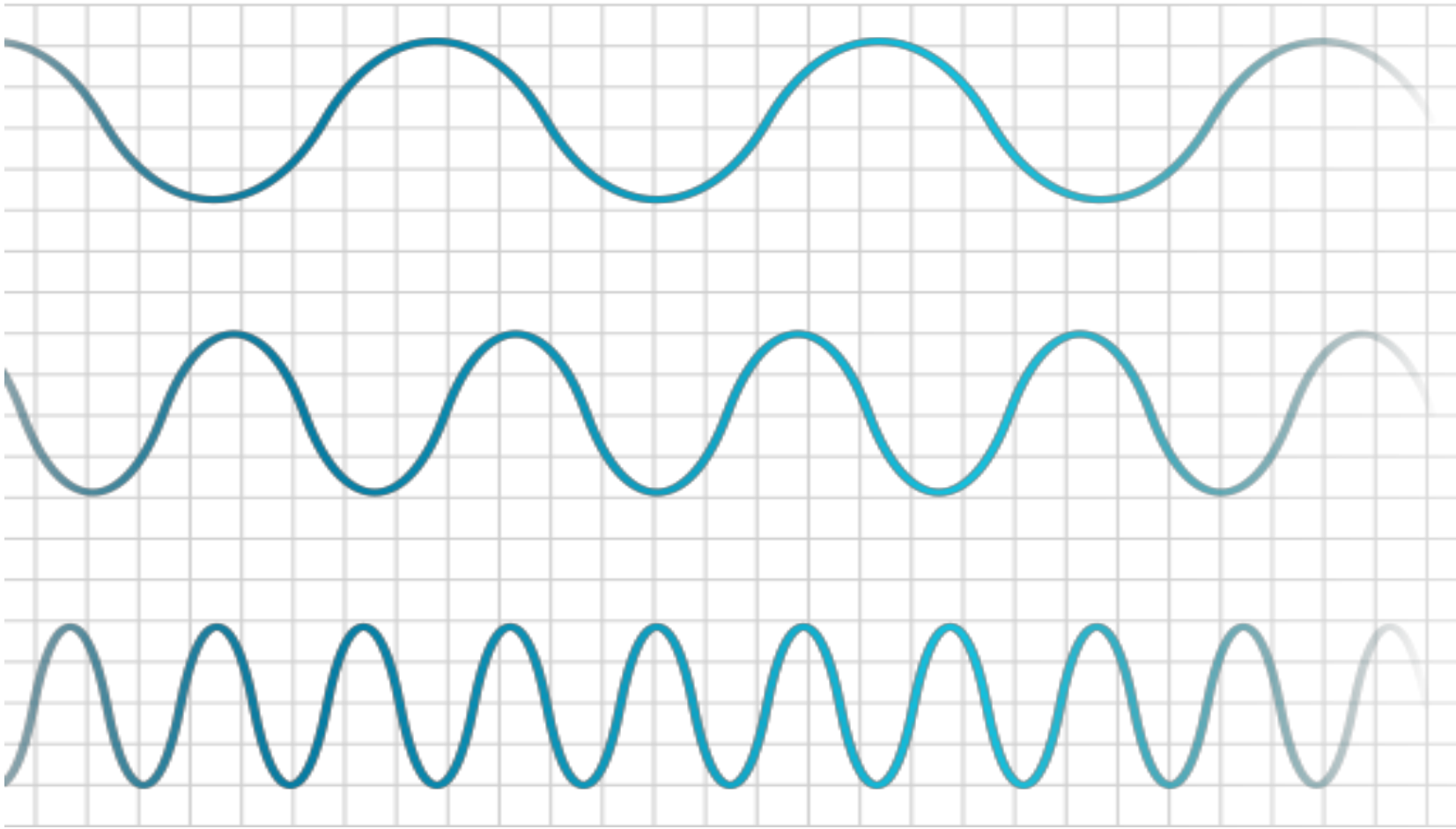




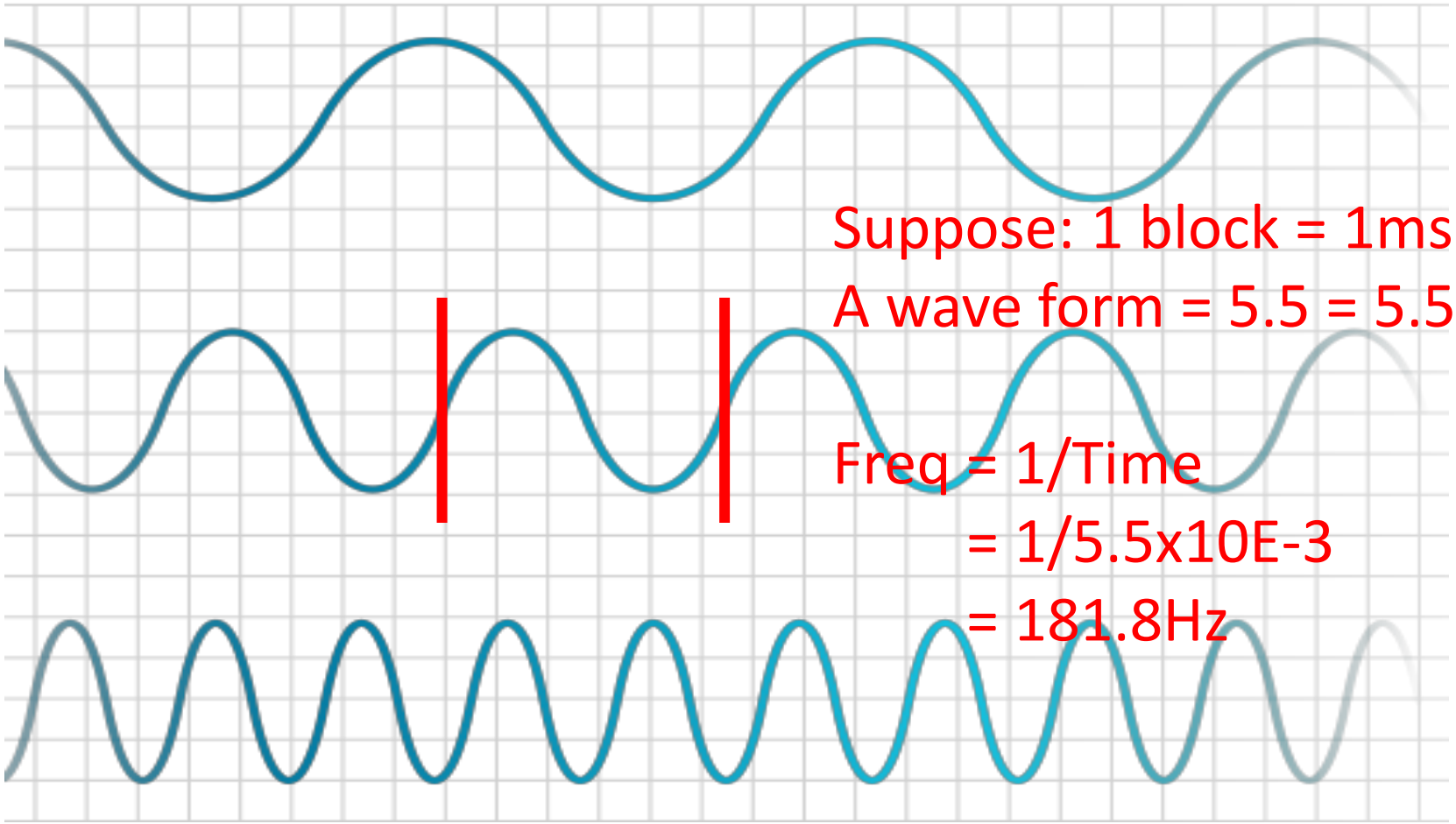
Signal Property



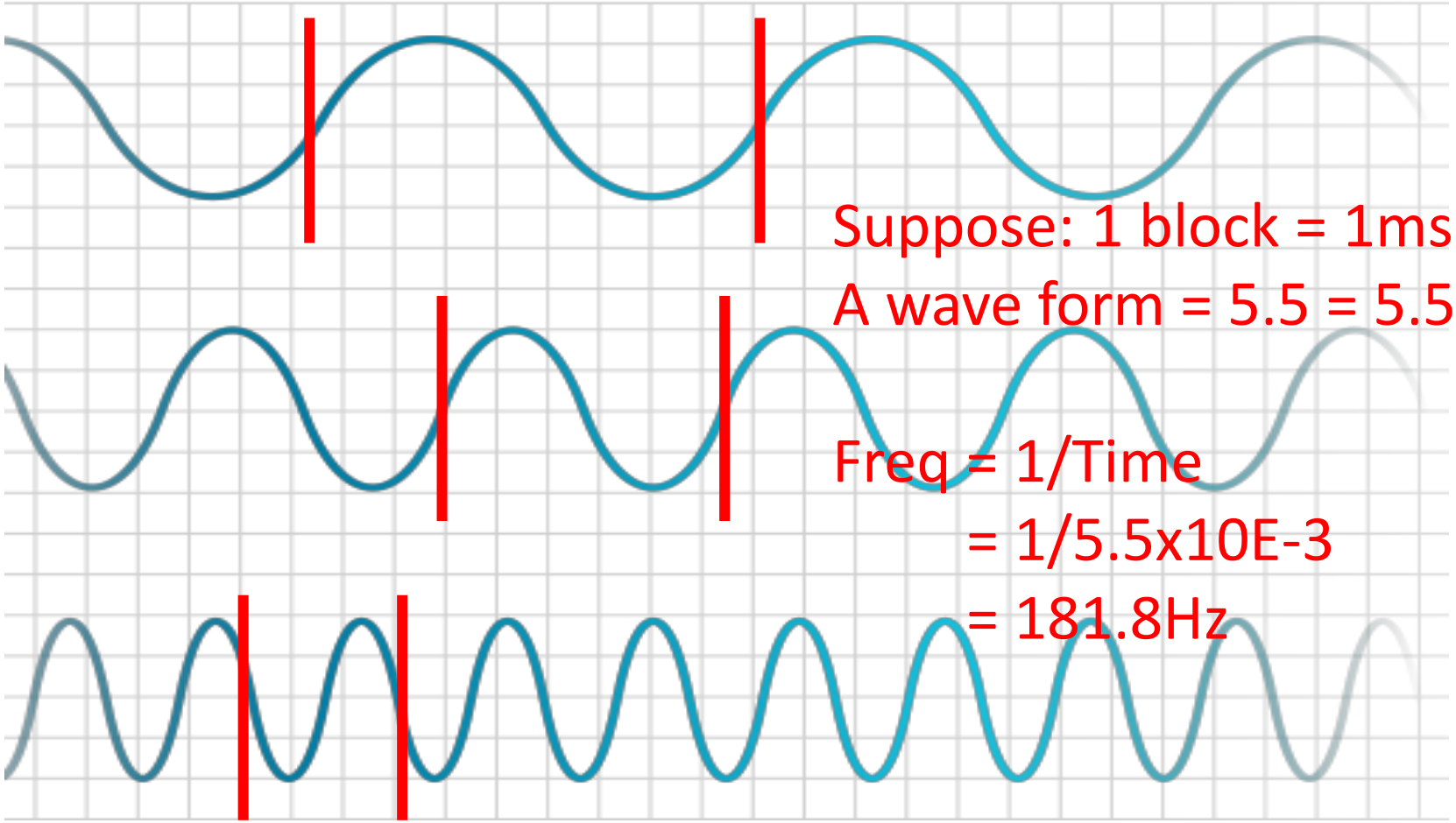
Which one is the low frequency?



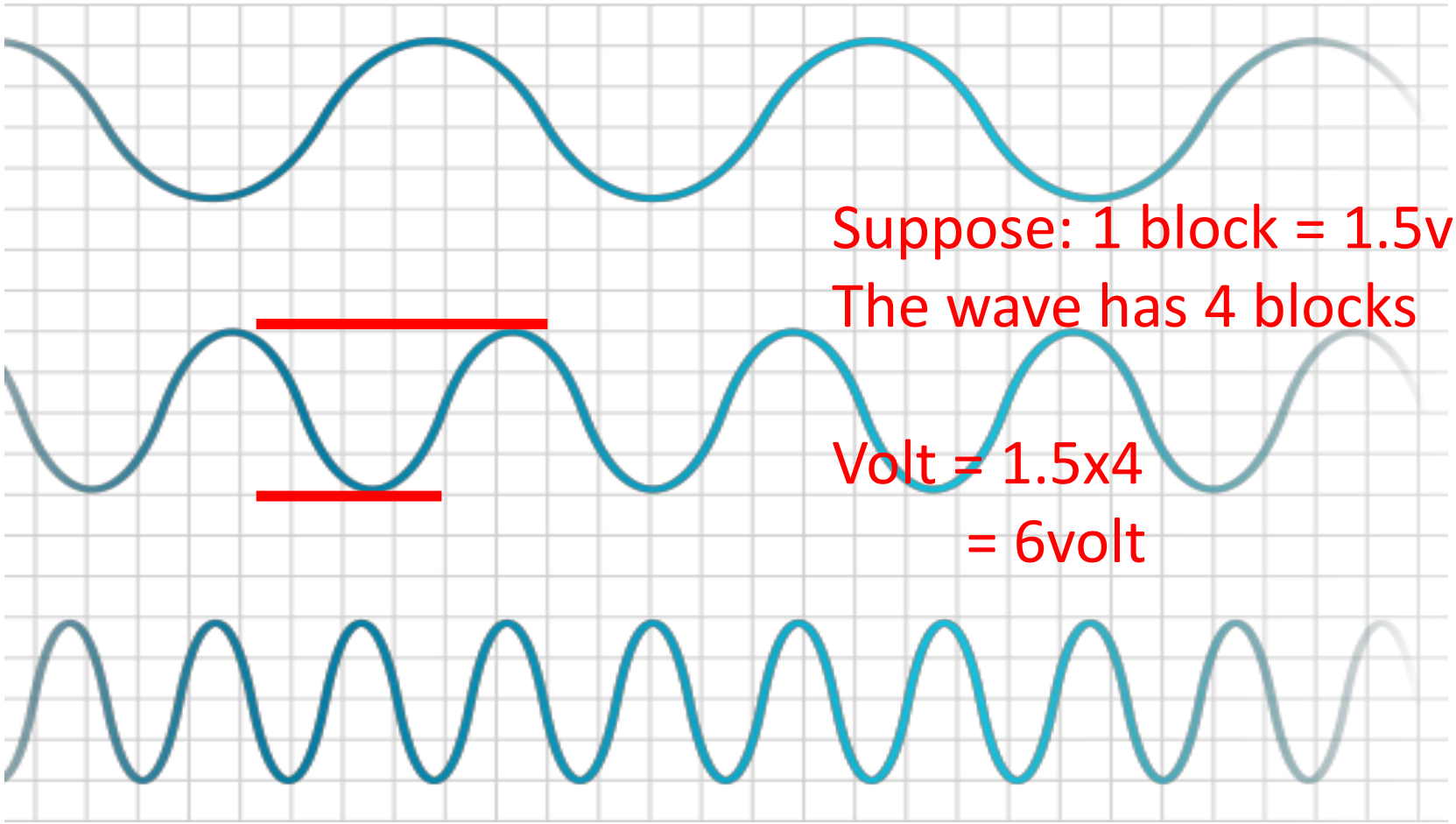
Which one is the low frequency?



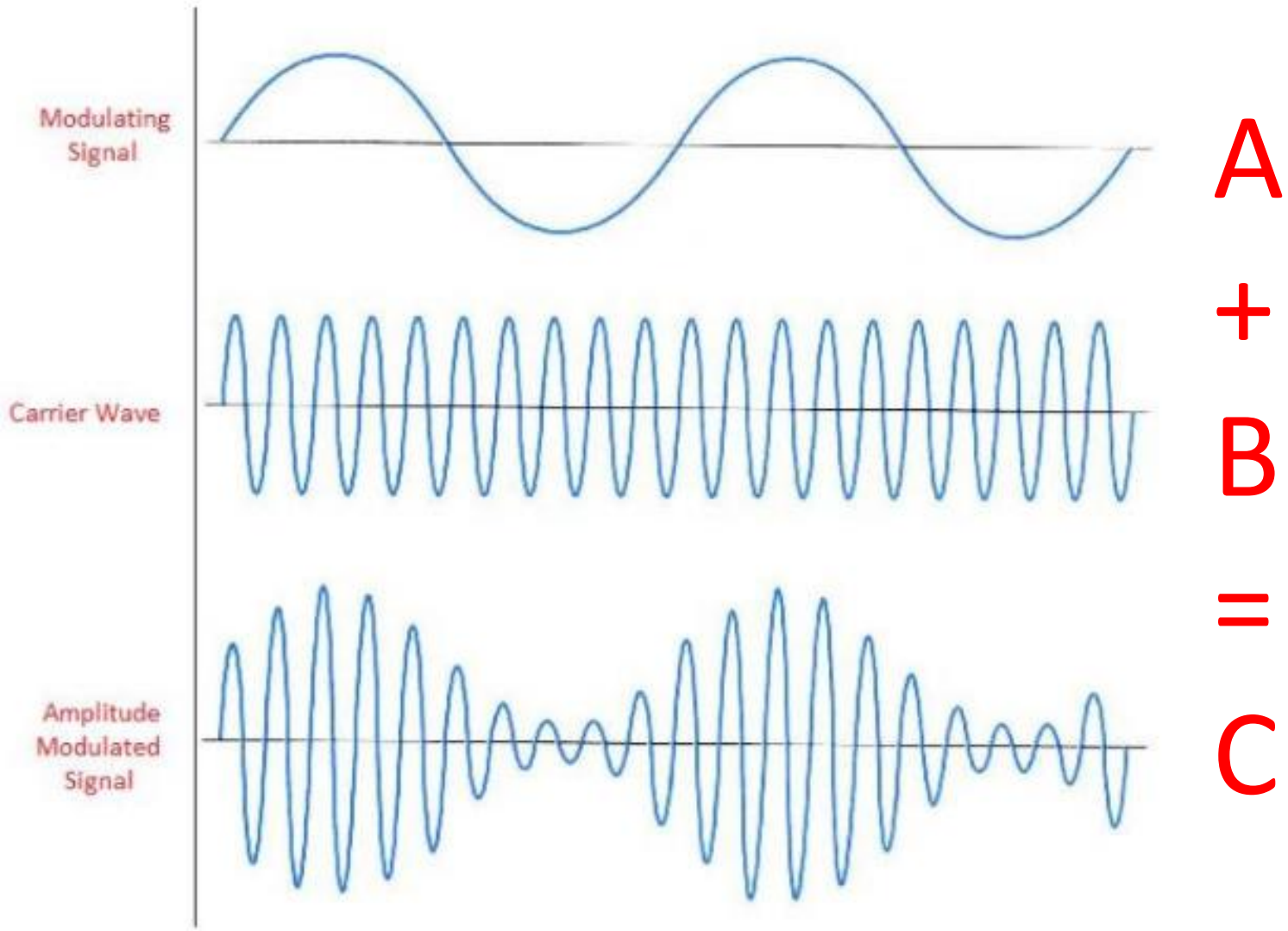
Activity 4.2 Frequency calculation



Amplitude, Voltage, Level

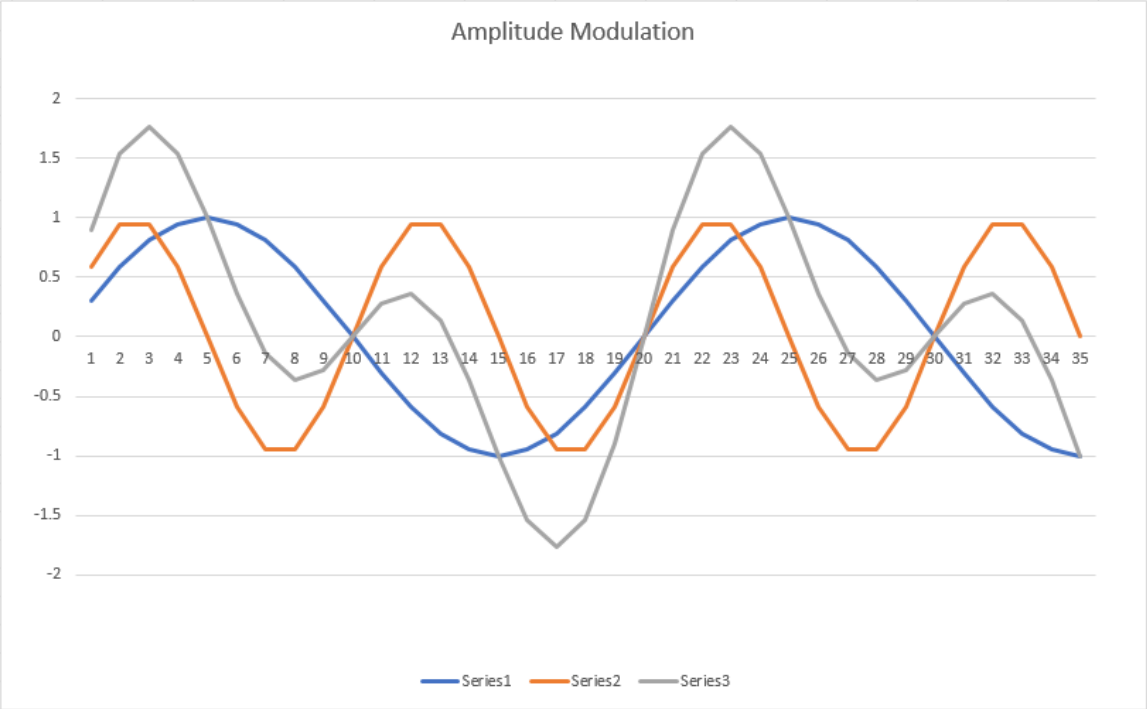


Modulation


Modulating Signal
Carrier Wave
Amplitude Modulated Signal
A
+
B
=
C

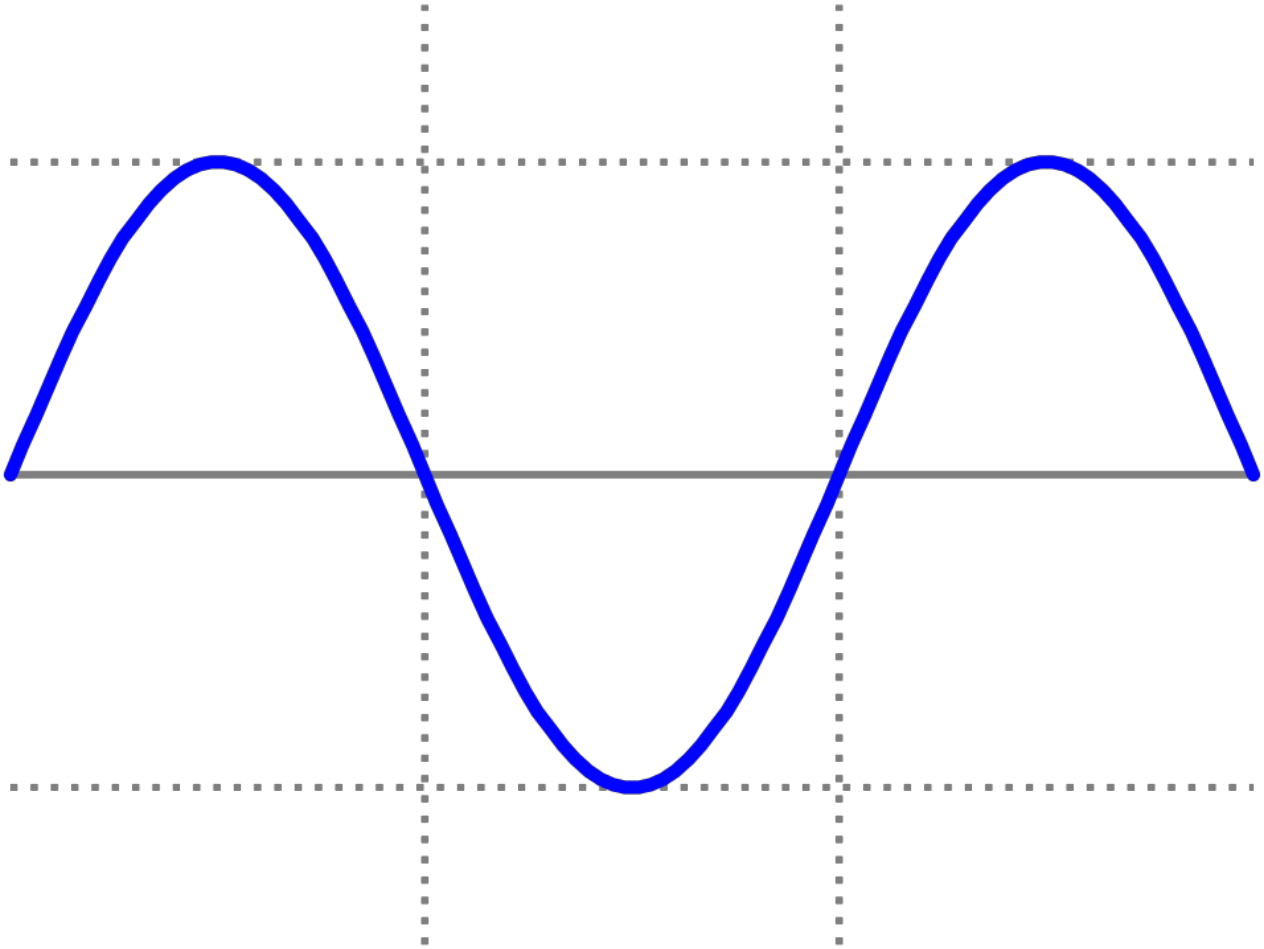
Activity 4.3 AM Simulation with Excel

	A		B	C
0.314159	0.309017	0.628319	0.587785	0.896802
0.628319	0.587785	1.256637	0.951057	1.538842
0.942478	0.809017	1.884956	0.951057	1.760074
1.256637	0.951057	2.513274	0.587785	1.538842
1.570796	1	3.141593	1.23E-16	1
1.884956	0.951057	3.769911	-0.58779	0.363271
2.199115	0.809017	4.39823	-0.95106	-0.14204
2.513274	0.587785	5.026548	-0.95106	-0.36327
2.827433	0.309017	5.654867	-0.58779	-0.27877
3.141593	1.23E-16	6.283185	-2.5E-16	-1.2E-16
3.455752	-0.30902	6.911504	0.587785	0.278768
3.769911	-0.58779	7.539822	0.951057	0.363271
4.08407	-0.80902	8.168141	0.951057	0.14204
4.39823	-0.95106	8.796459	0.587785	-0.36327
4.712389	-1	9.424778	3.68E-16	-1
5.026548	-0.95106	10.0531	-0.58779	-1.53884
5.340708	-0.80902	10.68142	-0.95106	-1.76007
5.654867	-0.58779	11.30973	-0.95106	-1.53884
5.969026	-0.30902	11.93805	-0.58779	-0.8968
6.283185	-2.5E-16	12.56637	-4.9E-16	-7.4E-16
6.597345	0.309017	13.19469	0.587785	0.896802
6.911504	0.587785	13.82301	0.951057	1.538842
7.225663	0.809017	14.45133	0.951057	1.760074
7.539822	0.951057	15.07964	0.587785	1.538842
7.853982	1	15.70796	6.13E-16	1
8.168141	0.951057	16.33628	-0.58779	0.363271
8.4823	0.809017	16.9646	-0.95106	-0.14204
8.796459	0.587785	17.59292	-0.95106	-0.36327
9.110619	0.309017	18.22124	-0.58779	-0.27877
9.424778	3.68E-16	18.84956	-7.4E-16	-3.7E-16
9.738937	-0.30902	19.47787	0.587785	0.278768
10.0531	-0.58779	20.10619	0.951057	0.363271
10.36726	-0.80902	20.73451	0.951057	0.14204
10.68142	-0.95106	21.36283	0.587785	-0.36327
10.99557	-1	21.99115	8.58E-16	-1



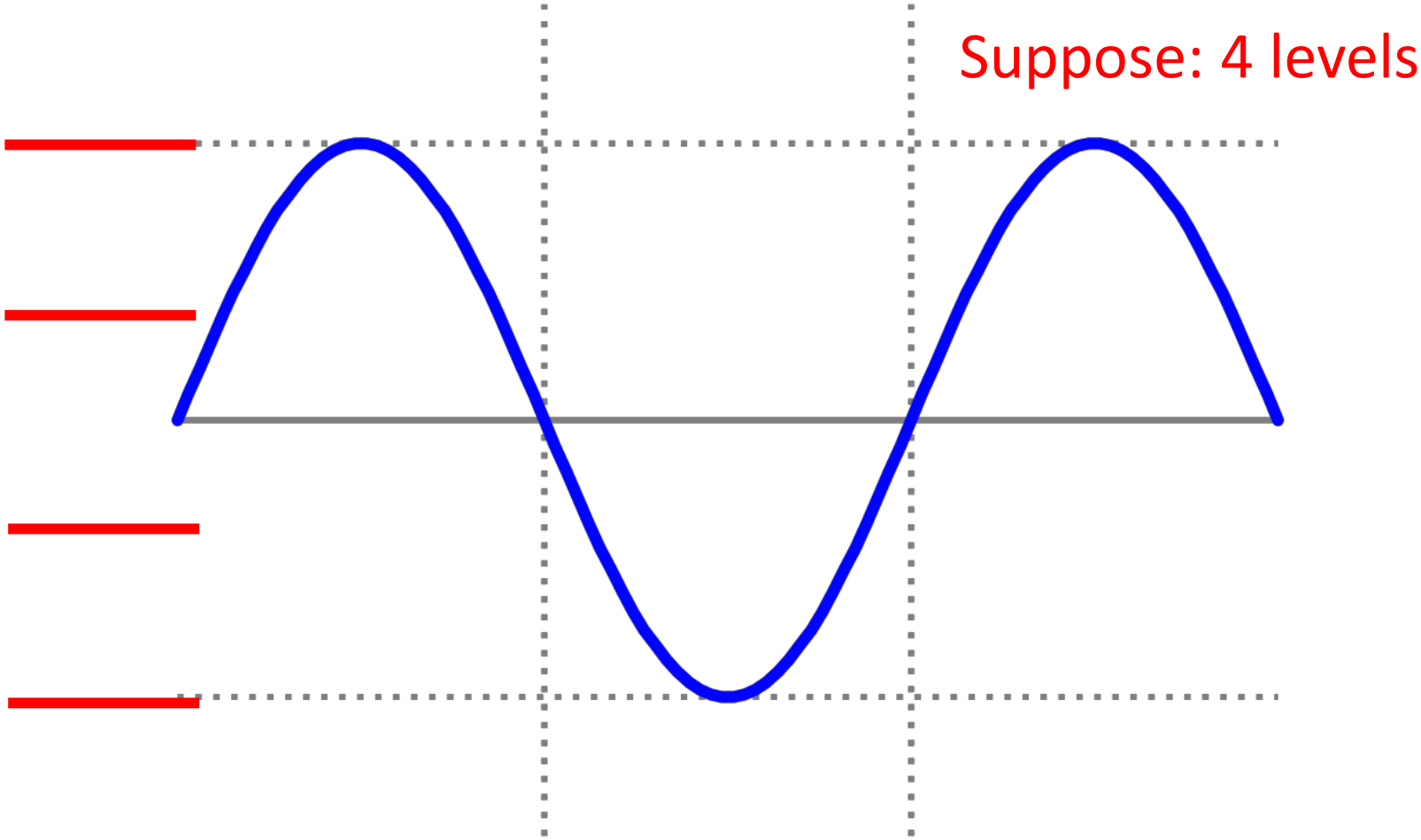
Convert Analog Signal to Digital Signal

- Step1: Analog signal



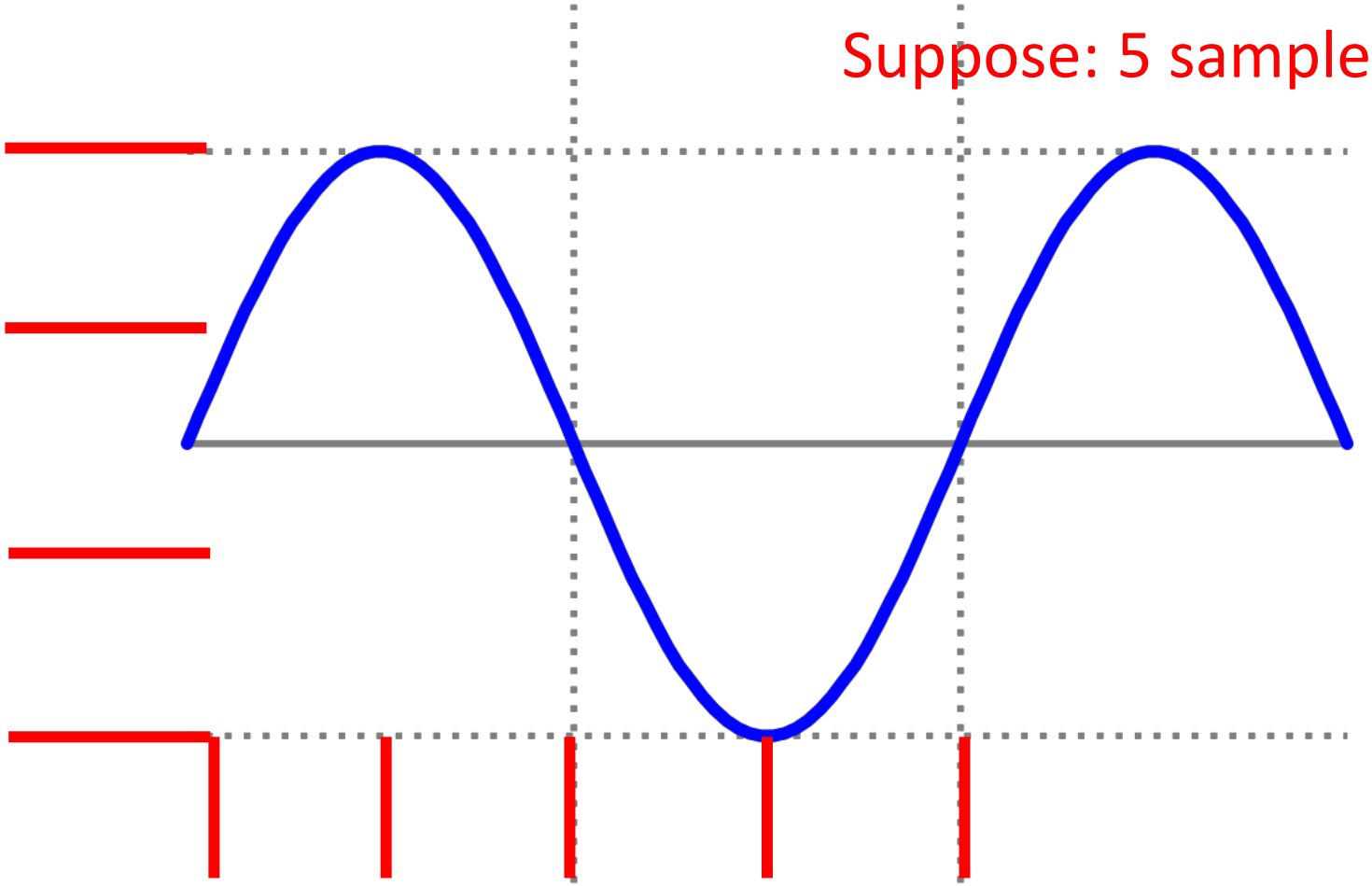
Convert Analog Signal to Digital Signal

- Step2: Define the number of levels (bits)



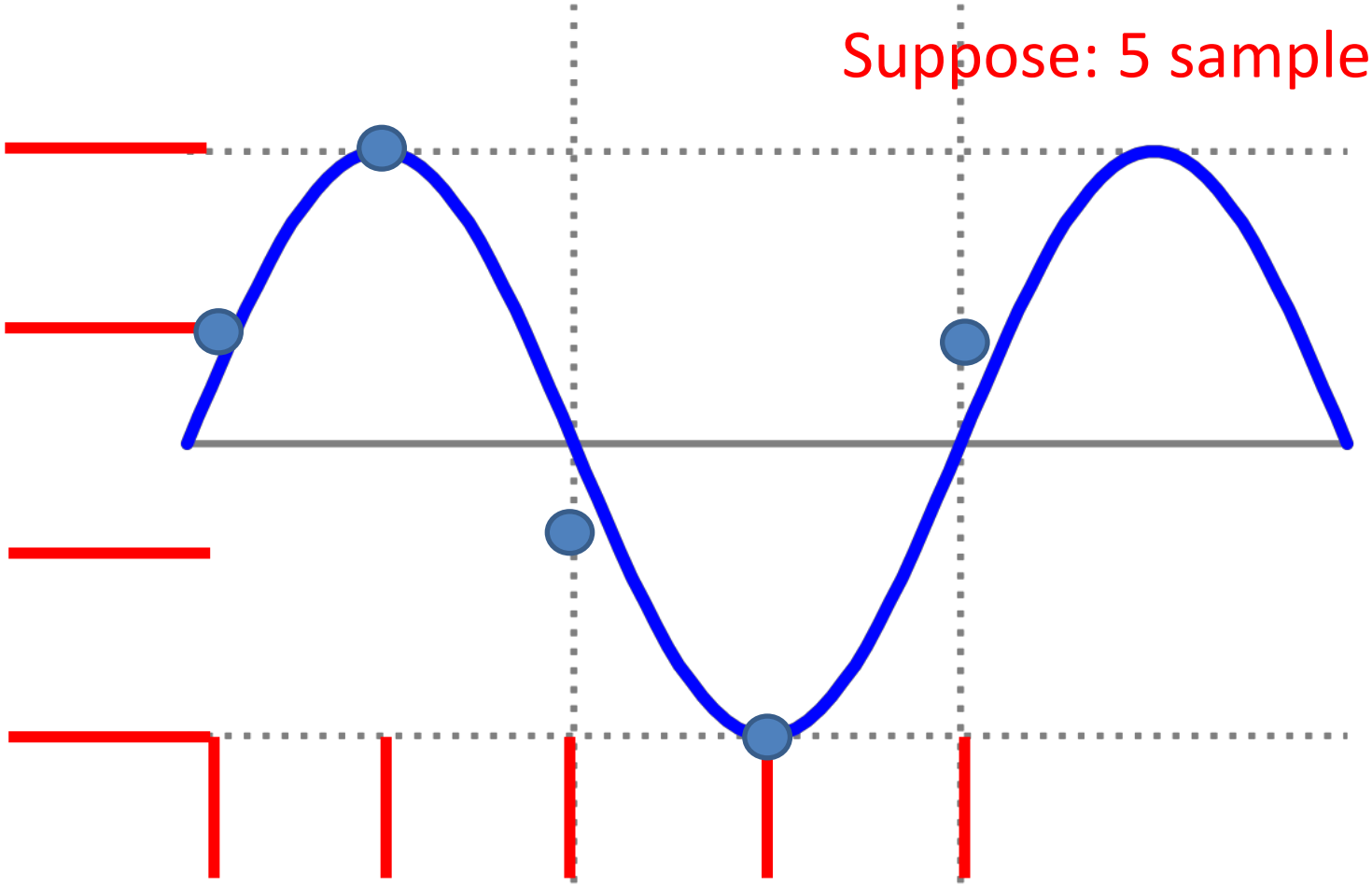
Convert Analog Signal to Digital Signal

- Step3: Define the number of sampling



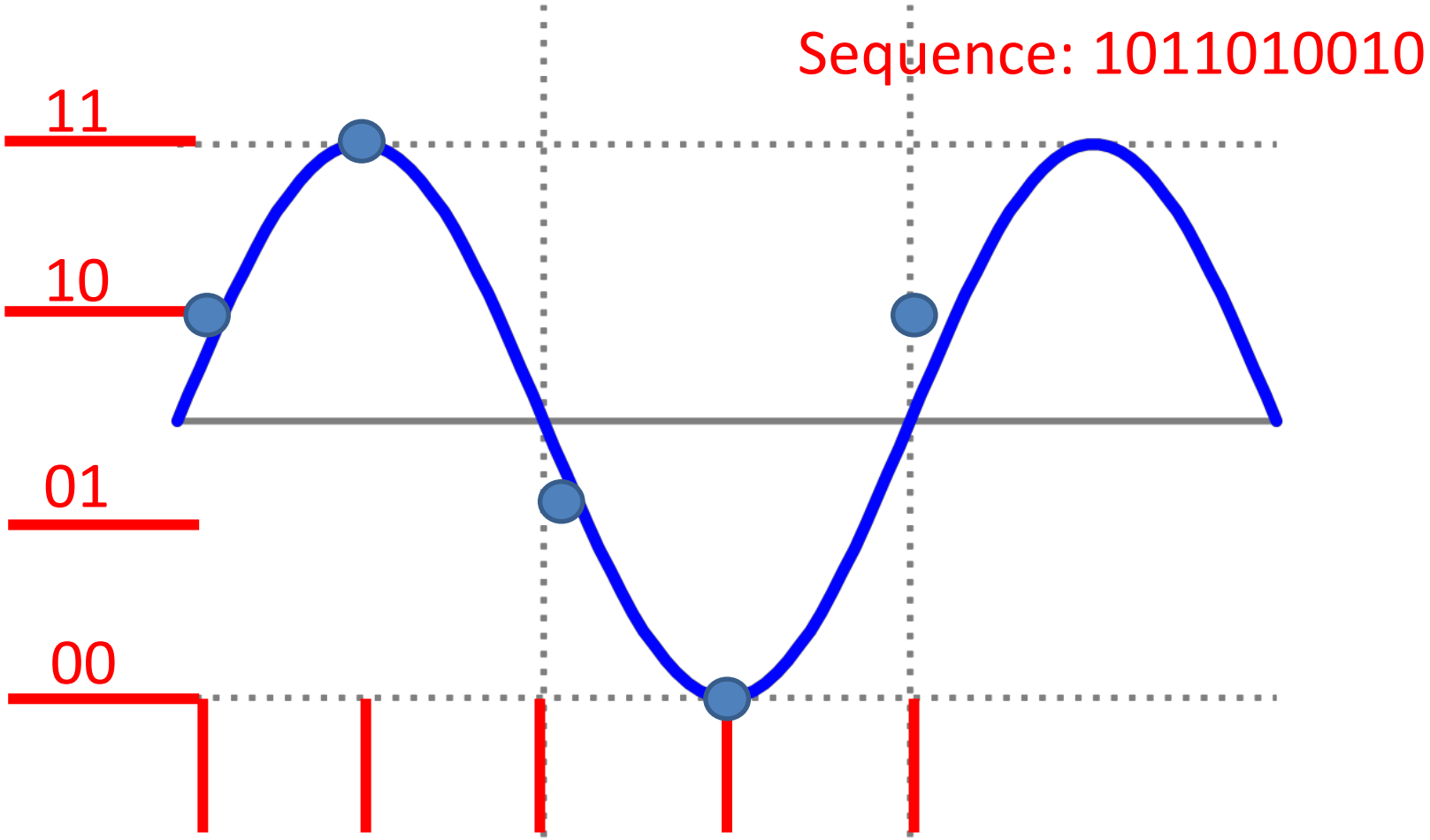
Convert Analog Signal to Digital Signal

- Step4: Map the level and sampling to the signal

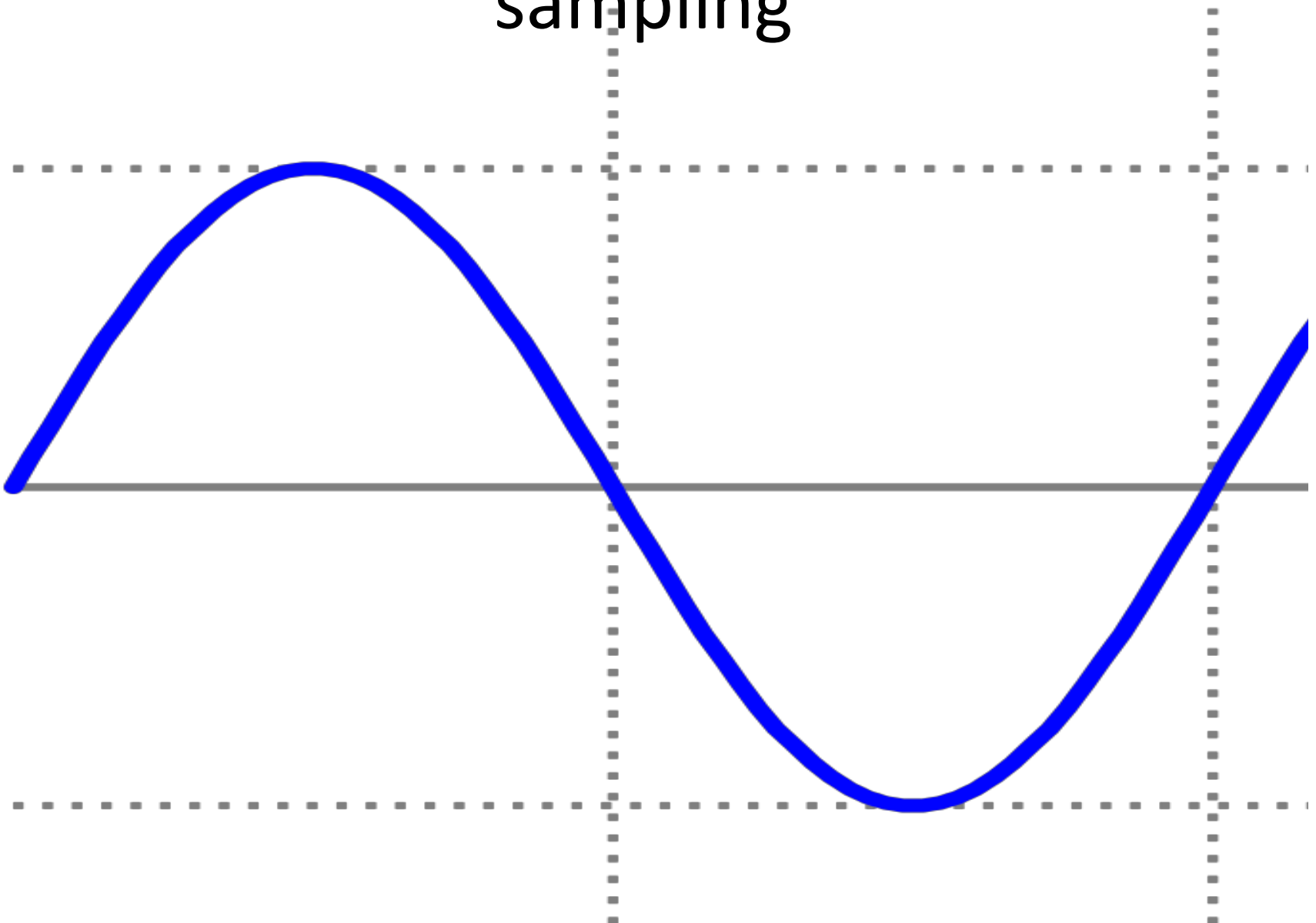


Convert Analog Signal to Digital Signal

- Step5: Reading digital signal



Activity 4.4 Drawing 8 levels and 10 sampling



Reference

- https://www.quora.com/What-is-an-application-of-an-RS-flip-flop
- https://electronics.stackexchange.com/questions/jk-flip-flop-toggle