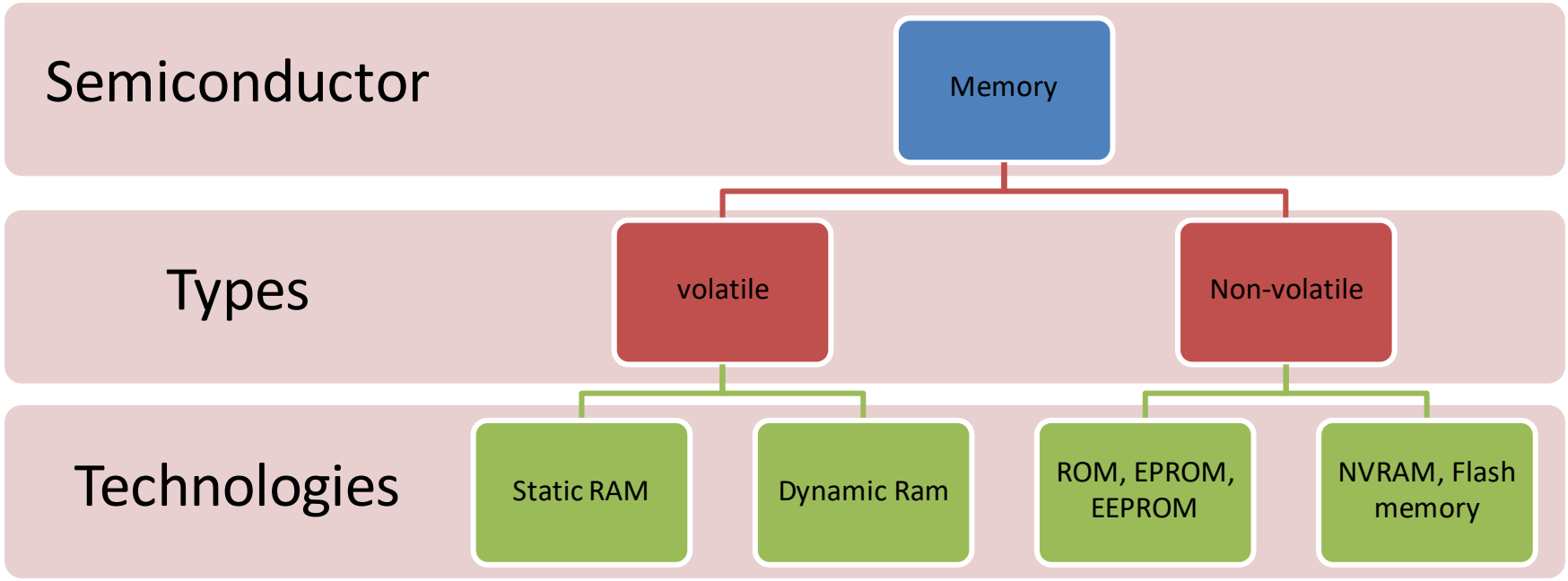
Chapter6:
Memory unit

Asst.Prof.Dr.Supakit Nootyaskool

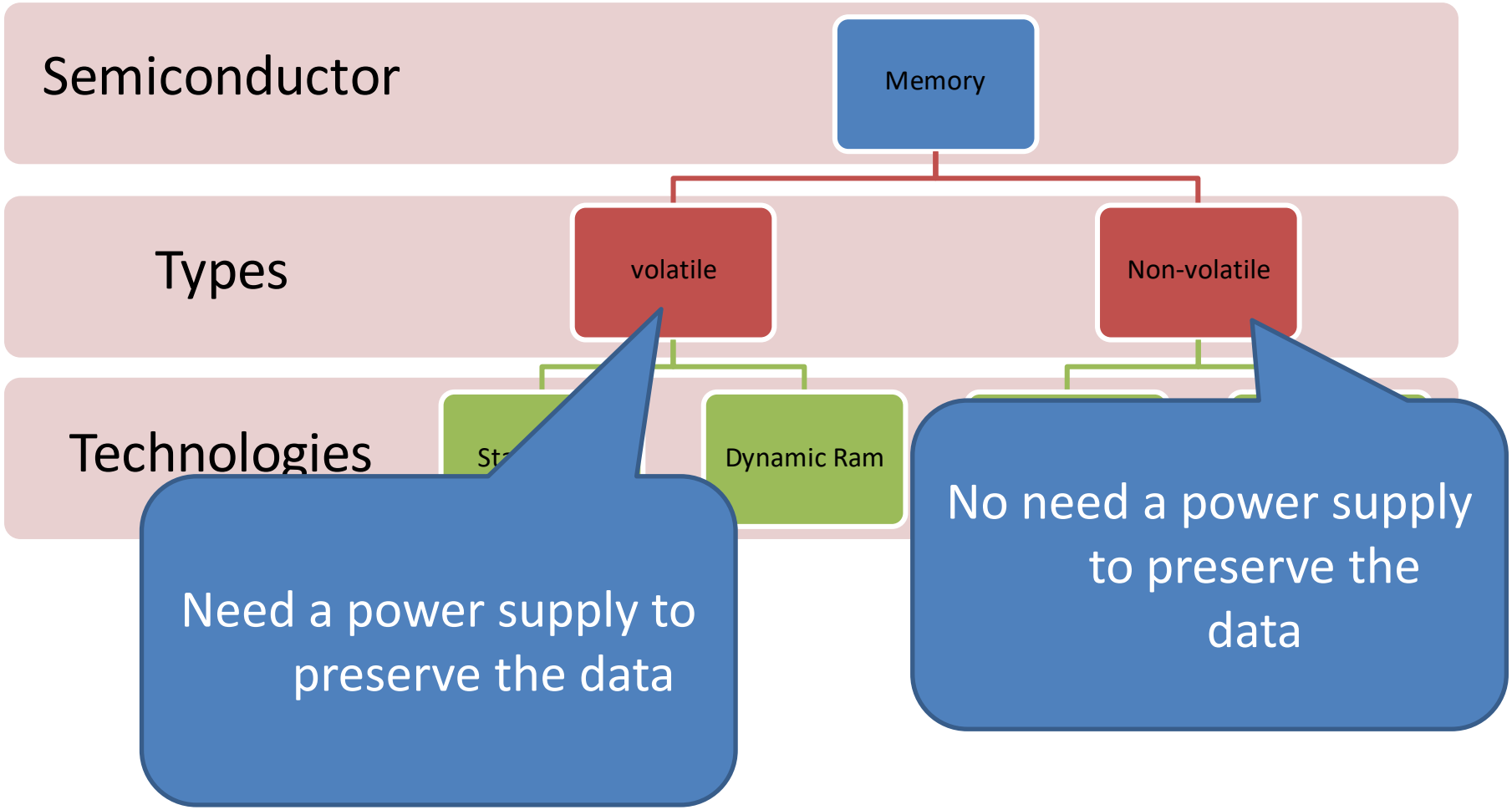
Objective

- To learn structure inside of memory
- To understand difference between static memory and dynamic memory
- To explain why the memory having address bus, data bus, and control signal.

Memory types

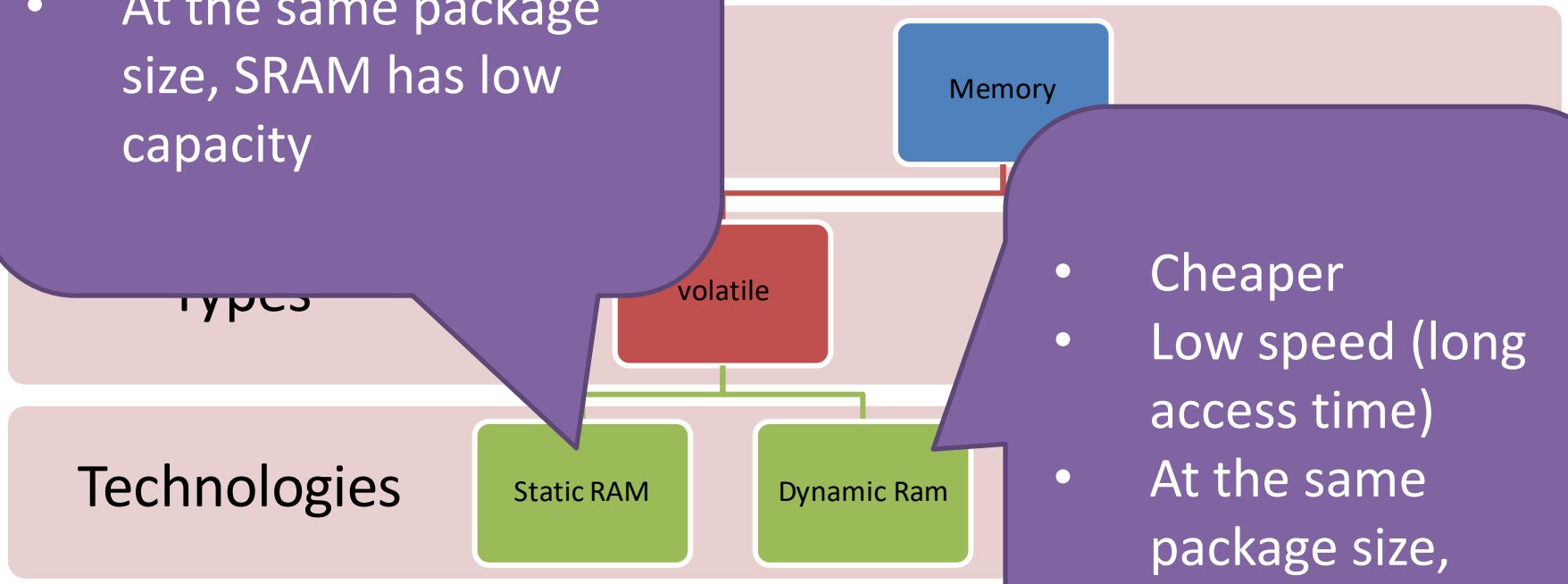


Memory types



ory types

- More expensive
- High speed (high access time)
- At the same package size, SRAM has low capacity

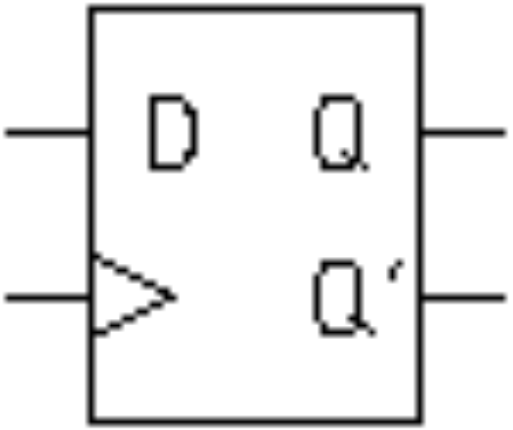


- Cheaper
- Low speed (long access time)
- At the same package size, DRAM has high capacity.

Static RAM (SRAM)

- SRAM created from D flip-flop.

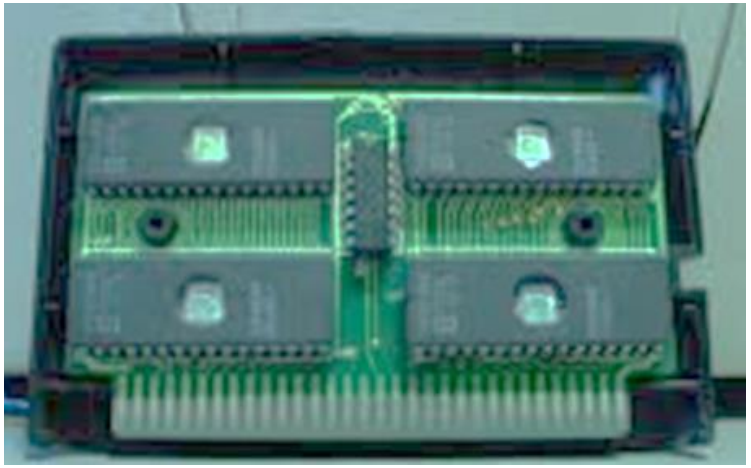
D	Clk	Q
0		0
1		1

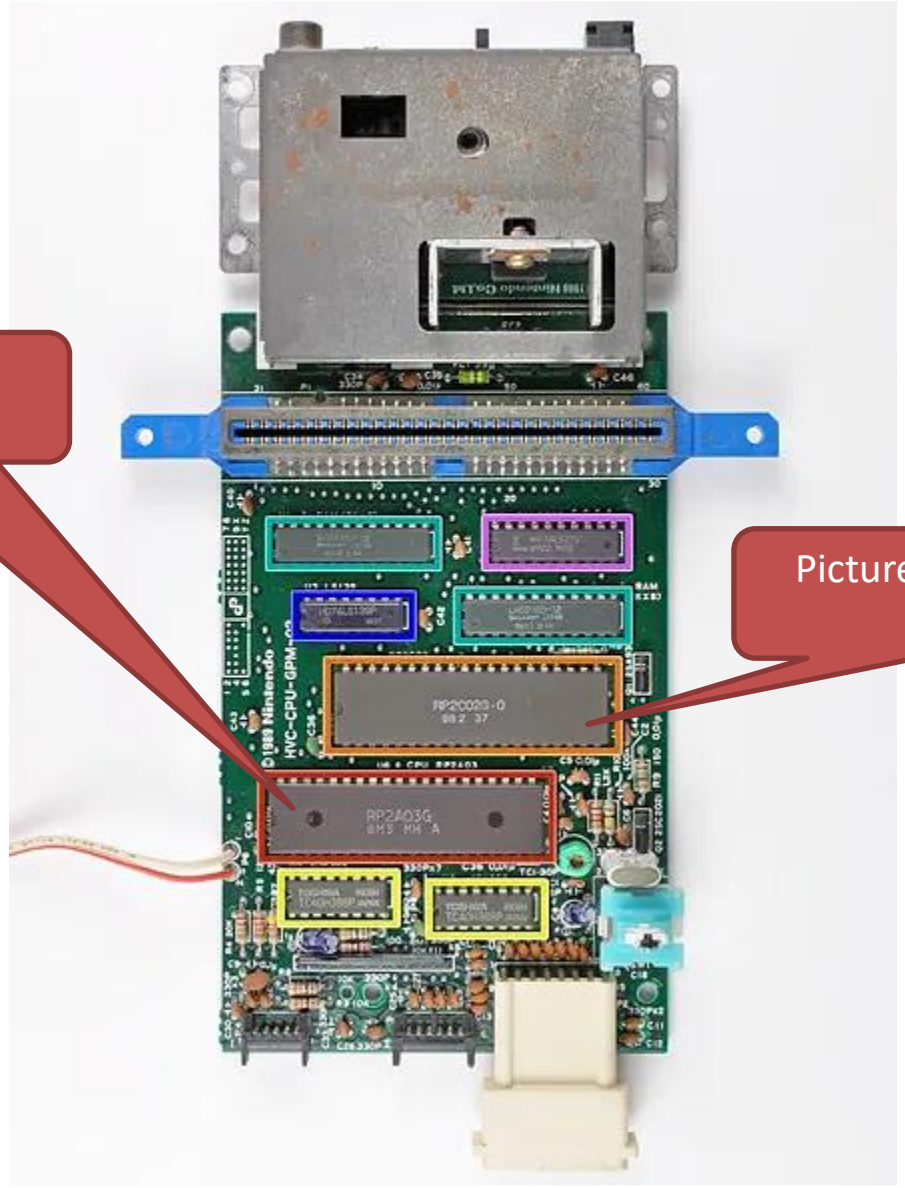


SRAM and DRAM in Video GAME

8-bit CPU

Picture processing Unit





Character representation in ASCII code “A”

41H = 01000001

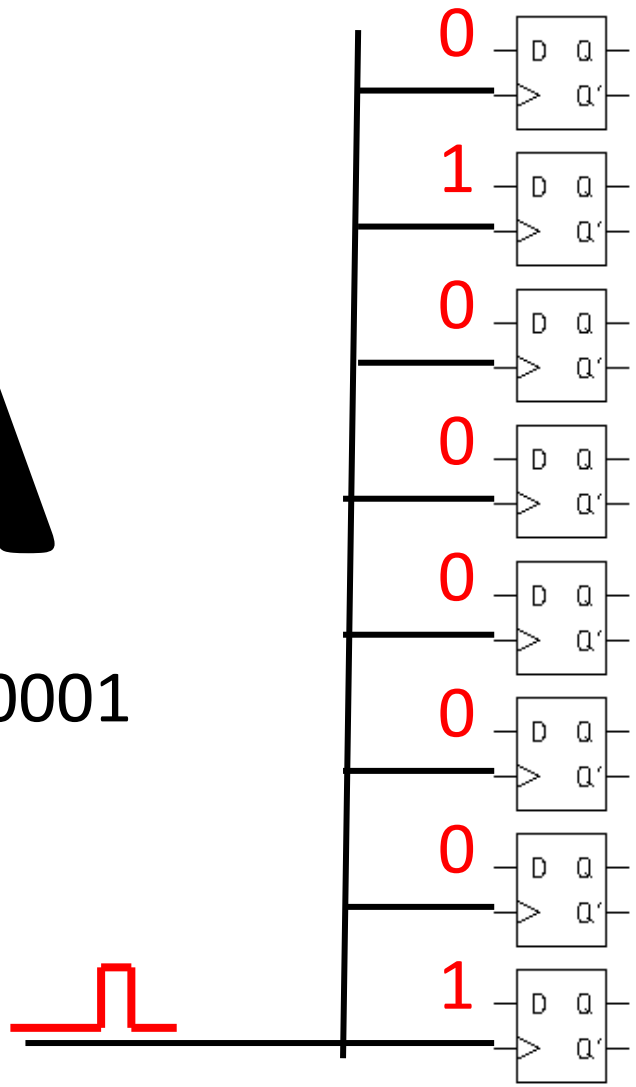
A

Column → / Row ↓	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
10	LF	SUB	*	:	J	Z	j	z
11	VT	ESC	+	;	K	[	k	{
12	FF	FS	,	<	L	\	l	|
13	CR	GS	-	=	M	]	m	}
14	SO	RS	.	>	N	^	n	~
15	SI	US	/	?	O	_	o	DEL

Static RAM keeps “A”

A

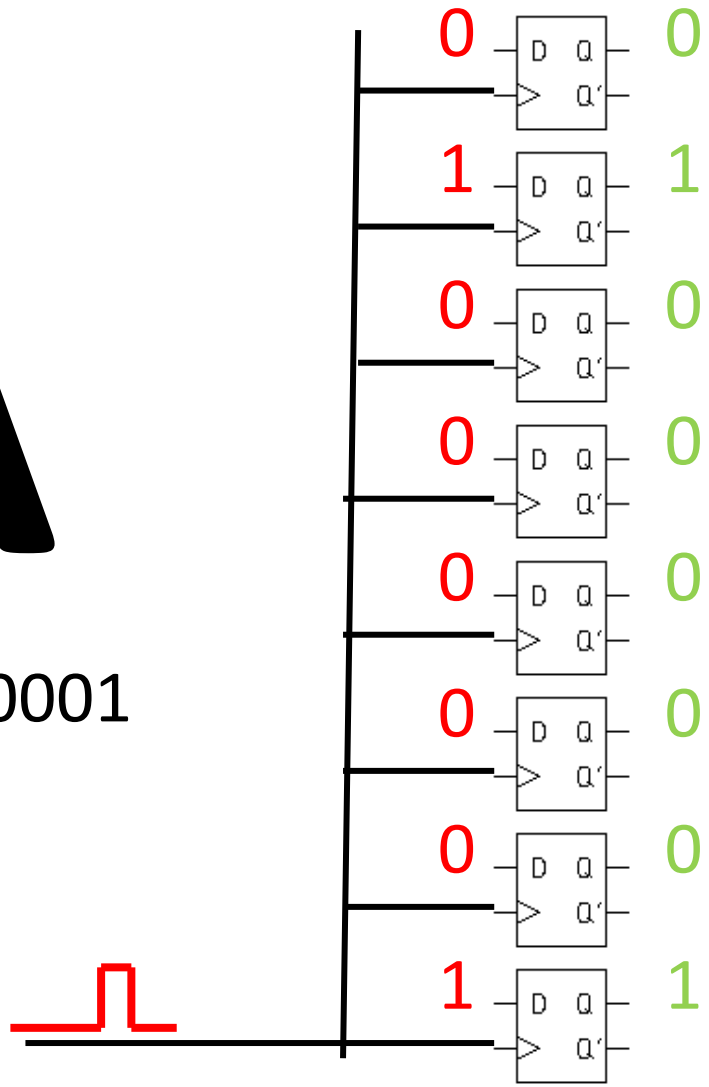
41 = 01000001



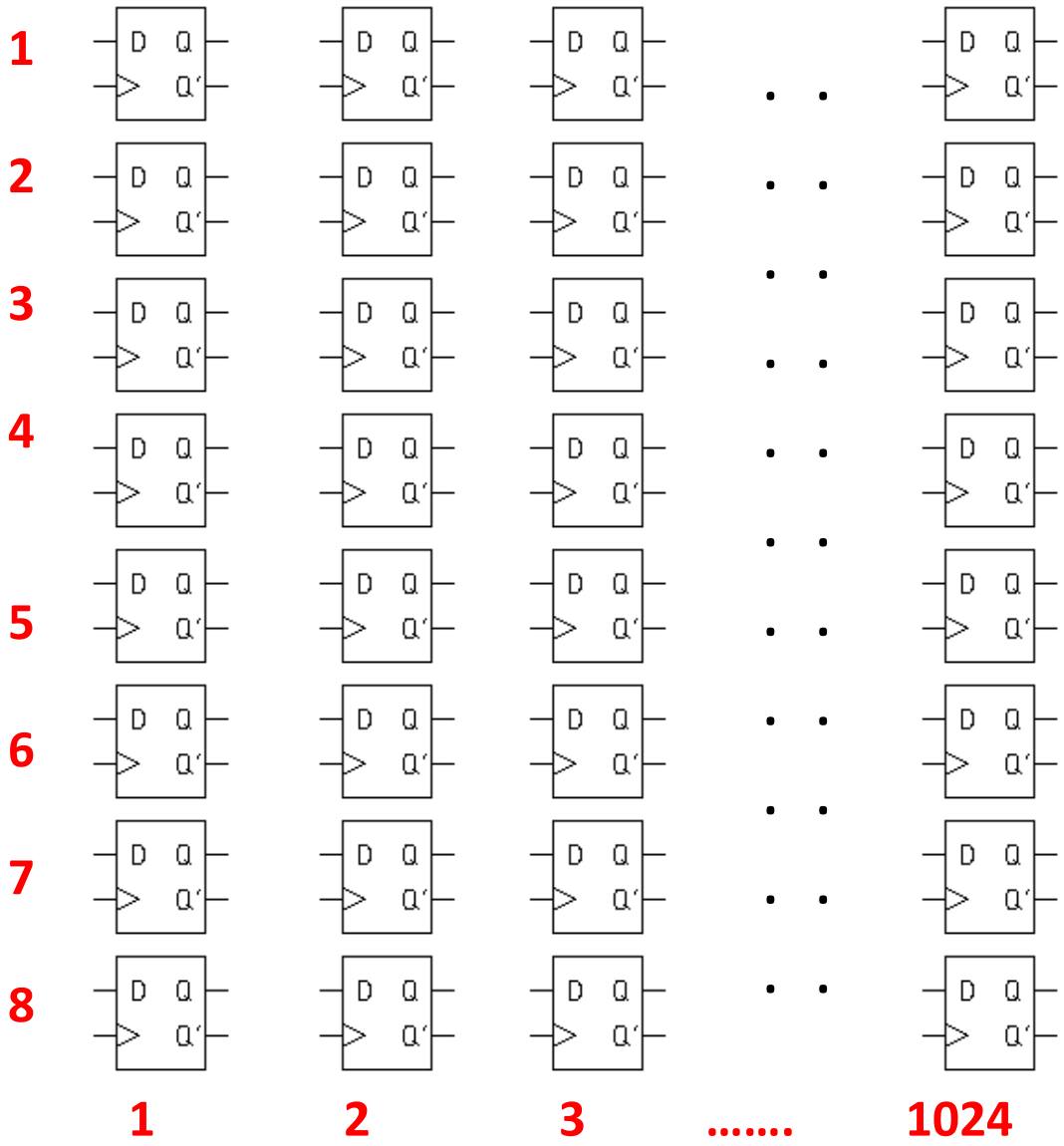
Static RAM keeps “A”

A

41 = 01000001



Static RAM

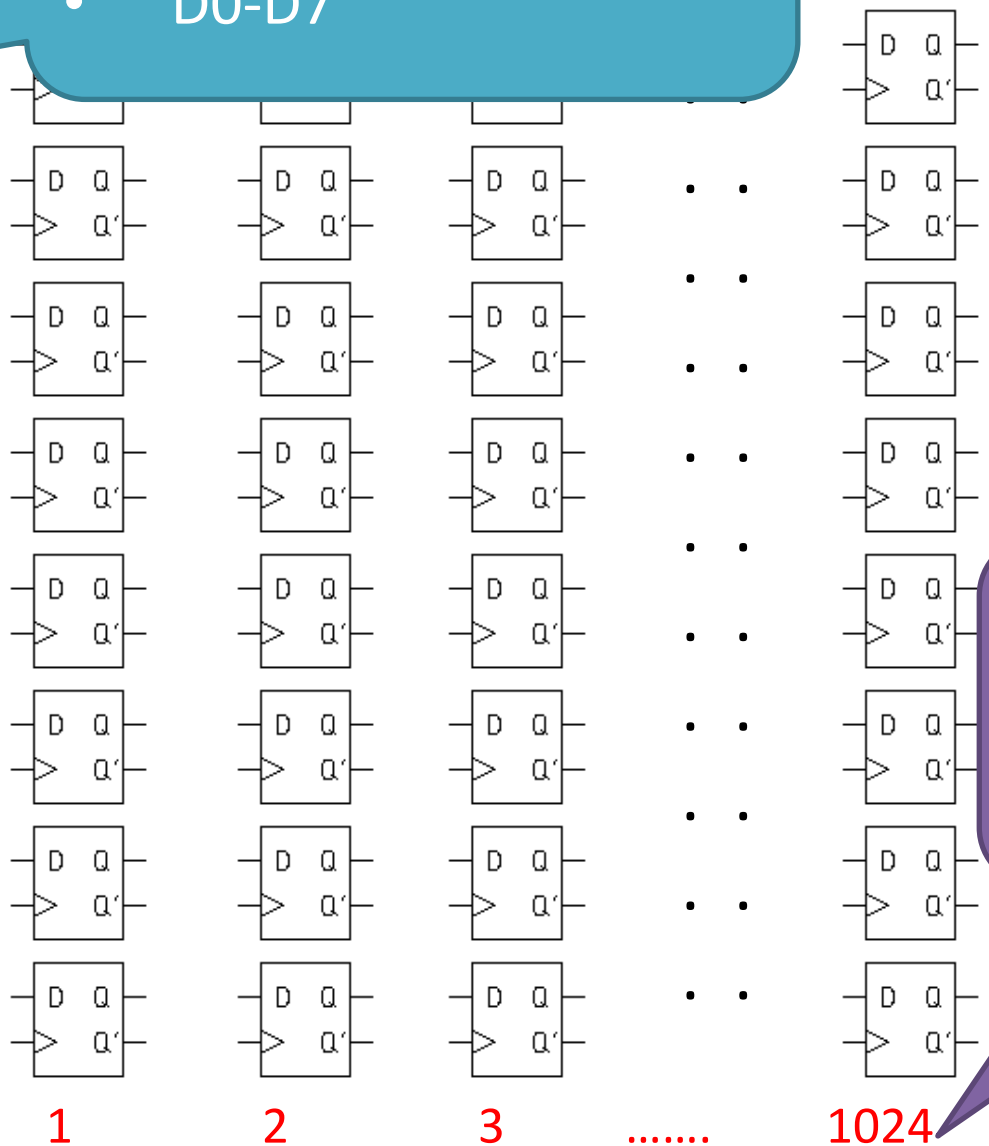


Memory Size

8 x 1024 = 8192 ≈ 8K

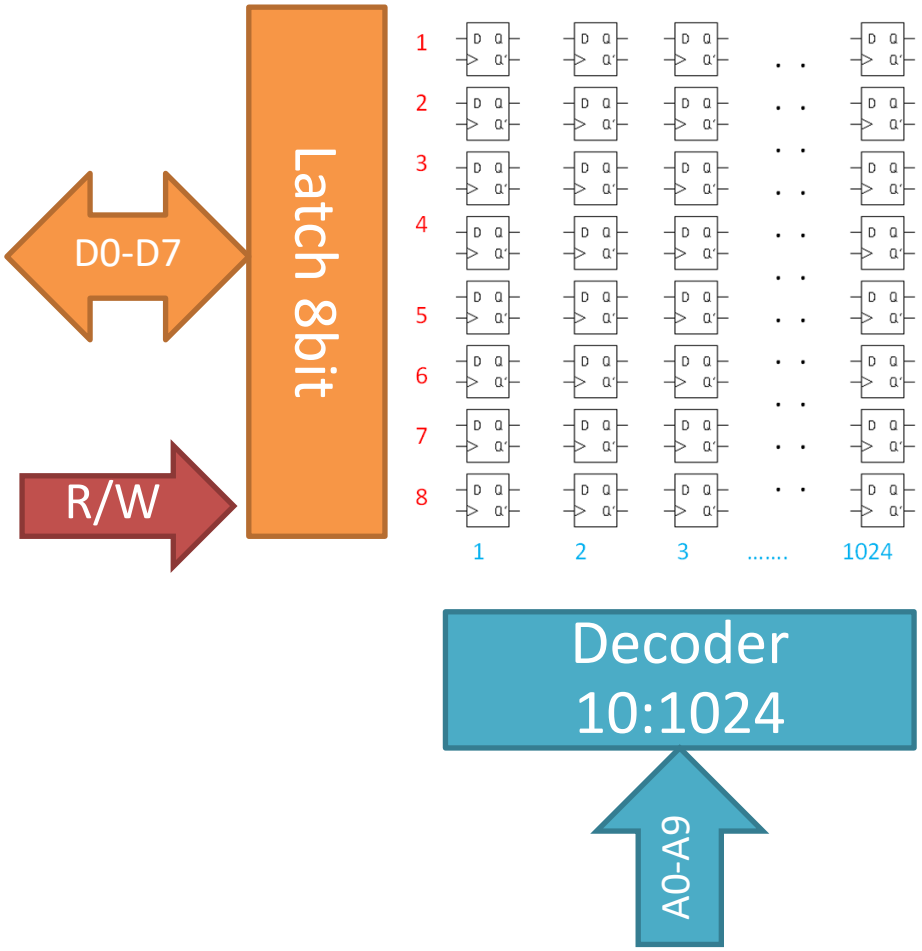
AM

- Data
- 8Bit
- D0-D7



- Address
- 1024 Address = 2^?
- 1 2 4 8 16 32 64 128 256
  512 = 10Lines (A0-A9)

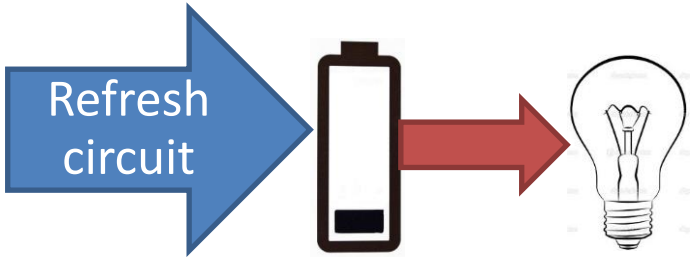
Static RAM

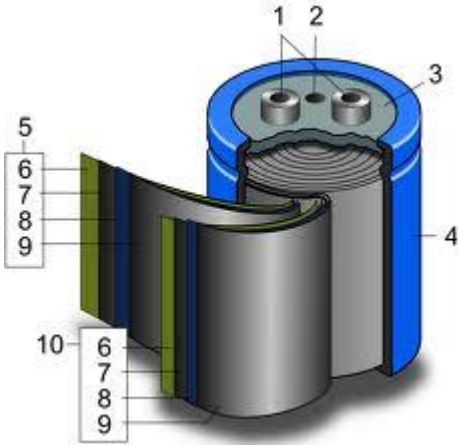


A memory chip has 3 group of pins

1) Data bus is bi-directional
2) Address bus is input
3) Control signals are read, write, chip enable,

Concept of Dynamic RAM





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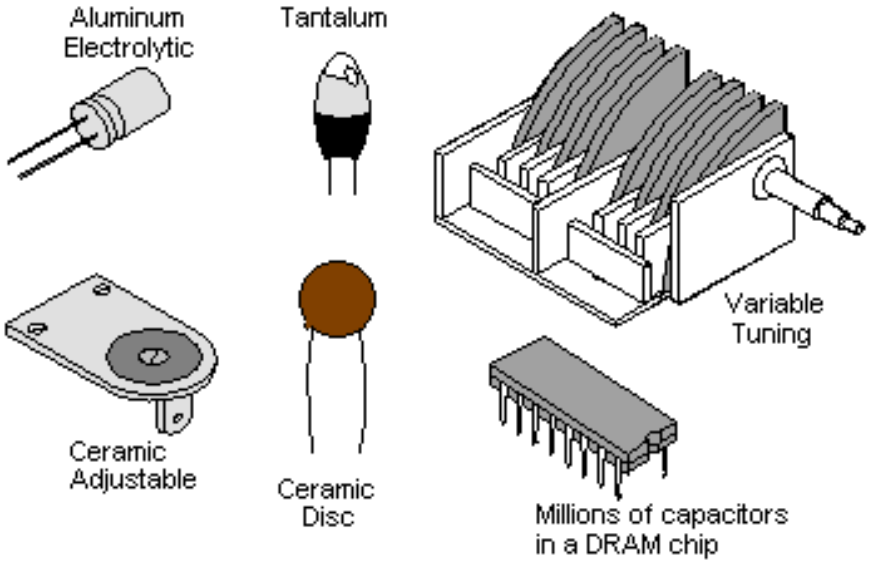
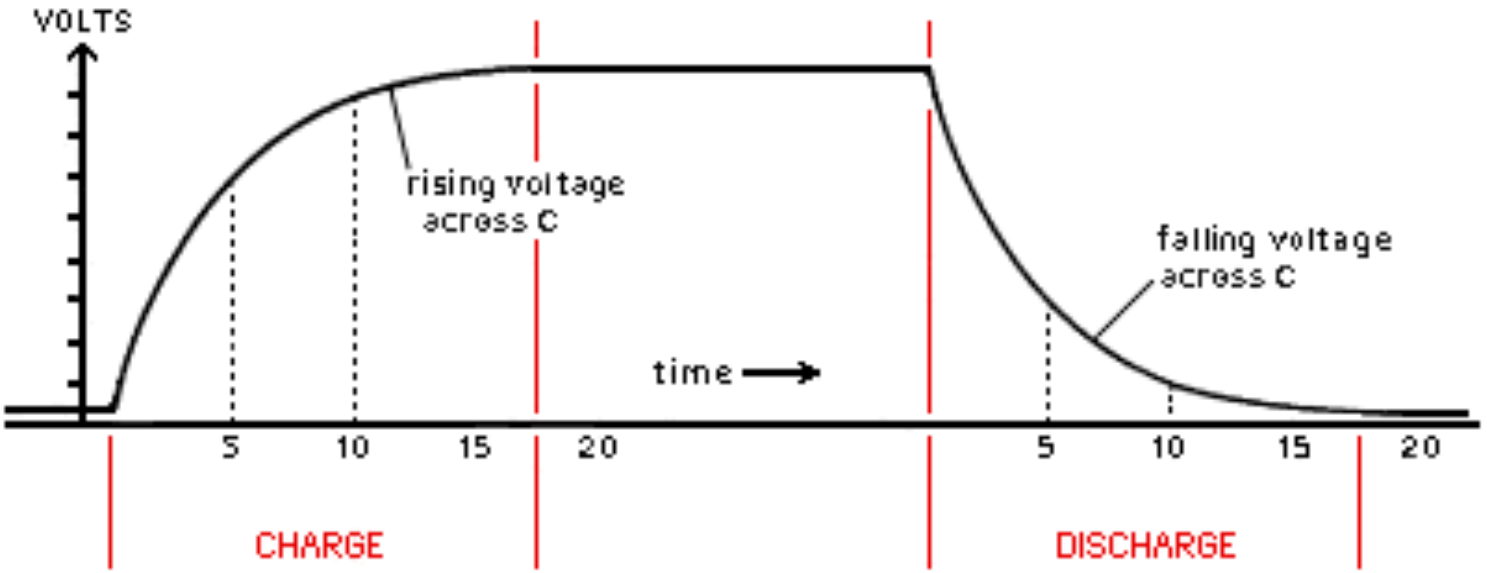
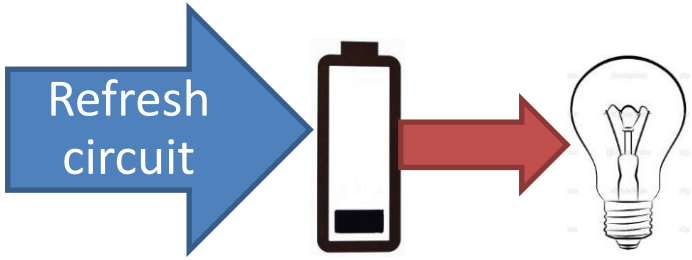
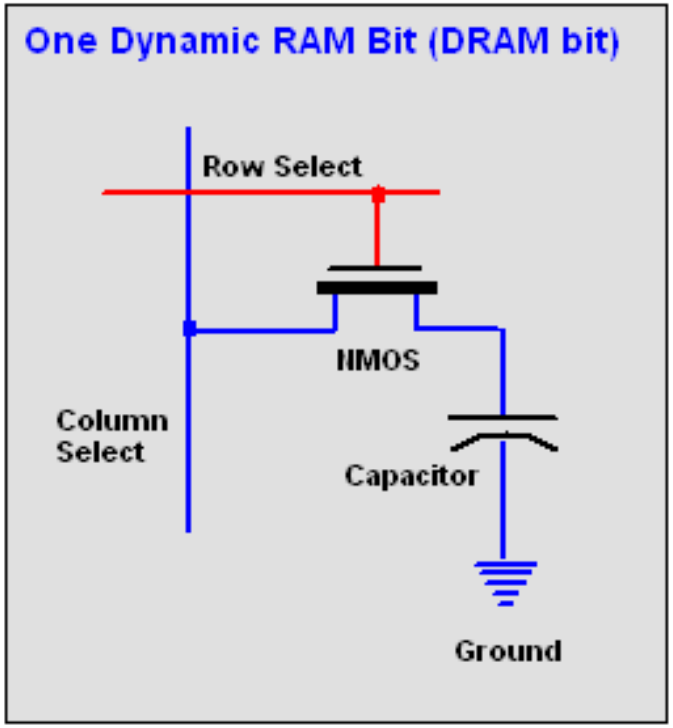


Charge/Discharge Capacitor

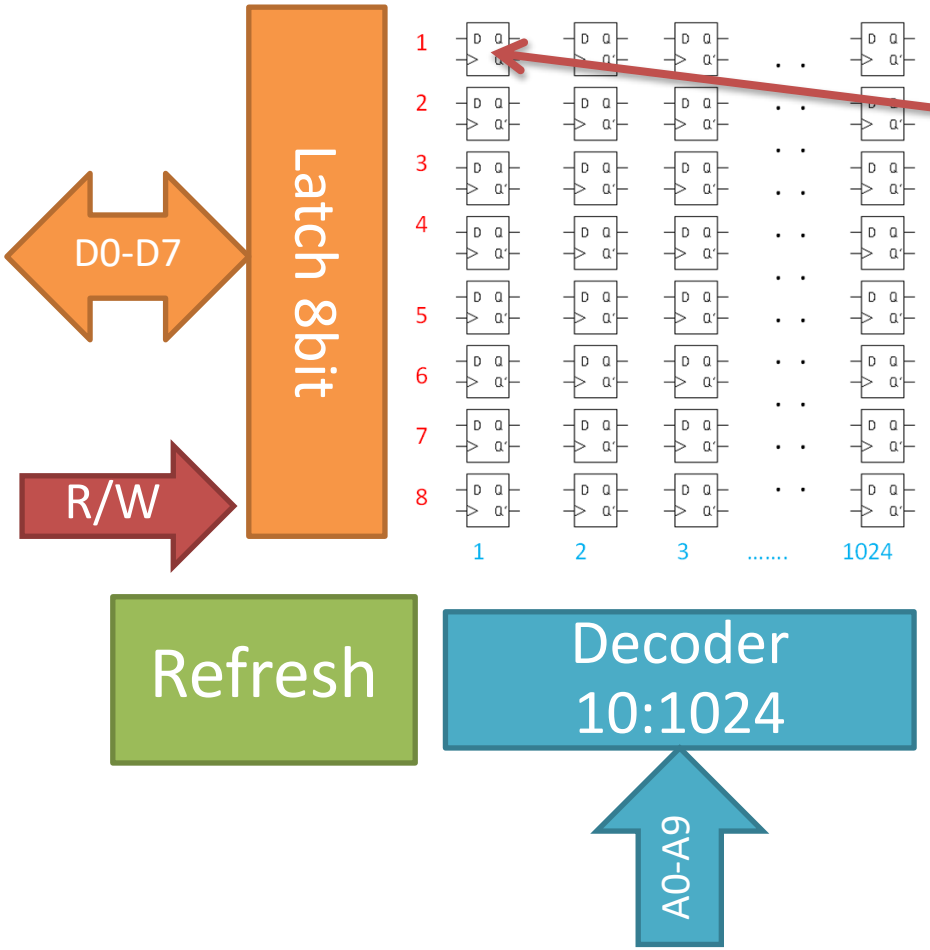


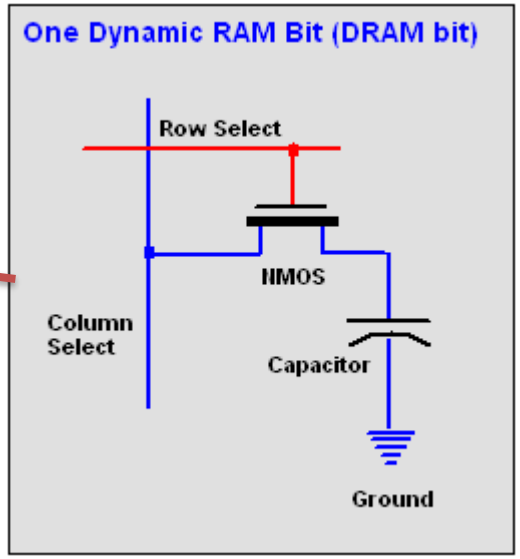
DRAM


Refresh
circuit

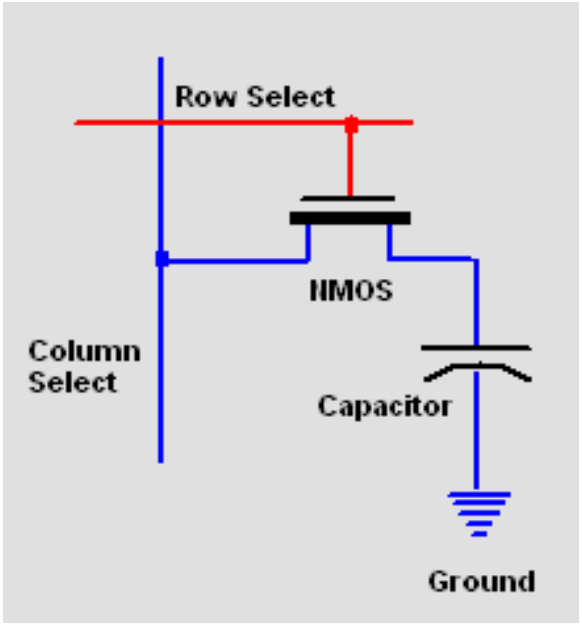

One Dynamic RAM Bit (DRAM bit)
Row Select
NMOS
Column
Select
Capacitor
Ground

DRAM

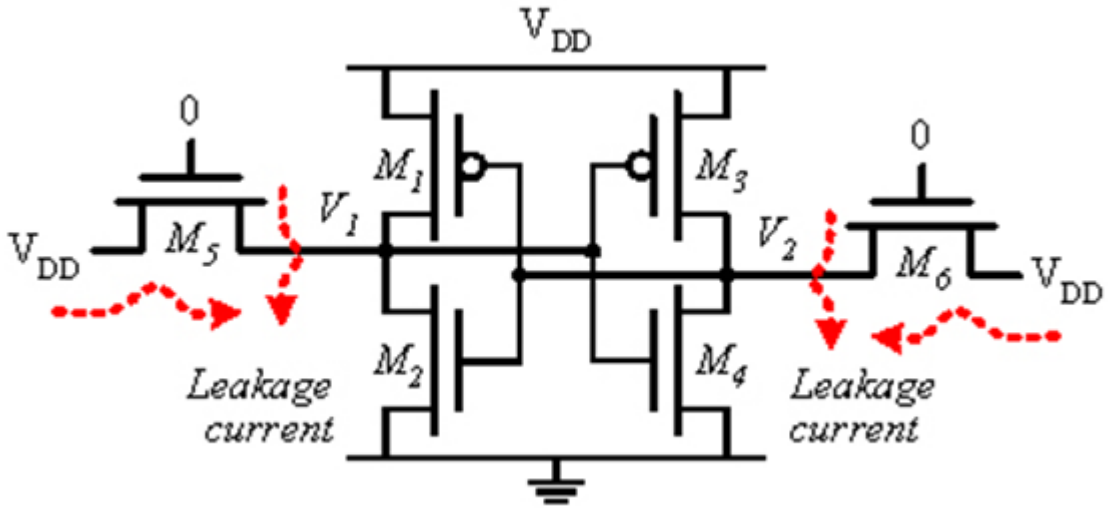

D0-D7
Latch 8bit
R/W
1
2
3
4
5
6
7
8
1
2
3
.....
1024
Refresh
Decoder
10:1024
A0-A9


One Dynamic RAM Bit (DRAM bit)
Row Select
NMOS
Column
Select
Capacitor
Ground

Comparing structure of memory devices in 1 bit



Dynamic RAM



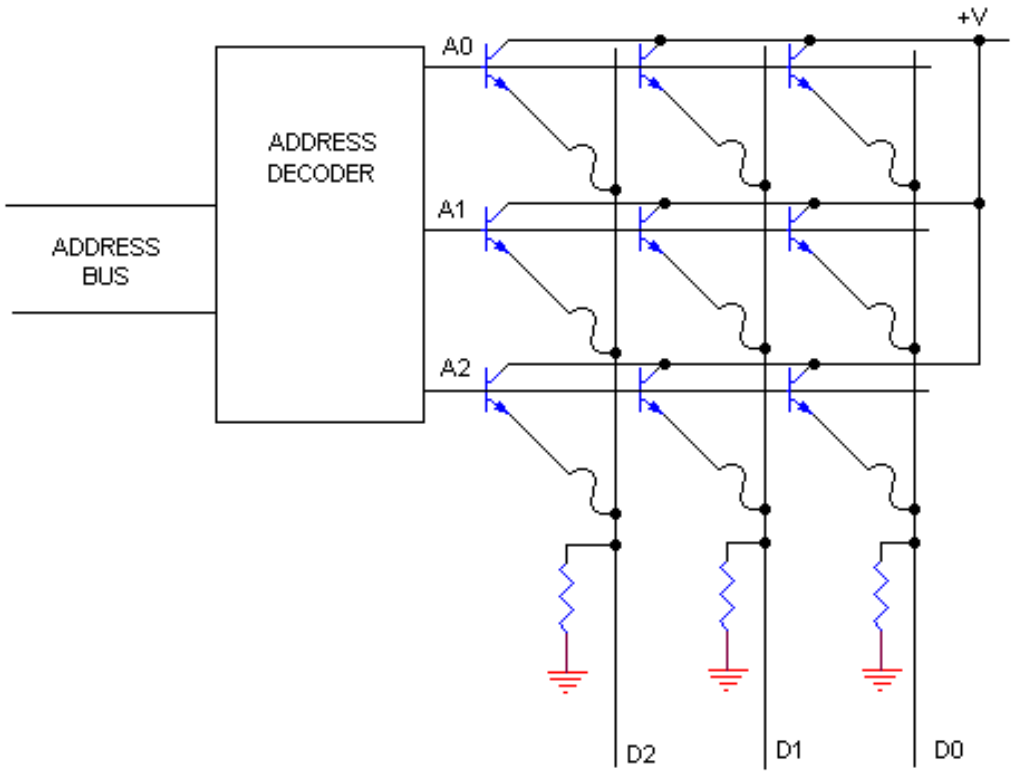
Static RAM

Other types

- Speed access improvement
  - EDO DRAM (Extended data-out DRAM)
  - SDRAM (Synchronous DRAM)
  - DDR SDRAM (Double data rate SDRAM)
  - RDRAM (Rambus DRAM)
- More than a data bus
  - VRAM (Video RAM)
  - SGRAM (Synchronous graphic ram)

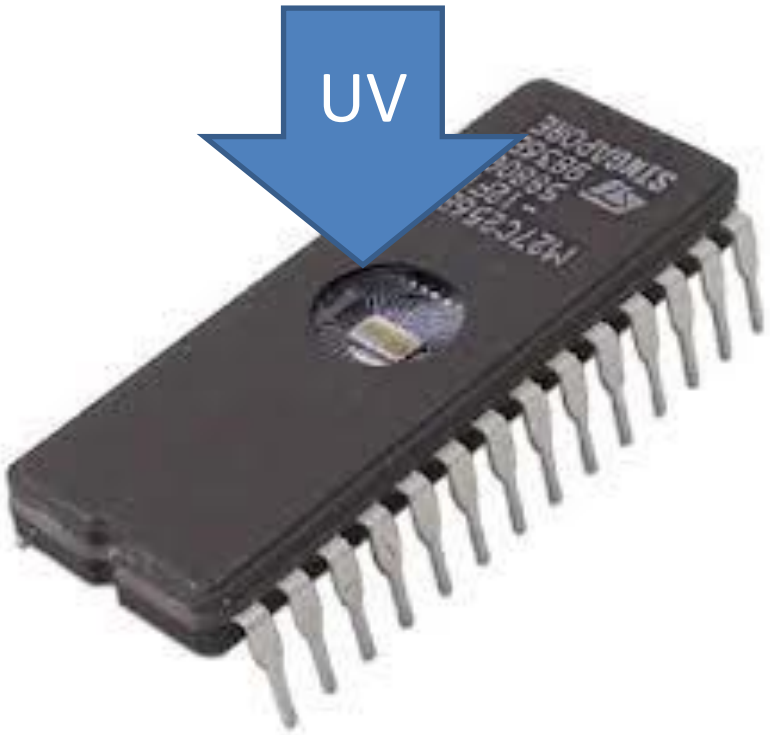
ROM

- PROM (Programmable read only memory)



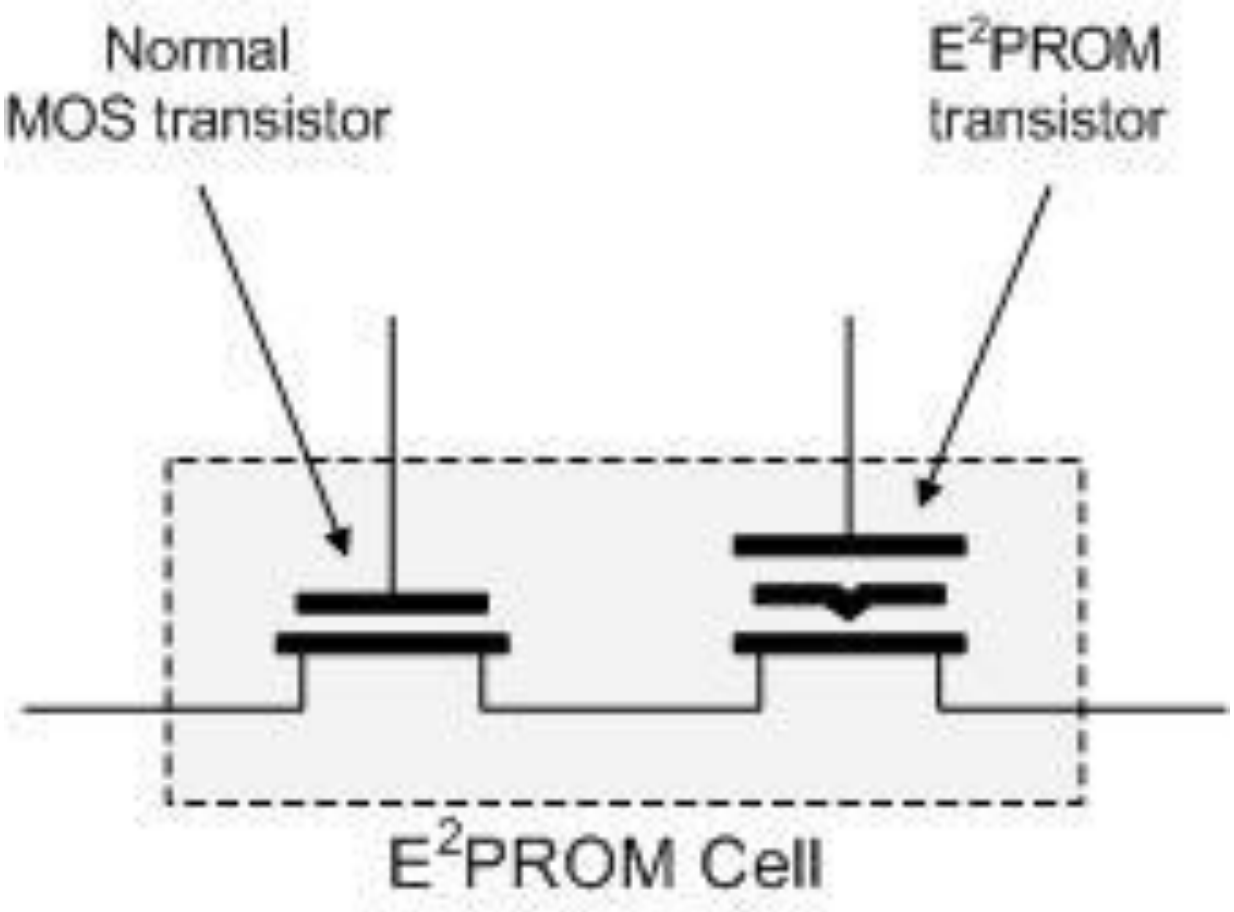
Read Only Memory (ROM)

- EPROM (Erasable PROM)



ROM

- Electrical EPROM (Erasable PROM)

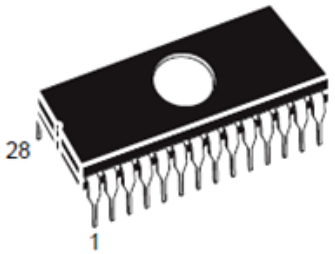


SGS-THOMSON MICROELECTRONICS

M2764A

NMOS 64K (8K x 8) UV EPROM

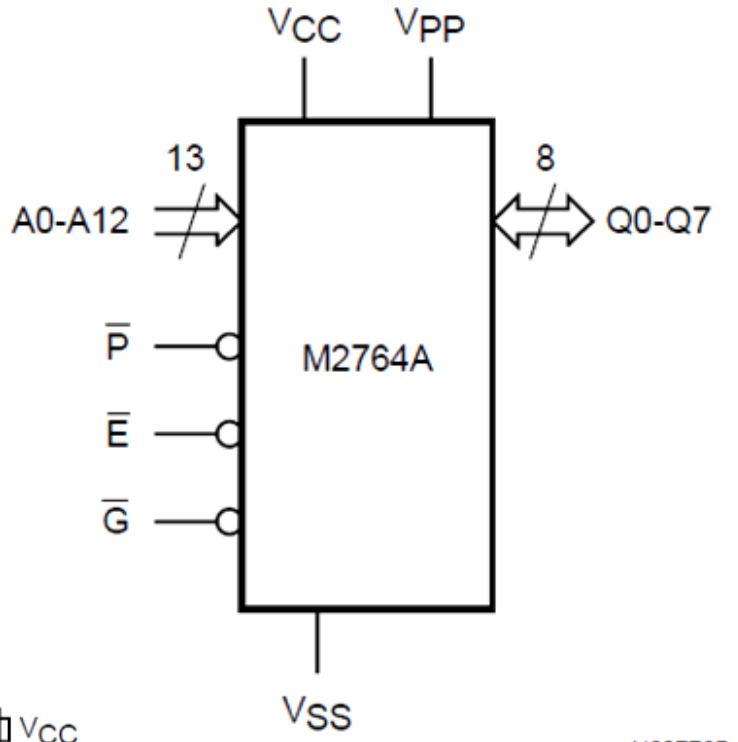
- FAST ACCESS TIME: 180ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V

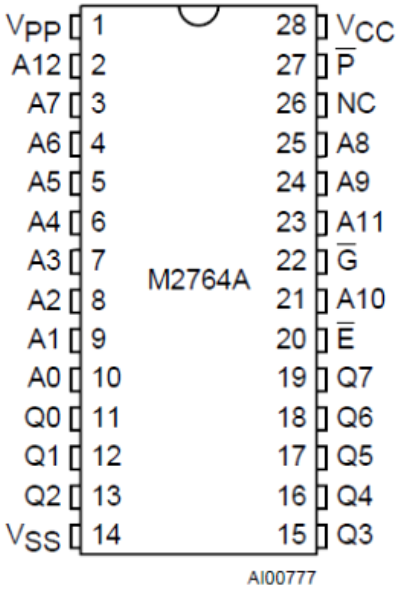


FDIP28W (F)

Table 1. Signal Names

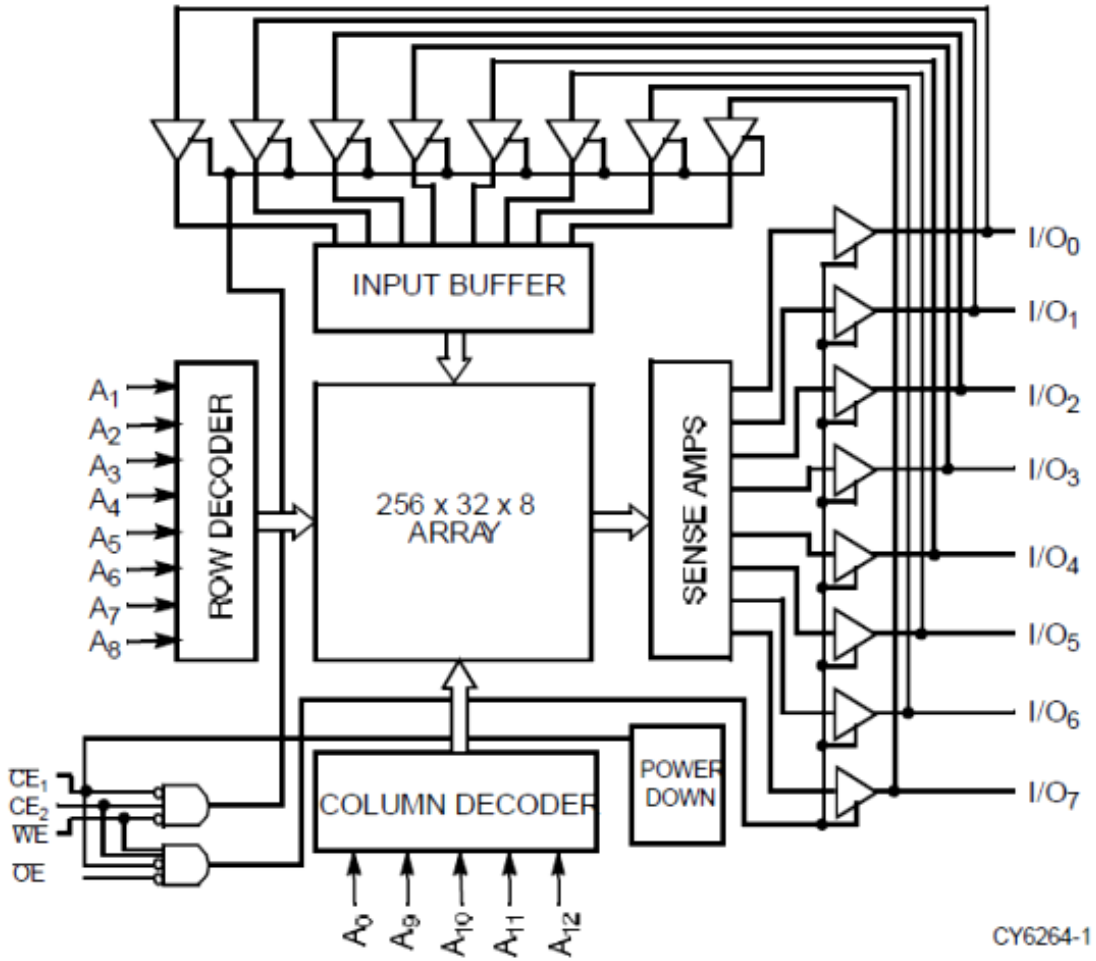
A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground





8K x 8 Static RAM

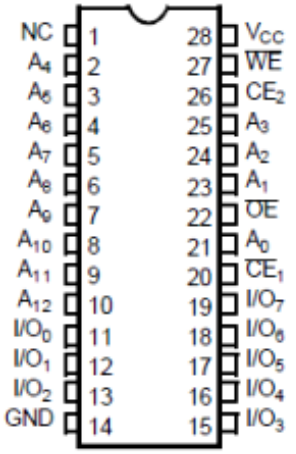
Logic Block Diagram



CY6264-1

Pin Configuration

SOIC
Top View



CY6264-2