Computer Z80 MSX compatible.

Flash memory: 64kB
Ram memory..: 32kB
2 RS232
CH376S fat reader

CPU Z80

File: CpuZ80.kicad_sch

Memory

File: Memory.kicad_sch

Interfaces

File: Interfaces.kicad_sch

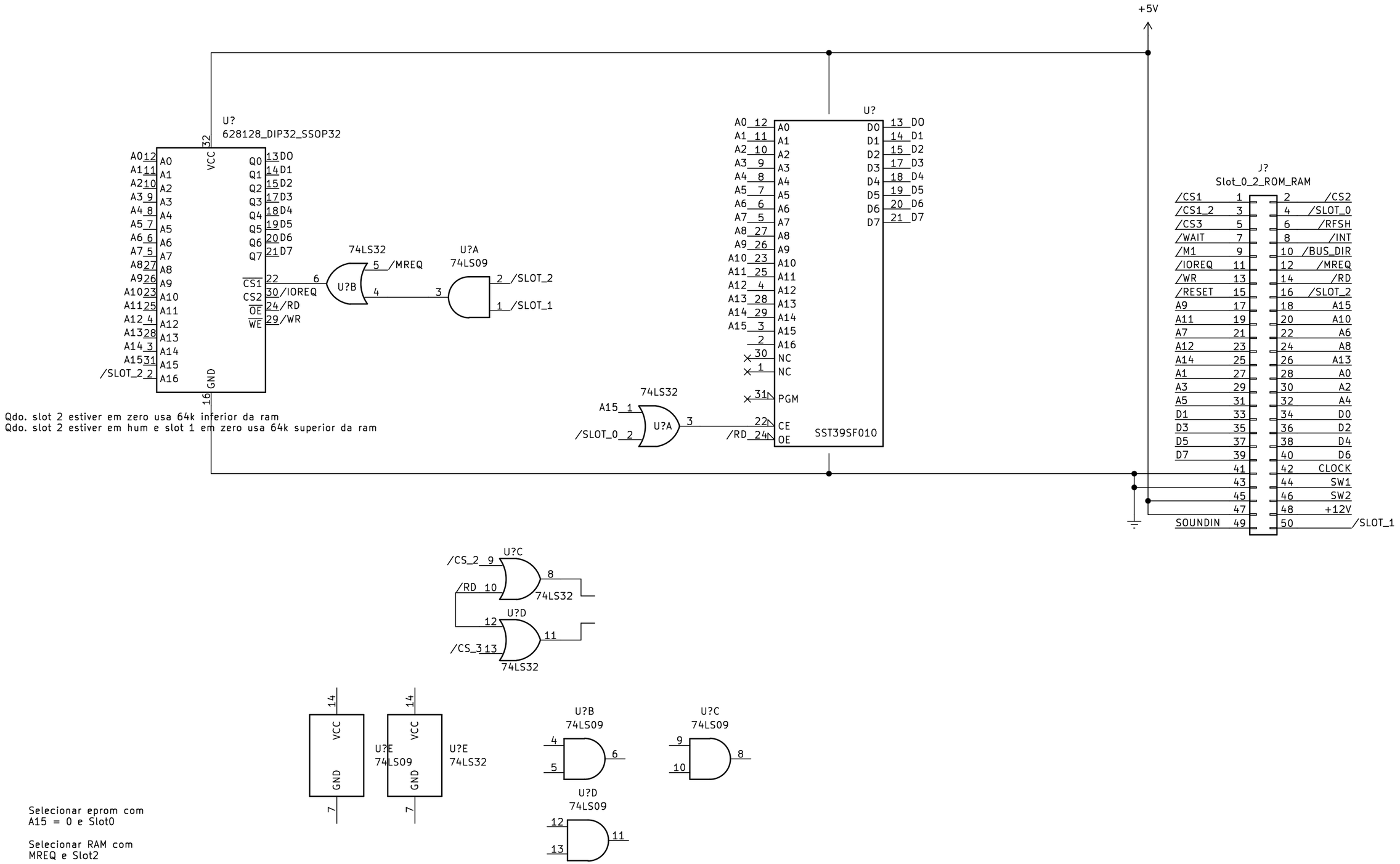
Connectors

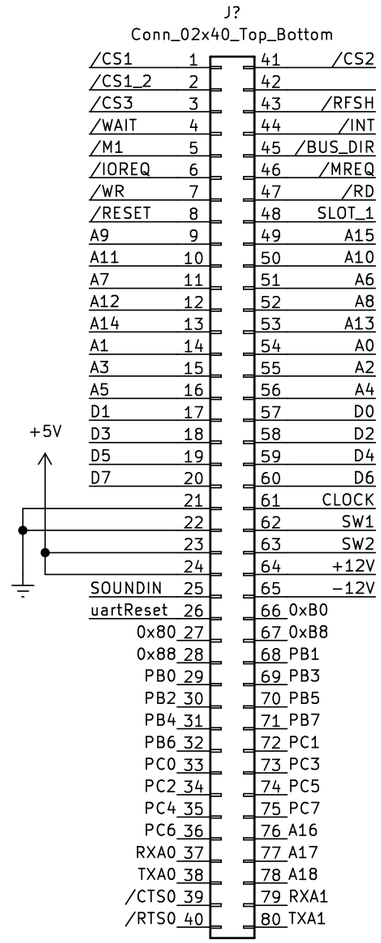
File: Connectors.kicad_sch

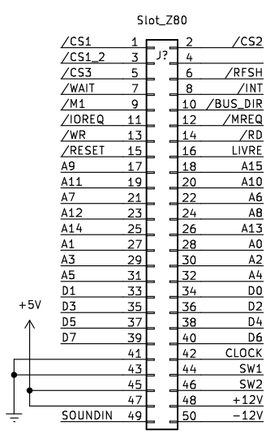
Backplane

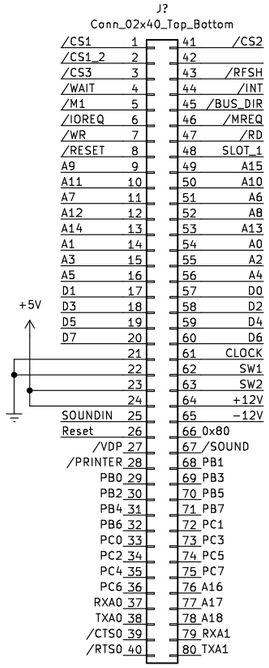
File: backplane.kicad_sch

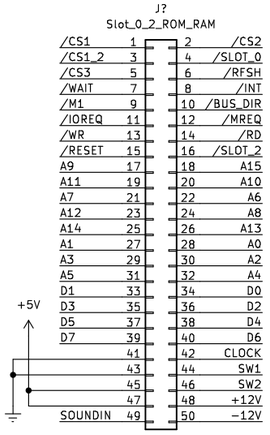
U1
Z80CPU
C?
100nF
/reset 26
/clock 6
/INT 16
/M1 27
/RFSH 28
/WAIT 24
/RD 21
/WR 22
/MREQ 19
/IORQ 20
/BUSCK 23
A0 30
A1 31
A2 32
A3 33
A4 34
A5 35
A6 36
A7 37
A8 38
A9 39
A10 40
A11 1
A12 2
A13 3
A14 4
A15 5
D0 14
D1 15
D2 12
D3 8
D4 7
D5 9
D6 10
D7 13
U2A
74HC14
U?F
74HC14
/0xB0 13
/WR 11
12 0xB0
10 WR
U?
74LS138
U?B
74LS09
C?
CAP
/M1 5
/IORQ 5
A6 4
A7 4
A3 1
A4 2
A5 3
0x80 SCL
0x88 SDA WR
/PRINTER 0x90
/VDP 0x98
/SOUND 0xA0
/CS8255 0xA8
0xB0 SDA RD
0xB8 UART
GNDREF
U?
8255
reset 35
/CS8255 6
/RD 5
/WR 36
/A0 9
/A1 8
D0 34
D1 33
D2 32
D3 31
D4 30
D5 29
D6 28
D7 27
PA0 4
PA1 3
PA2 2
PA3 1
PA4 40
PA5 39
PA6 38
PA7 37
PB0 18
PB1 19
PB2 20
PB3 21
PB4 22
PB5 23
PB6 24
PB7 25
PC0 14
PC1 15
PC2 16
PC3 17
PC4 13
PC5 12
PC6 11
PC7 10
U2B
/clock
R1 1M
Y1
CPU Crystal
R2 1k
C1 22pF
C2 22pF
X?
4.915200Mhz
/clock+
RN1 10K
RN2 10K
RN3 10K
RN? 10K
A0 A1 A2 A3 A4 A5 A6 A7
A8 A9 A10 A11 A12 A13 A14 A15
D0 D1 D2 D3 D4 D5 D6 D7
/M1 /IORQ /RD /WR /MREQ /INT /BUSRQ /WAIT
LCD Serial I2C
/reset
D0
0x80
U?A
74HC74
WR 2
74LS08
0x88
U?B
74HC74
U?C
74LS08
74LS126
U?B
U?C
74HC14
U?D
74HC14
D?
1N4148
R3 10K
S1
Reset
C3 100uF
reset
SCL
sda
R? 4K7
D? DIODE
+5V
C? 100nF
U?G
74HC14
U?C
74LS139
U?
628128_DIP32_SSOP32
AT29C512*-
U?
74LS139
/ROM_CE
/RAM_CS
J?
Jumper_ROM_RAM
/ROM_CE
/RAM_CE
/ROM_CE_msx
/RAM_CE_msx
Slot_cpu
/CS1 /CS1_2 /LIVRE /WAIT /M1 /IORQ /WR /RESET A9 A11 A7 A12 A14 A3 A5 D1 D3 D5 D7
/CS2 /RFSH /INT /BUS_DIR /MREQ /RD LIVRE A15 A10 A6 A8 A13 A0 A2 A4 D0 D2 D4 D6
/clock SW1 SW2 +12V −12V SOUNDIN
RS232 Pin Out
Connector:
D-Sub Male 9 pins
Pin Out
01 DCD Data Carrier Detect
02 RXD Receive Data
03 TXD Transmit Data
04 DTR Data Terminal Ready
05 GND Ground
Pin Out
Data Set Ready DSR 06
Request To Send RTS 07
Clear To Send CTS 08
Ring Indicator RI 09
Cable Tester
Copyright ©
www.cable-tester.com
U?A
74LS32
/ROM_CE_msx 3
2 A15
1 /SLOT_0
U?B 74LS32
/RAM_CS_msx 6
5 /MREQ
4 /SLOT_2
U?
74LS153
U?A
74LS139
U?B
74LS139
74LS153
1,15 A5|2 A14|14 INPUT OUTPUT
H X X X 7=0,9=0
L 0 0 D0,D1 7=D0,9=D1
L 0 1 D2,D3 7=D2,9=D3
L 1 0 D4,D5 7=D4,9=D5
L 1 1 D6,D7 7=D6,9=D7
/RESET 1
/CS8255_5
74LS00 U?A
74LS00 U?B
D0 D2 D4 D6
D1 D3 D5 D7
A14 A15
Ea Eb
I0a I1a I2a I3a
I0b I1b I2b I3b
Za Zb
S0 S1
/SLOT_0 /SLOT_1 /SLOT_2 /SLOT_3
/PAGE_0 /PAGE_1 /PAGE_2 /PAGE_3
/MREQ
74LS139
3 2 OUTPUT
0 0 /SLOT-0
0 1 /SLOT-1
1 0 /SLOT-2
1 1 /SLOT-3
U?
16550
U?
MAX232
7654 3210
Address: 0xB8 1011 1000
/0xB8 14
Y?
CPU Crystal
R? 1k5
C? 22pF
C? 47pF
/WR 18
/RD 21
reset 35
LOGIC
RS232
R2OUT R1OUT T2IN T1IN
R2IN R1IN T2OUT T1OUT
SIN SOUT
RXRDY TXRDY DDIS
BAUDOUT RCLK
C1− C1+ C2− C2+ VS− VS+
C? 1uF
J?
DB9_Male

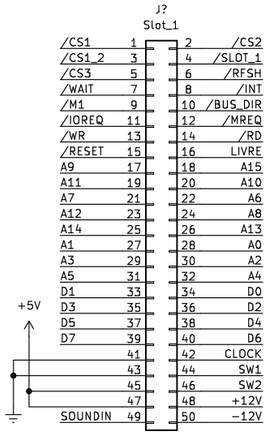

+5V
U?
628128_DIP32_SSOP32
VCC
GND
74LS32
U?B
U?A
74LS09
/MREQ
/IOREQ
/RD
/WR
/SLOT_2
/SLOT_1
U?
SST39SF010
74LS32
U?A
/SLOT_0
J?
Slot_0_2_ROM_RAM
/CS1
/CS1_2
/CS3
/WAIT
/M1
/IOREQ
/WR
/RESET
/CS2
/SLOT_0
/RFSH
/INT
/BUS_DIR
/MREQ
/RD
/SLOT_2
/SLOT_1
SOUNDIN
CLOCK
SW1
SW2
+12V
Qdo. slot 2 estiver em zero usa 64k inferior da ram
Qdo. slot 2 estiver em hum e slot 1 em zero usa 64k superior da ram
U?C
U?D
U?E
Selecionar eprom com
A15 = 0 e Slot0
Selecionar RAM com
MREQ e Slot2

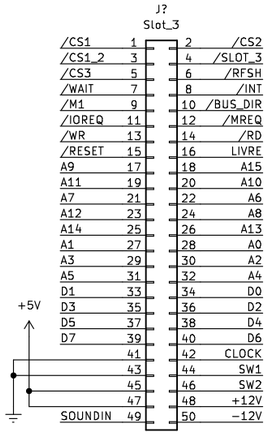

J?
Conn_02x40_Top_Bottom
/CS1 1
/CS1_2 2
/CS3 3
/WAIT 4
/M1 5
/IOREQ 6
/WR 7
/RESET 8
A9 9
A11 10
A7 11
A12 12
A14 13
A1 14
A3 15
A5 16
D1 17
D3 18
D5 19
D7 20
21
22
23
24
SOUNDIN 25
uartReset 26
0x80 27
0x88 28
PB0 29
PB2 30
PB4 31
PB6 32
PC0 33
PC2 34
PC4 35
PC6 36
RXA0 37
TXA0 38
/CTS0 39
/RTS0 40
41 /CS2
42
43 /RFSH
44 /INT
45 /BUS_DIR
46 /MREQ
47 /RD
48 SLOT_1
49 A15
50 A10
51 A6
52 A8
53 A13
54 A0
55 A2
56 A4
57 D0
58 D2
59 D4
60 D6
61 CLOCK
62 SW1
63 SW2
64 +12V
65 −12V
66 0xB0
67 0xB8
68 PB1
69 PB3
70 PB5
71 PB7
72 PC1
73 PC3
74 PC5
75 PC7
76 A16
77 A17
78 A18
79 RXA1
80 TXA1
+5V

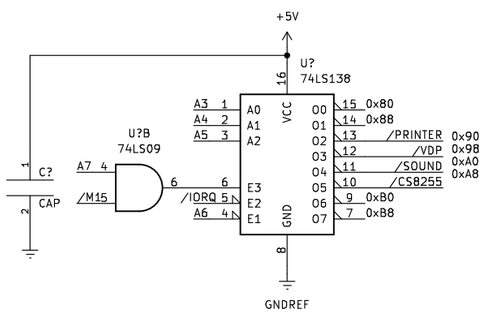
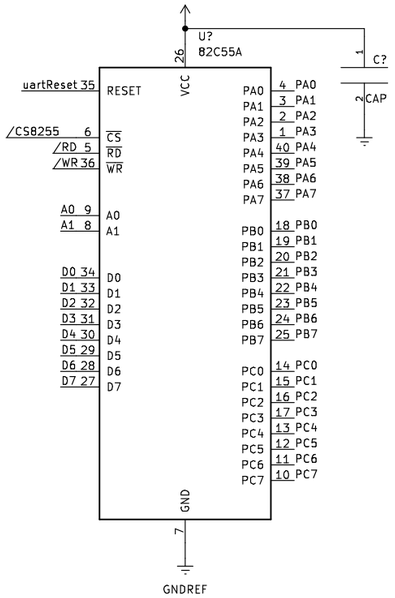
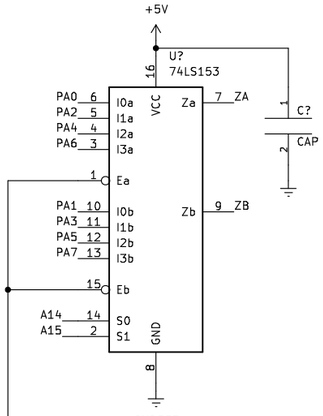
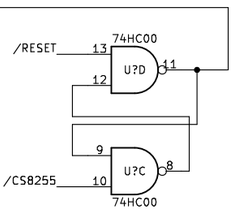
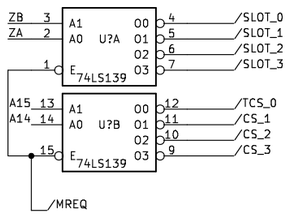
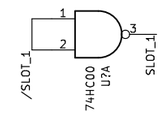
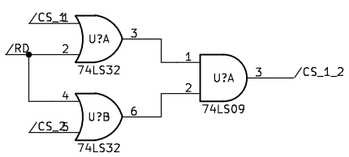
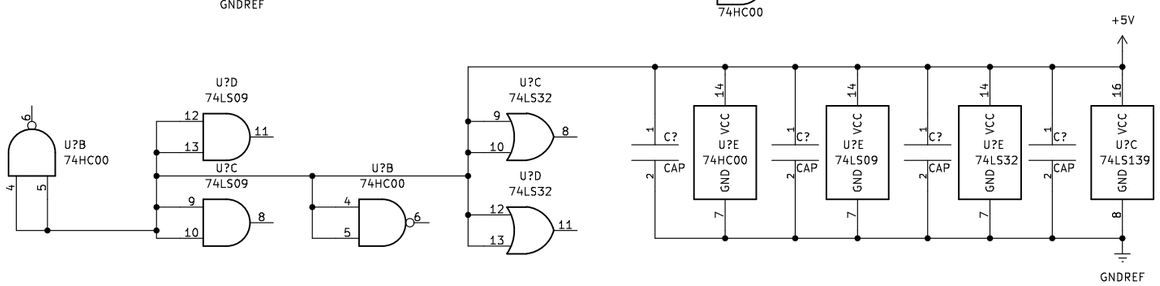











```
1 0 0 0  0 X X X -> 80
a
1 0 0 0  0 1 1 1 -> 87

1 0 0 0  1 X X X => 88
a
1 0 0 0  1 1 1 1 => 8F

1 0 0 1  0 X X X => 90
a
1 0 0 1  0 X X X => 97

1 0 0 1  1 X X X => 98
a
1 0 0 1  1 1 1 1 => 9F

1 0 1 0  0 X X X => A0
a
1 0 1 0  0 X X X => A7

1 0 1 0  1 X X X => A8
a
1 0 1 0  1 1 1 1 => AF

1 0 1 1  0 X X X => B0
a
1 0 1 1  0 X X X => B7

1 0 1 1  1 X X X => B8
a
1 0 1 1  1 1 1 1 => BF
```