

POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification For Approval

Customer : _____

Model Type : LCD Module

Sample Code : _____

Mass Production Code : PG12864LRS-JNN-B-SA

Edit : A

Customer Sign	Sales Sign	Approved By	Prepared By

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DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

1. SPECIFICATIONS

1.1 Features

- Full dot-matrix structure with 128 dots *64 dots
- 1/64 Duty, 1/9 bias
- STN LCD, positive
- Transflective LCD, gray
- 6 o'clock viewing angle
- 8 bits parallel data input
- LED Backlight

1.2 Mechanical Specifications

- Outline dimension : 75.0mm(L)*52.7mm(W)*8.4mm (H)
- Viewing area : 60.0mm *32.6mm
- Active area : 55.01mm *27.49mm
- Dot size : 0.39mm * 0.39mm
- Dot pitch : 0.43mm * 0.43mm

1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	VCC	-	0	6.7	V
LCD drive Supply voltage	VCC-VLC	-	0	8.15	V
Input voltage	VIN	-	0	VCC+0.3	V
Operating temperature	TOPR	-	0	+50	°C
Storage temperature	TSTG	-	-20	+70	°C
Humidity*1	HD	-	-	90	%RH

1.4 DC Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	VCC	-	4.5	5	5.5	V
“H” input voltage	VIH	-	0.7VCC	-	VCC	V
“L” input voltage	VIL	-	0	-	0.3VCC	V
Supply current	IDD	VCC=5V	-	1.32	0.33	mA
LCD driving voltage	VOP	VCC-VLC	8.14	-	9.20	V

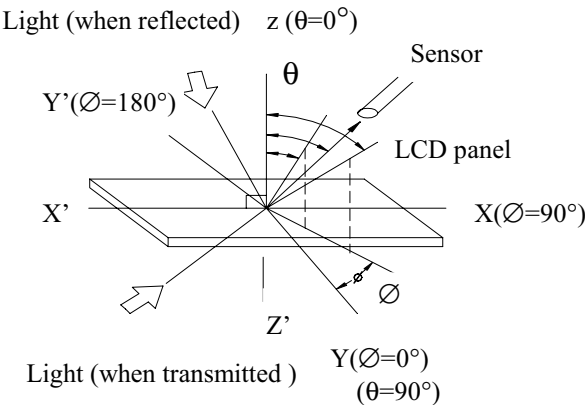


1.5 Optical Characteristics

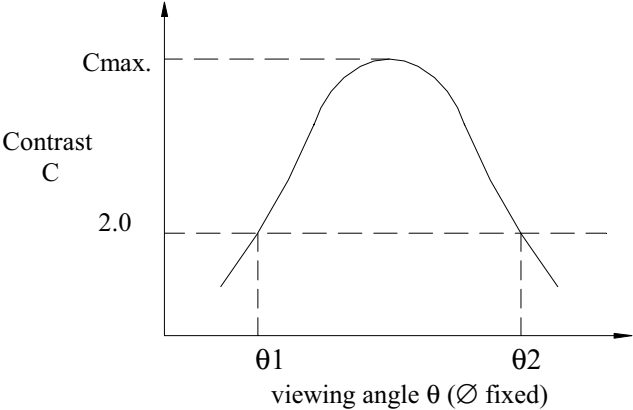
1/64 duty, 1/9 bias, Vopr=8.15V, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	θ	$C \geq 2.0, \varnothing = 0^\circ C$	30°	-	-	Notes 1 & 2
Contrast	C	$\theta = 5^\circ, \varnothing = 0^\circ$	2	3	-	Note 3
Response time(rise)	tr	$\theta = 5^\circ, \varnothing = 0^\circ$	-	130ms	200ms	Note 4
Response time(fall)	tf	$\theta = 5^\circ, \varnothing = 0^\circ$	-	300ms	500ms	Note 4

Note 1: Definition of angles θ and \varnothing



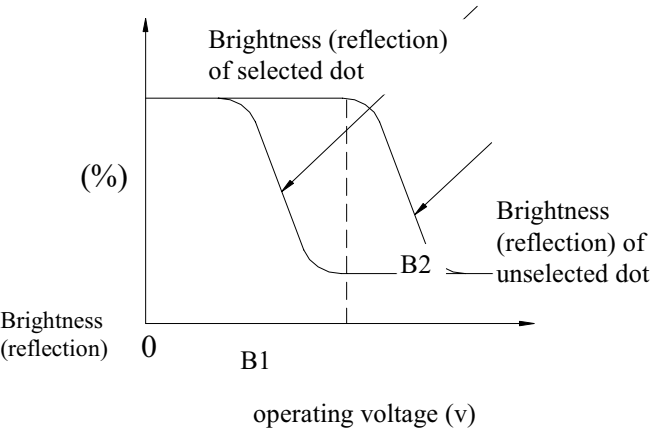
Note 2: Definition of viewing angles θ_1 and θ_2



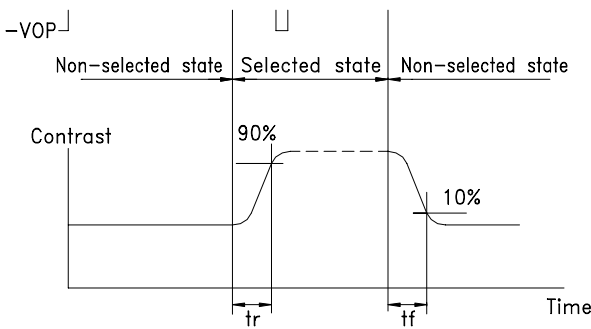
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same.

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm²

Vopr : Operating voltage
tr : Response time (rise)
fFRM : Frame frequency
tf : Response time(fall)



1.6 Backlight Characteristic

The LCD Module is backlight using a LED panel

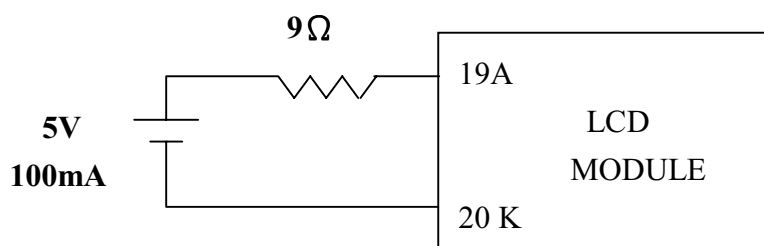
- Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward current	IF	TA=25°C	-	25	mA
Reverse voltage	VR	TA=25°C	-	8	V
Power dissipation	PO	TA=25°C	-	1.5	W
Operating Temperature	TOPR	-	-20	70	°C
Storage temperature	TSTG	-	-40	80	°C

- Electrical Ratings

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	VF	IF=100mA	-	4.1	4.4	V
Reverse current	IR	VR=8V	-	-	0.2	mA
Luminous intensity	IV	IF=100mA	-	20	-	cd/m ²
Wavelength	HUE	IF=100mA	571	-	576	nm
Color	Yellow Green					

- Light LED Backlight



2. MODULE STRUCTURE

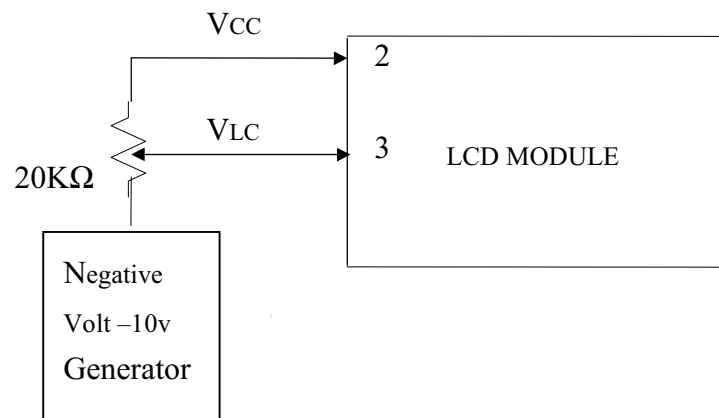
2.1 Counter Drawing

*See Appendix

2.2 Interface Pin Description

Pin No.	Symbol	Function
1	VDD	Power supply for logic (+5V)
2	VSS	Signal ground (GND)
3	VLC	Operating voltage for LCD (variable)
4 -7	DB0~ DB3	Four low order bi-directional three-state data bus lines. Use for data transfer between the MPU and the LCD module. These four are not used during 4-bit operation.
8 -11	DB4~ DB7	For high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. DB7 can be used as a busy flag.
12	/CS1	Chip enable for D2 (segment 1 to segment 64)
13	/CS2	Chip enable for D3 (segment 65 to segment 128)
14	$\overline{\text{RST}}$	Reset signal
15	R/ $\overline{\text{W}}$	R/W signal input is used to select the read/write mode High =Read mode, Low =Write mode
16	D/ $\overline{\text{I}}$	Register selection input High =Data register Low =Instruction register (for write) Busy flag address counter (for read)
17	E	Start enable signal to read or write the data
18	VSS	Ground
19	A	LED Backlight(+)
20	K	LED Backlight(-)

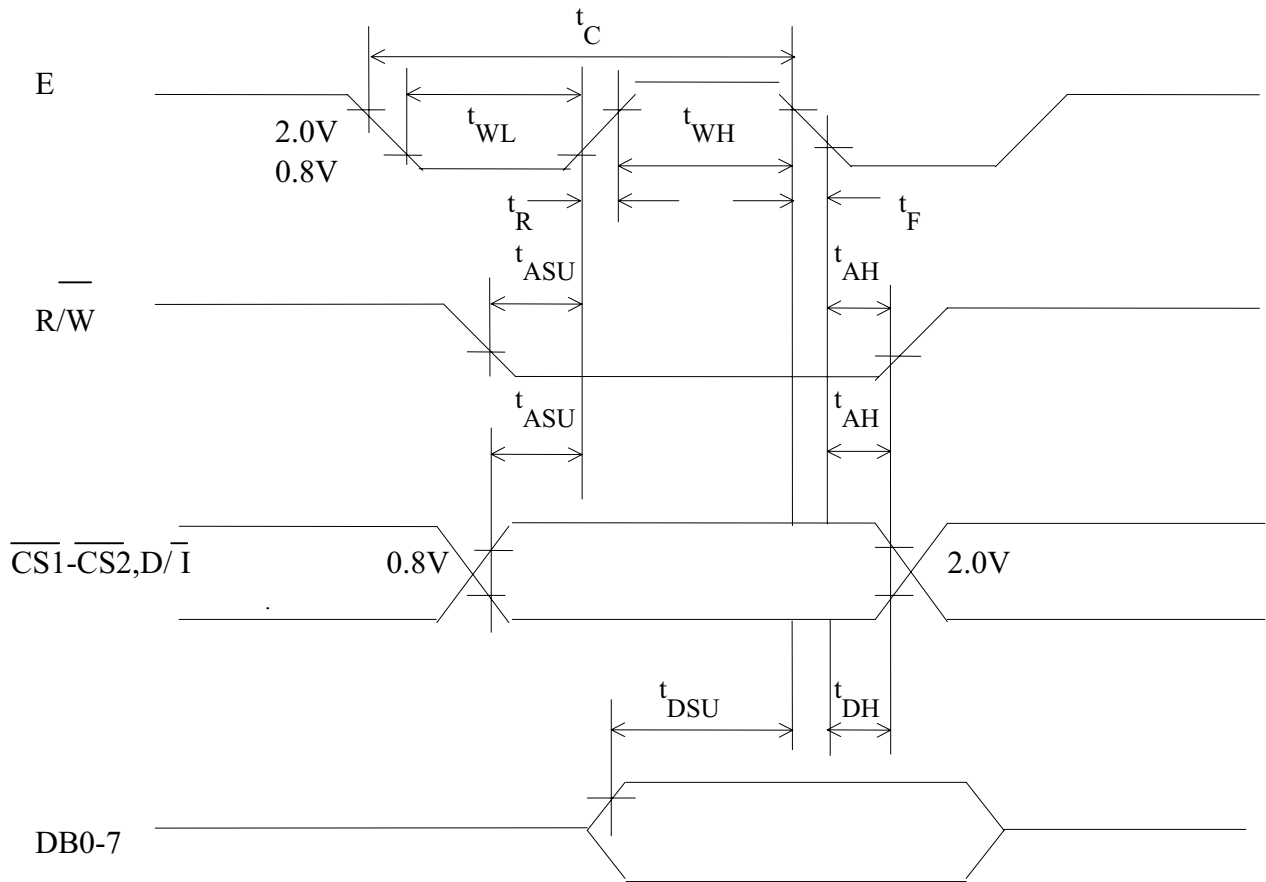
Contrast Adjust



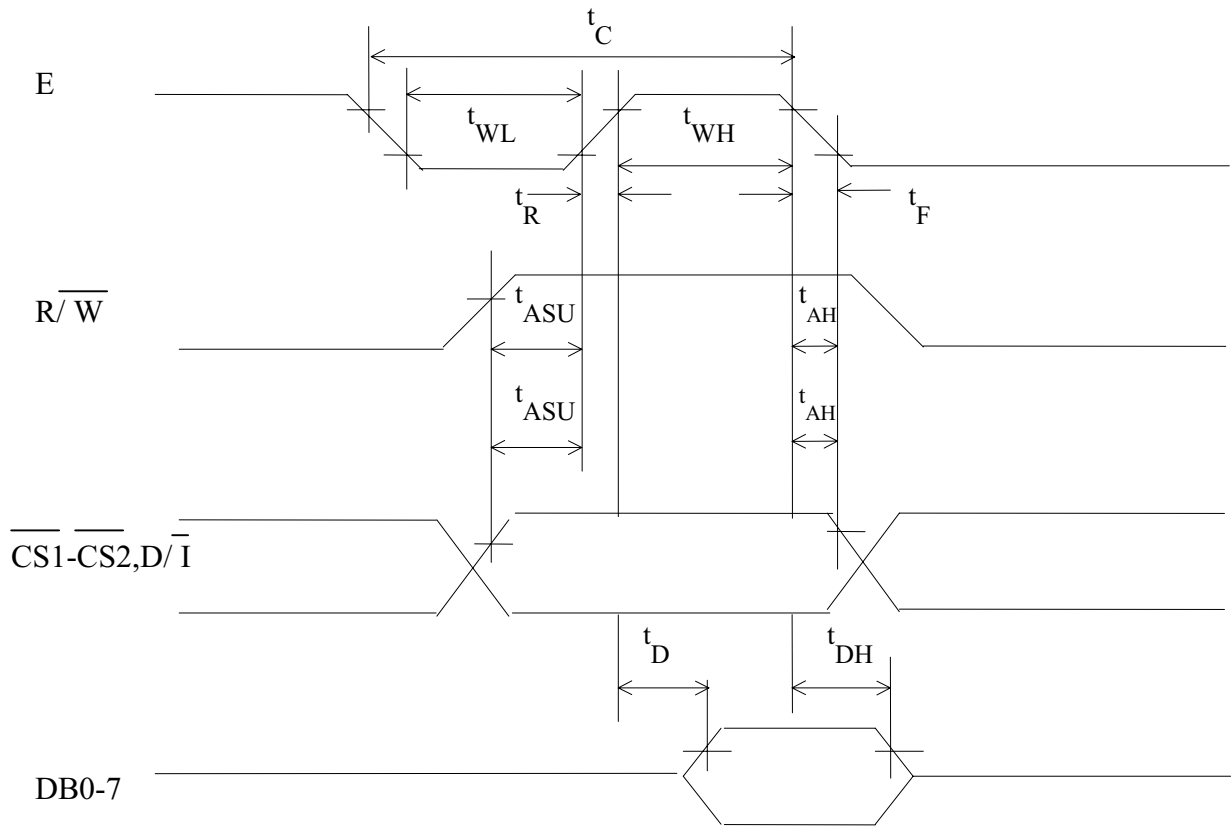
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2.3 Timing Characteristics



MPU Write timing



MPU Read timing

Characteristic	Symbol	Min.	Typ	Max	Unit
E Cycle	t_C	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	ns
E Low Level Width	t_{WL}	450	-	-	ns
E Rise Time	t_R	-	-	25	ns
E Fall Time	t_F	-	-	25	ns
Address Set-Up time	t_{ASU}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Set-Up Time	t_{SU}	200		-	ns
Data Delay Time	t_D	-	-	320	ns
Data Hold Time (Write)	t_{DHW}	10	-	-	ns
Data Hold Time (Read)	t_{DHR}	20	-	-	ns



2.4 Display command

Instructions	Code										Functions	
	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. (0:OFF,1:ON)	
Display start line	0	0	1	1	Display start line (0-63)					Specifies the RAM line displayed at the top of the screen.		
Set Page (x address)	0	0	1	0	1	1	1	Page (0-7)		Sets the page (X address) of RAM at the page (X address) register.		
Set Y address	0	0	0	1	Y address (0-63)					Sets the Y address in the Y address counter.		
Status read	1	0	Busy	0	ON/ OFF	Reset	0	0	0	0	Reads the status. Reset 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready	
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Detailed Explanation

Display On/Off

	R/W	D/I	DB7.....DB0							
Code	0	0	0	0	1	1	1	1	1	D
	MSB				LSB					

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.



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Display Start Line

	R/W	D/I	DB7.....DB0						
Code	0	0	1	1	A	A	A	A	A
	MSB				LSB				

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 1 shows examples of display (1/64 duty cycle) when the start line=0-3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed. See figure 1.

Set page (X address)

	R/W	D/I	DB7.....DB0						
Code	0	0	1	0	1	1	1	A	A
	MSB				LSB				

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 2.

Set Y Address

	R/W	D/I	DB7.....DB0						
Code	0	0	0	1	A	A	A	A	A
	MSB				LSB				

Y address AAAAAA (binary) of the display data RAM is set in the Y address Counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

Status Read

	R/W	D/I	DB7.....			DB0			
Code	1	0	Busy	0	ON/OFF	Reset	0	0	0	0
	MSB				LSB					

- Busy

When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is 1, so you should make sure that busy is 0 before writing the next instruction.



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- ON/OFF

Shows the liquid crystal display conditions: on condition or off condition.

When on/off is 1, the display is in off condition.

When on/off is 0, the display is in on condition.

- RESET

RESET=1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.

RESET=0 shows that initializing has finished and the system is in the usual operation condition.

Write Display Data

	R/W	D/I	DB7.....DB0						
Code	0	1	D	D	D	D	D	D	D
	MSB							LSB	

Write 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

Read Display Data

	R/W	D/I	DB7.....DB0						
Code	1	1	D	D	D	D	D	D	D
	MSB							LSB	

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in “Function of Each Block”.



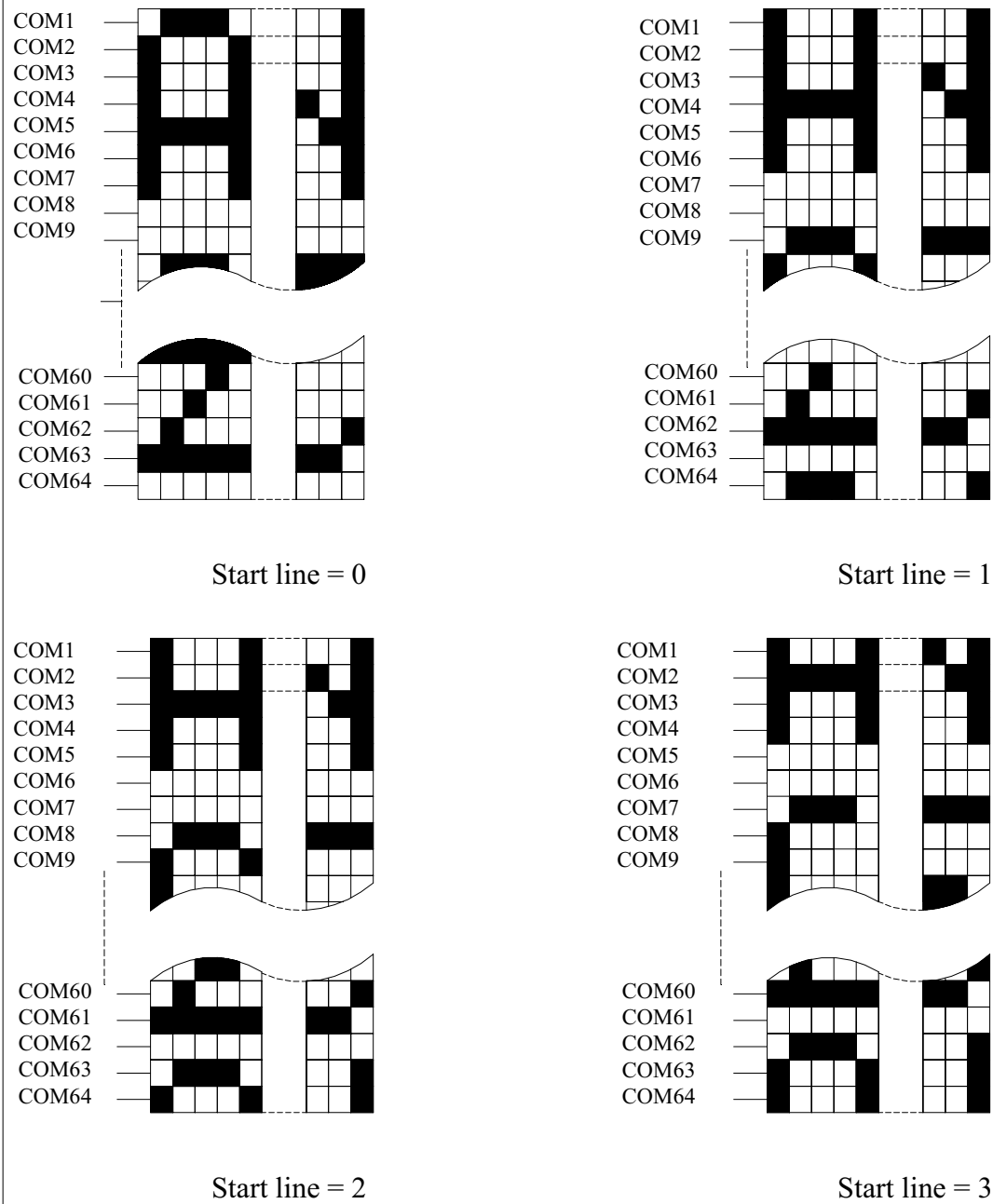


Figure 1 Relation between Start Line and Display



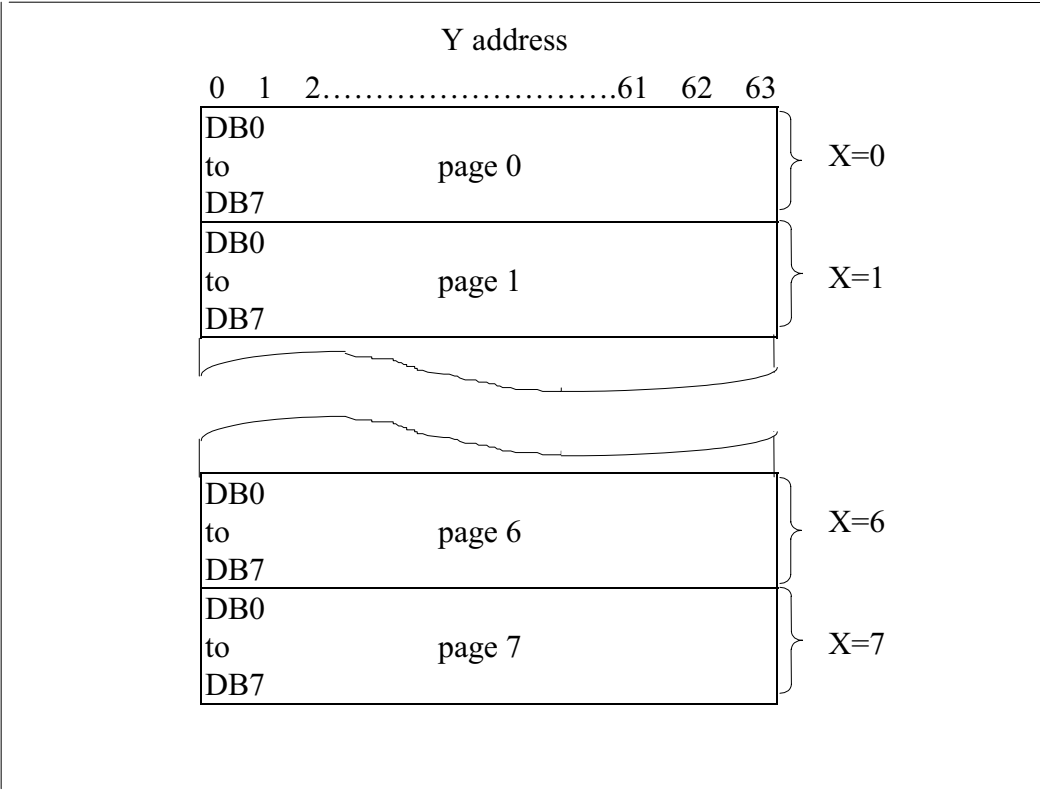
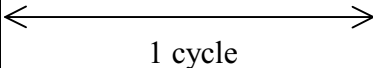


Figure 2 Address Configuration of Display Data RAM



3. RELIABILITY

3.1 Content of Reliability Test

Environmental Test			
NO	Test Item	Content of Test	Test Condition
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	70°C 100 hrs
2	Low temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 100 hrs
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 100 hrs
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 100 hrs
5	High temperature /Humidity Storage	Endurance test applying the high humidity storage for a long time.	70°C, 90%RH 50 hrs
6	High temperature /Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	70°C, 90%RH 50 hrs
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. -25°C → 25°C → 75°C 30min ← 5min ← 30min 	-25°C / 75°C 10 cycle



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