

## NTE6821 Integrated Circuit Peripheral Interface Adapter (PIA), NMOS, 1MHz

### **Description:**

The NTE6821 is a peripheral interface adapter (PIA) in a 40-Lead DIP type package capable of interfacing the Microprocessing Unit (MPU) to peripherals through two 8-Bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

### **Features:**

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmed Control Registers
- Two Programmed Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL Compatible
- Static Operation

### **Absolute Maximum Ratings:** (Note 1)

Supply Voltage, $V_{CC}$ .....	-0.3 to +7V
Input Voltage, $V_{in}$ .....	-0.3 to +7V
Operating Temperature Range, $T_A$ .....	0° to +70°C
Storage Temperature Range, $T_{stg}$ .....	-55° to +150°C
Thermal Resistance, Junction to Ambient, $R_{\theta JA}$ .....	82.5°C/W

Note 1. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance.

**Electrical Characteristics:** ( $V_{CC} = 5V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0^\circ$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Bus Control Inputs</b> (R/W, Enable, Reset, RS0, RS1, CS0, CS1, CS2)						
Input High Voltage	$V_{IH}$		$V_{SS} + 2.0$	–	$V_{CC}$	V
Input Low Voltage	$V_{IL}$		$V_{SS} - 0.3$	–	$V_{SS} + 0.8$	V
Input Leakage Current	$I_{in}$	$V_{in} = 0$ to $5.25V$	–	1.0	2.5	$\mu\text{A}$
Capacitance	$C_{in}$	$V_{in} = 0$ , $T_A = +25^\circ\text{C}$ , $f = 1\text{MHz}$	–	–	7.5	pF
<b>Interrupt Outputs</b> (IRQA, IRQB)						
Output Low Voltage	$V_{OL}$	$I_{Load} = 3.2\text{mA}$	–	–	$V_{SS} + 0.4$	V
Output Leakage Current (Off State)	$I_{LOH}$	$V_{OH} = 2.4V$	–	1.0	10	$\mu\text{A}$
Capacitance	$C_{out}$	$V_{in} = 0$ , $T_A = +25^\circ\text{C}$ , $f = 1\text{MHz}$	–	–	5.0	pF
<b>Data Bus</b> (D0 – D7)						
Input High Voltage	$V_{IH}$		$V_{SS} + 2.0$	–	$V_{CC}$	V
Input Low Voltage	$V_{IL}$		$V_{SS} - 0.3$	–	$V_{SS} + 0.8$	V
Three-State (Off State) Input Current	$I_{TSI}$	$V_{in} = 0.4$ to $2.4V$	–	2.0	10	$\mu\text{A}$
Output High Voltage	$V_{OH}$	$I_{Load} = -205\mu\text{A}$	$V_{SS} + 2.4$	–	–	V
Output Low Voltage	$V_{OL}$	$I_{Load} = 1.6\text{mA}$	–	–	$V_{SS} + 0.4$	V
Capacitance	$C_{in}$	$V_{in} = 0$ , $T_A = +25^\circ\text{C}$ , $f = 1\text{MHz}$	–	–	12.5	pF
<b>Peripheral Bus</b> (PA0 – PA7, PB0 – PB7, CA1, CA2, CB1, CB2)						
Input Leakage Current R/W, Reset, RS0, RS1, CS0, CS1, CS2, CA1, CB1, Enable	$I_{in}$	$V_{in} = 0$ to $5.25V$	–	1.0	2.5	$\mu\text{A}$
Three-State (Off State) Input Current PB0 – PB7, CB2	$I_{TSI}$	$V_{in} = 0.4$ to $2.4V$	–	2.0	10	$\mu\text{A}$
Input High Current PA0 – PA7, CA2	$I_{IH}$	$V_{IH} = 2.4V$	–200	–400	–	$\mu\text{A}$
Darlington Drive Current PB0 – PB7, CB2	$I_{OH}$	$V_O = 1.5V$	–1.0	–	–10	mA
Input Low Current PA0 – PA7, CA2	$I_{IL}$	$V_{IL} = 0.4V$	–	–1.3	–2.4	mA
Output High Voltage PA0 – PA7, PB0 – PB7, CA2, CB2	$V_{OH}$	$I_{Load} = -200\mu\text{A}$	$V_{SS} + 2.4$	–	–	V
PA0 – PA7, CA2		$I_{Load} = 10\mu\text{A}$	$V_{CC} - 1.0$	–	–	V
Output Low Voltage	$V_{OL}$	$I_{Load} = 3.2\text{mA}$	–	–	$V_{SS} + 0.4$	V
Capacitance	$C_{in}$	$V_{in} = 0$ , $T_A = +25^\circ\text{C}$ , $f = 1\text{MHz}$	–	–	10	pF
<b>Power Requirements</b>						
Power Dissipation	$P_D$		–	–	550	mW

**Bus Timing Characteristics:** ( $V_{CC} = 5V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0^\circ$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable Cycle Time	$t_{cycE}$		1000	–	–	ns
Enable Pulse Width, High	$PW_{EH}$		450	–	–	ns
Enable Pulse Width, Low	$PW_{EL}$		430	–	–	ns
Enable Pulse Rise and Fall Times	$t_{Er}$ , $t_{Ef}$		–	–	25	ns

**Bus Timing Characteristics (Cont'd):** ( $V_{CC} = 5V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0^\circ$  to  $+70^\circ\text{C}$  unless otherwise specified)

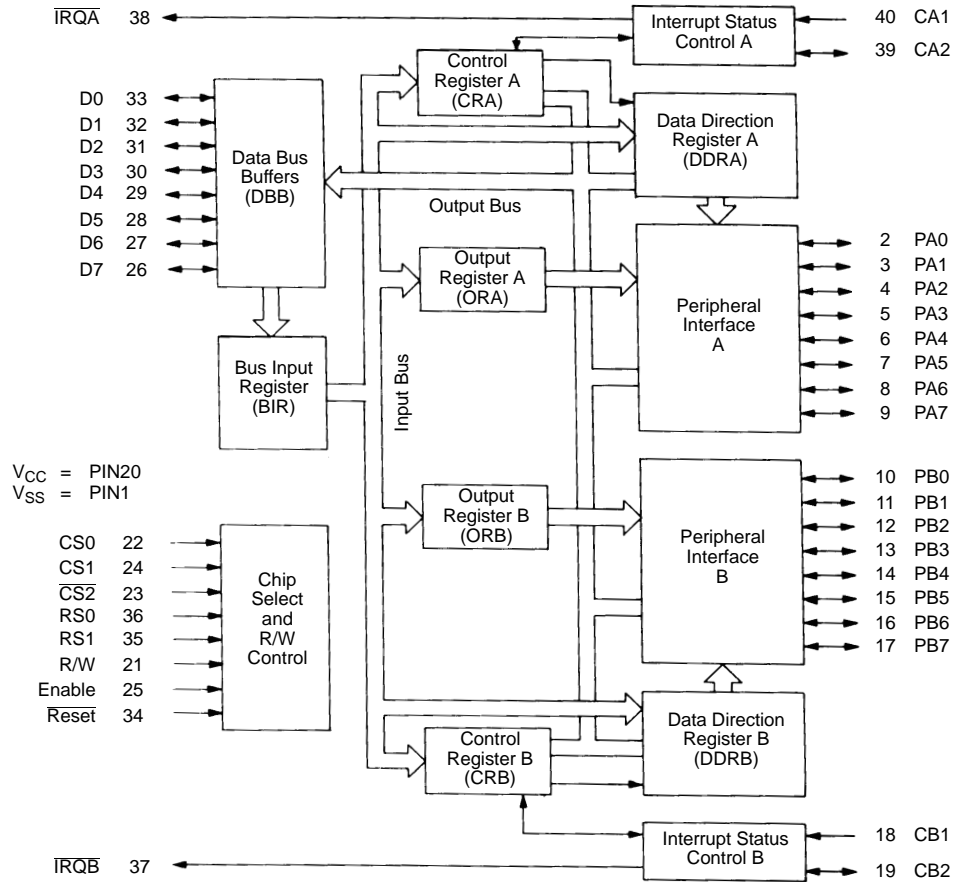
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Setup Time, Address and R/W Valid to Enable Positive Transition	$t_{AS}$		160	–	–	ns
Address Hold Time	$t_{AH}$		10	–	–	ns
Data Delay Time, Read	$t_{DDR}$		–	–	320	ns
Data Hold Time, Read	$t_{DHR}$		10	–	–	ns
Data Setup Time, Write	$t_{DSW}$		195	–	–	ns
data Hold Time, Write	$t_{DHW}$		10	–	–	ns

**Peripheral Timing Characteristics:** ( $V_{CC} = 5V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0^\circ$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min	Max	Unit
Peripheral Data Setup Time	$t_{PDSU}$	200	–	ns
Peripheral Data Hold Time	$t_{PDH}$	0	–	ns
Delay Time, Enable negative transition to CA2 negative transition	$t_{CA2}$	–	1.0	$\mu\text{s}$
Delay Time, Enable negative transition to CA2 positive transition	$t_{RS1}$	–	1.0	$\mu\text{s}$
Rise and fall Times for CA1 and CA2 input signals	$t_r, t_f$	–	1.0	$\mu\text{s}$
Delay Time from CA1 active transition to CA2 positive transition	$t_{RS2}$	–	2.0	$\mu\text{s}$
Delay Time, Enable negative transition to Peripheral Data Valid	$t_{PDW}$	–	1.0	$\mu\text{s}$
Delay Time, Enable negative transition to Peripheral CMOS Data Valid PA0 – PA7, CA2	$t_{CMOS}$	–	2.0	$\mu\text{s}$
Delay Time, Enable positive transition to CB2 negative transition	$t_{CB2}$	–	1.0	$\mu\text{s}$
Delay Time, Peripheral Data Valid to CB2 negative transition	$t_{DC}$	20	–	ns
Delay Time, Enable positive transition to CB2 postivie transition	$t_{RS1}$	–	1.0	$\mu\text{s}$
Peripheral Control Output Pulse Width, CA2/CB2	$PW_{CT}$	550	–	ns
Rise and Fall Time for CB1 and CB2 input signals	$t_r, t_f$	–	1.0	$\mu\text{s}$
Delay Time, CB1 active transition to CB2 positive transition	$t_{RS2}$	–	2.0	$\mu\text{s}$
Interrupt Release Time, $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$	$t_{IR}$	–	2.0	$\mu\text{s}$
Interrupt Response Time	$t_{RS3}$	–	1.0	$\mu\text{s}$
Interrupt Input Pulse Width	$PW_I$	500	–	ns
Reset Low Time (Note 2)	$t_{RL}$	1.0	–	$\mu\text{s}$

Note 2. The Reset line must be high a minimum of  $1.0\mu\text{s}$  before addressing the PIA.

## Expanded Block Diagram



## Pin Connection Diagram

