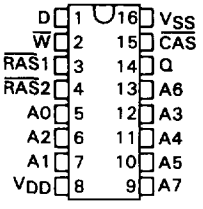
APRIL 1985—REVISED NOVEMBER 1985

- 2 X 65,536 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- Operating Free-Air Temperature . . . 0°C to 70°C
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 193 mW (Typ)
  - Standby . . . 35 mW (Typ)
- Max Access/Min Cycle Times:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS41128B-15	150 ns	85 ns	260 ns	315 ns

- SMOS (Scaled-MOS) N-Channel Technology

16-PIN PLASTIC
DUAL-IN-LINE STACKED PACKAGES †
(TOP VIEW)



† RAS1 (pin 3) selects the lower DRAM, and pin 3 on the upper DRAM is a no connect. RAS2 (pin 4) selects the upper DRAM, and pin 4 on the lower DRAM is a no connect.

PIN NOMENCLATURE	
A0-A7	Address Inputs
CAS	Column-Address Strobe
D	Data In
Q	Data Out
RAS1, RAS2	Row-Address Strobes
V_{DD}	5-V Supply
V_{SS}	Ground
W	Write Enable

4

Dynamic RAMs

description

The TMS41128B consists of two high-speed, 65,536-bit, dynamic random-access memories that are separately packaged. These DRAMs are electrically similar to TMS4164s; however, the pin out is different. The two packages are permanently connected, pin for pin, one on top of the other. The result is a 16-pin memory device organized as 131,072 words of one bit each with essentially the same characteristics of the TMS4164 NMOS dynamic RAM.

A logic low on the RAS1 input selects the lower DRAM; a logic low on the RAS2 input selects the upper DRAM.

The TMS41128B-15 features a RAS access time of 150 ns. Power dissipation is 193 mW typical operating, 35 mW typical standby.

Refresh period is extended to 4 ms, and during this period each of the 256 rows must be strobed with RAS1 and RAS2 in order to retain data. CAS can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clock, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS41128B is offered in 16-pin plastic dual-in-line stacked packages and is guaranteed for operation from 0°C to 70°C. This package is designed for insertion in mounting-hole rows on 300-mil (7,62-mm) centers.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}1$ or $\overline{RAS}2$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}1$, $\overline{RAS}2$, and $\overline{CAS}$. $\overline{RAS}1$ and $\overline{RAS}2$ are similar to a chip enable in that they activate the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers. When $\overline{CAS}$ is applied to the device, only one of the $\overline{RAS}$ signals (either $\overline{RAS}1$ or $\overline{RAS}2$) must be applied to select either the lower DRAM or the upper DRAM. When a $\overline{RAS}$-only refresh is performed ($\overline{CAS}$ logic high), both $\overline{RAS}1$ and $\overline{RAS}2$ may be applied simultaneously.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every 4 ms on both DRAMs to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, The $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with both $\overline{RAS}1$ and $\overline{RAS}2$ causes all bits in each row to be refreshed. $\overline{CAS}$ must remain high (inactive) for this refresh sequence.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power-up

After power up, $\overline{RAS}1$ and $\overline{RAS}2$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

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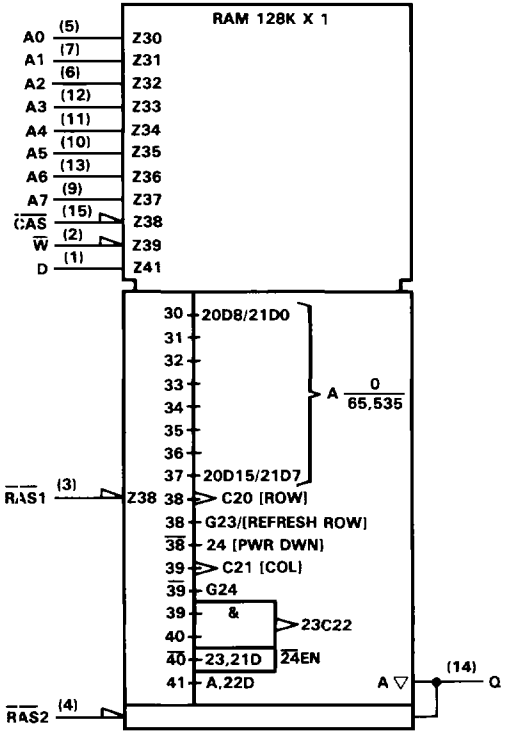
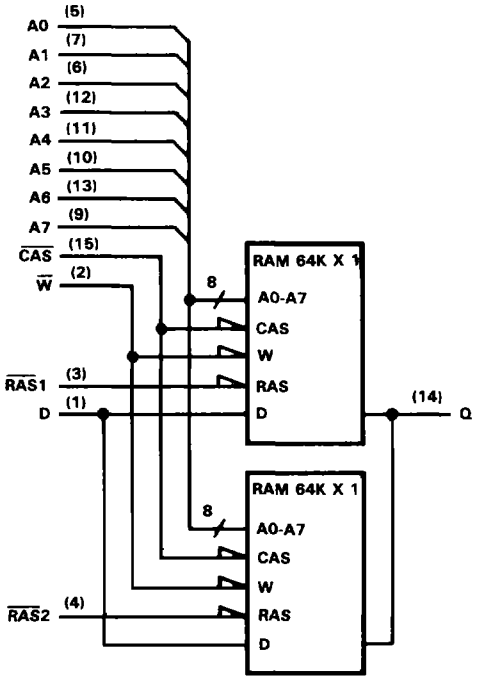
logic symbol†



functional block diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and EC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies"* in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 3 and 4)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±20	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±20	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		38.5	65	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		7	10	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open			90	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open			90	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ V_{IL} > −0.6 V.

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	8	14	pF
$C_{i(D)}$	Input capacitance, data input	8	14	pF
$C_{i(RC)}$	Inpuut capacitance strobe inputs	16	20	pF
$C_{i(W)}$	Input capacitance, write-enable input	16	20	pF
C_o	Output capacitance	10	16	pF

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	MIN	MAX	UNIT
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	MIN	MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	315		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	60		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	85	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	55		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	55		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	110		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	20		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	10		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	85		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	75		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	150		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write cycles also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

PARAMETER MEASUREMENT INFORMATION

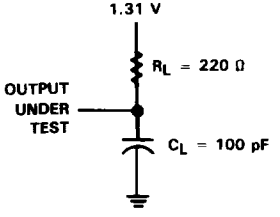
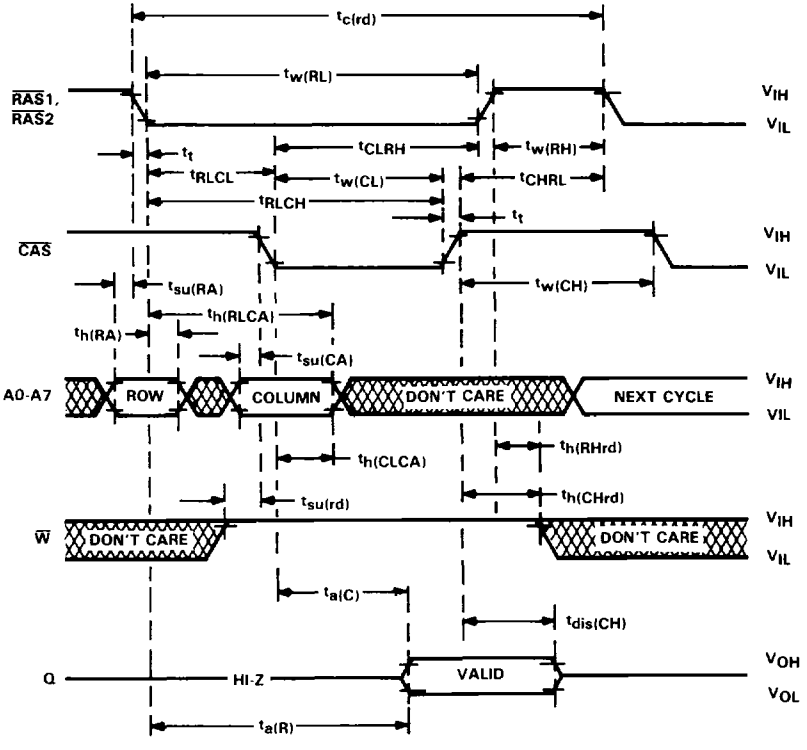
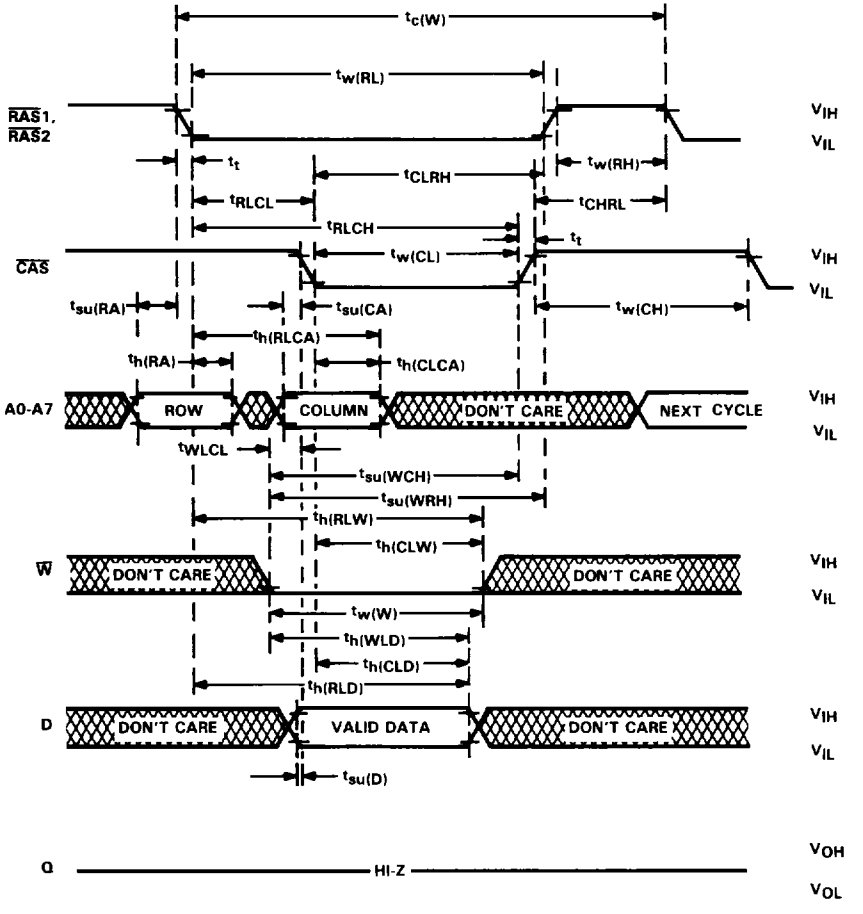


FIGURE 1. LOAD CIRCUIT

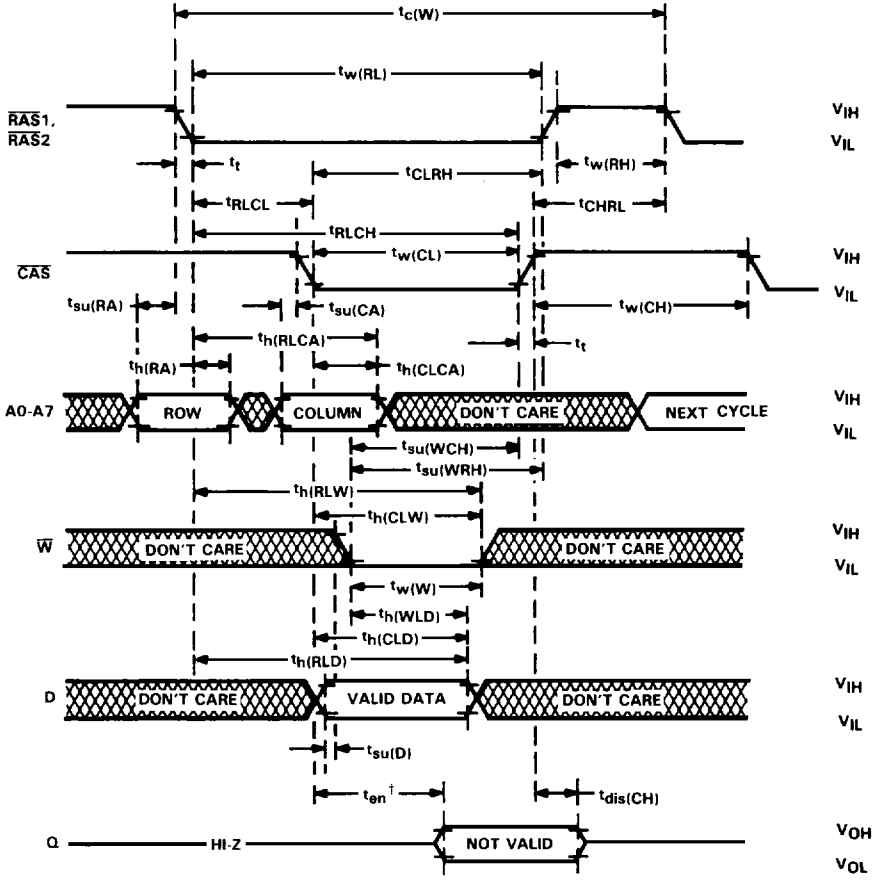
read cycle timing



early write cycle timing

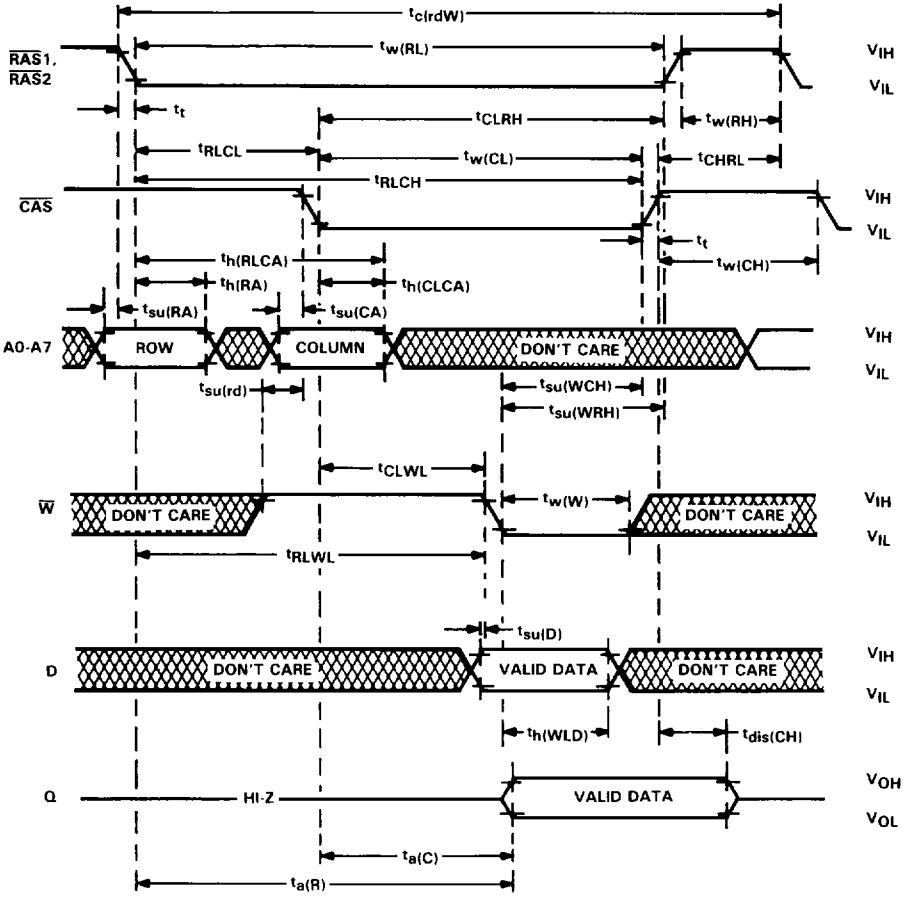


write cycle timing

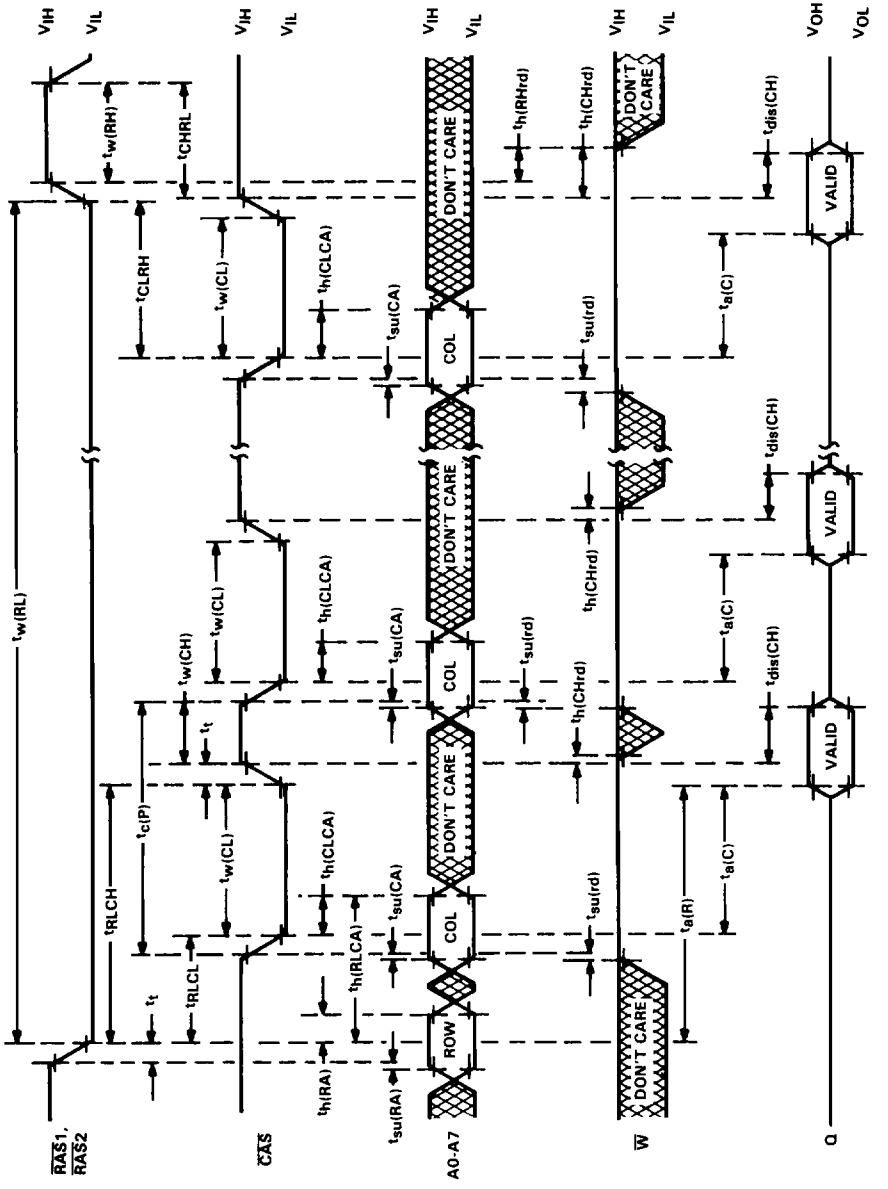


† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-modify-write cycle timing

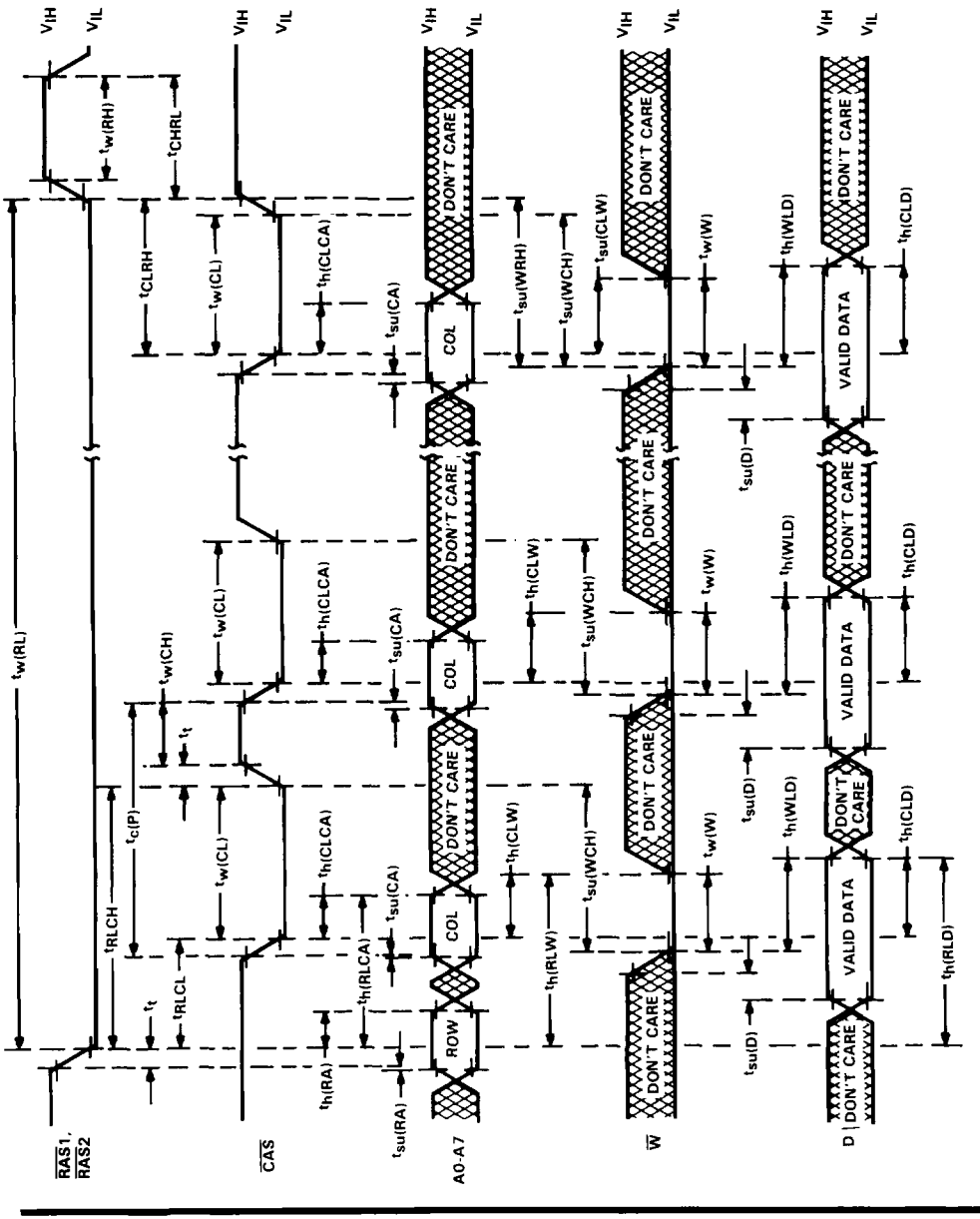


page-mode read cycle timing



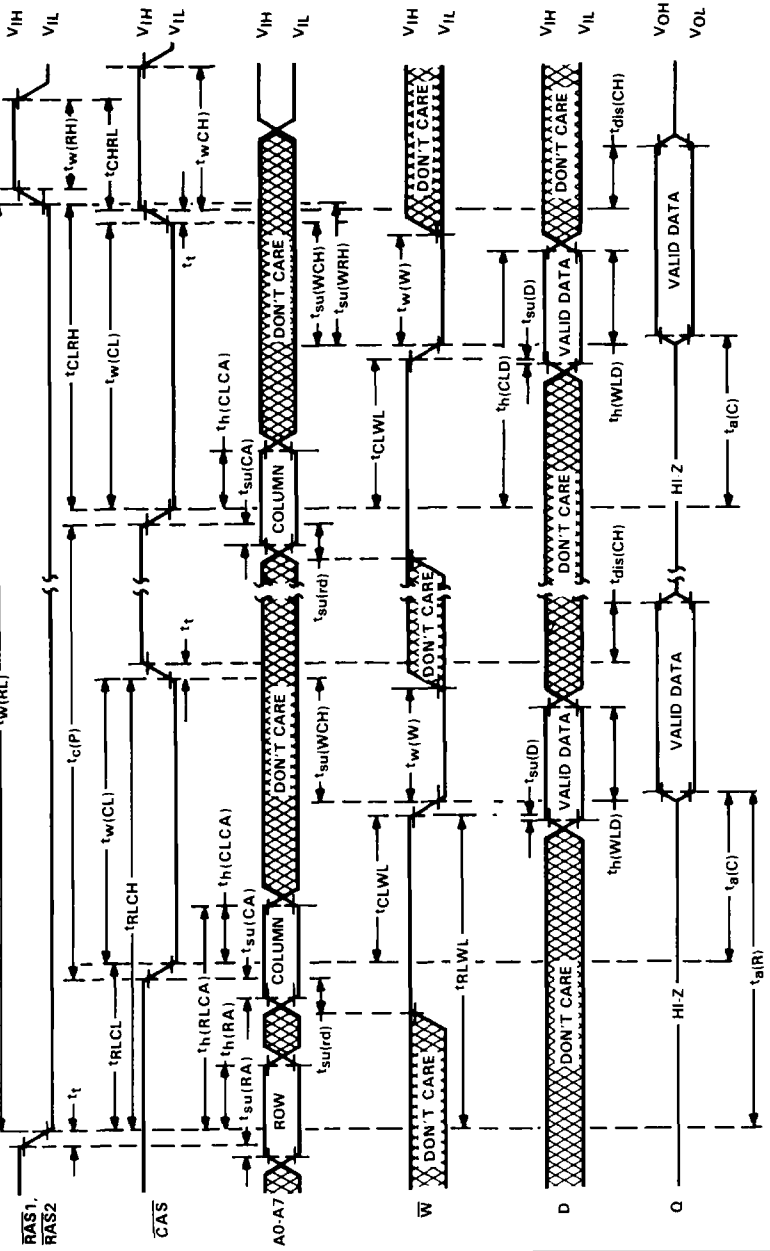
NOTE 6: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTE 7: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTE 8: A read or a write cycle can be intermixed with read modify write cycles as long as the read and write timing specifications are not violated.

$\overline{RAS}$-only refresh timing