TPS65381-Q1 Multi-Rail Power Supply for Microcontrollers in Safety Applications

1 Device Overview

1.1 Features

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- **Multi-Rail Power Supply Supporting Among Others**
  - Texas Instruments TMS570LS Series 16-Bit or 32-Bit RISC Flash Microcontroller
- **Supply Rails**
  - Input voltage range:
    - 5.8 V to 36 V (CAN, I/O, MCU Core, and Sensor-Supply Regulators Functional)
    - 4.5 V to 5.8 V (3.3-V I/O and MCU Core-Voltage Functional)
  - 6-V Asynchronous Switch-Mode Preregulator With Internal FET, 1.3-A Current-Limit, and Temperature Protection
  - 5-V (CAN) Supply Voltage, Linear Regulator With Internal FET, 350-mA Current-Limit, and Temperature Protection
  - 3.3-V or 5-V MCU I/O Voltage, Linear Regulator With Internal FET, 350-mA Current-Limit, and Temperature Protection
  - 0.8-V to 3.3-V Adjustable MCU Core Voltage, Linear Regulator Controller With External FET
  - Sensor Supply: Linear Tracking Regulator With Tracking Input, 100-mA Current-Limit, Temperature Protection, and Protection Against Short to Battery and Short to Ground
  - Charge Pump: Typ. 12 V Above Battery Voltage
- **Power Supply and System Monitoring**
  - Independent Undervoltage and Overvoltage Monitoring on All Regulator Outputs, Battery Voltage, and Internal Supplies
  - Independent Bandgap Reference for Voltage Monitoring
  - Independent Voltage References for Regulator References and Voltage Monitoring. Voltage-Monitoring Circuitry With Separate Battery Voltage Input Pin
  - Self-Check on all Voltage Monitoring (During Power-Up and After Power-Up Initiated by External MCU)
  - Junction Temperature Sensing With Shutdown Thresholds
- **Microcontroller Interface**
  - Open-Close Window or Question-Answer Watchdog Function
  - MCU Error-Signal Monitor (Supports TI TMS570 MCU Mode or Other MCUs with PWM-Like Signaling)
  - DIAGNOSTIC State for Performing Device Self-Tests, Diagnostics, and External Interconnect Checks
  - Safe-State for Device and System Protection on Error Event Detection
  - Clock Monitor for Internal Oscillators
  - Self-Tests for Analog- and Digital-Critical Circuits Executed With Every Device Power Up or Activated by External MCU in DIAGNOSTIC State
  - CRC on Non-Volatile Memory, Device, and System Configuration Registers
  - Reset circuit for MCU
  - Diagnostic Output Pin Allowing MCU to Observe Device Internal Analog and Digital Signals, Selectable Through Multiplexer
- **SPI**
  - Configuring IC Registers
  - Watchdog Question-Answering
  - Diagnostic Readout
  - Compliant With 3.3-V and 5-V Logic Levels
- **Enable-Drive Output for Disabling Safing-Path or External Power-Stages on Any Detected System-Failure**
- **Wake-Up Through IGNITION Pin or CAN WAKEUP Pin**
- **Package: 32-Pin HTSSOP PowerPAD™ IC Package**

1.2 Applications

- **Safety Automotive Applications**
  - Power Steering (EPS, or Electrical Power Steering, and EHPS, or Electro Hydraulic Power Steering)
  - Braking (ABS, ESC, and Electric Park Break)
  - Advanced Driver Assistance Systems (ADAS)
  - Suspension
- **Industrial Safety Applications**
  - Safety PLC Controllers
  - Safety I/O Control Modules
  - Test and Measurement
  - Railway and Subway Signal Control And Safety Modules
  - Elevator and Escalator Safety Control
  - Wind Turbine Control

1.3 Description

The TPS65381-Q1 device is a multi-rail power supply designed to supply microcontrollers (MCUs) in safety applications, such as those found in automotive and industrial applications. The device supports Texas Instruments' TMS570LS series 16- bit or 32-bit RISC flash MCU and other MCUs with dual-core lockstep (LS) or loosely-coupled architectures (LC).

The TPS65381-Q1 device integrates multiple supply rails to power the MCU, CAN, or FlexRay, and an external sensor. An asynchronous-buck switch-mode power-supply converter with an internal FET converts the input battery voltage to a 6-V preregulator output. This 6-V preregulator supplies the other regulators. Furthermore, the device supports wake-up from IGNITION or wake-up from the CAN transceiver.

A fixed 5-V linear regulator with an internal FET is integrated to be used as, for example, a CAN supply. A second linear regulator, also with an internal FET, regulates the 6 V to a selectable 5-V or 3.3-V MCU I/O voltage.

The TPS65381-Q1 device comprises a linear regulator controller with an external FET and resistor divider that regulates the 6 V to an externally adjustable core voltage of between 0.8 V and 3.3 V.

The device comprises a sensor supply with short-to-ground and short-to-battery protection. Therefore this supply can power a sensor outside the electronic-control unit (ECU).

The device has an integrated charge pump to provide overdrive voltage for the internal regulators. Reverse-battery protection is obtained by using the charge-pump output to control an external NMOS transistor. This solution allows for a lower minimum-battery-voltage operation compared to a traditional reverse-battery blocking diode.

The device monitors undervoltage and overvoltage on all regulator outputs, battery voltage, and internal supply rails. A second bandgap reference, independent from the main bandgap reference, is used for the undervoltage and overvoltage monitoring, to avoid any drifts in the main bandgap reference from being undetected. In addition, regulator current-limits and temperature protections are implemented.

The TPS65381-Q1 safety functions feature a question-answer watchdog, MCU error-signal monitor, clock monitoring on internal oscillators, self-check on the clock monitor, CRC on non-volatile memory, a diagnostic output pin allowing the MCU to observe the internal analog and digital signals of the device, a reset circuit for the MCU, and an enable output to disable the safing-path or external power-stages on any detected system-failure. A built-in self-test (BIST) monitors the device functionality at start-up. A dedicated DIAGNOSTIC state allows the MCU to check TPS65381-Q1 safety functions.

The TPS65381-Q1 device is offered in a 32-pin HTSSOP PowerPAD package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65381-Q1	HTSSOP (32)	11.00 mm × 6.20 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

1.4 Typical Application Diagram

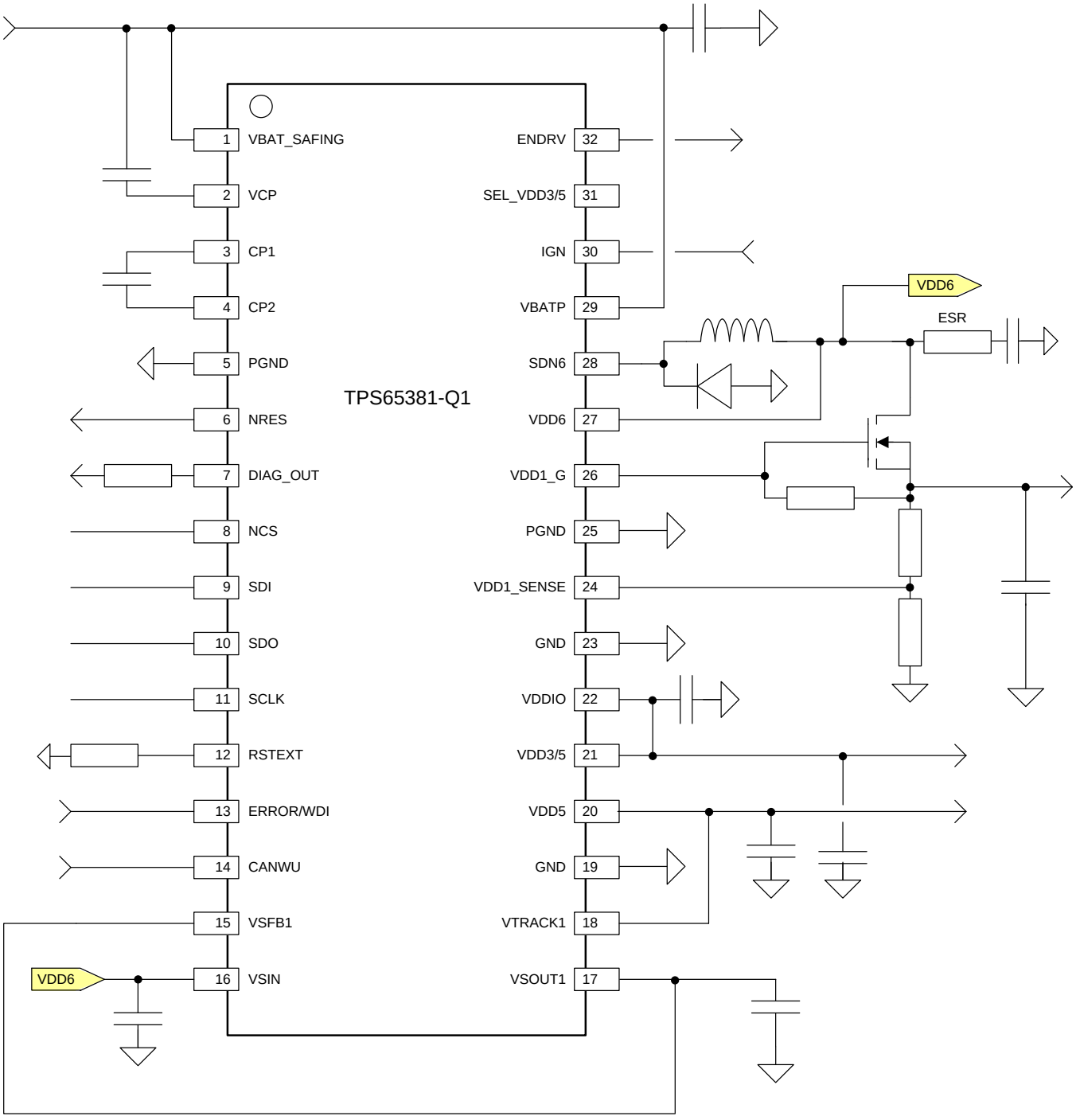

Figure 1-1. Typical Application Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2015) to Revision E — **Page**

- Changed the maximum UV value for VDD1 from 0.97 to 0.98 in the *Voltage Monitoring Overview* table. Also updated the VDD output voltage information 35
- Changed the MAX value for VDD1_UVN from 0.97 to 0.98 in the *Internal Error Signals* table. Also updated the *Device State When Flag Is Set* cells for VDD1_UVN 36
- Added clarification on the watchdog fail counter and reset event requirements in the *Watchdog Enable Function* image 46
- Added clarification on the watchdog fail counter and reset event requirements in the *Device Controller State Diagram* 65

Changes from Revision C (March 2015) to Revision D — **Page**

- Changed MIN value of $VDD1_{SENSE}$(4.2) from -2% to -1% in the *Electrical Characteristics* table 20
- Changed MAX value of VDD1 undervoltage level (6.16) from 0.97 to 0.98 in the *Electrical Characteristics* table 22
- Changed description of un-used VDD1 regulator in the *VDD1 Linear Regulator* section 29
- Added clarification in the nMASK_VDD1_UV_OV description in the *DEV_CFG1 Register* table 71

Changes from Revision B (July 2014) to Revision C — **Page**

- Changed Applications listed in the *Applications* Section 2
- Deleted the nominal storage temperature value of 27°C 17
- Changed the *Handling Ratings* to *ESD Ratings* and moved T_{stg} into the *Absolute Maximum Ratings* table 17
- Added clarification notes on output capacitance and ESR for VDD6 in the *ELECTRICAL CHARACTERISTICS* table 19
- Added the *Typical Characteristics* section 26
- Added clarification of ESR needed on VDD6 output capacitance in the *Functional Block Diagram* 27
- Added clarification on effective output capacitance and ESR in the*VDD6 Buck Switch-Mode Power Supply* section 28
- Added clarification on the IGN and CANWU pins with respect to transients *Wake-Up* section 31
- Added start-up delay to VCP in the *Power-Up and Power-Down Behavior* 32

- Added SPI Interface Note on use of the SPI while DIAG_OUT MUX is enabled in the *Diagnostic Output Pin DIAG_OUT*section 42
- Added clarification on the watchdog fail counter and reset event requirements in the *WDT Fail Counter, WDT Status, and WDT Fail Event* section 46
- Changed the RT bits from 4:0 to 6:0 in the T_{WCW} calculation in the *WDTI Configuration With an External Trigger Input (Default Mode)* section 47
- Deleted the RT bits from 4:0 to 6:0 in the T_{WCW} calculation in the *Watchdog Token-Response Sequence Run* section and changed the second calculation from T_{WOW} to T_{WCW} 50
- Changed WDT_ANSW_CNT answer order in *Set of 4-Bit WD Token Values and Corresponding 8-Bit Responses* table. 54
- Changed 4-bit watchdog answer conter to 2-bit watchdog answer counter (WDT_ANSW_CNT) in Watchdog Token-Response Sequence Run and WDT_STATUS Register Updates section 55
- Deleted logic BIST activated by MCU in SAFE state in the *MCU Error Signal Monitor (MCU ESM)* 56
- Deleted permanently text for the CRC check in the *Device Configuration Register Protection* section 60
- Changed CRC check to return to step one for continuous check in the *Device Configuration Register Protection* section 62
- Added clarification on the watchdog fail counter and reset event requirement in the *Reset and Enable Circuit* image 63
- Added or POST_RUN_RST = 1 & IGN_PWRL = 1 & re-cranking on IGN to*Global RESET Conditions* text bubble of the *Device Controller State Diagram* image 65
- Added clarification on watchdog fail counter text to the watchdog reset sub-bullet in the *RESET STATE* list 66
- Changed status bit STAT[1] function in *Device Status Flag Byte Response* table 69
- Added clarification for watchdog failure in the *SAFETY_STAT_2 Register* table 75
- Added clarification for watchdog failure in the *SAFETY_STAT_4 Register* table 77
- Added ERROR/WDI text to D[5] *cleared to* description in the *SAFETY_ERR_STAT Register* table 82
- Added watchdog fail counter text to D[4] *cleared to* description in the *SAFETY_ERR_STAT Register* table 82
- Changed the calculation in the *WDT_WIN1_CFG Register* table 85
- Changed the calculation in the *WDT_WIN2_CFG Register* table 85
- Changed data for SW_LOCK and SW_UNLOCK commands which were reversed in the *SPI Command Table* 88
- Added the *Typical Application* section 90
- Clarified ESR needed on VDD6 output capacitance in the *Typical Application Diagram* 91
- Added the *System Examples* section 98
- Added the *Layout* section 102

Changes from Revision A (December 2013) to Revision B **Page**

- Deleted the phrase *safety critical* from the document. 1
- Added device name to document title 1
- Added the following to the document: *Device Information* table, *Power Supply Recommendations* section, *Layout* section,*Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* section 2
- Changed the pin type for the VDD3/5 pin from I to PWR 16
- Changed the max value for the Charge-pump voltages from 50 to 52 V in the *ABSOLUTE MAXIMUM RATINGS* table 17
- Added the *Handling Ratings* table which now contains the storage temperature and ESD ratings 17
- Added added *with respect to the GND pin* to the condition statement in the *RECOMMENDED OPERATING CONDITIONS* 18
- Moved operating ambient temperature range from the *Absolute Maximum Ratings* table to the *Recommended Operating Conditions* table 18
- Changed changed *no undervoltage* to *no NRES event* and added VSOUT to the input supply voltage range on VBATP specification in the *Recommended Operating Conditions* 18
- Deleted Thermal Information table notes: all of these notes are included in the *IC Package Thermal Metrics* application report that is listed in the new table note. 18
- Added the power dissipation image and notes after the *Thermal Information* table 18
- Changed condition statement for the *ELECTRICAL CHARACTERISTICS* table by removing 125°C from the T_A temperature range and changingT_J to the maximum operating junction temperature. Removed VBATP range and added reference to R1.2 19
- Deleted letter *A* from beginning of POS number in the *VDD6-BUCK With Internal FET* and *VDD1 – LDO With External FET* sections of the *Electrical Characteristics* and *Timing Requirements* table 19

- Changed the parameter name of I_{VDD6} from output voltage to output current in the *Electrical Characteristics* table .. 19
- Added the test condition to the dVDD5/dt parameter in the *ELECTRICAL CHARACTERISTICS* table..... 19
- Changed condition statement for the *ELECTRICAL CHARACTERISTICS* table by removing 125°C from the T_A temperature range and changingT_J to the maximum operating junction temperature. Removed VBATP range and added reference to R1.2 20
- Changed the typ value from 3.35 to 3.3 and 5 for the VDD3/5 output voltage parameter in the *ELECTRICAL CHARACTERISTICS* table..... 20
- Changed the unit from † to V for the 3.3, VDD3/5 output voltage dynamic parameter in the *Electrical Characteristics* table 20
- Changed the parameter of 3.8 in the *Electrical Characteristics* table from VDD5 to VDD6..... 20
- Changed condition statement for the *ELECTRICAL CHARACTERISTICS* table by removing 125°C from the T_A temperature range and changingT_J to the maximum operating junction temperature. Removed VBATP range and added reference to R1.2 21
- Changed the parameter of A4.11 in the *Electrical Characteristics* table from VBATP to VDD6..... 21
- Changed MVVSOUT1 min and max values from –35 and 35 to –25 and 25 in the *Electrical Characteristics* table... 21
- Changed the max value for temperature range listed in the VdrS1 parameter test condition from 165 to 150 in the *Electrical Characteristics* table 21
- Changed the MIN and MAX values of the $LdReg_{VSOUT1}$ parameter from –25 and 25 to –35 and 35 in the *Electrical Characteristics* table 21
- Changed condition statement for the *ELECTRICAL CHARACTERISTICS* table by removing 125°C from the T_A temperature range and changingT_J to the maximum operating junction temperature. Removed VBATP range and added reference to R1.2 22
- Changed the typical value for the VDD3/5_OV 5-V hysteresis setting from 400 to 140 in the *Electrical Characteristics* table 22
- Added DC condition note to the VSOUT1_UV and VSOUT1_OV parameters in the *Electrical Characteristics* table 22
- Changed condition statement for the *ELECTRICAL CHARACTERISTICS* table by removing 125°C from the T_A temperature range and changingT_J to the maximum operating junction temperature. Removed VBATP range and added reference to R1.2 23
- Changed max value for the $R_{dson\_ENDRV\_NRES}$ (9.2a) parameter from 86 to 40 in the *Electrical characteristics* table .. 23
- Deleted note reference for the R_{RSTEXT} parameter (9.3) in the *Electrical Characteristics* table..... 23
- Changed min value from 300 to 350 for the $V_{ENDRV\_NRES\_TH}$ (9.5) parameter in the *ELECTRICAL CHARACTERISTICS* table 23
- Added note reference and test condition to the V_{DIGIN_HIGH} parameter (10.1) in the *ELECTRICAL CHARACTERISTICS* table 23
- Moved timing and switching characteristics out of the *Electrical Characteristics* table and into a *Timing Requirements* and *Switching Requirements* table (respectively). Also moved the capacitance at C_{SDO} note to the *Timing Requirements* and *Switching Requirements* tables..... 24
- Changed the TYP value to the MAX value of the SPI clock frequency parameter for the VDDIO = 5 V test condition in the *Electrical Characteristics* table 24
- Added image reference to timing and switching requirement parameters 24
- Changed max value of t_{tri} (13.11) from 25 to 53.3 in the *ELECTRICAL CHARACTERISTICS* table 25
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- Moved block diagram into the *Detailed Description* section and updated block colors..... 27
- Changed the OV max value for VDD3/5 (3.3 V) from 3.63 to 3.6 in the *Voltage Monitoring Overview* table 35
- Added nMASK comments to the UV and OV impact on device behavior for VDD1 in the *Voltage Monitoring Overview* table..... 35
- Moved the *Internal Error Signals* table to after the *Voltage Monitoring Overview* table in the *Detailed Description* section 36
- Changed the TYP value for the AVDD_UVN signal from 3.81 to 3.6 in the *Internal Error Signals* table. Also changed the device state from *Not changed* for NRES and ENDRV to *LOW*, and for State to *STAND-BY* 36
- Changed the TYP value for the VCP12_UVN signal from 7.32 to 7.43 in the *Internal Error Signals* table 36
- Changed the TYP value for the VCP12_OV signal from 14 to 14.2 in the *Internal Error Signals* table 36
- Changed the typ value for VCP_OV from 20 to 21 in the *Internal Error Signals* table 36
- Changed NUV on signal names to UVN throughout 36
- Changed the MIN value for the LOCLK signal from 0.740.7452 to 0.742 in the *Internal Error Signals* table 36
- Moved the *Internal Error Signals* table to after the *Voltage Monitoring Overview* table in the *Detailed Description* section 37
- Changed the VBATP_OV MIN and MAX values from 29 to 34.7 and 32 to 36.7 (respectively) in the *Internal Error Signals* table 37

- Changed the device state of the VDD3_5_OT bit from STANDBY to include change 37
- Changed the max values for VDD5_CL and VDD3_5_CL from 600 to 650 in the *Internal Error Signals* table 37
- Added the DVDD_UV signal to the *Internal Error Signals* table 37
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- Deleted *Watchdog function configuration* from the post-BIST-reset initialization list in the *Logic Built-In Self-Test (LBIST)* section 40
- Changed VCP voltage range from *0.8 to 5.5* to *0.6 to 4* 42
- Replaced the VSFB1 sensor-supply feedback voltage row wit the VSOUT1 sensor-supply voltage row in the *Analog MUX Selection Table* 42
- Changed the Voltage Range / Accuracy value for both MAIN_BG and VMON_BG from 1.226 to 2.5 V in the *Analog MUX Selection* table 42
- Changed the name bit that must be configured for DIGITAL MUX mode from DIAG_MUX to MUX_CFG in the *Digital MUX (DMUX)* section 45
- Deleted *Bits INT_CON[2:0] in DIAG_CFG_CTRL register must be set to 111* list item from the SDO diagnostic check sequence in the *MUX interconnect check* section 45
- Changed the RT bits from 4:0 to 6:0 in the T_{WCW} calculation in the *WDTI Configuration With an External Trigger Input (Default Mode)* section 47
- Deleted the CLOSE window note from the *Possible Cases for Bad Watchdog Event* image and updated the iamge 48
- Added + 1 to the duration time program calculations in the *Watchdog Token-Response Sequence Run* section and changed the second calculation from T_{WOW} to T_{WCW} 50
- Changed the filter time for the ERROR/WDI deglitch from 15-s to 15-µs in the *MCU Error Signal Monitor (MCU ESM)* section 56
- Changed the low-pulse duration increment from 15-s to 15-µs in the *PWM Mode* section 58
- Changed the *Reset and Enable Circuit* figure to reflect overtemperature behavior. 63
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- Deleted WDT failure text from the first list item in the *SAFE State* section 67
- Moved all of the registers into one *Register Map* section 70
- Changed D0 from 1 to 0 in the *DEV_REV Register* table 70
- Changed D1 and D0 from 0 to X in the *DEV_STATE Register* table 70
- Changed the deglitched minimum time from 7.7 to 7.5 for the IGN bit description in the DEV_STATE register 70
- Changed D7 from RSV and 1 to VDD_3_5_SEL and X in the *DEV_CFG1 Register* table 71
- Changed D6 from nMASK_VDD_UV and 1 to nMASK_VDD_UV_OV and 0 in the *DEV_CFG1 Register* table 71
- Changed the default value of the nMASK_VDD1_UV_OV bit from 1 to 0 and the VDD1 bit value from 0 to 1 in the *DEV_CFG1 Register* 71
- Changed bit D5 name from MASK_VBAT_OV to MASK_VBATP_OV in the *DEV_CFG2 Register* table 71
- Changed VDD6, clearing, and re-enabling text from the D[7] description when EN_VDD3/5_OT is set to '1' and changed to *when set to '"* in the *DEV_CFG2 Register* table 71
- Changed the D[7] description when EN_VDD3/5_OT is set to '0' by removing the SAFETY_STAT_REG1, VDD6 and re-enable text in the *DEV_CFG2 Register* table. Also changed from *when set to '0'* to *when set to '1'* 71
- Changed D[3:0] description in the *DEV_CFG2 Register* table from *bits are not read/writable* to *bits are read/writable* 71
- Deleted *after SPI read access* from the clear to 0 description of each bit in the *VMON_STAT_1 Register* 72
- Deleted *after SPI read access* from the clear to 0 description of each bit in the *VMON_STAT_2 Register* 73
- Deleted *after SPI read access* from the clear to 0 description of each bit in the *SAFETY_STAT_1 Register* 74
- Deleted *after SPI read access* from the clear to 0 description of each bit in the *SAFETY_STAT_2 Register* 75
- Added description to bit D[4] when set to one 1 when the device is the DIAGNOSTIC state 75
- Changed the name of bit D5 in the SAFETY_STAT_3 register from NRES_IN to NRES_ERR 76
- Changed the D[5] NRES_IN, Reset input status, register description to NRES_ERR, Reset input error and change first description for setting this bit to 1 76
- Updated *cleared to 0* description of the LBIST_ERR bit in the *SAFETY_STAT_3* register 76
- Added DIAGNOSTIC state description for setting bit D[3] and D[2] to 1 76
- Changed *SPI read access* to *internal NPOR* from the LOCLK bit description in the *SAFETY_STAT_4 Register* 77
- Changed bit D7 and bit D6 from 1 to 0 in the *SAFETY_ERR_CFG Register* table 78
- Changed the SAFETY_STAT4 register bit from D4 to D5 in the ABIST_EN[1:0] descriptions in the SAFETY_BIST_CTRL Register table 79
- Changed names of protected registers in the CRG_CRC_EN bit description in the *SAFETY_CHECK_CTRL Register* 80
- Changed monitored to not monitored in the NO_ERROR bit description for setting this bit to 1 in the

Changes from Original (May 2012) to Revision A **Page**

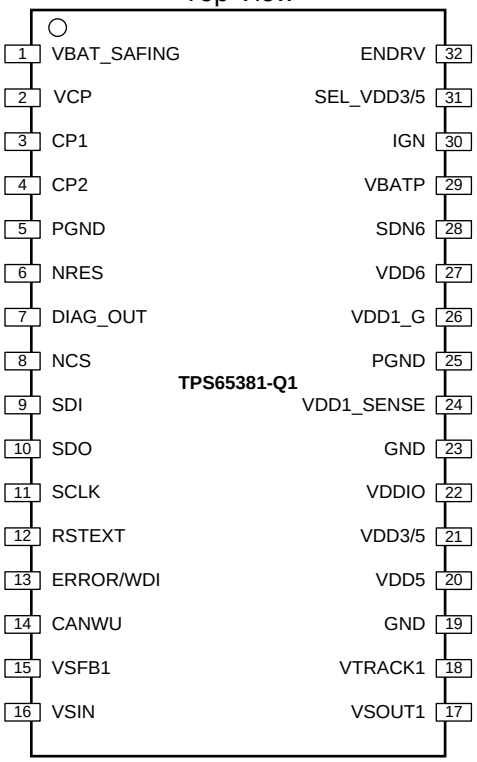
- Added Hysteresis parameter, min and max values to $Tprot_{VDD6}$ (A1.7) in the *ELECTRICAL CHARACTERISTICS* table. Changed test condition from *Global shutdown* to *Protection of VDD6, shared with VDD3/5 thermal protection.* for both $Tprot_{VDD6}$ parameters 19
- Added Hysteresis parameter, min and max values to $Tprot_{VDD5}$ (2.13) in the *ELECTRICAL CHARACTERISTICS* table. Changed test condition from *VDD5 switch-off* to *Protection of VDD5.In case of detected over-temperature, only VDD5 will be switched-off* for both $Tprot_{VDD5}$ parameters 19
- Changed condition statement for the *ELECTRICAL CHARACTERISTICS* table by adding T_A over junction temperature with up to 150°C 20
- Added VDD3/5 end-value to test condition for the dVDD35/dt parameter (3.11) in the *ELECTRICAL CHARACTERISTICS* table 20
- Added Hysteresis parameter, min and max values to $Tprot_{VDD3/5}$ (3.13) in the *ELECTRICAL CHARACTERISTICS* table. Changed test condition from *Global shutdown* to *Protection of VDD3/5, treated as global thermal shutdown (shutdown for all regulators)* for both $Tprot_{VDD3/5}$ parameters 20
- Changed condition statement for the *ELECTRICAL CHARACTERISTICS* table by adding T_A over junction temperature with up to 150°C 21
- Added test condition to the dVDD1/dt parameter (A4.14) in the *ELECTRICAL CHARACTERISTICS* table 21
- Added VSOUT1 text to test condition for VSOUT1 parameter (5.1) in the *ELECTRICAL CHARACTERISTICS* table 21
- Changed MVVSOUT1 min and max values from –15 and 15 to –35 and 35 in the *ELECTRICAL CHARACTERISTICS* table 21
- Added min and max values for the Threshold for tracking/non-tracking parameter in the *ELECTRICAL CHARACTERISTICS* table 21
- Added Hysteresis parameter, min and max values to $Tprot_{VSOUT1}$ (5.13) in the *ELECTRICAL CHARACTERISTICS* table. Changed test condition from *VSOUT1 switch-off* to *Protection of Sensor Supply. Only VSOUT1 switch-off* for both $Tprot_{VSOUT1}$ parameters 21
- Changed min and max values for $VBATP\_OV_{rise}$ parameter from 29.5 and 32.5 to 34.7 and 36.7 (respectively) in the *ELECTRICAL CHARACTERISTICS* table. Also added test condition 21
- Deleted VBATP_OVhys (POS 6.6) from the *ELECTRICAL CHARACTERISTICS* table 21
- Changed min and max values for $VBATP\_OV_{fall}$ parameter from 29 and 32 to 34.4 and 36.3 (respectively) in the *ELECTRICAL CHARACTERISTICS* table. Also added test condition 21
- Changed condition statement for the *ELECTRICAL CHARACTERISTICS* table by adding T_A over junction temperature with up to 150°C 22
- Added Hysteresis parameter, min and max values to VDD5_UV (6.8) in the *ELECTRICAL CHARACTERISTICS* table. 22
- Changed max value for VDD5_OV from 5.5 to 5.45 in the *ELECTRICAL CHARACTERISTICS* table 22
- Added Hysteresis parameter, min and max values to VDD5_OV (6.10) in the *ELECTRICAL CHARACTERISTICS* table. 22
- Changed min value for VDD3/5_UV with test condition of 3.3-V setting (undervoltage) from 2.97 to 3 in the *ELECTRICAL CHARACTERISTICS* table 22
- Changed max value for VDD3/5_UV with test condition of 5-V setting (undervoltage) from 4.8 to 4.85 in the *ELECTRICAL CHARACTERISTICS* table 22
- Added Hysteresis parameter for 3.3 and 5 V settings, min and max values to VDD3/5_UV (6.12) in the *ELECTRICAL CHARACTERISTICS* table. 22
- Changed max value for VDD3/5_OV with test condition of 3.3-V setting from 3.63 to 3.6 in the *ELECTRICAL CHARACTERISTICS* table 22
- Added Hysteresis parameter for 3.3 and 5 V settings, min and max values to VDD3/5_OV (6.14) in the *ELECTRICAL CHARACTERISTICS* table. 22
- Added Hysteresis parameter, min and max values to VDD1_UV (6.16) in the *ELECTRICAL CHARACTERISTICS* table. Changed test condition from *Sensed on VDD1_SENSE pin* to *Sensed on VDD1_SENSE pin. Relative thresholds are with respect to nominal 800-mV VDD1SENSE (Pos 4.2)* for both VDD1_UV parameters 22
- Added Hysteresis parameter, min and max values to VDD1_OV (6.17) in the *ELECTRICAL CHARACTERISTICS* table. Changed test condition from *Sensed on VDD1_SENSE pin* to *Sensed on VDD1_SENSE pin. Relative thresholds are with respect to nominal 800-mV VDD1SENSE (Pos 4.2)* for both VDD1_OV parameters 22
- Added Hysteresis parameter, min and max values to VSOUT1_UV (6.19) in the *ELECTRICAL CHARACTERISTICS* table. Changed test condition from *Sensed on VSFB1 pin* to *Sensed on VSFB1 pin Relative thresholds are:* for both VSOUT1_UV parameters 22
- Added Hysteresis parameter, min and max values to VSOUT1_UV (6.20) in the *ELECTRICAL CHARACTERISTICS* table. Changed test condition from *Sensed on VSFB1 pin* to *Sensed on VSFB1 pin*

- Added SPI command setting to the seventh paragraph in the *VSOUT1 Linear Regulator* section 30
- Added DIAGNOSTIC state text to the *Wake-Up* section..... 31
- Changed second paragraph in the *Wake-Up* section: changed edge-sensitive to level-sensitive and pulse duration to deglitch time. 31
- Added *during a power-up event* to the *Reset Extension* section and removed VDD1 from the description 31
- Changed the *Reset Extension* section by splitting paragraph into two and adding new VDD1 text in between 31
- Deleted open-connect and RESET state sentence from the last paragraph in the *Reset Extension* section..... 31
- Changed *Power-Up and Power-Down Behavior* image in the *Power-Up and Power-Down Behavior* section 32
- Added notes to the*IGN Power Latch and POST-RUN Reset* image in the *Power-Up and Power-Down Behavior* section 33
- Deleted reset driver from ENDRV bullet in the *Safety Functions and Diagnostics Overview* section 34
- Added the *Voltage Monitoring Overview* table and table reference to the *Voltage Monitor (VMON)* section..... 34
- Added Internal Error Signals table 36
- Deleted loss-of-power note and cleared-latched bullet from the clock failure list in the *Loss-of-Clock Monitor (LCMON)* section 38
- Added SPI register bit to the latched bullet in the clock failure list in the *Loss-of-Clock Monitor (LCMON)* section ... 38
- Added ABIST case paragraphs following the *Analog BIST Run States* image 39
- Moved *Logic Built-In Self-Test (LBIST)* section from after DMUX tables and added initialized registers list 40
- Deleted VDD5 and VSOUT1 supplies from first paragraph of the *Junction Temperature Monitoring and Current Limiting* section 40
- Added VSOUT1 supplies paragraph to the *Junction Temperature Monitoring and Current Limiting* section..... 40
- Deleted STANDBY State text from the *Junction Temperature Monitoring and Current Limiting* section and changed to regulated supplies. Also added ENDRV pin..... 40
- Changed third paragraph of the *Junction Temperature Monitoring and Current Limiting* section to include NRES asserted low and VDD5 reenable 40
- Added *Thermal and Overcurrent Protect Overview* table and table reference to the *Junction Temperature Monitoring and Current Limiting* section..... 41
- Added analog and digital signals and notes to the *Diagnostic Output Pin DIAG_OUT* image in the *Diagnostic Output Pin DIAG_OUT* section 41
- Added added diasabled sate description for the DIAG_OUT pin in the last paragraph of the *Diagnostic Output Pin DIAG_OUT* section 42
- Added ± percentage to the divide ratio values (except for MAIN_BG and VMON_BG) the *Analog MUX Selection* table 42
- Added *accuracy* and corresponding table note to the voltage range column in the *Analog MUX Selection* table 42
- Added the max output resistance column to the *Analog MUX Selection* table..... 42
- Changed the DIAG_MUX_SEL column and header in the *Analog MUX Selection* table..... 42
- Added the voltage/signal name for signal number A.7 from BG1 to MAIN_BG in the *Analog MUX Selection* table .. 42
- Added additional text and note to further explain the *Analog MUX Selection* Table 42
- Added second paragraph to the *Digital MUX (DMUX)* section..... 42
- Added diagnostic check text, *Diagnostic MUX Output state (by MUX_OUT bit)*, and *MUX interconnect check* section after DMUX tables 45
- Changed the *Watchdog Enable Function* image in the *WDT Fail Counter, WDT Status, and WDT Fail Event* section 46
- Added watchdog fail counter text after the *Watchdog Status for Fail Counter Value Range* table..... 46
- Changed trigger events paragraph (third) in the *WDTI Configuration with External Trigger Input (Default Mode)* section 47
- Added SPI register names and DIAGNOSTIC state to the open and close window programming sentence in the *WDTI Configuration with External Trigger Input (Default Mode)* section 47
- Added the WDTI window sequencing and SPI SW_LOCK paragraphs in the *WDTI Configuration with External Trigger Input (Default Mode)* section 47
- Added the WDTI rising edge paragraph in the *WDTI Configuration with External Trigger Input (Default Mode)* section and added t_{WD_pulse} filter time paragraph..... 47
- Added image to the *WDTI Configuration with External Trigger Input (Default Mode)* section 48
- Added image to the *WDTI Configuration with External Trigger Input (Default Mode)* section 48
- Deleted ASIC reference in the first paragraph of the *Watchdog Question /and Answer Configuration Through SPI* section 49
- Added added note in the *Watchdog Question /and Answer Configuration Through SPI* section 49
- Added *starts a new watchdog token-response sequence run* to the no-response event description in paragraph four of the *Watchdog Question /and Answer Configuration Through SPI* section..... 49
- Added 4-bit word bullet to the *Watchdog Token Request* definition list in the *Watchdog-Timer-Related SPI Event*

- Changed D[1] from not read/writable to read/writable in the *SAFETY_FUNC_CFG Register* table 81
- Added READ-ONLY bullet, RESET STATE sub-bullet, and connected and not-connected text to the D[0] description in the *SAFETY_FUNC_CFG Register* table 81
- Added ERROR/WDI and SAFE state text to the D[5] *set to* description in the *SAFETY_ERR_STAT Register* table . 82
- Added WD_RST_EN text to D[4] *set to* description in the *SAFETY_ERR_STAT Register* table 82
- Added watchdog fail counter text to D[4] *cleared to* description in the *SAFETY_ERR_STAT Register* table 82
- Added equation and oscillator text to the *SAFETY_ERR_PWM_H Register* table description 82
- Changed D4, D2, and D0 from 0 to 1 in the *SAFETY_ERR_PWM_L Register* description 82
- Added equations and oscillator text to the *SAFETY_ERR_PWM_H Register* table description 82
- Changed D4 from 1 to 0 in the*SAFETY_PWD_THR_CFG Register* table 83
- Changed _THR to PWD names for D3:D0 in the*SAFETY_PWD_THR_CFG Register* table 83
- Changed D7, D5, and D3 from 1 to 0 in the *SAFETY_CFG_CRC Register* table 83
- Changed D4 from 0 to 1 in the *SAFETY_CFG_CRC Register* table 83
- Changed D[7] description from high-impedance to tri-stated in the *DIAG_CFG_CTRL Register* table 84
- Added SDO diagnostics from D[1:0] description to the D[6] description in the *DIAG_CFG_CTRL Register* table 84
- Changed D2 from 1 to 0 in the *WDT_TOKEN_FDBCK Register* table 85
- Added bullets to the D[7:4] description in the *WDT_TOKEN_FDBCK Register* table 85
- Added new TOKEN seed bullet and sub-bullets to the D[3:0] description in the *WDT_TOKEN_FDBCK Register* table 85
- Changed D6:D0 from 0 to 1 in the *WDT_WIN1_CFG Register* table 85
- Changed D4:D3 from 0 to 1 in the *WDT_WIN2_CFG Register* table 85
- Changed D7 from 0 to 1 in the *WDT_TOKEN_VALUE Register* table 86
- Changed MCU sub-bullet from D[7] description to replace Q&A sub-bullet in the D[3:0] description of the *WDT_TOKEN_VALUE Register* table 86
- Changed D7:D6 from 0 to 1 in the *WDT_STATUS Register* table 86
- Changed D7:DF from RSV to WD_WRONG_CFG in the *WDT_STATUS Register* table 86
- Changed *set to* text of the D[5] description in the *WDT_STATUS Register* table 86
- Changed D[4] note from recommendation to clear bit to remains set to 1 in the *SENS_CTRL Register* table 87
- Added 8-bit hex column to the *SPI Command Table* 88
- Added 8-bit hex column to the *SPI Command Table* 89
- Changed *Typical Application Diagram* image 91

3 Pin Configuration and Functions

DAP Package
32-Pin HTSSOP With PowerPAD™
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VBAT_SAFING	PWR	Battery voltage (reverse protected) for safety functions
2	VCP	PWR	Charge-pump output voltage
3	CP1	PWR	Charge-pump external capacitor, high-voltage side
4	CP2	PWR	Charge-pump external capacitor, low-voltage side
5	PGND	GND	Ground (power)
25			
6	NRES	O	Cold-reset (NPOR_RST) output signal for the microcontroller (µC)
7	DIAG_OUT	O	Analog MUX output for MCU ADC
8	NCS	I	SPI chip select (active-low)
9	SDI	I	SPI serial data IN
10	SDO	O	SPI serial data OUT
11	SCLK	I	SPI clock
12	RSTEXT	I	Configuration pin for reset extension
13	ERROR/WDI	I	Error input signal from MCU / window watchdog input trigger
14	CANWU	I	Wake-up input signal from CAN transceiver
15	VSFB1	I	Feedback input reference for sensor supply regulator
16	VSIN	PWR	Sensor-supply regulator input supply voltage
17	VSOUT1	PWR	Sensor-supply regulator output voltage
18	VTRACK1	I	Tracking input reference for sensor-supply regulator

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
19	GND	GND	Ground (analog)
23			
20	VDD5	PWR	VDD5 regulator output voltage
21	VDD3/5	PWR	VDD3/5 regulator output voltage
22	VDDIO	PWR	I/O-level for pins to and from the MCU
24	VDD1_SENSE	I	Input reference for VDD1 regulator
26	VDD1_G	O	Gate of external FET for VDD1 regulator
27	VDD6	PWR	VDD6 switch-mode regulator output voltage
28	SDN6	PWR	Switching node for VDD6 switch-mode regulator
29	VBATP	PWR	Battery voltage (reverse protected)
30	IGN	I	Wake-up signal from ignition key
31	SEL_VDD3/5	I	Select input for VDD3/5 regulator
32	ENDRV	O	Enable output signal for peripherals (for example, motor-driver IC).
—	Thermal pad	—	Connected to GNDIO. Place thermal vias to large ground plane and connect to AGND and GNDIO pin.

4 Specifications

4.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

POS			MIN	MAX	UNIT
M1.1	Protected-battery voltage	VBATP, VBAT_SAFING, VSIN	–0.3	40	V
M1.2	Charge-pump voltage	VCP, CP1	–0.3	52	V
M1.3	Charge-pump pumping capacitor voltage	CP2	–0.3	40	V
M1.3a	Charge-pump overdrive voltage	VCP-VBATP	–0.3	16	V
M1.4	VDD6 switching-node voltage	SDN6	–0.3	40	V
M1.5	VDD6 output voltage	VDD6	–0.3	40	V
M1.6	VDD5 output voltage	VDD5	–0.3	7	V
M1.7	VDD3/5 output voltage	VDD3/5	–0.3	7	V
M1.8	VDD1_G voltage	VDD1_G	–0.3	15	V
M1.10	VDD1_SENSE voltage	VDD1_SENSE	–0.3	7	V
M1.11	Sensor supply tracking voltage	VTRACK1	–0.3	40	V
M1.12	Sensor supply feedback voltage	VSFB1	–2	40	V
M1.13	Sensor supply output voltage	VSOUT1	–2	40	V
M1.14	Analog/digital ref. output voltage	DIAG_OUT	–0.3	7	V
M1.15	Logic I/O voltage	VDDIO, ERROR/WDI, ENDRV, NRES, NCS, SDI, SDO, SCLK, RSTEXT	–0.3	7	V
M1.16		SEL_VDD3/5	–0.3	40	V
M1.17	IGN wake-up	IGN	–7	40	V
M1.18	CAN wake-up	CANWU	–0.3	40	V
M1.19	Operating virtual junction temperature range, T_J			150	°C
	Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin unless otherwise noted.

4.2 ESD Ratings

POS.					VALUE	UNIT
M1.21	$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins except VSOUT1 (17) and VSFB1 (15)	±2000	V
M1.20				On sensor supply pins VSOUT1 (17) and VSFB1 (15)	±4000	
M1.22			Charged device model (CDM), per AEC Q100-011	Corner pins (1, 16, 17, and 32)	±750	
M1.23				All pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 Specification

4.3 Recommended Operating Conditions

Over operating temperature range and with respect to the GND pin (unless otherwise noted)

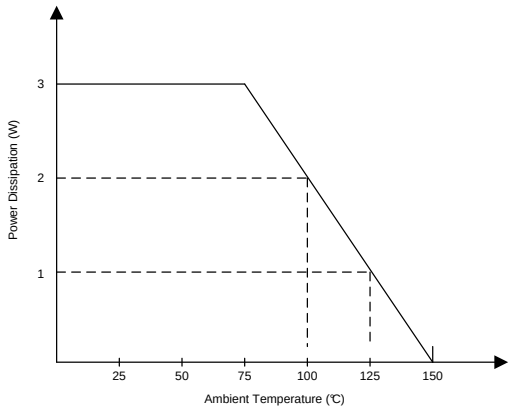
POS		MIN	MAX	UNIT
M1.20a	Operating ambient temperature range, T_A	–40	125	°C
R1.1	Input supply voltage range on VBATP pins for initial power up	5.8		V
R1.2	Input supply voltage range on VBATP(1) – VSOUT1 configured as 5 V or higher, VDD3/5 configured as 5 V and VDD5 regulators are in undervoltage when VBATP is between 5.8 V and 6.6 V. – The VDD3/5 regulator undervoltage event causes NRES to be pulled low	5.8(1)	36	V
R1.3	Input supply-voltage range on VBATP – VDD6, VDD5 regulators in low dropout, VDD3 and VDD1 regulator outputs functional (no undervoltage). VSOUT1 either functional or in low dropout, depending on configuration.	4.5		V
R1.3a	Input supply voltage for VBAT_SAFING (when below minimum, device does not start up and NRES, ENDRV is pulled low.)	4.2	40	V
R1.4	VDDIO supply-voltage range	3.3	5	V
R1.5	Current consumption in standby mode (all regulator outputs disabled) IGN = 0 V, CANWU = 0 V, 5.8 V ≤ VBAT ≤ 20 V for T_J < 85°C or 5.8 V ≤ VBAT ≤ 14 V tor T_J = 125°C		75	µA

(1) Under slow VBAT ramp-down and when VDD3/5 rails is configured as a 5-V rail, the NRES output can be pulled low when VBAT is at approximately 6.3 V. This occurs because of an undervoltage transient on the VDD3/5 rail.
Under slow VBAT ramp-up and when VDD3/5 rail is configured as a 5-V rail, the NRES output can be pulled low when VBAT is at approximately 6.6 V. This occurs because of an undervoltage transient on VDD3/5 rail. Under similar conditions, undervoltage transients are observed on VDD5 and VSOUT rails (refer to the Application Report, *Device Behavior Under Slow VBAT Ramp-Up and Ramp-Down*, SLVA643).

4.4 Thermal Information

THERMAL METRIC(1)		HTSSOP (DAP) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	14.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	15.3	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	15.2	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	0.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.



(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_A$max) is dependent on the maximum operating junction temperature ($T_J$max), the maximum power dissipation of the device in the application ($P_D$max), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_A$max = $T_J$max – ($R_{\theta JA}$ × $P_D$max).

(2) Maximum power dissipation is a function of $T_J$max, $R_{\theta JA}$ and T_A. The maximum-allowable power dissipation at any allowable ambient temperature is P_D = ($T_J$max – T_A) / $R_{\theta JA}$.

Figure 4-1. Derating Profile for Power Dissipation Based on High-K JEDEC PCB

4.5 Electrical Characteristics

Over operating ambient temperature T_A = –40°C to the maximum-operating junction temperature T_J = 150°C, and recommended operating VBATP range (see R1.2 in Section 4.3) (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD6-BUCK With Internal FET							
AN	C_{VDD6}	Value of output ceramic capacitor(1)	ESR range 100 mΩ to 300 mΩ(2)	22		47	µF
AN	L_{VDD6}	Value of inductor		22	33		µH
1.1	VDD6	VDD6 output voltage	Average DC value excluding ripple and load transients, VBAT > 7 V, 0 < I_{VDD6} < 1.3 A, including dc line and load regulation, temperature drift, and long-term drift	–10%	6	10%	V
1.1a	$VDD6_{ripple}$	VDD6 ripple voltage	Peak-to-peak, ensured by design VBAT = 14 V, L = 33 µH, C = 22 µF		200		mV
1.2	I_{VDD6}	VDD6 output current I_{VDD5} + I_{VDD3} + I_{VDD1}+ I_{VSOUT1}	Load currents from VDD5, VDD3_5, VDD1 and VSOUT1; VDD6 not recommended to be loaded directly			1.3	A
1.3	$V_{dropout6}$	VDD6 output dropout voltage $V_{dropout6}$ = (VBATP – SDN6)	I_{VDD6} = 1.3 A (example: $R_{DS(on)}$ = 0.46 Ω)			0.6	V
1.4	I_{VDD6_limit}	Peak current out of SDN6 pin		1.5		2.5	A
1.5	f_{clk_VDD6}	Clock Frequency (3)		–10%	440	10%	kHz
1.6	DC_{VDD6}	t_{on}/t_{period}	0 < I_{VDD6} < 1.3 A VDD6 enters dropout mode for VBATP < 7 V	7%		100%	
1.7	$Tprot_{VDD6}$	Temperature protection threshold	Protection of VDD6, shared with VDD3/5 thermal protection.	175		210	°C
		Hysteresis		10		20	
VDD5 – LDO With Internal FET							
AN	C_{VDD5}	Value of output ceramic capacitor	ESR range 0 mΩ to 100 mΩ	1		5	µF
2.1	VDD5	VDD5 output voltage	0 < I_{VDD}5 < 300 mA, including line and load regulation, temperature drift, and long-term drift	–2%	5	2%	V
2.2	I_{VDD5}	VDD5 output current	Min. load with internal resistor of 660 Ω (typ.)			300	mA
2.3	$VDD5_{dyn}$	VDD5 output voltage dynamic	Load step 10% to 90% in 1 µs, with 5-µF C_{VDD5}	4.85	5	5.15	V
2.4	$VDD5_{max}$	Maximum VDD5 output voltage during VBATP step from 5.5 V to 13.5 V within 10 µs	C_{VDD5} = 5 µF, I_{VDD5} < 300 mA			5.5	V
2.5	$V_{dropout5}$	VDD5 output dropout voltage $V_{dropout5}$ = (VDD6-VDD5)	I_{VDD5} < 300 mA			0.3	V
2.6	$PSRR_{VDD5}$	Power supply rejection ratio	50 < f < 20 kHz,VBATP = 10 V, U = 4 Vpp, C_{VDD5} = 5 µF, 0 < I_{VDD5} < 300 mA	40			dB
2.7	$LnReg_{VDD5}$	Line regulation (I_{VDD5} constant)	0 < I_{VDD5} < 300 mA, 8 V < VBATP < 19 V	–25		25	mV
2.8	$LdReg_{VDD5}$	Load regulation (VDD6 constant)	0 < I_{VDD5} < 300 mA, 8 V < VBATP < 19 V	–25		25	mV
2.9	$TmpCo_{VDD5}$	Temperature drift	Normalized to 25°C value	–0.5%		0.5%	
2.11	dVDD5/dt	dV/dt at VDD5 at startup	Between 10%-90% of VDD5 end-value	5		50	V/ms
2.13	$Tprot_{VDD5}$	Temperature protection threshold	Protection of VDD5. In case of detected over-temperature, only VDD5 will be switched-off	175		210	°C
		Hysteresis		10		20	
2.14	I_{VDD5_limit}	Current-limit		350		650	mA

(1) Capacitance is effective capacitance after derating for operating voltage, temperature and lifetime.
(2) ESR is total effective series resistance of the capacitors and if necessary added series resistor.
(3) Actual switching on SND6 depends on whether output voltage on VDD6 is above or below PWM comparator threshold at the moment of the rising edge of the F_{clk_VDD6} clock.

Electrical Characteristics *(continued)*

Over operating ambient temperature T_A = –40°C to the maximum-operating junction temperature T_J = 150°C, and recommended operating VBATP range (see R1.2 in Section 4.3) (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD3/5 – LDO With Internal FET							
AN	$C_{VDD3/5}$	Value of output ceramic capacitor	ESR range 0 mΩ to 100 mΩ	1		5	µF
3.1	VDD3/5	VDD3/5 output voltage	SEL_VDD3/5 pin open: 3.3 V SEL_$V_{DD3/5}$ to ground: 5 V 0 < $I_{VDD3/5}$ < 300 mA, inclusive of line and load regulation, temperature drift	–2%	3.3 5	+2%	V
3.2	$I_{VDD3/5}$	VDD3/5 output current	Min. load with internal resistor: 440 Ω for 3.3-V setting 660 Ω for 5-V setting			300	mA
3.3	$VDD3/5_{dyn}$	VDD3/5 output voltage dynamic	Depending on 3.3 V/5 V setting Load step 10% to 90% in 1 µs, with 5 µF CVDD3/5	3.17 4.85	3.3 5	3.43 5.15	V
3.4	$VDD3/5_{max}$	Maximum VDD3/5 output voltage during VBATP step from 5.5 V to 13.5 V within 10 µs	Depending on 3.3 V/5 V setting $C_{VDD3/5}$ = 5 µF, $I_{VDD3/5}$ < 300 mA			3.6 5.5	V
3.5	Vdropout3/5	VDD3/5 output dropout voltage Vdropout3/5= (VDD6-VDD3/5)	$I_{VDD3/5}$ < 300 mA			0.3	V
3.6	$PSRR_{VDD3/5}$	Power-supply rejection ratio	50 < f < 20 kHz, VBATP = 10 V, U = 4 Vpp $C_{VDD3/5}$ = 5 µF, 0 < $I_{VDD3/5}$ < 300 mA	40			dB
3.7	$LnReg_{VDD3/5}$	Line regulation (I_{VDD3} constant)	0 < $I_{VDD3/5}$ < 300 mA, 8 V < VBATP < 19 V	–25		25	mV
3.8	$LdReg_{VDD3/5}$	Load regulation (VDD6 constant)	0 < $I_{VDD3/5}$ < 300 mA 8 V < VBATP < 19 V	–25		25	mV
3.9	$TmpCo_{VDD3/5}$	Temperature drift	Normalized to 25°C value	–0.5%		0.5%	
3.11	dVDD35/dt	dV/dt at VDD3/5 at start-up	Depending on 3.3 V/5 V setting is between 10%-90% of VDD3/5 end-value	3 5		30 50	V/ms
3.13	$Tprot_{VDD3/5}$	Temperature protection threshold	Protection of VDD3/5, treated as global thermal shutdown (shutdown for all regulators)	175		210	°C
		Hysteresis		10		20	
3.14	$I_{VDD3\_5\_limit}$	Current-limit		350		650	mA
3.15	$I_{pu\_SEL\_VDD3/5}$	Pullup current on SEL_VDD3/5 pin				20	µA
VDD1 – LDO With External FET							
AN	Vgs(th)	Gate threshold voltage, external FET	ID = 1 mA	0.3		3	V
AN	Ciss	Gate capacitance, external FET	VGS = 0 V			3200	pF
AN	Qgate	Gate Charge ext. FET	VGS = 0 V to 10 V			70	nC
AN	gfs	Forward transconductance, external FET	ID = 50 mA	0.4			S
AN	C_{VDD1}	Value of output ceramic capacitor	ESR range 0 mΩ to 100 mΩ	5		40	µF
4.1	VDD1	VDD1 output voltage	Depends on external resistive divider	0.8		3.3	V
4.2	$VDD1_{SENSE}$	VDD1 reference voltage	10 mA < I_{VDD1} < 600 mA, including line and load regulation, temperature drift and long-term drift	–1%	0.8	2%	V
4.3	I_{VDD1}	VDD1 output current	Minimum current realized with external resistive divider	10		600	mA
4.4	$VDD1_G$	VDD1_G output voltage	Referenced to GND			15	V
4.5	$VDD1_{G\_off}$	VDD1_G voltage in OFF condition	Test condition: 20 µA into VDD1_G pin			0.3	V
4.6	I_VDD1_G	VDD1_G DC load current				200	µA
4.7	$VDD1_{dyn}$	VDD1 output voltage dynamic	Load step 10% to 90% in 1 µs, with 40 µF C_{VDD1}	–4%		4%	V
4.8	$VDD1_{max}$	Maximum VDD1 output voltage during VBATP step from 5.5 V to 13.5 V within 10 µs	C_{VDD1} > 6 µF, I_{VDD1}< 600 mA			10%	V

Electrical Characteristics *(continued)*

Over operating ambient temperature T_A = –40°C to the maximum-operating junction temperature T_J = 150°C, and recommended operating VBATP range (see R1.2 in Section 4.3) (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.9	$PSRR_{VDD1}$	Power-supply rejection ratio	50 < f < 20 kHz, VBATP = 10 V, U = 4 Vpp, C_{VDD1} = 10 µF, 10 mA < I_{VDD1} < 600 mA	40			dB
4.10	$LnReg_{VDD1}$	Line regulation on VDD1_SENSE (I_{VDD1} constant)	10 mA < $_{IVDD1}$< 600 mA, 8 V < VBATP < 19 V	–7		7	mV
4.11	$LdReg_{VDD1}$	Load regulation on VDD1_SENSE (VDD6 constant)	10 mA < I_{VDD}1 < 600 mA, 8 V < VBATP < 19 V	–7		7	mV
4.12	$TmpCo_{VDD1}$	Temperature drift	Normalized to 25°C value	–0.5%		0.5%	
4.14	dVDD1/dt	dV/dt at VDD1_SENSE at start-up	Between 10%-90% of VDD1 end-value	0.8		8	V/ms
VSOUT1 – LDO With Protected Internal FET							
AN	C_{VSOUT1}	Value of output ceramic capacitor	ESR range 0 mΩ to 100 mΩ	0.5		10	µF
5.1	VSOUT1	VSOUT1 output voltage	Depends on external resistive divider. VSOUT1 can track VDD3/5 in 3.3 V setting.	3.3		9.5	V
5.2	MV_{VSOUT1}	For tracking mode: Matching output errorMV_{VSOUT1} = (VTRACK1 – VSFB1)	0 < I_{VSOUT1} < 100 mA For specified I_{VSOUT} range, referenced to VTRACK1 input, including long-term and temperature drift.	–25		25	mV
5.3	VSFB1	For non-tracking mode: VSOUT1 reference voltage	10 mA < I_{VSOUT} < 100 mA, including line and load regulation, temperature drift and long-term drift	–2%	2.5	2%	V
5.3a	$VTRACK1_{th}$	Threshold for tracking/non-tracking	VTRACK1 > 1.2 V; VSOUT1 in tracking mode VTRACK1 < 1.2 V; VSOUT1 in non-tracking mode	1.1	1.2	1.3	V
5.3b	$VTRACK1_{pd}$	Internal pulldown resistance on VTRACK1 pin			100		kΩ
5.4	I_{VSOUT1}	VSOUT1 output current	internal resistor to dissipate min current			100	mA
5.5	VdrS1	VSOUT1 dropout voltage VdrS1 = (VSIN-VSOUT1)	T_J = –40°C to 150°C 0 < I_{VSOUT1} < 100 mA			0.75	V
5.6	$PSRR_{VSOUT1}$	Power-supply rejection ratio	With stable VTRACK1 input voltage 50 < f < 20 kHz, VBATP = 10 V, U = 4 Vpp C_{VSOUT1} = 1 µF, 0 < I_{VSOUT1} < 100 mA	40			dB
5.7	$LnReg_{VSOUT1}$	Line regulation (I_{VSOUT1} constant)	0 < I_{VSOUT1} < 100 mA, 8 V < VBATP < 19 V	–25		25	mV
5.8	$LdReg_{VSOUT1}$	Load regulation (VSIN constant)	0 < I_{VSOUT1} < 100 mA, 8 V < VBATP < 19 V	–35		35	mV
5.9	$TmpCo_{VSOUT1}$	Temperature drift	Normalized to 25°C value	–0.5%		0.5%	
5.11	$VSOUT1_{SH}$	Output short circuit voltage range		–2		40	V
5.12	$–I_{VSIN}$	Output reverse current	VSOUT1 = 14 V and VBATP = 0 V, regulator switched off			20	mA
5.13	$Tprot_{VSOUT1}$	Temperature protection threshold	Protection of Sensor Supply. Only VSOUT1 switch-off	175		210	°C
		Hysteresis		10		20	
5.14	I_{VSOUT1_limit}	Current-limit		100		500	mA
Voltage Monitoring							
6.1	VBATP_UVoff	VBATP level for switching off VDDx		4.2		4.5	V
6.2	VBATP_UVon	VBATP level for switching on VDDx		5.4		5.8	V
6.3	$VBATP\_UV_{hys}$	Undervoltage hysteresis		1.1		1.4	V
6.4	$VBATP\_OV_{rise}$	VBATP level for setting VBAT_OV flag	Brings device into RESET state and sets flag in SPI	34.7		36.7	V
6.5	$VBATP\_OV_{fall}$	VBATP level for clearing VBAT_OV flag	Clears flag in SPI	34.4		36.3	V

Electrical Characteristics *(continued)*

Over operating ambient temperature T_A = –40°C to the maximum-operating junction temperature T_J = 150°C, and recommended operating VBATP range (see R1.2 in Section 4.3) (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.8	VDD5_UV	VDD5 undervoltage level		4.5		4.85	V
		Hysteresis			140		mV
6.9	$VDD5\_UV_{head}$	VDD5 undervoltage headroom (VDD5act – VDD5_UVact)		200			mV
6.10	VDD5_OV	VDD5 overvoltage level		5.2		5.45	V
		Hysteresis			140		mV
6.11	$VDD5\_OV_{head}$	VDD5 overvoltage headroom (VDD5_OVact – VDD5act)		200			mV
6.12	VDD3/5_UV	VDD3/5 undervoltage level	3.3-V setting	3		3.17	V
			5-V setting	4.5		4.85	
		Hysteresis	3.3-V setting		100		mV
			5-V setting		140		
6.13	VDD3/5_UVhead	VDD3/5 undervoltage headroom (VDD3/5act – VDD3/5_UVact)	3.3-V setting	170			mV
			5-V setting	200			
6.14	VDD3/5_OV	VDD5_3 overvoltage level	3.3-V setting	3.43		3.6	V
			5-V setting	5.2		5.5	
		Hysteresis	3.3-V setting		100		mV
			5-V setting		140		
6.15	VDD3/5_UVhead	VDD3/5 undervoltage headroom (VDD3/5_OVact – VDD3/5act)	3.3-V setting	170			mV
			5-V setting	200			
6.16	VDD1_UV	VDD1 undervoltage level	Sensed on VDD1_SENSE pin. Relative thresholds are with respect to nominal 800-mV VDD1SENSE (Pos 4.2)	0.94		0.98	VDD1
		Hysteresis			10		mV
6.17	VDD1_OV	VDD1 overvoltage level	Sensed on VDD1_SENSE pin. Relative thresholds are with respect to nominal 800-mV VDD1SENSE (Pos 4.2)	1.03		1.06	VDD1
		Hysteresis			9		mV
6.19	VSOUT1_UV	VSOUT1 undervoltage level	Sensed on VSFB1 pin. Relative thresholds are: • for non-tracking mode with respect to nominal 2.5-V VSFB1 (Pos 5.3) • for tracking mode with respect to voltage applied on VTRACK1 pin. • in tracking mode, VSOUT1_UV comparator output is valid for VTRACK1 DC condition.	0.88		0.94	VSOUT 1
		Hysteresis			23		mV
6.20	VSOUT1_OV	VSOUT1 overvoltage level	Sensed on VSFB1 pin. Relative thresholds are: • for non-tracking mode with respect to nominal 2.5-V VSFB1 (Pos 5.3) • for tracking mode with respect to voltage applied on VTRACK1 pin. • in tracking mode, VSOUT1_OV comparator output is valid for VTRACK1 DC condition.	1.06		1.12	VSOUT 1
		Hysteresis			23		mV
6.22	VDD6_UV	VDD6 undervoltage level	Information in SPI register only	5.2		5.4	V
		Hysteresis			115		mV
6.23	VDD6_OV	VDD6 overvoltage level	Information in SPI register only	7.8		8.2	V
		Hysteresis			115		mV
IGNITION and CAN WAKE-UP							
7.1	IGN_WUP	IGN wake-up threshold		2		3	V

Electrical Characteristics *(continued)*

Over operating ambient temperature T_A = –40°C to the maximum-operating junction temperature T_J = 150°C, and recommended operating VBATP range (see R1.2 in Section 4.3) (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.2	CAN_WUP	CAN wake-up threshold		2		3	V
7.3	WUP_hyst	Wake-up hysteresis		50		200	mV
7.4	I_IGN	IGN pin forward leakage current	IGN pin at 40 V			50	µA
7.5	I_IGN_rev	IGN current at –7 V				–1	mA
7.7	I_CANWU	CANWU pin forward leakage current	CANWU pin at 40 V			50	µA
7.8	I_CAN_rev	CAN current at –0.3 V				–1	mA
Charge Pump							
AN	C_{pump}	Pumping capacitor			10		nF
AN	C_{store}	Storage capacitor			100		nF
8.1	VCP_{on}	VCP output voltage in on-state	VBATP > 5.8 V	VBATP + 4		VBATP + 15	V
8.2	I_{CP}	External load	Load coming from R_{GS} of Reverse Battery Protection			100	µA
8.3	f_{CP}	Charge-pump switching frequency		225	250	275	kHz
Reset and Enable Outputs							
9.1	$V_{NRES\_ENDRV\_L}$	NRES / ENDRV low output level	With external 5-mA open-drain current			0.2	V
9.2	$R_{NRES\_ENDRV\_PULLUP}$	NRES / ENDRV internal pullup resistance		3		6	kΩ
9.2a	$R_{DS(on)\_ENDRV\_NRES}$	$R_{DS(on)}$ NRES/ENDRV pulldown transistor				40	Ω
9.3	R_{RSTEXT}	Value of external reset extension resistor	In case of open-connect, device stays in RESET state.	0	22		kΩ
9.5	$V_{ENDRV\_NRES\_TH}$	ENDRV and NRES input readback *logic 1* threshold	Read-back muxed to DIAG_OUT pin	350	400	450	mV
Digital Input / Output							
10.1	V_{DIGIN_HIGH}	Digital input, high level(4)	Input buffers using internal DVDD supply	2			V
10.2	V_{DIGIN_LOW}	Digital input, low level(4)	Input buffers using internal DVDD supply			0.8	V
10.3	V_{DIGIN_HYST}	Digital input hysteresis(4)	Input buffers using internal DVDD supply	0.1			V
10.4	$R_{DIAGOUT\_AMUX}$	Output resistance at DIAG_OUT pin in AMUX mode	BG1 selected on AMUX, < 200 nA current in or out of DIAG_OUT pin			15	kΩ
10.5	V_{DIGOUT_HIGH}	Digital output, high level(5)	I_{OUT} = –2 mA (out of pin)	VDDIO – 0.2			V
10.6	V_{DIGOUT_LOW}	Digital output, low level(5)	I_{OUT} = 2 mA (into pin)			0.2	V
Serial Peripheral Interface							
13.12	R_{PULL_UP}	Internal pullup resistor on NCS input pin		40	70	100	kΩ
13.13	R_{PULL_DOWN}	Internal pulldown resistor on SDI and SCLK input pins		40	70	100	kΩ

(4) For pins NCS, SDI, SCLK, ERROR/WDI
(5) For pins SDO and DIAG_OUT in DMUX mode

4.6 Timing Requirements

Over operating ambient temperature T_A = –40°C to the maximum-operating junction temperature T_J = 150°C, and recommended operating VBATP range (see R1.2 in the Section 4.3) (unless otherwise noted)

POS				MIN	NOM	MAX	UNIT
VDD5 – LDO With Internal FET							
2.12	$t_{delayVDD5}$	VDD5 voltage stabilization delay	Maximum delay between rising edge on CANWU pin until VDD5 reaches the end-value within 2%			2.5	ms
VDD3/5 – LDO With Internal FET							
3.12	$t_{VDD3/5}$	VDD3/5 voltage stabilization delay	Maximum delay after CAN wake-up for VDD3/5 output to settle			2.5	ms
VDD1 – LDO With External FET							
4.15	$t_{delayVDD1}$	VDD1 voltage stabilization delay	Maximum delay after CAN wake-up for VDD1 output to settle			2.5	ms
Voltage Monitoring							
6.7	$VBATP_{\_deglitch}$	VBATP undervoltage and overvoltage monitor deglitch time	240 µs for VBAT-UV deglitch and 260 µs for VBAT-OV deglitch	200	240	280	µs
6.18	VDDx_deglitch	VDDx undervoltage and overvoltage monitor deglitch time		10		40	µs
6.21	VSOUT1_deglitch	VSOUT1 undervoltage and overvoltage monitor deglitch time		10		40	µs
IGNITION and CAN WAKE-UP							
7.6	IGN_deg	IGN deglitch filter time		7.5		22	ms
7.9	CAN_deg	CAN deglitch filter time		100		350	µs
Reset and Enable Outputs							
9.4	$t_{RSTEXT(22k\Omega)}$	Reset extension delay	22 kΩ	4.05	4.5	4.95	ms
9.4a	$t_{RSTEXT(0k\Omega)}$		0 kΩ	0.98	1.4	1.89	ms
Internal System Clock							
11.1	f_{Sysclk}	System clock frequency	Also used for watchdog timer	3.8	4	4.2	MHz
Window Watchdog							
12.1	$t_{ERROR\_WDI\_deglitch}$	Deglitch time on ERROR/WDI pin for MCU error signal monitor		14.25	15	16.25	µs
12.2	t_{WD_pulse}	Deglitch time on ERROR/WDI pin for watchdog-trigger input signal		28	30	32	µs
Serial Peripheral Interface Timing(1)							
13.1	f_{SPI}	SPI clock (SCLK) frequency	VDDIO = 3.3 V			5(2)	MHz
			VDDIO = 5 V			6	
13.2	t_{SPI}	SPI clock period	VDDIO = 3.3 V	200			ns
			VDDIO = 5 V	167			
13.3	t_{high}	High time: SCLK logic high duration	See Figure 4-2	45			ns
13.4	t_{low}	Low time: SCLK logic low duration		45			ns
13.5	t_{sucs}	Setup time NCS: time between falling edge of NCS and rising edge of SCLK		45			ns
13.7	t_{susi}	Setup time at SDI: setup time of SDI before the falling edge of SCLK		15			ns
13.9	t_{hcs}	Hold time: time between the falling edge of SCLK and rising edge of NCS		45			ns
13.10	t_{hlcs}	SPI transfer inactive time (time between two transfers) during which NCS must remain high		788			ns

(1) Capacitance at C_{SDO} = 100 pF
(2) MAX SPI Clock tolerance is ±10%

4.7 Switching Characteristics

Over operating ambient temperature T_A = –40°C to the maximum-operating junction temperature T_J = 150°C, and recommended operating VBATP range (see R1.2 in Section 4.3) (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Serial Peripheral Interface Timing(1)							
13.6	t_{d1}	Delay time: time delay from falling edge of NCS to SDO transitioning from tri-state to 0	See Figure 4-2			53.3	ns
13.8	t_{d2}	Delay time: time delay from rising edge of SCLK to data valid at SDO		0		85.7	ns
13.11	t_{tri}	Tristate delay time: time between rising edge of NCS and SDO in tri-state				53.3	ns

(1) Capacitance at C_{SDO} = 100 pF

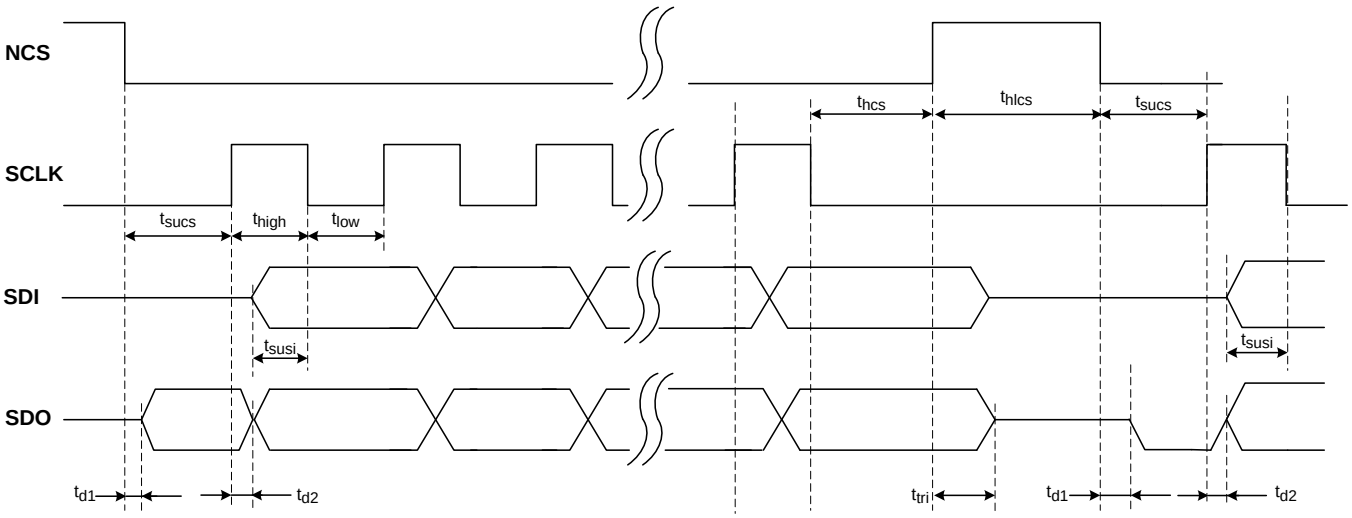


Figure 4-2. SPI Timing Parameters

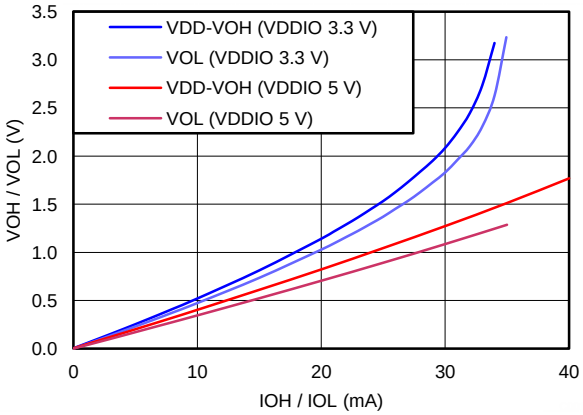


Figure 4-3. SPI SDO Buffer Source/Sink Current

4.8 Typical Characteristics

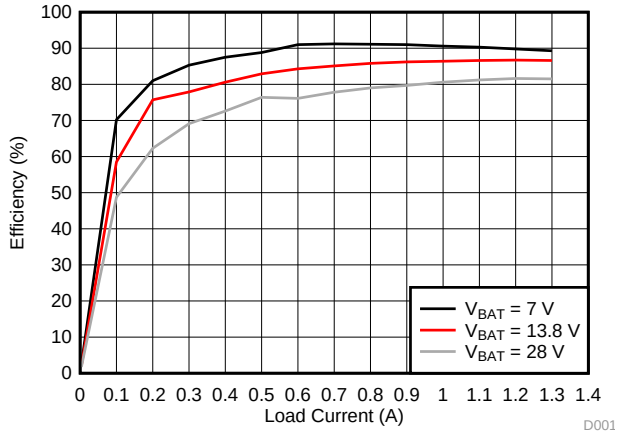


Figure 4-4. VDD6 BUCK Efficiency

5 Detailed Description

5.1 Overview

The device integrates an asynchronous-buck switch-mode power-supply converter with an internal FET that converts the input battery voltage to a 6-V preregulator output. This 6 V supplies the other regulators.

A fixed 5-V linear regulator with an internal FET is integrated to be used as, for example, a CAN supply. A second linear regulator, also with an internal FET, regulates the 6 V to a selectable 5-V or 3.3-V MCU I/O voltage.

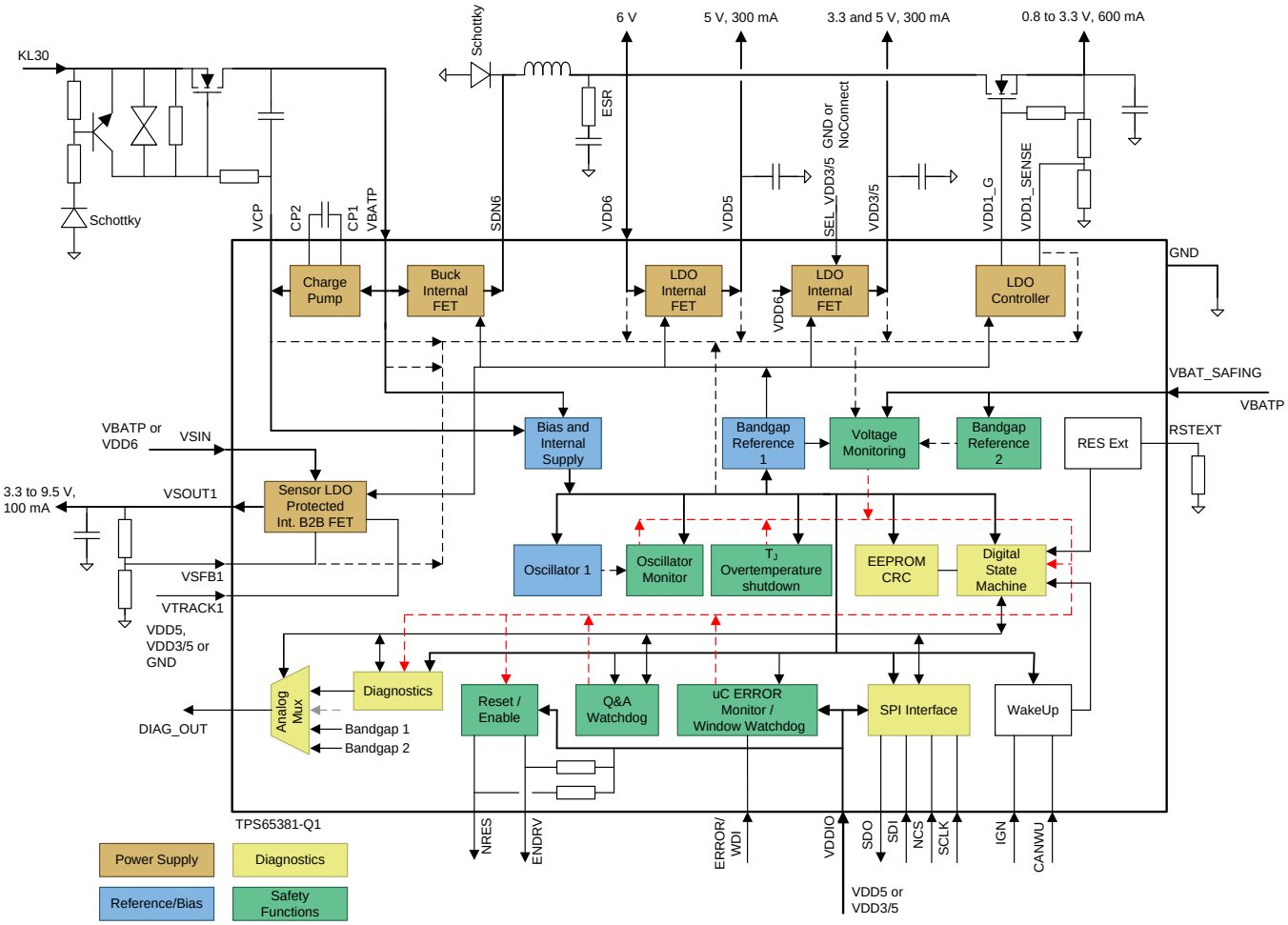
A linear regulator controller with an external FET and resistor divider regulates the 6 V to an externally adjustable core voltage of between 0.8 V and 3.3 V.

A linear regulator with two different modes of operation (tracking mode and non-tracking mode), with short-to-ground and short-to-battery protection and adjustable voltage between 3.3V and 9.5V can be used as a supply for external sensor.

The device monitors undervoltage and overvoltage on all regulator outputs, battery voltage, and internal supply rails. A second band-gap reference, independent from the main band-gap reference used for regulation circuit, is used for the undervoltage and overvoltage monitoring. In addition, regulator current-limits and temperature protections are implemented

The device supports wake-up from IGNITION or wake-up from the CAN transceiver.

5.2 Functional Block Diagram



5.3 Feature Description

5.3.1 VDD6 Buck Switch-Mode Power Supply

The purpose of the VDD6 buck switch-mode power supply is to reduce the power dissipation inside the IC. The VDD6 pin converts the ingoing power for the VDD5, VDD3/5, VDD1, and VSOUT1 pins from the battery-voltage domain to the 6-V voltage domain. Therefore the VDD6 pin is intended for use as a preregulator only; the output voltage is less accurate compared to the VDD5, VDD3/5, VDD1, and VSOUT1 pins. The VDD6 output-current capability is dimensioned to supply the VDD5, VDD3/5, VDD1, and VSOUT1 pins at their respective maximum output currents.

This switch-mode power supply (SMPS) operates with fixed-frequency adaptive on-time control pulse-width modulation (PWM). The control loop of the SMPS is based on a hysteretic comparator. The internal N-channel MOSFET is turned on at the beginning of each cycle when the output voltage on the VDD6 pin is below the PWM comparator threshold. This MOSFET is turned off when the hysteretic PWM comparator resets the latch. When this internal MOSFET is turned OFF, the external Schottky diode recirculates the energy stored in the inductor for the remainder of the switching period. In order to preserve sufficient headroom for the VDD5 regulator at low battery voltage, the VDD6 regulator enters dropout mode for a battery voltage below 7 V.

The internal MOSFET is protected from excess power dissipation with a current-limit circuit and junction-overtemperature protection shared with the VDD3/5 pin. In case of an overtemperature condition in the VDD6 pin detected by the VDD3/5 overtemperature protection, the TPS65381-Q1 device enters the STANDBY state (all regulators switched off).

Because the control loop of the VDD6 SMPS is based on a hysteretic comparator, the output effective capacitance and effective series resistance (ESR) must be considered. The effective capacitance at the operating voltage (6-V DC), temperature range and lifetime of the capacitors must meet the output capacitance range for VDD6. The capacitor supplier should provide the necessary derating data to calculate the effective capacitance. The hysteretic comparator also requires a specified ESR to ensure balanced operation. Typically low-ESR ceramic capacitors are used for the output so an external resistor is required to bring the total ESR into the specified ESR range for VDD6. A general guideline to achieve balanced operation is $R_{ESR} = L / (15 \times C_{Effective})$. Using a higher effective output capacitance allows for a lower ESR which leads to lower voltage ripple. The inductance influences the system where using a lower inductance value allows for lower ESR, however the peak current will be higher.

5.3.2 VDD5 Linear Regulator

The VDD5 pin is a regulated supply of 5 V ±2% overtemperature and battery supply range. A low-ESR ceramic capacitor is required for loop stabilization. This capacitor must be placed close to the pin of the IC. This output is protected against shorts to ground by a current-limit. This output also limits output-voltage overshoot during power up and during line or load transients.

On an initial IGN or CANWU power cycle, the soft-start circuit on this regulator is initiated which is typically in the 1-ms to 2-ms range. This output can require a larger output capacitor to ensure that during load transients the output does not drop below the required regulation specifications.

The internal MOSFET is protected from excess power dissipation with junction-overtemperature protection. In case of an overtemperature condition in the VDD5 pin, only the VDD5 regulator switches off by clearing bit D4 in the SENS_CTRL register. In order to re-enable the VDD5 pin, bit D4 in the SENS_CTRL register must be set again.

5.3.3 VDD3/5 Linear Regulator

The VDD3/5 pin is a regulated supply of 3.3 V or 5 V ±2% overtemperature and battery supply range. The output voltage level is selected with the SEL_VDD3/5 pin (open pin selects 3.3 V, grounded pin selects 5 V). The state of this selection pin is sampled and latched directly at the first initial IGN or CANWU power cycle. When latched, any change in the state of this selection pin after the first initial IGN or CANWU power cycle does not change the initially selected state of the VDD3/5 regulator.

A low-ESR ceramic capacitor is required for loop stabilization. This capacitor must be placed close to the pin of the IC. This output is protected against shorts to ground by a current-limit. This output also limits output-voltage overshoot during power up or during line or load transients.

On an initial IGN or CANWU power cycle, the soft-start circuit on this regulator is initiated which is typically in the 1-ms to 2-ms range. This output may require a larger output capacitor to ensure that during load transients the output does NOT drop below the required regulation specifications.

The internal MOSFET is protected from excess power dissipation with a current-limit circuit and junction overtemperature protection. In case of an over-temperature in the VDD3/5 pin, the TPS65381-Q1 device enters STANDBY state (all regulators switched-off).

5.3.4 VDD1 Linear Regulator

The VDD1 pin is an adjustable supply between 0.8 V and 3.3 V ±2% over temperature and battery supply range.

In order to reduce on-chip power consumption, an external power NMOS is used. The regulation loop and the command gate drive are integrated. TI recommends to apply a resistor in the range of 100 kΩ to 1 MΩ between the gate and source of the external power NMOS. The VDD1 gate output is limited to prevent gate-source overvoltage stress during power up or during line or load transients.

On an initial IGN or CANWU power cycle, the soft-start circuit on this regulator is initiated which is typically in the 1-ms to 2-ms range. This soft-start is meant to prevent any voltage overshoot at start-up. The VDD1 output may require larger output capacitor to ensure that during load transients the output does not drop below the required regulation specifications.

The VDD1 LDO has no current-limit and no overtemperature protection for the external NMOS FET. Therefore, supplying the VDD1 pin from the VDD6 pin is recommended (see). In this way, the VDD6 pin current-limit acts as current-limit for the VDD1 pin and the power dissipation is limited as well. In order to avoid damage in the external NMOS FET, selecting the current rating of the VDD1 pin well above the maximum-specified VDD6 current-limit is recommended.

If the VDD1 regulator is not being used, leave the VDD1_G and VDD1_SENSE pins open. An internal pullup device on the VDD1_SENSE pin detects the open connection and pulls up the VDD1_SENSE pin. This forces the regulation loop to bring the VDD1_G output down. This mechanism also masks the VDD1_OV flag in VMON_STAT2 register and thus ENDRV pin action from a VDD1 OV condition is also masked. These actions are equivalent to clearing the nMASK_VDD1_UV_OV bit in the DEV_CFG1 register to 0. This internal pullup device on the VDD1_SENSE pin also prevents a real VDD1 overvoltage on the MCU core supply in case of an open connection to the VDD1_SENSE pin, as it brings the VDD1_G pin down. Therefore in this situation, the VDD1 output voltage is 0 V.

By default, VDD1 monitoring is disabled. If the VDD1 pin is used in the application, TI recommends to set the nMASK_VDD1_UV_OV bit in the DEV_CFG1 register to 1 when the device is in DIAGNOSTIC state. This setting enables driving and extending the reset to the external MCU when VDD1 under-voltage is detected.

5.3.5 VSOUT1 Linear Regulator

The VSOUT1 pin is a regulated supply with two separate modes: tracking mode and non-tracking mode. The mode selection occurs with the VTRACK1 pin. When the voltage applied on the VTRACK1 pin is above 1.2 V, the VSOUT1 pin is in tracking mode. When the VTRACK1 pin is shorted to ground, the VSOUT1 pin is in non-tracking mode. This mode selection occurs during the first ramp-up of the VDDx rails, and is latched after the first VDDx ramp-up is completed. Therefore, after completion of the VDDx ramp-up, any change in the VSOUT1 pin no longer affects the selected tracking or non-tracking mode.

In tracking mode, the VSOUT1 pin tracks the input reference voltage on the VTRACK1 pin with a gain factor determined by the external resistive divider. The tracking offset between the VTRACK1 and VSFB1 pins is ±35 mV over temperature and battery supply range. This mode allows, for instance, the VSOUT1 pin to be 5 V while tracking the VDD3 (3.3-V) supply. In unity-gain feedback, the VSOUT1 pin can directly follow the VDD5 pin or the VDD3 pin.

In non-tracking mode, the VSOUT1 output voltage is proportional to a fixed reference voltage of 2.5 V at the VSFB1 pin, with a gain factor determined by the external resistive divider. This mode allows the VSOUT1 pin to be any factor of the internal reference voltage.

Both in tracking and non-tracking mode, the VSOUT1 output voltage must 3.3 V or higher. The VSOUT1 pin can track the VDD3/5 pin in 3.3-V setting within the specified limits.

VSOUT1 has a separate input supply to reduce the internal power dissipation. For an output voltage of 3.3 V or 5 V, for instance, VDD6 can be used as the input supply. For an output voltage of greater than 5 V, The VBATP pin can be used as the input supply. Here, the maximum power dissipation for the internal FET must not exceed 0.6 W to avoid thermal shutdown.

A low-ESR ceramic capacitor is required for loop stabilization; this capacitor must be placed close to the pin of the IC. This output is intended for going outside the ECU and therefore is protected against shorts to external chassis ground by a current-limit. Furthermore, in case of output shorted to battery voltage, any potential reverse current going back inside the ECU is blocked, hence preventing any unintended supplying of the ECU by this VSOUT1 output. This regulator also limits output-voltage overshoot during power up or during line or load transients.

The VSOUT1 pin is disabled by default on start-up. After the NRES pin release, the MCU can enable the VSOUT1 pin through a SPI command by setting bit D0 in the SENS_CTRL register. After this SPI command, the soft-start circuit on this regulator is initiated which is typically in the 1-ms to 2-ms range. This output may require a larger output capacitor to ensure that during load transients the output does NOT drop below the required regulation specifications. Regardless of tracking or non-tracking mode, the VSFB1 pin is ramped to the desired value after completion of the soft start.

The internal MOSFET is protected from excess power dissipation with a current-limit circuit and junction-overtemperature protection. In case of an overtemperature condition in the VSOUT1 pin, only the VSOUT1 regulator is switched off by clearing bit 0 in the SENS_CTRL register. In order to re-enable the VSOUT1 pin, first bit 2 in the SAFETY_STAT 1 register must be cleared on read-out, and afterwards bit 0 in the SENS_CTRL register must be set again.

The VSOUT1 pin can be observed at an ADC input of the MCU through the DIAG_OUT pin (see Section 5.4.1.8) which allows the detection of a short to any other supply prior to enabling the VSOUT1 LDO.

5.3.6 Charge Pump

The charge pump is configured to supply an overdrive voltage of typically 12 V to the supply voltage. This overdrive voltage is required for driving the gate voltages of the internal NMOS-FETs of the VDDx and VSOUT1 supply rails. Furthermore, this overdrive voltage can drive the gate of an external NMOS power FET acting as reverse-battery protection. Such reverse-battery protection allows for lower minimum-battery-voltage operation compared to a traditional reverse-battery blocking diode. If such reverse battery protection is used, a series resistance of about 10 kΩ must be connected between the VCP pin and the gate of the NMOS power FET (see). This series resistance is required to limit any current out of the VCP pin when the gate of the NMOS power FET is driven to negative voltage, because the absolute-maximum rating of the VCP pin is limited to –0.3 V because of a parasitic reverse diode to the substrate, that is, ground.

The charge pump requires two external capacitors, one bucket capacitor and one buffer capacitor. In order to have sufficient overdrive voltage out of the charge pump even at low battery voltage, the external load current on the VCP pin must be less than 100 µA.

5.3.7 Wake-Up

The TPS65381-Q1 device has two wake-up pins: IGN and CANWU. Both pins have a wake-up threshold level between 2 V and 3 V, and a hysteresis between 50 mV and 200 mV.

The IGN wake-up pin is level-sensitive and has a deglitch (filter) time between 7.5 ms and 22 ms. The TPS65381-Q1 device provides a power-latch function (POST_RUN) for this IGN pin, allowing the MCU to decide when to power down the TPS65381-Q1 device through SPI command. For this, the MCU must set the IGN power-latch bit 4 (IGN_PWRL) in the SPI SAFETY_FUNC_CFG register, and read the unlatched status of the deglitched (filtered) IGN pin on theSPI register, DEV_STAT, bit 0 (IGN). To enter the STANDBY state, the MCU must clear the IGN_PWRL bit. For this, the TPS65381-Q1 device must be in DIAGNOSTIC state because this SPI register is only writable in DIAGNOSTIC state. The IGN_PWRL bit is also cleared after a detected CANWU wake-up event. Furthermore, the TPS65381-Q1 device provides an optional transition to the RESET state after a detected IGN wake-up during the POST_RUN (see Figure 5-2).

The CANWU pin is level sensitive and has a minimum 350-µs deglitch (filter) time. The deglitched (filtered) CANWU wake-up signal is latched, allowing the MCU to decide when to power down the TPS65381-Q1 device through SPI command WR_CAN_STBY.

Both the IGN and CANWU pins are high voltage pins. If the pins are connected to lines with transients, the application should provide proper filtering and protection to ensure the pins stay within the specified voltage range.

5.3.8 Reset Extension

During a power-up event, the TPS65381-Q1 device releases the reset to the external MCU through the NRES pin with a certain delay time (reset extension time) after the VDD3/5 and VDD1 pins have crossed the respective undervoltage thresholds.

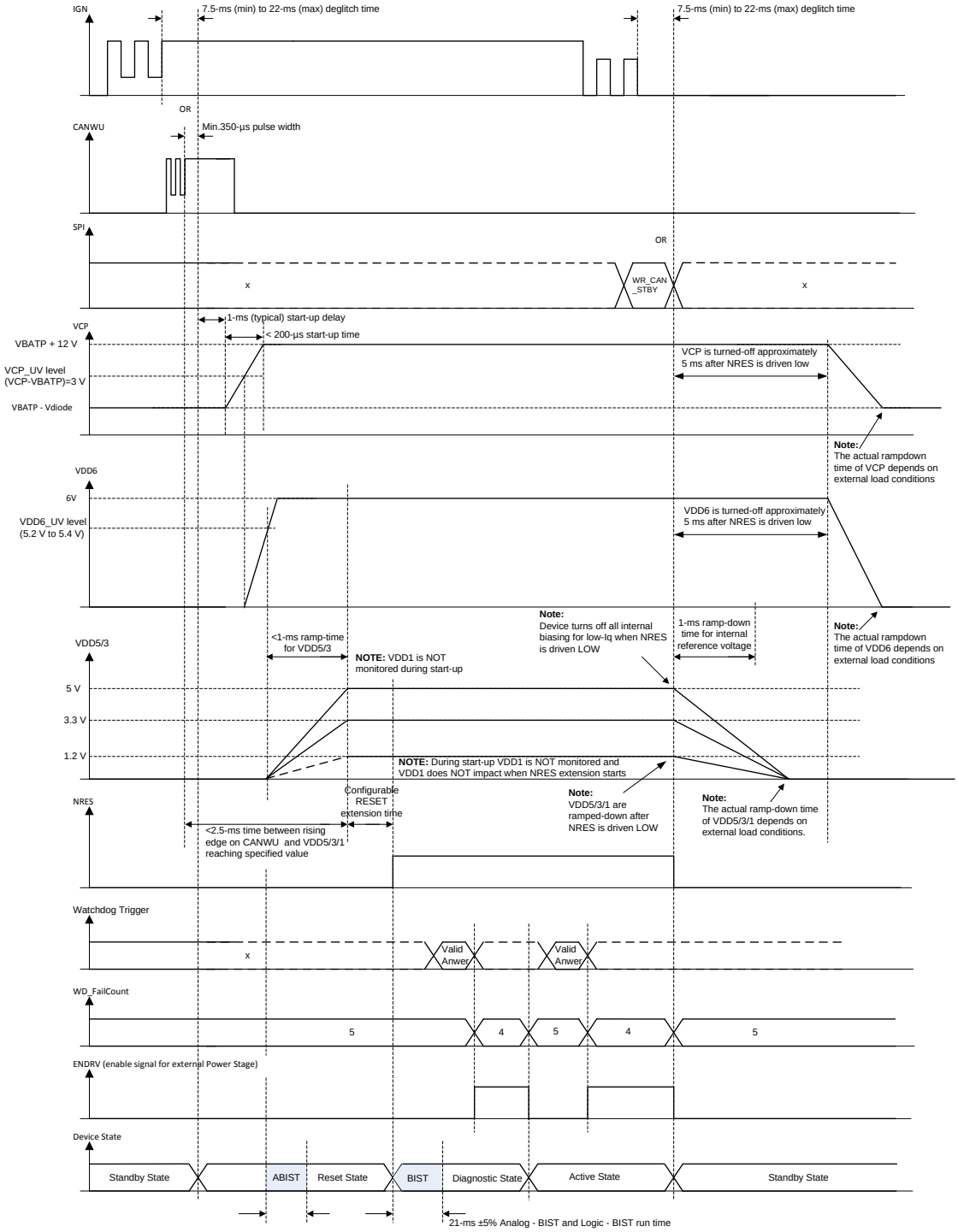
By default, VDD1 monitoring is disabled. If VDD1 is used in the application, TI recommends to set the nMASK_VDD1_UV_OV bit in the DEV_CFG1 register to 1 when the device is in DIAGNOSTIC state. This setting enables driving and extending the reset to the external MCU when VDD1 under voltage is detected.

This reset extension time is externally configurable with a resistor between the RESEXT pin and ground. When shorting this RESEXT pin to ground, the minimum reset extension time is typically 1.4 ms. For a 22-kΩ external resistor, the typical reset extension time is 4.5 ms.

5.4 Device Functional Modes

5.4.1 Power-Up and Power-Down Behavior

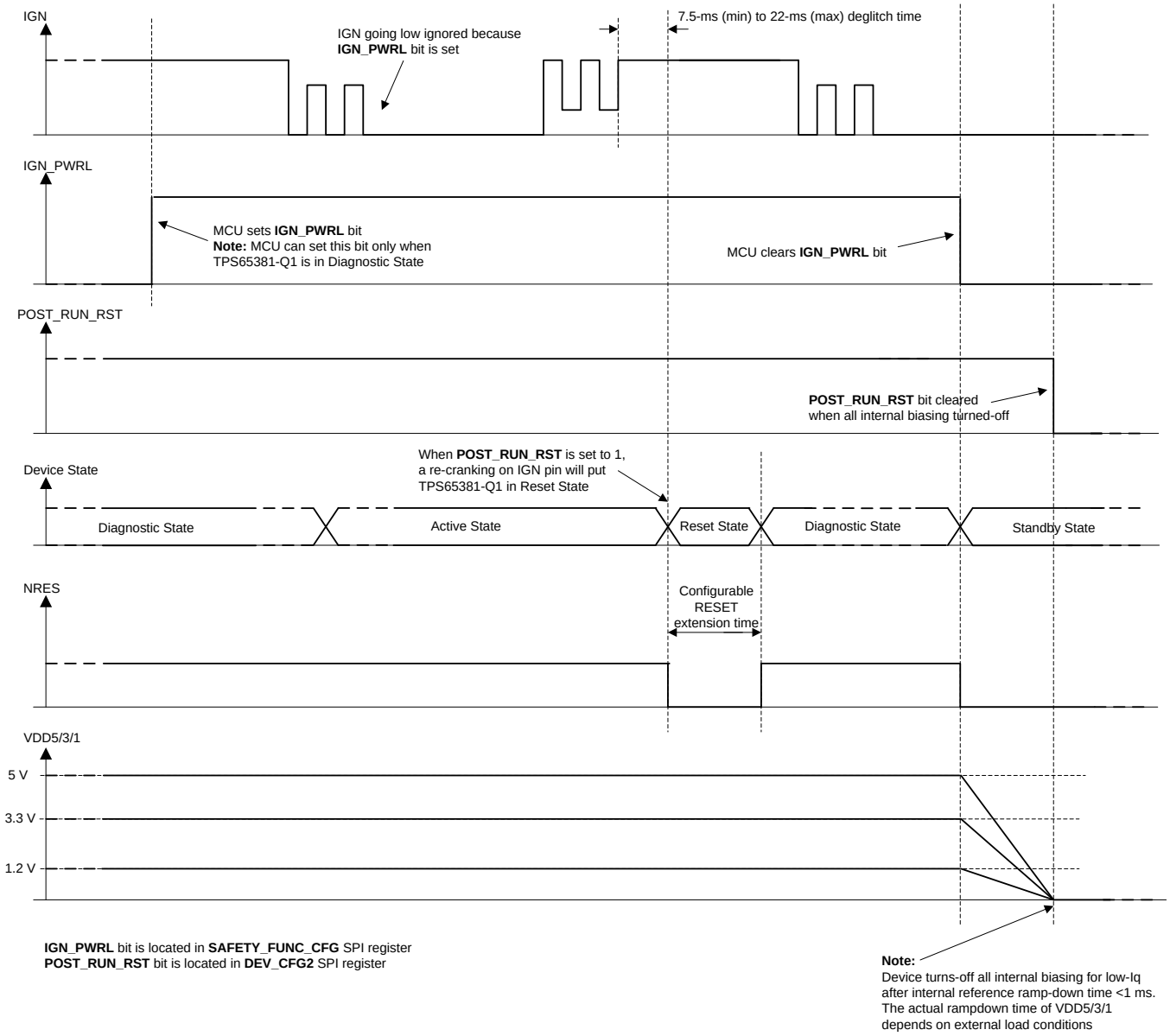
Figure 5-1 shows the power-up and power-down behavior.



(1) During a power-up event, the Analog-BIST begins automatically after the VDD6 rail ramps above the UV threshold. If Analog-BIST fails device enters SAFE state after RESET state.

(2) If the MCU boots faster than BIST run-time, the TPS65381-Q1 device may not be able to respond to MCU SPI communication. If the Analog-BIST, Logic-BIST, or both fail, the device enters SAFE state.

Figure 5-1. Power-Up and Power-Down Behavior



(1) Under slow VBAT ramp-down and when the VDD3/5 rail is configured as a 5-V rail, the NRES output can be pulled low when VBAT is at approximately 6.3 V. This occurs because of an undervoltage transient on VDD3/5 rail.

(2) Under slow VBAT ramp-up and when the VDD3/5 rail is configured as a 5-V rail, the NRES output can be pulled low when VBAT is at approximately 6.6 V. This occurs because of an undervoltage transient on VDD3/5 rail.

(3) Under similar conditions, undervoltage transients are observed on VDD5 and VSOUT rails.

Figure 5-2. IGN Power Latch and POST-RUN Reset

5.4.1.1 Safety Functions and Diagnostics Overview

The IC is intended to be used in automotive safety applications. The following diagnostic blocks are implemented to achieve a better diagnostic coverage or a lower rate of dangerous undetected faults.

- Voltage monitor (VMON)
- Analog built-in self-test (ABIST) diagnostics for safety analog blocks
- Loss of clock monitor (LCMON)
- Junction temperature monitoring for all power supplies with internal FET
- Current-limit for all power supplies
- Analog MUX (AMUX) for externally monitored diagnostics/debug
- Digital MUX (DMUX) for externally monitored diagnostics/debug
- Logic built-in self-test (LBIST) for safety controller functions
- Configurable open and close window or question-answer watchdog timer (WDT)
- MCU error signal monitor (ESM)
- Controlled and protected enable output (ENDRV) for external power stages or peripheral wake-up
- Device configuration register CRC protection
- SPI command decoder with parity check
- SPI data output feedback check
- Reset circuit for initializing external MCU
- EEPROM analog trim content CRC protection
- Device state controller with SAFE state in case of detected error event

5.4.1.2 Voltage Monitor (VMON)

The VBAT supply voltage, all regulator outputs and internally generated voltages are supervised by a voltage monitor module (VMON). An undervoltage or overvoltage condition is indicated by the corresponding VMON register status flag bits:

- VMON flag bit set to 0 when power supply is within specification
- VMON flag bit set to 1 when power supply is outside tolerance band

The monitoring occurs by undervoltage and overvoltage comparators. The reference voltage (BANDGAP_REF2) for the VMON module is independent of the system reference voltage (BANDGAP_REF1) used by the regulators. A glitch-filtering function ensures reliable monitoring without false setting of the VMON status flag bits. The complete VMON block is supplied by a separate supply pin, VBAT_SAFING.

VMON comparator diagnostics are covered by analog built-in self-test (ABIST) executed during device startup and power up or activated with the SPI command by the external MCU SPI request when the device is in the DIAGNOSTIC or ACTIVE state. Each monitored voltage rail is emulated for undervoltage and overvoltage conditions on the corresponding comparator inputs, hence forcing the corresponding comparator to toggle multiple times (in a toggling pattern observed and checked by the ABIST controller). The monitored voltage rails themselves are not affected during this self-test, so no real under voltage or over voltage occurs on any of these rails because of this self-test.

Table 5-1 lists an overview of the performed voltage monitoring. As listed in this table, an overvoltage protection is implemented for some of the internal supply rails.

Table 5-1. Voltage Monitoring Overview(1)

VOLTAGE RAIL	OUTPUT VOLTAGE	CREATED FROM REFERENCE	MONITORING DETECTION THRESHOLDS		MONITORED AGAINST REFERENCE	MONITORED PIN	OV PROTECTION LEVEL	OV PROTECTION REFERENCE	IMPACT ON DEVICE BEHAVIOR	
			UV	OV					UV	OV
Supply Input										
VBAT	N/A	N/A	4.2 to 4.5 V	34.7 to 36.7 V	VMON_BG	VBATP	N/A	N/A	SPI flag VMON_STAT1 D6 STANDBY state NRES = 0, ENDRV = 0	SPI flag VMON_STAT1 D7 RESET state (when MASK_VBATP_OV = 0)
Supply Outputs										
VDD6	6 V ± 10%	MAIN_BG	5.2 to 5.4 V	7.8 to 8.2 V	VMON_BG	VDD6	N/A	N/A	SPI flag VMON_STAT2 D7	SPI flag VMON_STAT2 D7
VDD5	5 V ± 2%	MAIN_BG	4.5 to 4.85 V	5.2 to 5.45 V	VMON_BG	VDD5	N/A	N/A	SPI flag VMON_STAT2 D4	SPI flag VMON_STAT2 D5 ENDRV = 0
VDD3/5 (5 V)	5 V ± 2%	MAIN_BG	4.5 to 4.85 V	5.2 to 5.5 V	VMON_BG	VDD3/5	N/A	N/A	SPI flag VMON_STAT2 D2 RESET state NRES = 0, ENDRV = 0	SPI flag VMON_STAT2 D3 ENDRV = 0
VDD3/5 (3.3 V)	3.3 V ± 2%		3 to 3.17 V	3.43 to 3.6 V						
VDD1	0.8 V to 3.3 V –1% to +2% VDD1_SENSE = 800 mV –1% to +2%	MAIN_BG	0.94 to 0.98 × VDD1	1.03 to 1.06 × VDD1	VMON_BG	VDD1_SENSE	N/A	N/A	SPI flag VMON_STAT2 D0 RESET state NRES = 0, ENDRV = 0 (when nMASK_VDD1_UV_OV=1)	SPI flag VMON_STAT2 D1 ENDRV = 0 (when nMASK_VDD1_UV_OV=1)
VSOUT1 (non-tracking)	3.3 V to 9.5 V ± 2% VDSFB1 = 2.5 V ± 2%	MAIN_BG	0.88 to 0.94 × VSOUT1	1.06 to 1.12 × VSOUT1	MAIN_BG	VSFB1	N/A	N/A	SAFETY_STAT1 D5	SPI flag SAFETY_STAT1 D4
VSOUT1 (tracking)	3.3 V to 9.5 V ± 2% VDSFB1 = VTRACK1 ± 20 mV	VTRACK1			VTRACK1	VSFB1	N/A	N/A		
Internal Supplies										
VCP17	17 V (typ)	MAIN_BG	N/A	21 V (typ)	VMON_BG	N/A	21 V (typ)	VMON_BG	N/A	SPI flag VMON_STAT1 D5 VSOUT1 not operational
VCP12	12 V (typ)	MAIN_BG	7.43 V (typ)	14.2 V (typ)	VMON_BG	N/A	14.2 V (typ)	VMON_BG	SPI flag VMON_STAT1 D3	SPI flag VMON_STAT1 D4 VDD5, VDD3/5 and VDD1 not operational → RESET state NRES = 0, ENDRV = 0
AVDD	6.9 V (typ)	Internal LV Zener	3.6 V (typ)	N/A	Independent local band gap	N/A	< 10.48 V	Internal MV Zener	NPOR → STANDBY state NRES = 0, ENDRV = 0	NPOR → STANDBY state NRES = 0, ENDRV = 0
AVDD_VMON	6.9 V (typ)	Internal LV Zener	3.56 V (typ)	N/A	Independent local band gap	Indirectly monitoring VBAT_SAFING	< 10.48 V	Internal MV Zener	SPI flag VMON_STAT1 D2	NPOR → STANDBY state NRES = 0, ENDRV = 0
DVDD	3 V (typ)	MAIN_BG	2.472 V (typ)	3.501 V (typ)	VMON_BG	N/A	N/A	N/A	NPOR → STANDBY state NRES = 0, ENDRV = 0	NPOR → STANDBY state NRES = 0, ENDRV = 0
Internal References										
MAIN_BG	2.5 V ± 2%	MAIN_BG	2.364 V (typ)	2.617 V (typ)	VMON_BG	N/A	N/A	N/A	SPI flag VMON_STAT1 D0	SPI flag VMON_STAT1 D1
VMON_BG	2.5 V ± 2%	VMON_BG	2.364 V (typ)	2.617 V (typ)	MAIN_BG	N/A	N/A	N/A	SPI flag VMON_STAT1 D1	SPI flag VMON_STAT1 D0

(1) N/A = Not applicable

5.4.1.3 TPS65381-Q1 Internal Error Signals

Table 5-2 lists a useful overview of the TPS65381-Q1 device internal error signals and the impact of the signals on the device behavior.

Table 5-2. Internal Error Signals

DETECTIVE CONDITION (THRESHOLD LEVEL)								DEGLITCH TIME TO SET FLAG (µS)				DEVICE STATE WHEN FLAG IS SET		
DMUX POS. NO.	SIGNAL NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	ELEC. CHAR. NO.	MIN	TYP	MAX	ELEC. CHAR. NO.	NRES	ENDRV	DEVICE STATE
D1.2	AVDD_UVN	AVDD undervoltage comparator output		3.6		V		15		30		LOW	LOW	STAND-BY
D1.3	BG_ERR1	VMON or main bandgap is OFF (set to 1 when VMON bandgap > main bandgap)		Main bandgap = 2.364 (VMON bandgap = 2.477)		V		15		30		Not changed (unless VDD3/5_UV or VDD1_UV detected, causing NRES = LOW)	Not changed (unless VDD3/5_UV or VDD1_UV detected, causing ENDRV = LOW)	Not changed (unless VDD3/5_UV or VDD1_UV detected, causing transition to RESET)
D1.4	BG_ERR2	VMON or main bandgap is OFF (set to 1 when VMON bandgap < main bandgap)		Main bandgap = 2.617 (VMON bandgap = 2.477)		V		15		30		Not changed	Not changed (unless VDD3/5_UV or VDD1_UV detected, causing ENDRV = LOW)	Not changed
D1.5	VCP12_UVN	VCP12 charge pump undervoltage comparator		7.43		V		15		30		Not changed	Not changed	Not changed
D1.6	VCP12_OV	VCP12 charge pump overvoltage comparator		14.2		V		15		30		Not changed	Not changed	Not changed
D1.7	VCP_OV	VCP17 charge pump overvoltage comparator		21		V		15		30		Not changed	Not changed	Not changed
D1.8	VDD6_UVN	VDD6 undervoltage comparator	5.2		5.4	V	6.22	10		40	6.18	Not changed	Not changed	Not changed
D1.9	VDD6_OV	VDD6 overvoltage comparator	7.8		8.2	V	6.23	10		40	6.18	Not changed	Not changed	Not changed
D1.10	VDD5_UVN	VDD5 undervoltage comparator	4.5		4.85	V	6.8	10		40	6.18	Not changed	Not changed	Not changed
D1.11	VDD5_OV	VDD5 overvoltage comparator	5.2		5.45	V	6.10	10		40	6.18	Not changed	LOW	Not changed
D1.12	VDD3/5_UVN	VDD3/5 undervoltage comparator; 3.3-V setting	3		3.17	V	6.12	10		40	6.18	LOW	LOW	RESET
		VDD3/5 undervoltage comparator; 5-V setting	4.5		4.85									
D1.13	VDD3/5_OV	VDD3/5 overvoltage comparator; 3.3-V setting	3.43		3.6	V	6.14	10		40	6.18	Not changed	LOW	Not changed
		VDD3/5 overvoltage comparator; 5-V setting	5.2		5.5									
D1.14	VDD1_UVN	VDD1 undervoltage comparator	0.94		0.98	VDD1	6.16	10		40	6.18	Not changed when nMASK_VDD1_UV_OV = 0 (default config) When nMASK_VDD1_UV_OV = 1: NRES = LOW	Not changed when nMASK_VDD1_UV_OV = 0 (default config) When nMASK_VDD1_UV_OV = 1: ENDRV = LOW	Not changed when nMASK_VDD1_UV_OV = 0 (default config) When nMASK_VDD1_UV_OV = 1: RESET
D1.15	VDD1_OV	VDD1 overvoltage comparator	1.03		1.06	VDD1	6.17	10		40	6.18	Not changed	Not changed (default config) When MASK_VDD1_UV_OV = 1: ENDRV = LOW	Not changed
D1.16	LOCLK	Loss-of-system-clock comparator	0.742		2.64	MHz		0.379		1.346		LOW	LOW	STANDBY

Table 5-2. Internal Error Signals (continued)

DETECTIVE CONDITION (THRESHOLD LEVEL)								DEGLITCH TIME TO SET FLAG (µS)				DEVICE STATE WHEN FLAG IS SET		
DMUX POS. NO.	SIGNAL NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	ELEC. CHAR. NO.	MIN	TYP	MAX	ELEC. CHAR. NO.	NRES	ENDRV	DEVICE STATE
D3.4	CP_OV	Charge pump overvoltage comparator		VBAT + 12		V		N/A	N/A	N/A		Not changed	Not changed	Not changed
D3.5	CP_UVN	Charge pump undervoltage Comparator		VBAT + 6		V		N/A	N/A	N/A		Not changed	Not changed	Not changed
D3.8	CP_DIFF3V	Indicates VCP-VBATP > 3 V		VBAT + 3		V		N/A	N/A	N/A		Not changed	Not changed	Not changed
D3.10	VBAT_UVN	VBAT undervoltage comparator	4.2		4.5	V	6.1		200		6.7	LOW	LOW	STANDBY
D3.11	VBATP_OV	VBAT overvoltage comparator	34.7		36.7	V	6.5		200		6.7	LOW (default config) When MASK_VBATP_OV = 1: NRES unchanged	LOW (default config) When MASK_VBATP_OV = 1: ENDRV unchanged	RESET (default config) When MASK_VBATP_OV = 1: device state unchanged
D3.12	VDD5_OT	VDD5 overtemperature	175		210	°C	3.13	45		60		LOW	LOW	RESET
D3.13	VDD3_5_OT	VDD3/5 overtemperature	175		210	°C	2.13	45		60		LOW	LOW	Device state depends on EN_VDD35_OT bit setting: EN_VDD35_OT = 0 : VDD3/5 disabled -> VDD3/5 UV event -> RESET EN_VDD35_OT = 1 : STAND-BY
D3.14	VSOUT_OT	VSOUT overtemperature	175		210	°C	5.13	45		60		Not changed	Not changed	Not changed
D3.15	VDD5_CL	VDD5 current-limit	350		650	mA	2.14	15		30		Not changed	Not changed	Not changed
D3.16	VDD3_5_CL	VDD3/5 current-limit	350		650	mA	3.14	15		30		Not changed	Not changed	Not changed
D4.2	VSOUT1_ILIM	VSOUT1 current-limit	100		500	mA	5.19	15		30		Not changed	Not changed	Not changed
D4.3	VSOUT1_UVN	VSOUT1 undervoltage comparator	0.88		0.94	VSOUT1	6.19	10		40	6.21	Not changed	Not changed	Not changed
D4.4	VSOUT1_OV	VSOUT1 overvoltage comparator	1.06		1.12	VSOUT1	6.20	10		40	6.21	Not changed	Not changed	Not changed
D4.5	DVDD_UVN	DVDD undervoltage comparator		2.472		V			0			LOW	LOW	STANDBY
D4.6	DVDD_OV	DVDD overvoltage comparator		3.501		V			0			LOW	LOW	STANDBY
D4.8	VS_TRK_MODE	VSOUT1 in track-mode indication		1.2		V	5.3a	N/A	N/A	N/A		Not changed	Not changed	Not changed
D4.9	VMON_TRIM_ERR	VMON trim error	Set when bit-flip in VMON trim registers is detected					15		30		Not changed	Not changed	Not changed

5.4.1.4 Loss-of-Clock Monitor (LCMON)

The clock monitor detects internal oscillator failures including:

- Oscillator clock stuck high or stuck low
- Reduced clock frequency

The clock monitor is enabled during a power-up event after power-on reset is released (driven high). The clock monitor remains active during device normal operation (STANDBY, RESET, DIAGNOSTIC, ACTIVE, and SAFE states). In case of a clock failure:

- The device transitions to the STANDBY state.
- All regulators are disabled.
- The digital core is reinitialized.
- Reset to the external MCU is asserted low.
- The failure condition is latched outside the digital core in the SPI register SAFETY_STAT_4, bit D5

The loss-of-clock monitor has a self-test structure that is activated and monitored by an analog BIST (ABIST). The external MCU can re-check the clock monitor any time when the device is in the DIAGNOSTIC state or ACTIVE state. The enabled diagnostics emulate a clock failure that causes the clock-monitor output to toggle. The clock-monitor toggling pattern is checked by the ABIST, while the external MCU can check that the loss-of-clock status bit is being set during active test. During this self-test, the actual oscillator frequency (4 MHz) is not changed because of this self-test.

5.4.1.5 Analog Built-In-Self-Test (ABIST)

The ABIST is the controller and monitor circuit for performing self-checking diagnostics on critical analog functions:

- VMON undervoltage and overvoltage comparators
- Clock monitor (LCMON)
- EEPROM analog-trim content check (CRC protection)

During the self-test on the VMON undervoltage and over voltage comparators, the monitored voltage rails are left unchanged, so no real undervoltage or overvoltage occurs on any of these rails because of these self-tests. Furthermore, also during the self-check on the clock monitor, the actual oscillator frequency (4 MHz) is not changed because of this self-test.

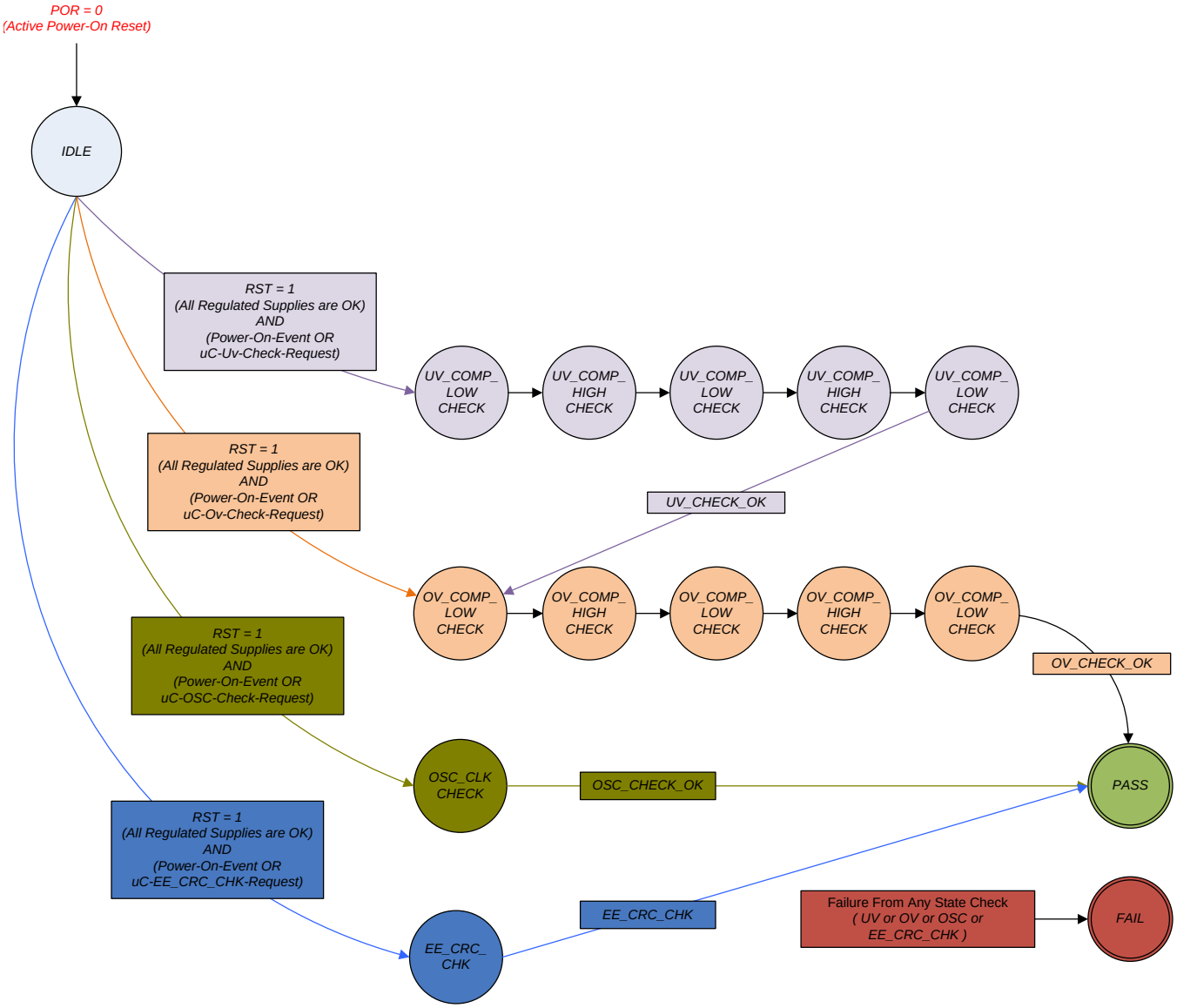


Figure 5-3. Analog BIST Run States

In case of an ABIST failure, the device enters SAFE state without asserting a reset to external MCU, while all ABIST status flag bits remain latched in the digital core. This allows the external MCU to detect the ABIST failure root caused by reading the ABIST status register.

The ABIST is activated with every device power-up event or any transition to RESET state, or by external MCU when the device is in DIAGNOSTIC state (by writing to the SAFETY_BIST_CTL register, note that this register has a SW WRITE PROTECT). During an active ABIST run, the device cannot monitor the state of the regulated supplies, and the ENDRV pin is pulled low. The full ABIST run time is approximately 300 µs. The ABIST can also be performed in ACTIVE state on MCU request, depending on system safety requirements (such as system-fault response time).

A running ABIST is indicated in the ABIST_RUN bit (bit D0) in the SAFETY_STAT_3 register. This bit is set to 1 during the ABIST run and is cleared to 0 when the ABIST is completed.

5.4.1.6 Logic Built-In Self-Test (LBIST)

The logic BIST (LBIST) tests the digital-core safety functions.

- Includes an application controllable logic BIST engine which applies test vectors to the digital core.
- The LBIST engine provides at least 95% stuck-at fault grade to logic blocks under test.
- The LBIST run time is typically 4.2 ms (±5%). After the LBIST, a 16-ms (typical) wait period occurs to fill the digital filters covered by the LBIST. During this time, the ABIST is performed. The total BIST time is approximately 21 ms.
- The LBIST engine has a timeout counter as a fail-safe feature.

The LBIST is activated with every device power-up event, any transition to RESET state, or by external MCU when device is in DIAGNOSTIC state (by writing to the SAFETY_BIST_CTL register, note that this register has a *SW WRITE PROTECT*). The LBIST can also run in ACTIVE state (together with the ABIST), depending on whether system-safety timing requirements can allow the total 21-ms BIST time. During an active LBIST run, the TPS65381-Q1 device cannot monitor the state of regulated supplies, cannot respond to any SPI command and therefore cannot monitor state of MCU through the watchdog timer. During the LBIST run, the ENDRV pin is pulled low and the watchdog fail counter reinitializes to 5. After the LBIST is complete, the post-BIST-reset initializes following functions and registers:

- DEV_STAT
- SAFETY_STAT_2
- SAFETY_STAT_4
- SAFETY_STAT_5
- WD_TOKEN_VALUE
- WD_STATUS
- SAFETY_CHECK_CTRL
- DIAG_CFG_CTRL
- DIAG_MUX_SEL

A running LBIST is indicated in the LBIST_RUN bit (bit D1) in the SAFETY_STAT_3 register. This bit is set to 1 while the LBIST is running, and is cleared to 0 when the LBIST is completed. After the release of the NRES to the MCU, completion of the complete BIST is confirmed by the MCU by reading 0 for both the ABIST and LBIST bits

5.4.1.7 Junction Temperature Monitoring and Current Limiting

Each LDO with an internal power FET has junction temperature monitoring with thermal shutdown protection. In case of thermal shutdown, a regulated supply can enable only after the thermal shutdown condition is removed.

For VSOUT1 supplies, the thermal shutdown disables the regulator until the VSOUT1 overtemperature condition is no longer present.

For the configurable VDD3/5 regulator, a thermal shutdown event disables regulated supplies, and reset to the external MCU (NRES) and the ENDRV pin are asserted low. The VDD6 buck preregulator shares the thermal protection with the VDD3/5 thermal shutdown.

For the VDD5 regulator, thermal shutdown clears the enable bit and places the device into RESET state with a reset to the external MCU (NRES) asserted low, while all other regulators remain enabled. When the VDD5 overtemperature condition is gone, the external MCU must set this enable control bit again to reenable the regulator.

The VDD3/5, VDD5, and VSOUT1 regulators include a current-limit circuit for additional protection against excessive power consumption and thermal overstress. Respective status bits are set in the SAFETY_STAT_1 register when a current-limit is detected on any of these rails.

Table 5-3 lists an overview of the thermal and overcurrent protections on the supply output rails.

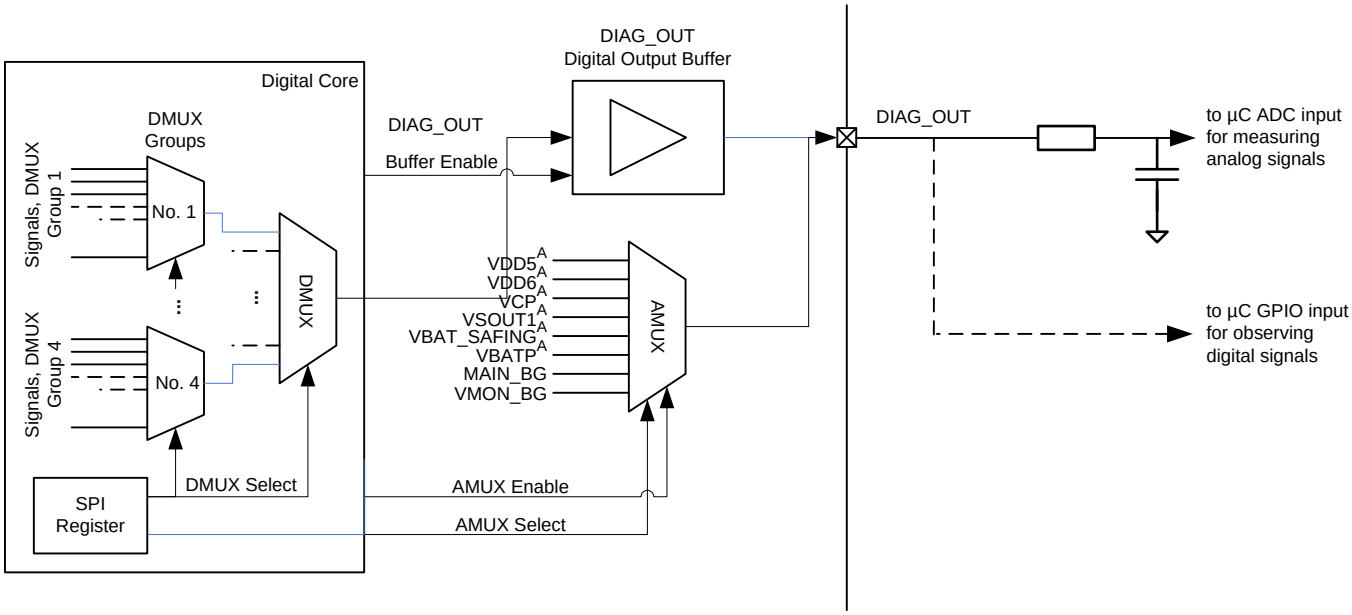
Table 5-3. Thermal and Overcurrent Protect Overview

VOLTAGE RAIL	THERMAL PROTECT		OVERCURRENT PROTECTION	
	THRESHOLD (°C)	IMPACT ON DEVICE BEHAVIOR	CURRENT-LIMIT	IMPACT ON DEVICE BEHAVIOR
VDD6	175 to 210 (shared with VDD3/5)	SPI flag SAFETY_STAT_1 D0 STANDBY state	1.5 to 2.5 A	None
VDD5	175 to 210	SPI flag SAFETY_STAT_1 D1 RESET state Bit D4 in SENS_CTRL register cleared → VDD5 switched off	350 to 650 mA	SPI flag SAFETY_STAT_1 D7
VDD3/5	175 to 210	SPI flag SAFETY_STAT_1 D0 STANDBY state	350 to 650 mA	SPI flag SAFETY_STAT_1 D6
VDD1	None	N/A	None	N/A
VSOUT1	175 to 210	SPI flag SAFETY_STAT_1 D2 VSOUT1 switched off	100 to 500 mA	SPI flag SAFETY_STAT_1 D3

5.4.1.8 Diagnostic Output Pin DIAG_OUT

Analog and digital critical signals, which are not directly connected to the MCU, are switched by a multiplexer to the external DIAG_OUT pin. The programming of the multiplexer is done through the SPI register, DIAG_MUX_SEL. The digital signals are buffered to have sufficient drive capabilities.

This multiplexer facilitates external pin interconnect tests by feeding back the input pin state or feeding back internal module self-test status or safety comparator outputs.



Marked analog signals put out with divider ratio
If the user wants to measure analog signals by µC ADC and observe digital signals by µC GPIO, it must assure that GPIO input stage does not affect µC ADC measurements.
If isolating µC GPIO is not possible within µC, the user must achieve isolation externally.

Figure 5-4. Diagnostic Output Pin, DIAG_OUT

In case the DIAG_OUT pin is connected to a mixed analog or digital input pin of the MCU, TI recommends to configure this MCU input pin and the DIAG_OUT pin simultaneously in accordance with the desired type of signal (analog or digital). The type of signal (analog or digital) on the DIAG_OUT1 pin can be configured with the MUX_CFG bits in the DIAG_CFG_CTRL register. The DIAG_OUT multiplexer can be globally enabled and disabled with bit 7 in the DIAG_CFG_CTRL register. When disabled, the DIAG_OUT pin is in high-ohmic state (tri-stated).

NOTE

When enabling DIAG_OUT MUX while using SPI communication, the SDO pin is not in high impedance while NCS = High and DIAG_OUT MUX is enabled. Software or hardware modification may be needed in the application. For hardware modifications check the SDO threshold level and drive capability if resistors are used to adjust the voltage level of SDO on the SPI bus.

5.4.1.9 Analog MUX (AMUX)

Table 5-4 lists the selectable-analog internal signals on the DIAG_OUT pin. In the DIAG_CFG_CTRL register, the MUX_CFG bits must be set to 10 for the analog MUX mode.

Table 5-4. Analog MUX Selection Table

SIGNAL NUMBER	VOLTAGE RAIL/ SIGNAL NAME	DESCRIPTION	DIVIDE RATIO	VOLTAGE RANGE / ACCURACY(1)	MAXIMUM OUTPUT RESISTANCE (kΩ)	DIAG_MUX_SEL[3:0]
A.1	VDD5	Linear VDD5 regulator output	2 ± 1.5%	2.5 V ±2%	55	0x01
A.2	VDD6	Switch-mode preregulator	3 ± 2.2%	2 V ±5%	140	0x02
A.3	VCP	External charge pump	13.5 ± 2%	0.6 to 4 V	1640	0x04
A.4	VSOUT1	Sensor-supply voltage	4 ± 0.5%	0.825 to 2.375 V	240	0x08
A.5	VBAT_SAFING	Safing battery supply	10 ± 2%	0.4 to 4 V	1755	0x10
A.6	VBAT	Battery supply	10 ± 2%	0.4 to 4 V	1755	0x20
A.7	MAIN_BG	Regulators bandgap reference	1	2.5 V ±2%	15	0x40
A.8	VMON_BG	Voltage-monitor band gap	1	2.5 V ±2%	15	0x80

(1) The given accuracies are without the DC load-current drawn from DIAG_OUT pin. For overall accuracy calculation, the divide ratio accuracy and the drop voltage caused by I_{DIAG_OUT} × Max. Output Resistance must be considered.

In case one of these analog signals comes to a voltage above VDDIO, a clamp becomes active to avoid any voltage level higher than VDDIO on the DIAG_OUT pin.

In order to achieve the fastest stabilization of the signal switched to DIAG_OUT, following the AMUX switching order from A.1 up to A.8 is not recommended.

The recommendation is to switch the order from high to low voltage, starting with A.8. For example: A.8 - A.7 - A.1 - A.2 - A.3 - A.5 - A.6 - A.4.

NOTE

The sensor-supply output voltage (VSOUT1) is 0 V in this example. If VSOUT1 is higher, then the switching order described in the previous example must be changed. In the application, a series resistance of at least 100 kΩ is required on the input capacitor filter of the ADC input of the MCU.

5.4.1.10 Digital MUX (DMUX)

The following tables list the selectable digital internal signals on the DIAG_OUT pin. In the DIAG_CFG_CTRL register, the MUX_CFG bits must be set to 01 for the digital MUX mode.

Most of these signals are internal error signals that influence the device state and behavior of the NRES pin and the ENDRV pin. See Table 5-2 for a more detailed table listing the internal error signals and their impact on the device behavior.

Table 5-5. Digital MUX Selection Table – Group 1

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D1.1	RSV	Reserved, logic 0	000	0000
D1.2	AVDD_UVN	AVDD undervoltage comparator output	000	0001
D1.3	BG_ERR1	VMON or main band gap is OFF	000	0010
D1.4	BG_ERR2	VMON or main band gap is OFF	000	0011
D1.5	VCP12_UVN	VCP12 charge-pump undervoltage comparator	000	0100
D1.6	VCP12_OV	VCP12 charge-pump overvoltage comparator	000	0101
D1.7	VCP17_OV	VCP17 charge-pump overvoltage comparator	000	0110
D1.8	VDD6_UVN	VDD6 undervoltage comparator	000	0111
D1.9	VDD6_OV	VDD6 overvoltage comparator	000	1000
D1.10	VDD5_UVN	VDD5 undervoltage comparator	000	1001
D1.11	VDD5_OV	VDD5 overvoltage comparator	000	1010
D1.12	VDD3/5_UVN	VDD3/5 undervoltage comparator	000	1011
D1.13	VDD3/5_OV	VDD3/5 overvoltage comparator	000	1100
D1.14	VDD1_UVN	VDD1 undervoltage comparator	000	1101
D1.15	VDD1_OV	VDD1 overvoltage comparator	000	1110
D1.16	LOCLK	Loss-of-system-clock comparator	000	1111

Table 5-6. Digital MUX Selection Table – Group 2

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D2.1	RSV	Reserved, logic 0	001	0000
D2.2	SYS_CLK	System clock source	001	0001
D2.3	DFT	Signal reserved for production test	001	0010
D2.4	WDT_CLK	Watchdog clock reference (0.55-ms period time)	001	0011
D2.5	RST_EXT_CLK	Reset extension oscillator output	001	0100
D2.6	T_5US	5-µs time reference	001	0101
D2.7	T_15US	15-µs time reference	001	0110
D2.8	T_40US	40-µs time reference	001	0111
D2.9	T_2MS	2-ms time reference	001	1000
D2.10	UC_ERROR/WDI	External MCU ERROR/WDI input pin	001	1001
D2.11	SPI_NCS	SPI chip-select input pin	001	1010
D2.12	SPI_SDI	SPI slave-data input pin	001	1011
D2.13	SPI_CLK	SPI clock input pin	001	1100
D2.14	SDO_RDBCK	SPI slave-data output-pin readback	001	1101
D2.15	UC_ERROR/WDI	Same signal as 2.10	001	1110
D2.16	NRST_EXT_IN	NRES pin readback (reset to external MCU)	001	1111

Table 5-7. Digital MUX Selection Table – Group 3

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D3.1	RSV	Reserved, logic 0	010	0000
D3.2	DFT	Signal reserved for production test	010	0001
D3.3	DFT	Signal reserved for production test	010	0010
D3.4	CP_OV	Charge-pump overvoltage comparator	010	0011
D3.5	CP_UVN	Charge-pump undervoltage comparator	010	0100
D3.6	CP_PH1	Charge-pump switching phase 1	010	0101
D3.7	CP_PH2	Charge-pump switching phase 2	010	0110
D3.8	CP_DIFF3V	Indicates VCP-VBATP > 3 V	010	0111
D3.9	DFT	Signal reserved for production test	010	1000
D3.10	VBAT_UVN	VBAT undervoltage comparator	010	1001
D3.11	VBATP_OV	VBAT overvoltage comparator	010	1010
D3.12	VDD5_OT	VDD5 overtemperature	010	1011
D3.13	VDD3_5_OT	VDD3/5 overtemperature	010	1100
D3.14	VSOUT_OT	VSOUT overtemperature	010	1101
D3.15	VDD5_CL	VDD5 current-limit	010	1110
D3.16	VDD3_CL	VDD3 current-limit	010	1111

Table 5-8. Digital MUX Selection Table – Group 4

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D4.1	RSV	Reserved, logic 0	011	0000
D4.2	VSOUT_ILIM	VSOUT1 current-limit	011	0001
D4.3	VSOUT_UVN	VSOUT1 undervoltage comparator	011	0010
D4.4	VSOUT_OV	VSOUT1 overvoltage comparator	011	0011
D4.5	DVDD_UVN	DVDD undervoltage comparator	011	0100
D4.6	DVDD_OV	DVDD overvoltage comparator	011	0101
D4.7	RSV	Reserved	011	0110
D4.8	VS_TRK_MODE	VSOUT1 in track-mode indication	011	0111
D4.9	VMON_TRIM_ERR	VMON trim error	011	1000
D4.10–16	RSV	Reserved	011	1001–1111

Table 5-9. Digital MUX Selection Table – Group 5

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D5.1	RSV	Reserved, logic 0	111	0000
D5.2	TI_TEST_MODE	TI production test mode indication	111	0001
D5.3 – 16	DFT	Signal reserved for production test	111	0010–1111

A diagnostic check at the SDO digital-output pin is also possible in DMUX mode. For this diagnostic check, the following sequence is required:

- MUX_CFG[1:0] configuration must be set to 01 for DIGITAL MUX mode
- SPI NCS must be kept HIGH
- The state of SDO is controlled by the SPI_SDO bit (bit D6 in the DIAG_CFG_CTRL register)

During this SDO check at the SDO pin, the DIAG_OUT pin is kept low if no signal from the Digital MUX table is selected.

5.4.1.10.1 Diagnostic MUX Output State (by MUX_OUT bit)

For a diagnostic interconnect check between the DIAG_OUT pin and the MCU analog-digital input pin, the state of the DIAG_OUT pin is controlled with SPI bit MUX_OUT in DIAG_CFG_CTRL register. For using this mode, the MUX_CFG[1:0] bits must be set to 00 in DIAG_CFG_CTRL register.

5.4.1.10.2 MUX Interconnect Check

For performing a diagnostic interconnect check at the digital input pins (ERROR/WDI, NCS, SDI, and SCLK) the MUX_CFG[1:0] bits in the DIAG_CFG_CTRL register must be set to 11. With bits INT_CON[2:0] in the DIAG_CFG_CTRL register, it can be selected which of these digital inputs is multiplexed to the DIAG_OUT pin (see description of DIAG_CFG_CTRL register in Section 5.5.1).

5.4.1.11 Watchdog Timer (WDT)

To monitor proper function of the external MCU, the TPS65381-Q1 device includes a closed-loop digital watchdog. This watchdog requires specific trigger messages to be passed between the MCU and the TPS65381-Q1 device at specific timing intervals to enable operation of the safing path or external power stages through the ENDRV pin. This function is consequently referred to as the watchdog-enabled function. When improper MCU operation is detected, the ENDRV pin is pulled low to disable the safing path or external power stages.

Normal MCU operation is indicated when the MCU periodically sends a watchdog trigger which is received by the watchdog timer within a defined time window. The TPS65381-Q1 device has two different watchdog timer configurations for the external MCU to send the watchdog trigger:

Watchdog trigger input configuration (WDTI Configuration): The MCU sends watchdog triggers by asserting the ERROR/WDI input pin.

Question-answer configuration (Q&A configuration): The MCU sends watchdog triggers through SPI.

The WD_CFG bit (bit 5) in the safety-function configuration register (SAFETY_FUNC_CFG) controlls the WDT configuration. The default configuration is the WDTI configuration.

5.4.1.12 WDT Fail Counter, WDT Status, and WDT Fail Event

The watchdog function includes a watchdog fail counter which increases and decreases because of *good* and *bad* events, respectively. When the value of the watchdog fail counter is 5 or more, the watchdog status is out-of-range, and the watchdog-enabled function is disabled (the ENDRV pin is low).

When the watchdog fail counter is 4 or less, the watchdog status is in-range, and the closed-loop watchdog no longer disables the watchdog-enabled function (the ENDRV pin is high). Note that this function can be disabled by individual control methods (through the ENABLE_DRV control bit in the SAFETY_CHECK_CTRL register).

The watchdog fail counter operates independently of the state of the WD_RST_EN bit in the SAFETY_FUNC_CFG register. The internal WD_RST_EN bit and watchdog status signals are ANDed together to disable the watchdog-enabled function when the watchdog fail counter is above the count of 4 and the ENABLE_DRV control bit in the SAFETY_CHECK_CTRL register is set.

The watchdog fail counter responds as follows:

- A *good event* decreases the fail counter by 1.
- A *bad event* increases the fail counter by 1.
- A *time-out event* increases the fail counter by 1 and sets the TIME_OUT flag (WDT_STATUS register, bit 1)

The definitions of *good event*, *bad event* and *time-out event* are listed in the sections describing the WDTI configuration and question and answer (Q&A) configuration.

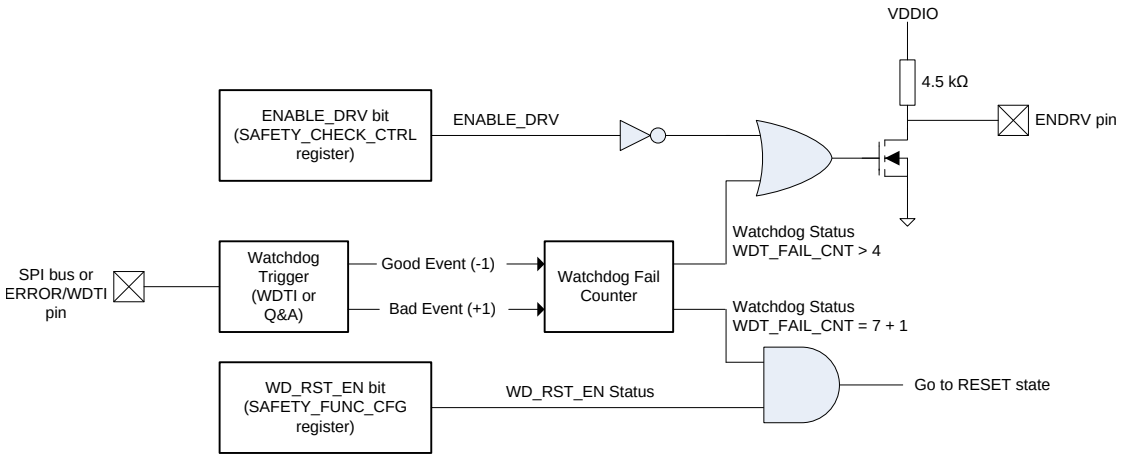


Figure 5-5. Watchdog Enable Function

Table 5-10. Watchdog Status for Fail Counter Value Range

WATCHDOG FAIL COUNTER *WDT_FAIL_CNT[2:0]*	0b000–0b100	0b101–0b111	0b111
Watchdog status	Closed-loopis watchdog in-range.	Closed loop watchdog is out-of-range.	NRES pulled low

The watchdog fail counter is initialized to a count of 5 after the NRES-output pin low-to-high transition (reboot of the MCU) when TPS65381-Q1 device enters DIAGNOSTIC state. When the TPS65381-Q1 device transitions from DIAGNOSTIC state to ACTIVE state, the watchdog fail counter reinitializes to a count of 5.

When the watchdog fail counter reaches a count of 7, any new *bad event* does not change the counter state: the counter state remains at 7. However, depending on device configuration (when the WD_RST_EN bit in the SAFETY_FUNC_CFG register is set to 1; default state for this bit is 0), on the next failure (7 + 1) an external reset to the MCU is asserted by pulling the NRES pin low and the TPS65381-Q1 device enters RESET state. In RESET state, the watchdog fail counter reinitializes to 5.

5.4.1.13 WDTI Configuration With an External Trigger Input (Default Mode)

After a power-on event, the reset output at the NRES pin is kept low for the reset extension time (externally configurable with a resistor between the RESEXT pin and ground, minimum time is 1.44 ms). After a low-to-high transition on the NRES output pin (reboot of the MCU), the watchdog function starts with the default CLOSE window duration, t_{WCW}. A received watchdog trigger interrupt (WDTI) within this CLOSE window interval is interpreted as a *bad event*.

The OPEN window with duration t_{WOW} begins after the CLOSE window. The OPEN window lasts at minimum until a WD interrupt is received and at maximum the programmed t_{WOW} time. A received watchdog trigger interrupt (WDTI) within this OPEN window interval is interpreted as a *good event*.

When the MCU suspends sending trigger events to the ERROR/WDI pin during the WDTI window sequence, the watchdog considers this as *no response event*. This sets the TIME_OUT flag (WDT_STATUS register, bit D1), and begins the next WDTI window sequence. This TIME_OUT flag is useful for the MCU software to synchronize the watchdog trigger events on the required watchdog timing. When synchronizing in this way, the MCU must not send any trigger event on the ERROR/WDI pin directly after reboot or after reconfiguring watchdog timer, until the TIME_OUT flag is set, and the first watchdog trigger pulse i sent in the correct timing after in the next CLOSE window or OPEN window. Note that such a *timeout event* increases the watchdog fail count, and a new CLOSE window or OPEN window begins immediately.

The watchdog OPEN window and the watchdog CLOSE window duration time, t_{WOW} and t_{WCW}, are programmed through the SPI registers, WDT_WIN2_CFG and WDT_WIN1_CFG respectively, when the TPS65381-Q1 device is in DIAGNOSTIC state. For the WDTI configuration which occurs as follows:

$$t_{WOW}\ (WDTI) = RW[4:0] \times 0.55\ ms \text{ (Bits RW[4:0] are located in the SPI register, WDT_WIN2_CFG)} \quad (1)$$

$$t_{WCW}\ (WDTI) = RT[6:0] \times 0.55\ ms \text{ (Bits RT[6:0] are located in the SPI register, WDT_WIN1_CFG)} \quad (2)$$

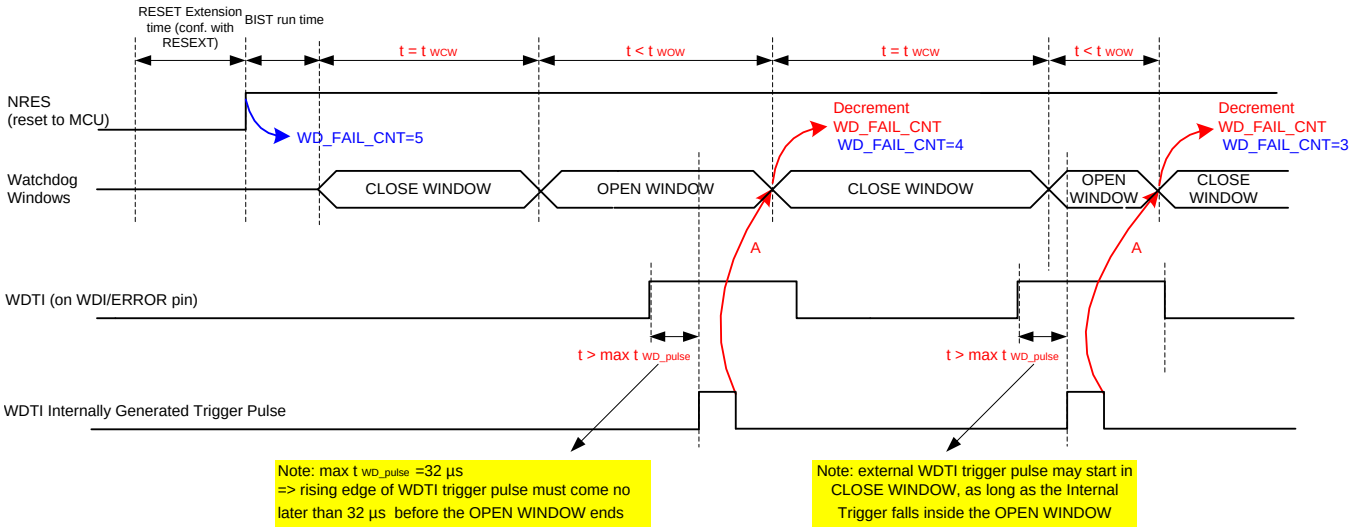
Writing a new watchdog OPEN window or CLOSE window time immediately begins a new WDTI Window Sequence (starting with a CLOSE Window), and increases the watchdog fail count. As an alternative to the TIME_OUT flag, this can be used for the MCU software to synchronize the watchdog trigger events on the required watchdog timing.

The SPI SW_LOCK command locks a write update for the WDT_WIN1_CFG register and the WDT_WIN2_CFG SPI register.

The watchdog function uses an internal 4-MHz (with ±5% accuracy) system clock as a time reference for creating the 0.55-ms time step. Any CLOSE window duration (t_{WCW}) update occurs during the next active watchdog OPEN window. Any OPEN window duration (t_{WOW}) update occurs during the next watchdog CLOSE window.

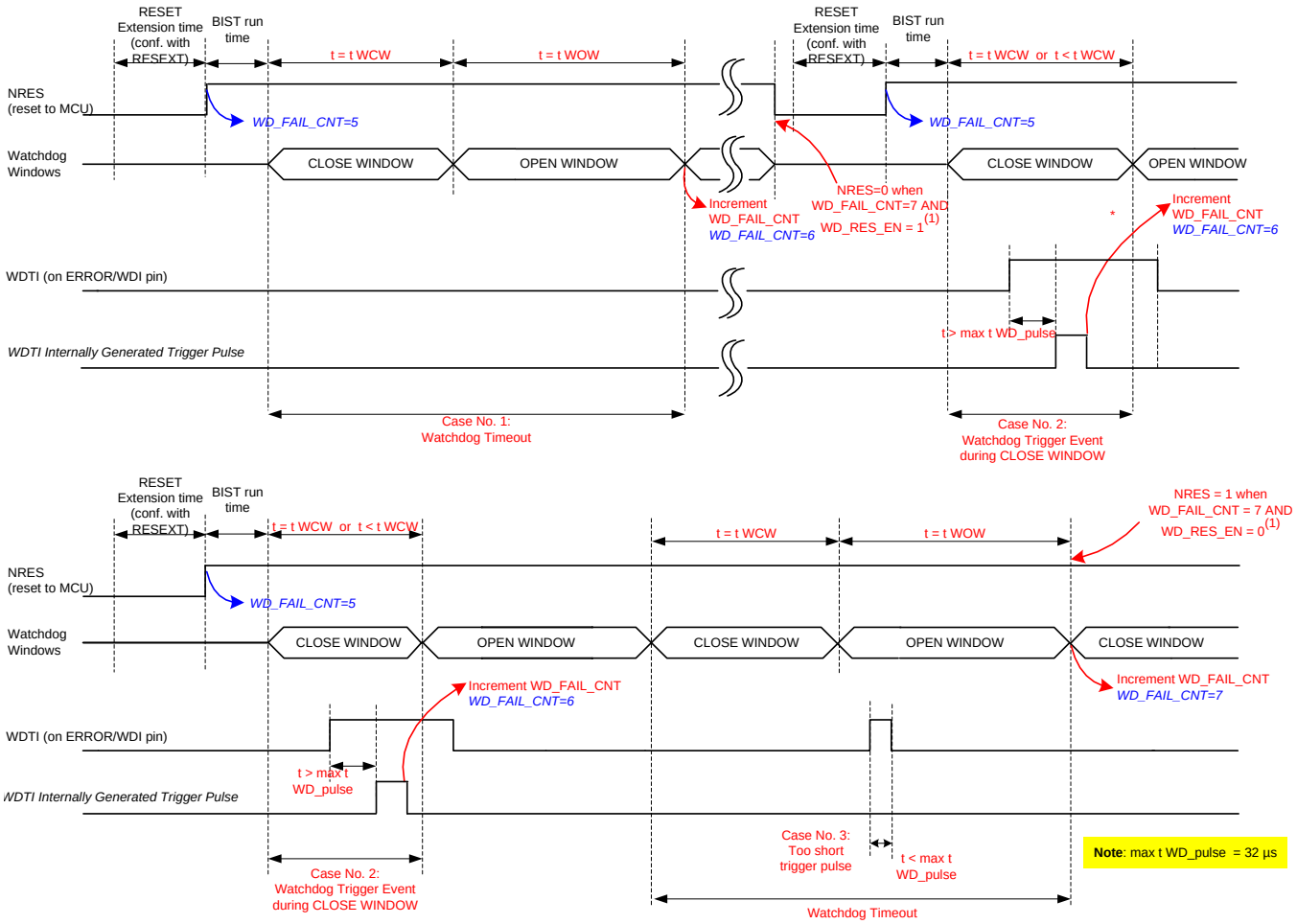
A watchdog trigger interrupt (WDTI) rising edge on the ERROR/WDI input pin, followed by watchdog trigger interrupt (WDTI) falling edge on ERROR/WDI input pin, is considered to be a watchdog trigger event. The watchdog trigger event is considered valid (such as a *good-event*) if received during a watchdog OPEN window (WOW), and is considered invalid (such as a *bad-event*) if received during watchdog CLOSE window (WCW). A valid watchdog trigger event (such as a trigger pulse in OPEN window) closes the current OPEN window and starts the next CLOSE window. In this way, the MCU and TPS65381-Q1 watchdog timing stay synchronized.

The ERROR/WDI input pin is deglitched with a t_{WD_pulse} filter time (32 µs maximum), and synchronized to internal system clock within 500 ns (with ±5% accuracy). The internally generated trigger pulse (see Figure 5-6 and Figure 5-7) is generated from the deglitched or synchronized trigger signal on the ERROR/WDI pin. Therefore the external watchdog trigger input (WDTI) rising edge must occur no later than 32 µs (t_{WD_pulse} maximum) before the end of the OPEN window to generate a *good-event*.The valid watchdog trigger event, power-up event, or power-down event resets the watchdog window sequence. This reset is always followed by starting a watchdog CLOSE window (WCW).



Note: When a correct watchdog trigger is received in an OPEN window, 1 system clock-cycle (250 ns, typical) later the next CLOSE window begins. Therefore the actual length of an OPEN window depends on when the MCU sends the correct trigger.

Figure 5-6. Possible Cases for *Good* Watchdog Events in WDTI Configuration



(1) WD_RST_EN = 0 per default

Figure 5-7. Possible Cases for *Bad* Watchdog Event and *Timeout event* in WDTI Configuration

5.4.1.14 Watchdog Question and Answer Configuration Through SPI

Setting the WD_CFG bit in the SAFETY_FUNC_REG register to 11 when the TPS65381-Q1 device is in DIAGNOSTIC state configures the TPS65381-Q1 watchdog in question-and-answer (Q&A) mode. In Q&A configuration, upon an MCU request, the TPS65381-Q1 device provides a *token* (or *question*) to the MCU over SPI (latched in the WDT_TOKEN register). The MCU performs a fixed series of arithmetic operations on the token value and returns the resulting token value *answers* to the ASIC over SPI (by writing to the WDT_ANSWER register). The TPS65381-Q1 device verifies that the MCU returns the token value results (answers) within the specified timing windows, and that the token value responses (answers) are correct.

When the MCU performs the watchdog-related SPI communications within the correct timing windows, and returns the correctly calculated token (question) responses (answers), the watchdog considers these *good events*.

NOTE

In Q&A mode, each watchdog period (such as a watchdog token-response sequence run) starts with an OPEN window and is followed by a CLOSE window.

When the MCU performs the watchdog-related SPI communications outside of the correct timing windows, or returns an incorrectly calculated token (question) responses (answers), or returns the correct answers in the wrong sequence, the watchdog considers these *bad events*.

When the MCU suspends watchdog-related SPI communications for the duration of the watchdog time-out window (after an elapse of the CLOSE window), the watchdog considers this as a *no-response event*. This sets the TIME_OUT flag (WDT_STATUS register, bit 1) and starts a new watchdog token-response sequence run. This TIME_OUT flag is useful for the MCU software to synchronize the watchdog trigger events on the required watchdog timing. When synchronizing in this way, the MCU must not send any trigger event on the ERROR/WDI pin directly after reboot or after reconfiguring the watchdog timer or after configuring watchdog from WDTI to Q&A until this TIME_OUT flag is set. Then the watchdog starts sending the first answer sequence in the correct order and correct timing during the next watchdog Token-Response Sequence Run. Note that such a *no-response event* increases the watchdog fail count, and a new watchdog token-response sequence run starts immediately.

5.4.1.14.1 Watchdog-Timer-Related SPI Event Definitions

- **Watchdog Token Request (*Question*)**
  - The question is a 4-bit word (see Section 5.4.1.14.3).
  - This event occurs when the MCU requests a read of the *Watchdog Token Value SPI* register (bit TOKEN[3:0] in the WDT_TOKEN_VALUE register).
  - If the SPI frame is not successfully transmitted (that is, there is a SPI fault detected), the watchdog token request event does not occur.
  - The MCU can request each new generated token at the start of the OPEN window, but this is not a required condition for a *good event*. The MCU can also generate the TOKEN by mimicking the TOKEN generation circuit as shown in Figure 5-9. Nevertheless, the valid responses (*answers*) are always based on the TOKEN generated inside the TPS65381-Q1 device. So if the MCU generates a wrong TOKEN and gives responses (*answers*) based on the MCU (wrong) TOKEN, a *bad event* is detected in the TPS65381-Q1 device.
- **Watchdog Timer Token Response (*Answer*)**
  - The response is a 32-bit word that is made up of 4 bytes (WD_TOKEN_RESP_3, WD_TOKEN_RESP_2, WD_TOKEN_RESP_1, and WD_TOKEN_RESP_0).
  - This event occurs when the MCU writes to the watchdog answer register (bit WDT_ANSW[7:0] in the WDT_ANSWER register).
  - Each watchdog token request requires four watchdog token responses (three responses during an OPEN window and one response during a CLOSED window).

5.4.1.14.2 Watchdog Token-Response Sequence Run

In general, each new Watchdog Token-Response Sequence Run begins by writing WD_TOKEN_RESP_0 (final answer-byte of the previous Token-Response Sequence Run). Every Token-Response Sequence Run starts with an OPEN Window, followed by a CLOSE window. The OPEN Window and the CLOSE window duration time t_{WOW} and t_{WCW} are programmed through the SPI registers, WDT_WIN1_CFG and WDT_WIN2_CFG respectively, when the TPS65381-Q1 device is in DIAGNOSTIC state. For watchdog question and answer (Q&A) configuration, the duration times are programmed as follows:

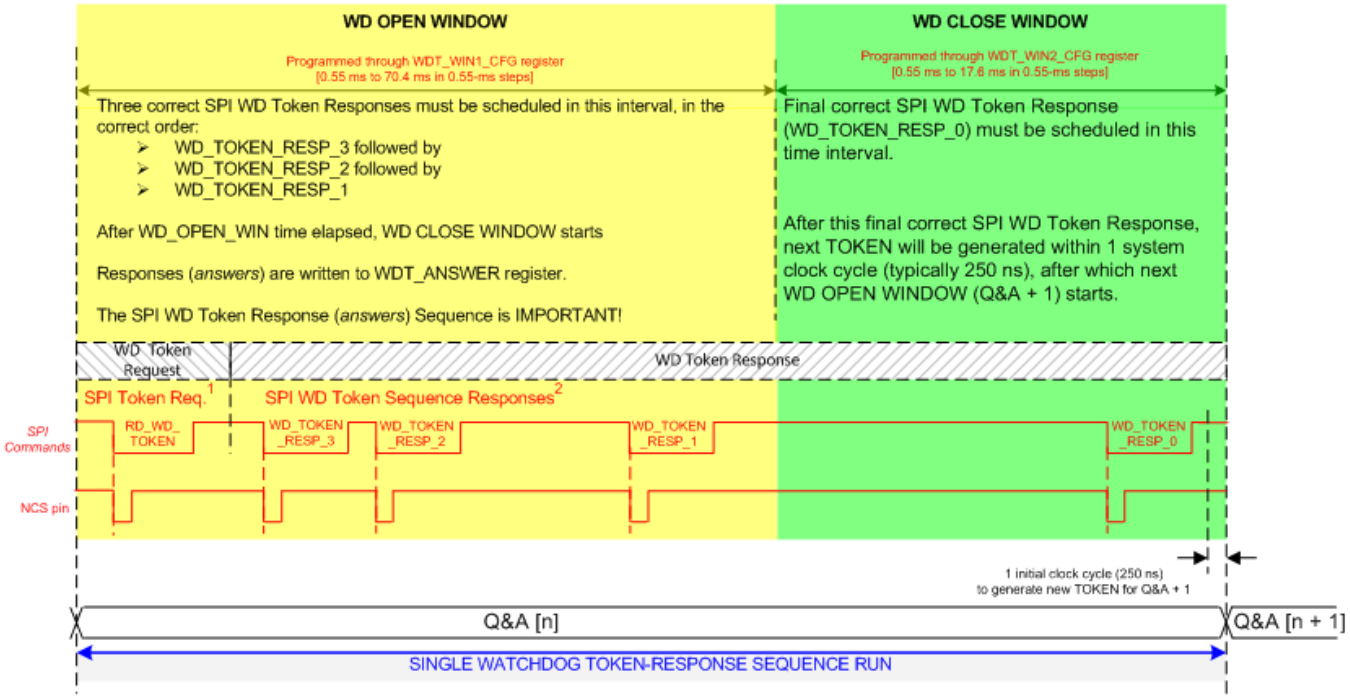
t_{WOW} *(Q&A) = RT[6:0] × 0.55 ms* (The bits RT[6:0] are located in the SPI register, WDT_WIN1_CFG) (3)

t_{WCW} *(Q&A) = RW[4:0] × 0.55 ms* (The bits RW[4:0] are located in the SPI register, WDT_WIN2_CFG) (4)

Any write access to the WDT_WIN1_CFG register or the WDT_WIN2_CFG register immediately starts a new Watchdog Token-Response Sequence Run, and increases the watchdog fail count. As an alternative to the TIME_OUT flag, this can be used for MCU software to synchronize the WD Token Responses on the required watchdog timing.

The SPI SW_LOCK command locks a write update for the WDT_WIN1_CFG register and the WDT_WIN2_CFG SPI register.

The watchdog function uses an internal 4MHz (with ±5% accuracy) system clock as a time reference for creating the 0.55-ms time-step.



(1) The MCU is not required to request the TOKEN: the MCU can start when given the correct answers WD_TOKEN_RESP_3..1 anywhere within the OPEN WINDOW. The new TOKEN is always generated within 1 system clock-cycle after the final WD_TOKEN_RESP_0.

(2) The MCU can put any other SPI Commands in-between the WD_TOKEN_RESPx answers (even re-requesting the TOKEN) without any influence on the watchdog function, as long as the WD_TOKEN_RESP_3-1 are given within the OPEN Window and WD_TOKEN_RESP_0 is given within the CLOSE Window.

Figure 5-8. WDT Token and Response Sequence Run

5.4.1.14.3 Watchdog Token Value Generation (or Watchdog Question Generation)

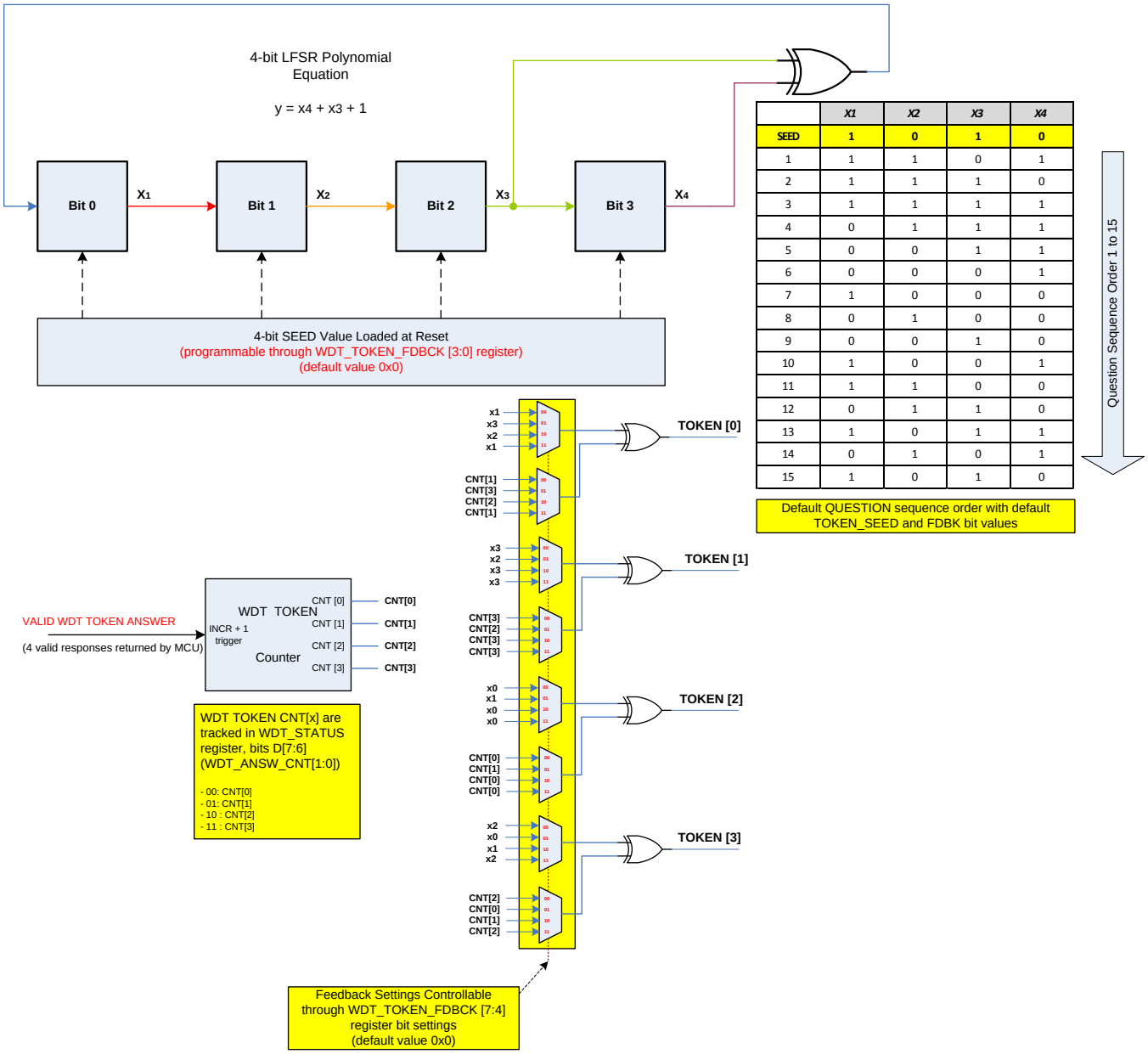
The TPS65381-Q1 device generates a new 4-bit token value only after valid and complete WD token responses.

- Three correct SPI watchdog-token responses received during a watchdog open window.
- One correct SPI watchdog-token response received during a watchdog close window must follow.

- In addition to the previous timing, the sequence of four responses must be correct.

The *Watchdog Token Value* is latched in the *Watchdog Token Value* SPI register and can be read at any time.

The 4-bit question TOKEN [3:0] is generated with a 4-bit counter and a 4-bit Markov chain. The 4-bit counter is clocked by the sequencer if the value of the given answer is correct and the answer is received within the time window. The Markov chain is clocked by the 4-bit counter at the transition from 1111 bin 0000 bin. This includes the condition of a correct answer in value and timing. Figure 5-8 shows the logic combination of the 4-bit questions TOKEN generation.



	X1	X2	X3	X4
SEED	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

Figure 5-9. Watchdog TOKEN Generation

A Watchdog Token-Response Sequence Run starts by writing the WDT_WIN1_CFG register or the WDT_WIN2_CFG registers, or the end of time window is not allowed to clock either the 4-bit counter or the Markov chain, therefore no new TOKEN is generated in any of these events. The 4-bit counter and the Markov chain are set to the singular point b0000 at reset. To leave the singular point the feedback logic combination is implemented. The logic combination of the 4-bit counter with the Markov chain generates the 4-bit questions is shown in Figure 5-9.

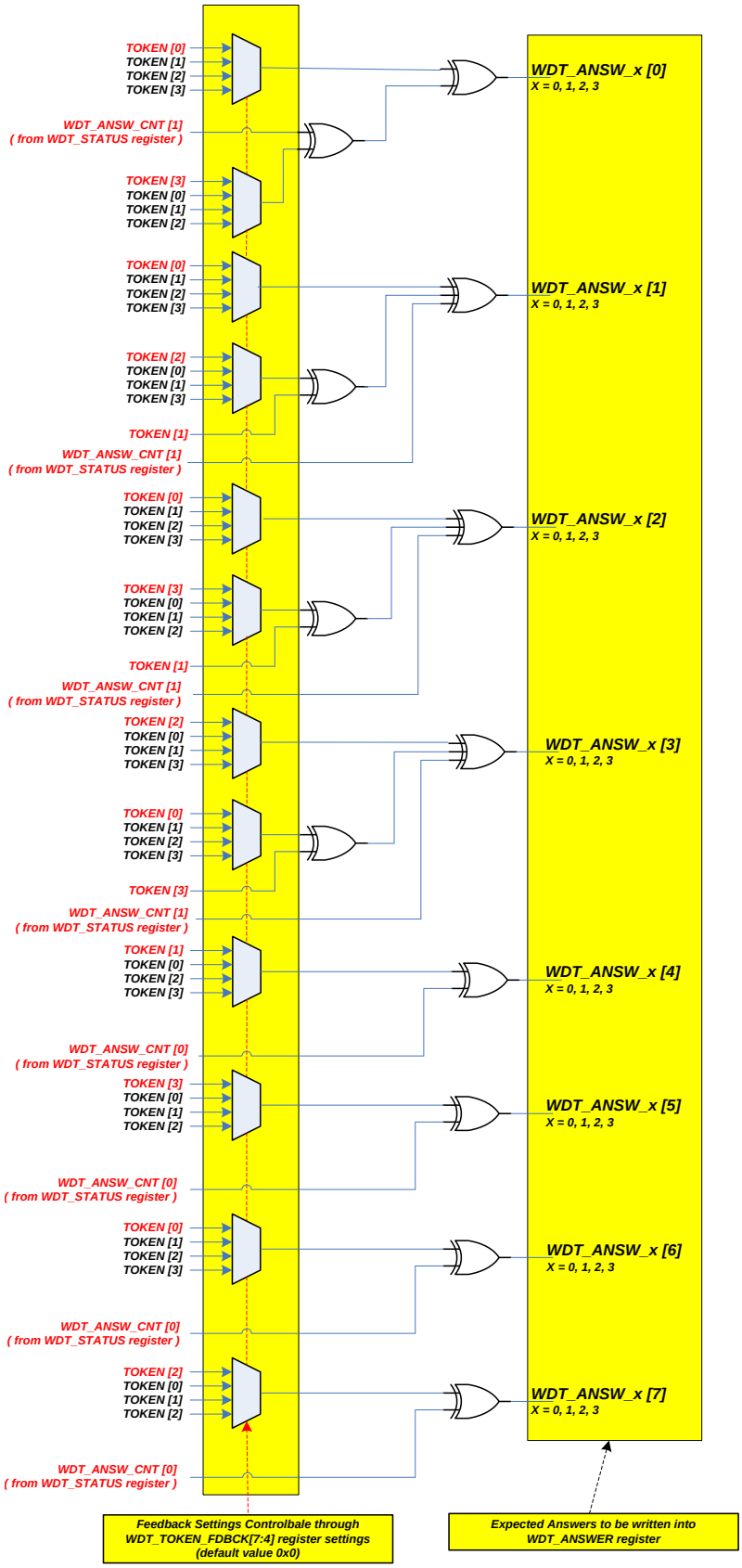


Figure 5-10. Watchdog Token Value Response Calculation (or Watchdog Answer Calculation)

5.4.1.14.3.1 Answer Comparison and Reference Answer

The 2-bit watchdog answer counter (the WDT_ANSW_CNT[1:0] bit in the WDT_STATUS register) counts the number of received 4-byte answers and controls the generation of the reference value. The default value is 11 (this corresponds to *Waiting for WDT_RESP_3 byte*).

Sequence of the 2-bit counter

- WDT_ANSW_CNT[1:0] = 11:
  - The WDT_ANSW_3 byte of the reference answer is applied to the comparator.
  - Write access: WD_TOKEN_RESP_3 from the MCU written in the WDT_ANSWER register
  - Set the WDT_ANSW_CNT[1:0] bit to 10 and update the TOKEN_ERR flag bit.
- WDT_ANSW_CNT[1:0] = 10:
  - The WDT_ANSW_2 byte of the reference answer is applied to the comparator
  - Write access: WD_TOKEN_RESP _2 from the MCU written in the WDT_ANSWER register
  - Set the WDT_ANSW_CNT[1:0] bit to 01 and update the TOKEN_ERR flag bit.
- WDT_ANSW_CNT[1:0] = 01:
  - The WDT_ANSW_1 byte of the reference answer is applied to the comparator
  - Write access: WD_TOKEN_RESP _1 from the MCU written in the WDT_ANSWER register
  - Set the WDT_ANSW_CNT[1:0] bit to 00 and update the TOKEN_ERR flag bit.
- WDT_ANSW_CNT[1:0] = 00
  - The WDT_ANSW_0 byte of the reference answer is applied to the comparator
  - Write access: WD_TOKEN_RESP _0 from the MCU written in the WDT_ANSWER register
  - Update the TOKEN_ERR flag bit
  - Start a new Watchdog Token Sequence Run and reset the WDT_ANSW_CNT[1:0] bit to 11 and the TOKEN_ERR flag bit to 0.

Table 5-11. Set of 4-Bit WD Token Values and Corresponding 8-Bit Responses

4-BIT WDT IN WDT_TOKEN_VALUE REGISTER	WDT ANSWER (TO BE WRITTEN INTO WDT_ANSW REGISTER)			
	8-BIT WD_TOKEN_ RESP_3	8-BIT WD_TOKEN_ RESP_2	8-BIT WD_TOKEN_ RESP_1	8-BIT WD_TOKEN_ RESP_0
TOKEN [3:0]	*WDT_ANSW_CNT [1:0] = 11*	*WDT_ANSW_CNT [1:0] = 10*	*WDT_ANSW_CNT [1:0] = 01*	*WDT_ANSW_CNT [1:0] = 00*
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

5.4.1.14.4 Watchdog Token-Response Sequence Run and WDT_STATUS Register Updates

- If the answer was correct in value (TOKEN_ERR = 0) and Timing:
  - The watchdog fail counter decreases by one
  - The 2-bit watchdog answer counter (WDT_ANSW_CNT) increases by one
  - The SEQ_ERR bit resets
  - The TOKEN_EARLY bit resets
- If the answer was correct in value (TOKEN_ERR = 0) but not in Timing:
  - The watchdog fail counter increases by one
  - The 2-bit watchdog answer counter (WDT_ANSW_CNT) has no change
  - The SEQ_ERR bit is set
  - The TOKEN_EARLY bit is set
- If the answer was not correct in value (TOKEN_ERR = 1) but Timing was correct:
  - The watchdog fail counter increases by one
  - The 2-bit watchdog answer counter (WDT_ANSW_CNT) has no change
  - The SEQ_ERR bit is set
  - The TOKEN_EARLY bit is reset
- If the answer was not correct in value (TOKEN_ERR = 1) and Timing was not correct:
  - The watchdog fail counter increases by one
  - The 2-bit watchdog answer counter (WDT_ANSW_CNT) has no change
  - The SEQ_ERR bit is set
  - The TOKEN_EARLY bit is set
- If the Watchdog Token-Response Sequence Run is started by a no-response event (such as a timeout event):
  - The watchdog fail counter increases by one
  - The value of the 2-bit watchdog answer counter (WDT_ANSW_CNT) has no change
  - The TIME_OUT bit is set
- If Watchdog Token-Response Sequence Run is started by updating Watchdog OPEN or CLOSE window duration:
  - The watchdog fail counter increases by one
  - The WD_CFG_CHG bit is set

Table 5-12. WDT_STATUS Bits Versus Possible Token-Response-Sequence Run Events

WATCHDOG TOKEN-RESPONSE SEQUENCE RUN EVENTS					WDT_STATUS REGISTER BITS			
All MCU Answer Bytes Correct?	MCU Last Answer Byte Arrived During Watchdog CLOSE Window interval?	MCU Last Answer Byte Arrived During Watchdog OPEN Window Interval	Timeout Occurred While Waiting for Complete MCU Answer?	Watchdog OPEN or CLOSE Window Duration Changed?	WD_CFG_CHG	SEQ_ERR	TIME_OUT	TOKEN_EARLY
Yes	Yes	No	No	No	0	0	0	0
Yes	No	Yes	No	No	0	1	0	1
No	Yes	No	No	No	0	1	0	0
No	No	Yes	No	No	0	1	0	1
Yes			Yes	No	0	0	1	0
No			Yes	No	0	1	1	0
				Yes	1	0	0	0

See Figure 6-11 for an example software flowchart of how to synchronize the MCU with the TPS65381-Q1 watchdog function.

5.4.1.15 MCU Error Signal Monitor (MCU ESM)

This block monitors the external-MCU error conditions signaled over the ERROR/WDI input pin. This block is configurable to monitor two different signaling options:

- Detecting a low-pulse signal with programmable low-pulse duration threshold (TMS570 mode, see Section 5.4.1.15.1)
- Detecting the PWM signal with programmable frequency and duty cycle (PWM mode, see Section 5.4.1.15.2) (1)

The error-signal monitor is deactivated by default, and activates by setting bit NO_ERROR to 0 in the SAFETY_CHECK_CTRL SPI register. Note that activating the error-signal monitor is only recommended when the watchdog is configured in question-answer (Q&A) mode, otherwise the ERROR/WDI pin is used both for watchdog trigger input and MCU error signaling.

The operating mode is controlled through the ERROR_CFG bit in the SAFETY_FUNC_CFG register. The low-signaling duration threshold (for TMS570 mode) or the expected PWM low-pulse duration (for PWM mode) is set through the SAFETY_ERR_PWM_L register, and expected PWM high-pulse duration (for PWM mode) is set through the SAFETY_ERR_PWM_H register.

A detected MCU signaling error is stored in bit ERROR_PIN_FAIL in the SAFETY_ERR_STAT SPI register. When the TPS65381-Q1 device is in DIAGNOSTIC state, the MCU emulates a signaling error (emulated fault-injection) for a diagnostic check of the error-signal monitor by checking the status of the ERROR_PIN_FAIL bit. When the TPS65381-Q1 device is in ACTIVE state, a detected MCU signaling error leads to a transfer into SAFE state, and a dedicated 4-bit error counter (bits DEV_ERR_CNT[3:0] in the SAFETY_ERROR_STAT SPI register) counts the transitions from ACTIVE state to SAFE state.

For both error-signal monitor operating-modes, the ERROR/WDI input pin is deglitched with a 15-µs (with ± 5% accuracy) filter time, and synchronized to internal system clock within 500 ns (with ± 5% accuracy). The deglitched and synchronized ERROR/WDI signal is monitored.

The module is covered by a logic BIST and is activated at a device power-up event or by the external MCU when the device is in the DIAGNOSTIC or ACTIVE state.

5.4.1.15.1 TMS570 Mode

An error condition is detected when the ERROR/WDI pin remains low for a programmed amount of time set by the SAFETY_ERR_PWM_L register. The programmable time range is 5 µs to 1.28 ms, with 5-µs steps.

The SAFETY_ERR_PWM_L register must be set to the desired value based on the maximum required time for the TMS570 MCU to detect an error or fault and to potentially recover from or correct the error or fault. Figure 5-11 shows the error-detection case scenarios.

The low-pulse monitoring on the ERROR/WDI pin is implemented as follows:

- When NO_ERROR = 0, every falling edge of the deglitched or synchronized ERROR/WDI signal reinitializes the low-pulse duration counter to 0 within one system clock-cycle (250 ns ± 5%).
- After reinitialization, the low-pulse counter restarts one system clock-cycle (250 ns ± 5%).
- The low-pulse duration counter increases every 5 µs (with ± 5% accuracy) as long as the ERROR/WDI pin is low. A rising edge on the ERROR/WDI pin stops the low-pulse duration counter
- When low-pulse duration counter is equal SAFETY_ERR_PWM_L register setting, the ERROR/WDI pin signaling failure is detected.

The ERROR_PIN_FAIL bit in the SAFETY_ERR_STAT SPI register is set within one system clock cycle (250 ns ± 5%) after detecting an MCU signaling error. When the device is in ACTIVE state, a transition to SAFE state occurs after one more system clock-cycle.

(1) PWM mode can be used as an external clock-monitor function.

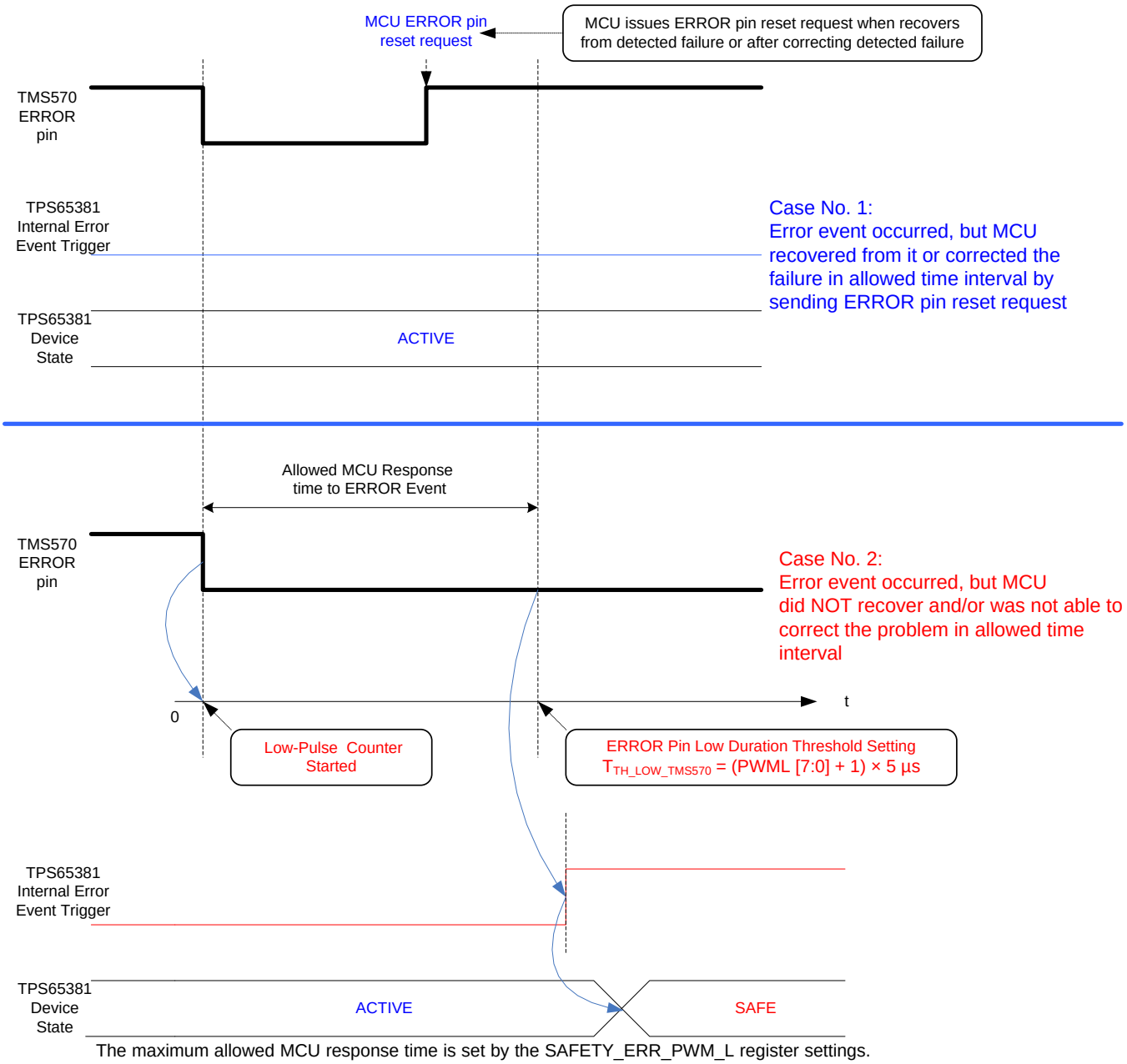


Figure 5-11. Error-Detection Case Scenarios for the TMS570 MCU

5.4.1.15.2 PWM Mode

The TPS65381-Q1 device detects an MCU signaling error on the ERROR/WDI pin if the following occurs:

- The ERROR/WDI pin high-pulse duration exceeds the threshold value programmed by the PWM_H register

  OR

- The ERROR/WDI pin low-pulse duration exceeds the threshold value programmed by the PWM_L register

The TPS65381-Q1 device does NOT detect an MCU signaling error on the ERROR/WDI pin if the following occurs:

- The ERROR pin high-pulse duration is less than the threshold value programmed by the PWM_H register

AND

- The ERROR pin low-pulse duration is less than the threshold value programmed by the PWM_L register

The programmable time range for the expected HIGH and LOW pulse duration is 5 µs to 1.28 ms, with 5-µs resolution steps.

The monitoring of the high-pulse duration and low-pulse duration is implemented as follows:

Low-Phase Monitoring:

- Every falling edge of the deglitched and synchronized ERROR/WDI signal, or setting the NO_ERROR bit from 1 to 0 when the ERROR/WDI pin is low, re-initializes the low-pulse duration counter to 0 within one system clock-cycle (250 ns ± 5%).
- After reinitialization, the low-pulse counter re-starts after one system clock-cycle (250 ns ± 5%).
- The low-pulse duration counter increases every 15 µs (with ± 5% accuracy)
- When the low-pulse duration counter is equal to the SAFETY_ERR_PWM_L register setting, ERROR-pin signaling failure is detected

High-Phase Monitoring:

- Every rising edge of the deglitched and synchronized ERROR/WDI signal, or setting the NO_ERROR bit from 1 to 0 when the ERROR/WDI pin is high, reinitializes the high-pulse duration counter to 0 within one system clock-cycle (250 ns ± 5%).
- After reinitialization, the high-pulse counter re-starts after one system clock-cycle (250 ns ± 5%).
- The high-pulse duration counter increases every 15 µs (with ± 5% accuracy)
- When high-pulse duration counter is equal SAFETY_ERR_PWM_H register setting, error pin signaling failure is detected

The ERROR_PIN_FAIL bit in the SAFETY_ERR_STAT register is set within one system clock cycle (250 ns ± 5%) after detecting an MCU signaling error. When the device is in ACTIVE state, a transition to SAFE state occurs after one more system clock-cycle.

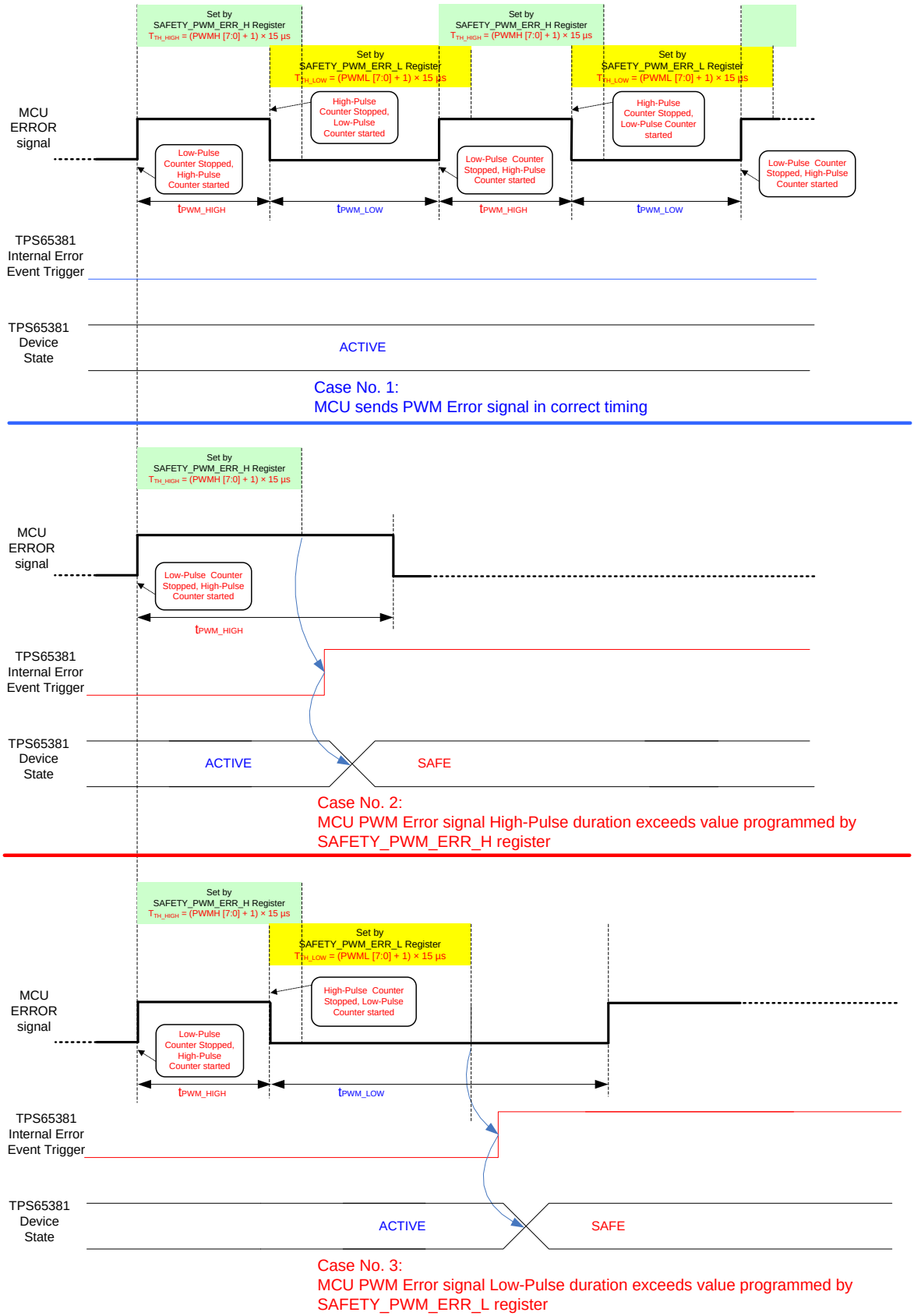


Figure 5-12. ERROR Pin Monitor – PWM Mode

5.4.1.16 Device Configuration Register Protection

This function offers a mechanism to protect safety SPI-mapped registers by means of SPI write-access protection and CRC check.

The register access protection includes two distinctive features:

- A register cannot be written after write-access lock protection is set. The lock is cleared by software or by a power-on reset.
- CRC protection for configuration registers

A CRC occurs on safety data after an SPI write updates to verify the SPI register contents are correctly programmed. The CRC controller is a diagnostic module which performs CRC to verify the integrity of the SPI-mapped register space. A signature representing the content of the safety registers is obtained when the content is read into the CRC controller. The responsibility of the CRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a predetermined good-signature value. The predetermined CRC signature value is stored in the SAFETY_CFG_CRC register. The external MCU uses the SAFETY_CHECK_CTL register to enable a CRC check and the SAFETY_STAT_2 register to monitor the status. When enabled, a CRC check on the configuration registers is performed. In case of a detected signature error, a flag called CFG_CRC_ERR is set in SPI register in the SAFETY_STAT_2 register. The device state and the ENDRV pin state remain unchanged. In case of a detected checksum error with the TPS65381-Q1 device in DIAGNOSTIC state, clearing bit CFG_CRC_EN to 0 brings the TPS65381-Q1 device into SAFE state (the ENDRV pin is pulled low).

A standard CRC-8 polynomial is used: X8 + X2 + X1 + 1

The CRC monitor test is covered by a logic BIST.

A 64-bit string is protected by CRC. The following registers are protected:

- SAFETY_FUNC_CFG
- DEV_REV
- SAFETY_PWD_THR_CFG
- SAFETY_ERR_CFG
- WDT_TOKEN_FDBCK
- WDT_WIN2_CFG
- WDT_WIN1_CFG
- SAFETY_ERR_PWM_L
- DEV_CFG2
- DEV_CFG1 (only bit number 6)

Table 5-13 lists the CRC bus structure.

Table 5-13. CRC Bus Structure

REGISTER NAME	64-BIT BUS ORDERING
SAFETY_FUNC_CFG [6:0]	[63:57]
DEV_REV [7:0]	[56:49]
SAFETY_PWD_THR_CFG [3:0]	[48:45]
SAFETY_ERR_CFG [7:0]	[44:37]
WDT_TOKEN_FDBCK [7:0]	[36:29]
WDT_WIN2_CFG [4:0]	[28:24]
WDT_WIN1_CFG [6:0]	[23:17]
SAFETY_ERR_PWM_L [7:0]	[16:9]
DEV_CFG2 [7:0]	[8:1]
DEV_CFG1 [6]	0

In the external MCU, the CRC calculation must be done byte-wise, starting with the lowest byte of the 64-bit bus ordering value. The most significant bit is first in the bit order. The resulting CRC of one calculation is the seed value for the next calculation. The initial seed value is 0xFF. The CRC result of the 8th byte-wise calculation is the CRC signature value, which must be stored in the SAFETY_CFG_CRC register (see Figure 5-13).

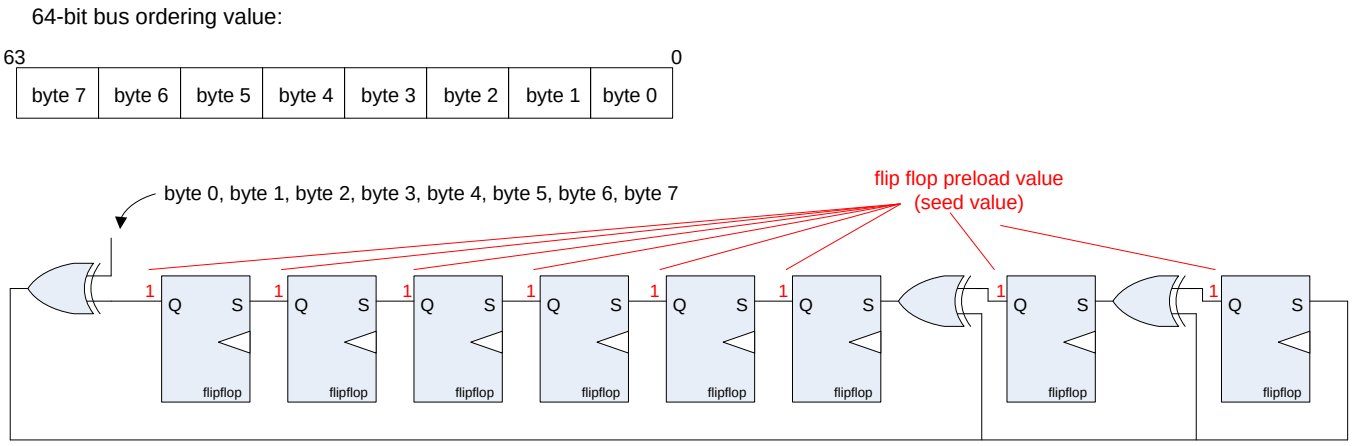


Figure 5-13. CRC Calculation Logic

Table 5-14 lists some CRC calculation examples.

Table 5-14. CRC Calculation Examples

64-BIT BUS ORDERING VALUE	CRC-8 RESULT
0x0000 0000 0000 0000	0xDB
0xFFFF FFFF FFFF FFFF	0x0C
0x0A0A 0505 0A0A 0505	0xD4
0x0505 0A0A 0505 0A0A	0x17
0xA0A0 5050 A0A0 5050	0x2B
0x0A23 E000 18FE 7B80	0x1B

In case the CRC controller detects a signature error on the configuration registers, care must be taken when performing an EEPROM CRC check afterwards. In case of a detected signature error in the configuration registers, the device reports an EEPROM signature error when the CFG_CRC_EN bit in the SAFETY_CHECK_CTL register is set to 0 first before performing the EEPROM CRC check by setting the EE_CRC_CHK bit in the SAFETY_BIST_CTRL register to 1, even when the EEPROM bits do not have an error. Therefore, when performing an EEPROM CRC check after a CRC check on the configuration registers, the steps must always occur in the following order:

1. Calculate CRC8 in the MCU and store in the SAFETY_CFG_CRC register.
2. Set the CFG_CRC_EN bit in the SAFETY_CHECK_CTL register to 1 to perform a CRC Check on configuration registers.
3. After the SPI command sets the CFG_CRC_EN bit to 1 (for example: after rising edge on NCS), wait at least 2.1 µs for the configuration register to complete the CRC check.
4. Read the results of configuration register CRC check in the SAFETY_STAT_2 register, bit CFG_CRC_ERR. If continuous CRC check on the configuration register must be performed, clear the CFG_CRC_EN bit in the SAFETY_CHECK_CTL register to 0 and repeat beginning with Step 1.

   If the CRC check on EEPROM registers must be performed, proceed to Step 5.

NOTE

A correct EEPROM CRC check afterwards (as described in Step 5) clears this CFG_CRC_ERR bit. Therefore, TI recommends to read out this CFG_CRC_ERR bit before performing the EEPROM CRC check.

5. Set the EE_CRC_CHK bit in the SAFETY_BIST_CTRL register to 1 to perform the CRC Check on EEPROM registers.
6. After the SPI command sets the EE_CRC_CHK bit to 1 (for example: after rising edge on NCS), wait at least 811 µs for the EEPROM CRC check to finish.
7. Completion of the EERPOM CRC check is observed by reading the EE_CRC_CHK bit. When EEPROM CRC is complete, this EE_CRC_CHK bit is cleared to 0.
8. Clear the CFG_CRC_EN bit in the SAFETY_CHECK_CTL register to 0
9. Read the results of the EEPROM CRC check in the SAFETY_STAT_2 register, bit EE_CRC_ERR.
10. Go back to Step 1.

NOTE

Returning to Step 1 is not required; returning to Step 2 is also an option.

5.4.1.17 Enable and Reset Driver Circuit

Figure 5-14 shows the Enable and reset circuit.

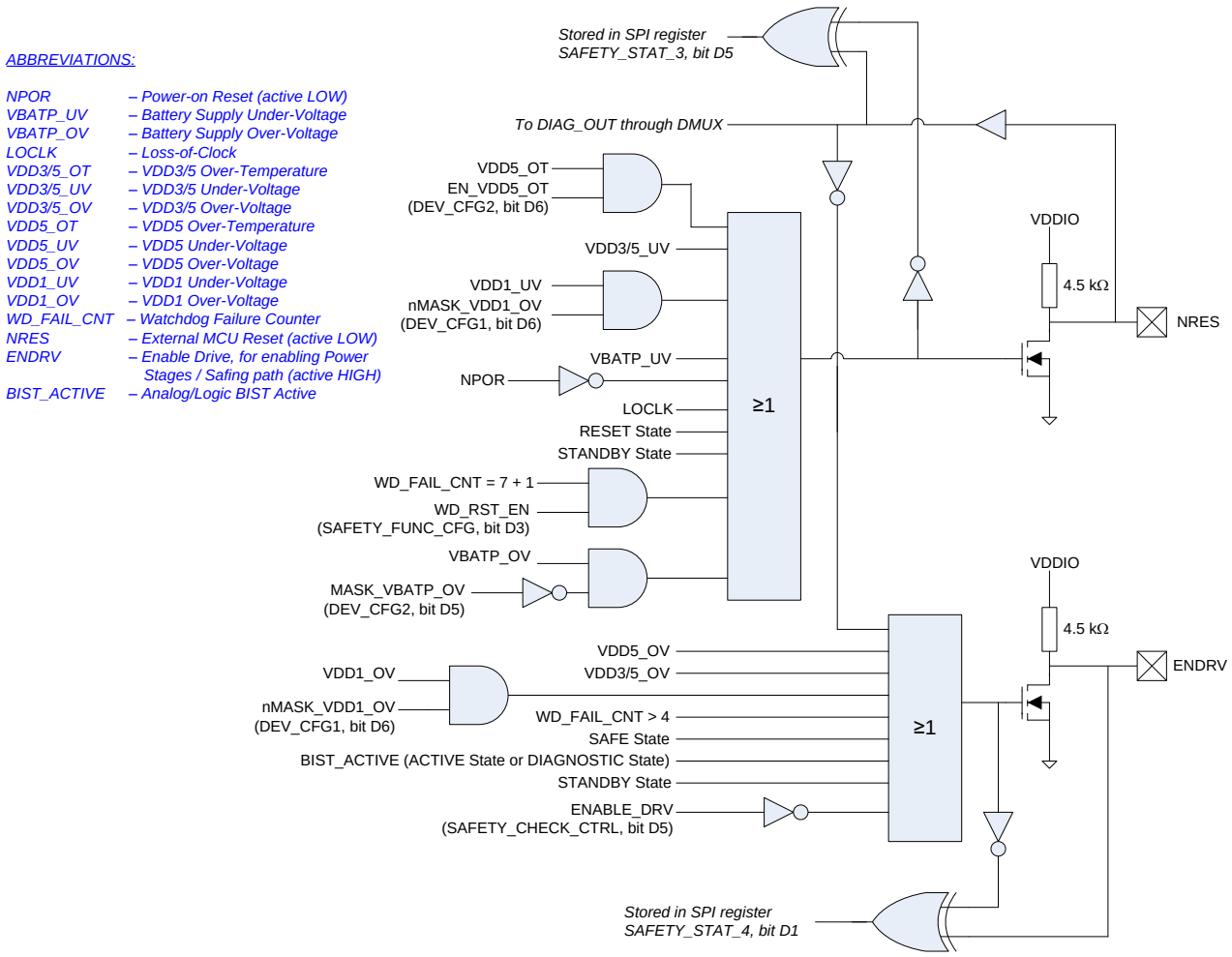


Figure 5-14. Reset and Enable Circuit

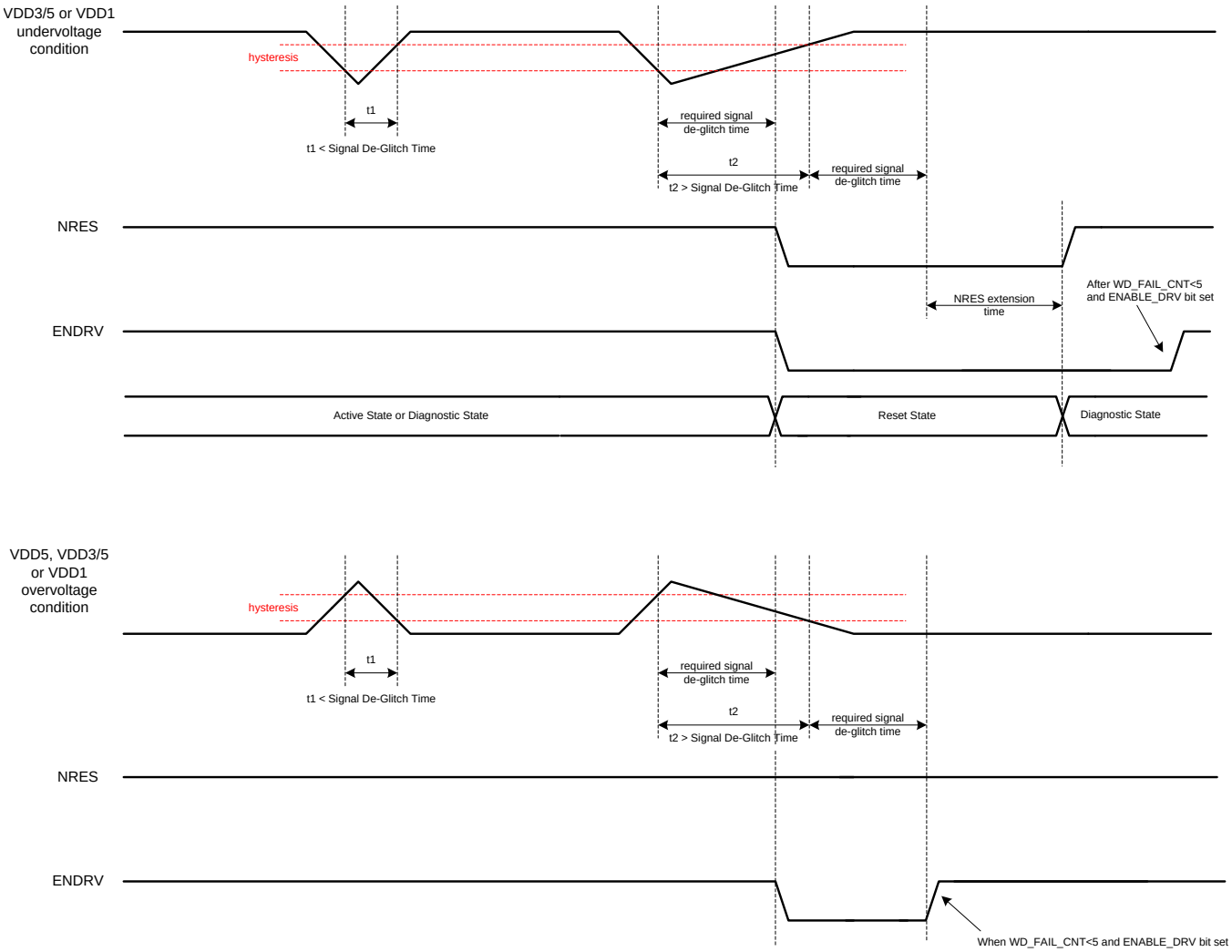
The ENDRV pin features a read-back circuit to compare the external ENDRV level with the internally applied ENDRV level. This feature detects any possible failure in the ENDRV pullup or pulldown components. A failure is detected by the MCU through the SPI register SAFETY_STAT_4, bit 1.

The ENDRV pin is pulled low for the ABIST duration time (approximately 300 µs) when activating the ABIST function after the ENDRV output is turned on and driven high. This is part of ENDRV diagnostics to validate all monitoring functions that disable ENDDRV output and confirm ENDRV output is controllable by utilizing ENDRV read-back path.

The NRES pin features a readback of the external NRES level. The value is read on the DIAG_OUT pin and in the SPI register SAFETY_STAT_3, bit 5.

For both the ENDRV therminal and the NRES pin, the logic readback-threshold level is typically 400 mV.

Figure 5-15 shows the timing-response diagram for the NRES and ENDRV pins to any VDDx undervoltage or overvoltage condition.



(1) The signal deglitch time is defined for each undervoltage or overvoltage condition as given in Section 4.
(2) The NRES extension time is defined by the external resistor value as given in Section 4.

Figure 5-15. Timing-Response Diagram for NRES and ENDRV Pins to any VDDx Undervoltage or Overvoltage Condition

5.4.1.18 Device Controller State Diagram

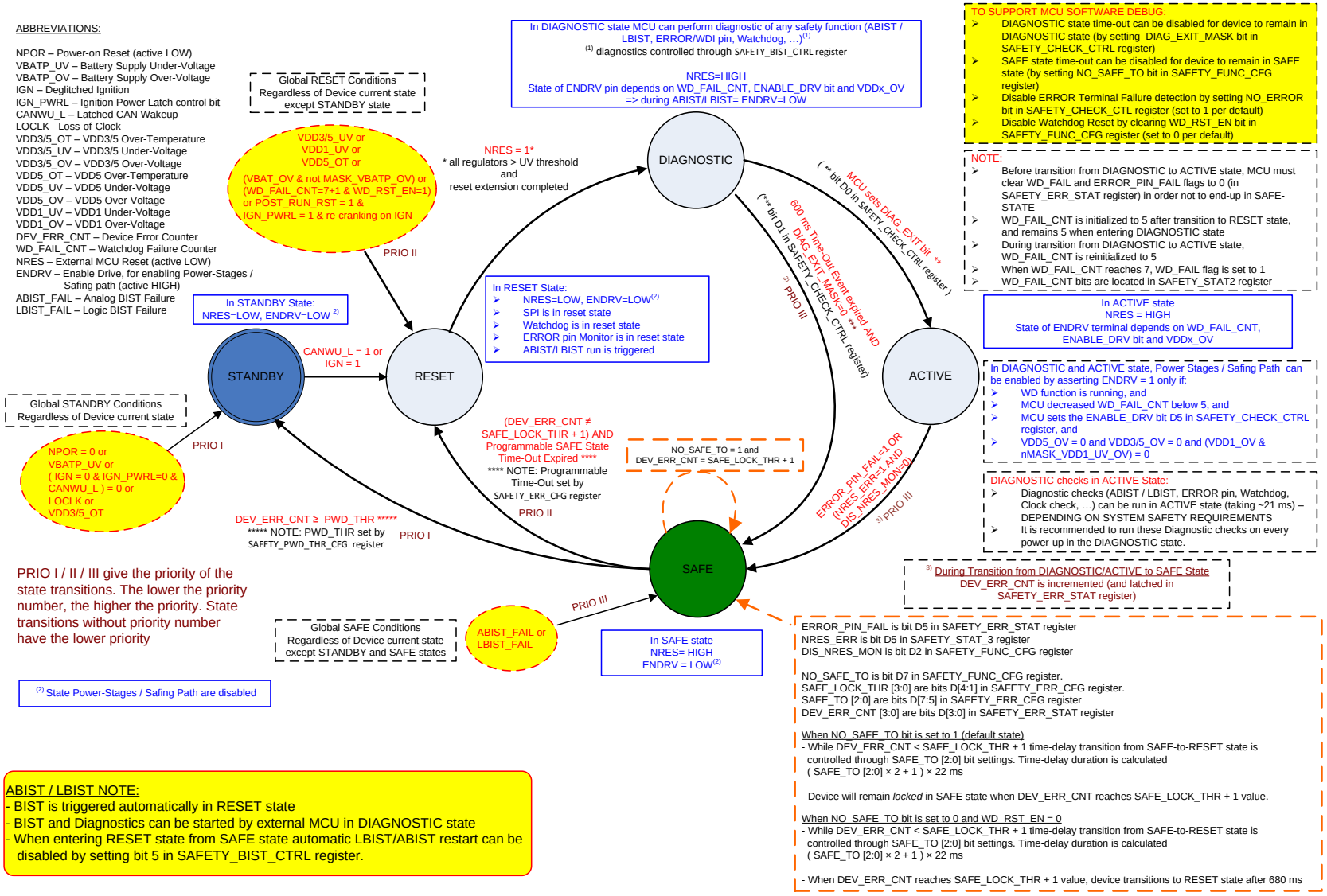


Figure 5-16. Device Controller State Diagram

5.4.1.19 STANDBY State

- This state is the default state at power up.
- All regulators are disabled, ENDRV is disabled, and NRES to the external MCU is driven low.
- The device transitions to the STANDBY state from any state because of the following:
  - VBATP undervoltage event
  - Deglitched IGN = 0 and IGN_PWRL = 0 (cleared IGN power-latch control bit) and CANWU_L = 0
  - VDD3/5 overtemperature event
  - Loss-of-clock detection
  - The error count reached the programmed power-down threshold
  - Internal NPOR (power-on reset)

5.4.1.20 RESET State

- Enters from the STANDBY state after an IGN or CANWU event
  - In this case, the VDDx regulators are ramping up.
- Enters from the SAFE state after a reset delay time-out expires when the device error count is below the programmed SAFE_LOCK_THR + 1
- The device transitions to the RESET state from any other state because of the following:
  - VDD3/5 undervoltage event
  - VDD1 undervoltage event
  - VBATP overvoltage event
  - Watchdog reset. A watchdog reset occurs after the watchdog fail counter has reached a value of 7 and another bad event occurs (7+1)
    (which sets the WD_FAIL flag) when WDT_RST_EN = 1
  - VDD5 overtemperature event

In all transitions to RESET state (except when coming from STANDBY state), the VDDx regulator stays on, but the VSOUT1 regulator is disabled. The NRES and ENDRV pins are low in RESET state.

5.4.1.21 DIAGNOSTIC State

- Enters from the RESET state after all regulators are ramped-up and the MCU reset (NRES pin) extension is completed and the NRES pin is pulled up
- VSOUT1 regulator is disabled per default, can be enabled and disabled through SPI
- Watchdog and ERROR/WDI pin monitoring functions can be configured and operated. Emulated MCU_ERROR on the ERROR/WDI pin does not cause a transition to the SAFE state
- Upon entry of DIAGNOSTIC state, watchdog failure counter is initialized to 5.
- State of the ENDRV pin is determined by the watchdog fail count value, VDDx_OV, and the ENABLE_DRV bit
- This state performs all device self-tests and diagnostics by the MCU (failures are induced to emulate internal failures and confirm detection).

NOTE

If the DIAG_EXIT_MASK or DIAG_EXIT bit is not set to 1 within 600 ms, the DIAGNOSTIC state time-out interval expires, causing a transition to the SAFE state (both the ERROR_PIN failure and WDT failure status bits are set to 1 in the SAFETY_ERR_STATUS register, and the error count is incremented). When setting the DIAG_EXIT_MASK bit to 1 (only recommended for software debug), the device stays in the DIAGNOSTIC state until the DIAG_EXIT bit is set. Setting the DIAG_EXIT bit to 1 causes a controlled transition to the ACTIVE state.

5.4.1.22 ACTIVE State

- Enters from the DIAGNOSTIC state after the MCU sets the DIAG_EXIT bit in the SAFETY_CHECK_CTRL register

NOTE

While in DIAGNOSTIC state, the MCU must clear the ERROR_PIN_FAIL bit and the WD_FAIL bit in the SAFETY_ERR_STAT register before setting the DIAG_EXIT bit. Otherwise, a transition to SAFE state occurs

- Watchdog and ERROR/WDI pin monitoring functions are operated as configured but cannot be reconfigured.
- Upon entry to the ACTIVE state, the watchdog failure counter reinitializes to 5.
- The VDDx regulators are up and running, and the VSOUT1 regulator maintains the same state as configured in DIAGNOSTIC state
- The NRES pin is pulled up, and the state of the ENDRV pin is determined by the watchdog fail count value, VDDx_OV, and ENABLE_DRV bit.

5.4.1.23 SAFE State

- Enters from the ACTIVE state after an ERROR/WDI pin.
- Enters from the ACTIVE state after detected read-back error on NRES pin (bit NRES_ERR in SAFETY_STAT_3 register) when bit DIS_NRES_MON = 0 (1 in default state) in SAFETY_FUNC_CFG register.
- Enters from the DIAGNOSTIC state after a 600 ms time-out event expires when the DIAG_EXIT_MASK is not set to 1.
  - Uncontrolled transition in case of error in MCU which sets the ERROR_PIN_FAIL and WD_FAIL status bits in the SAFETY_ERR_STATUS register and causes transition to the SAFE state and Device Error Count is incremented.
- Enters from RESET, DIAGNOSTIC, or ACTIVE state after ABIST or LBIST failure.
- Every transition to the SAFE state increments the error count.
- Stays in SAFE state when NO_SAFE_TO = 1 (default state) and DEV_ERR_CNT = SAFE_LOCK_THR + 1 which allows programming the MCU without triggering a reset.
- NRES is pulled high, but the ENDRV pin is kept low regardless of the watchdog fail count value, VDDx_OV and ENABLE_DRV bit.
- VDDx regulators are up and running, and the VSOUT1 regulator maintains the same state as configured in ACTIVE state.

5.4.1.24 State Transition Priorities

For all global or possible double-state transitions, the following priorities hold true:

1. All conditions for STANDBY state transition
2. All conditions for RESET state transition
3. All conditions for SAFE state transition

All other state transitions have a lower priority compared to any of the state transitions previously listed.

5.5 Register Maps

5.5.1 SPI Interface

The primary communication between the IC and the external the MCU is through an SPI bus which provides full-duplex communications in a master-slave configuration. The external MCU is always an SPI master which sends command requests on the SDI pin, and receives device responses on the SDO pin. The TPS65381-Q1 device is always an SPI slave device which receives command requests and sends responses (status, measured values) to the external MCU over the SDO line.

- SPI is a 4-pin interface.
  - NCS—SPI chip select (active-low)
  - SCLK—SPI clock
  - SDI—SPI slave-in / master-out (SIMO)
  - SDO—SPI slave-out / master-in (SOMI, three-state output)
- Frame size is 16 bits.
- Speed is up to 6 Mbit/s.
- Commands and data are shifted MSB first, LSB last.
- The SDI line is sampled on the falling edge of SCLK.
- The SDO line is shifted out on the rising edge of SCLK.

The SPI communication starts with the NCS falling edge, and ends with NCS rising edge. The NCS high level keeps the SPI slave interface in the reset state, and the SDO output is tri-stated.

5.5.1.1 SPI Command Transfer Phase

Table 5-15 lists the SPI command-transfer frame during a command or read access.

Table 5-15. SPI Command Transfer Phase

BIT	D7	D6	D5	D4	D3	D2	D1	D0
FUNCTION	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	PARITY

CMD[6:0]	Register WR or RD command
PARITY	Parity bit for 7-bit command filed

The SPI Interface does not support back-to-back SPI frame operation. After each SPI command or read access, the NCS pin must go from low to high before the next SPI transfer can start. The minimum time (t_{hlcs}) between two SPI commands during which the NCS pin must remain high is 788 ns.

5.5.1.2 SPI Data-Transfer Phase

Table 5-16 lists the SPI data-transfer frame format during a write access:

Table 5-16. SPI Data-Transfer Phase

BIT	D7	D6	D5	D4	D3	D2	D1	D0
FUNCTION	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

DATA[7:0]	Data value for write access (8-bit)

The SPI interface does not support back-to-back SPI frame operation. After each SPI transfer, the NCS pin must go from low to high before the next SPI transfer can start. The minimum time (t_{hlcs}) between two SPI commands during which the NCS pin must remain high is 788 ns.

5.5.1.3 Device Status Flag Byte Response

Table 5-17 lists the SPI data status response frame format during a command, read access, or write access:

Table 5-17. Device Status Flag Byte Response

BIT	R7	R6	R5	R4	R3	R2	R1	R0
FUNCTION	STAT[7]	STAT[6]	STAT[5]	STAT[4]	STAT[3]	STAT[2]	STAT[1]	STAT[0]

- STAT[7]: 1
- STAT[6]: 0
- STAT[5]: 1
- STAT[4]: 0
- STAT[3]: SPI WR access (during previous SPI frame-command phase)
- STAT[2]: SPI SDO error (during previous SPI frame)
- STAT[1]: 0
- STAT[0]: Invalid SPI transfer

The status bits sent during the current SPI command are reflecting the status of the previous SPI command.

NOTE

If a reset to the MCU is asserted during a SPI frame transfer (causing a truncated SPI frame), these SPI Error Status bits are not cleared, but maintain the status according to the truncated previous SPI frame until SPI Read access.

5.5.1.4 Device SPI Data Response

Table 5-18 lists the device SPI data-response frame format during a read access:

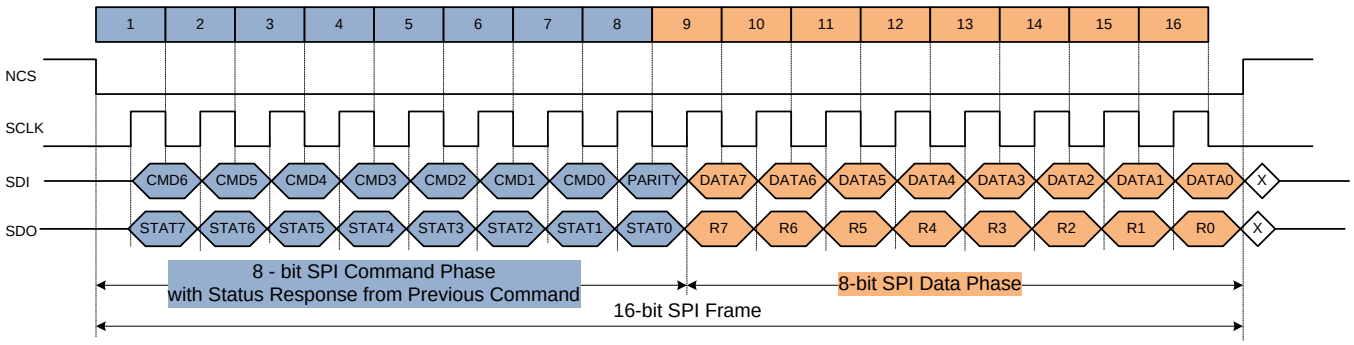
Table 5-18. Device SPI Data Response

BIT	R7	R6	R5	R4	R3	R2	R1	R0
FUNCTION	R7	R6	R5	R4	R3	R2	R1	R0

- R[7:0] Internal register value. All unused bits are set to zero.

5.5.1.5 SPI Frame Overview

Figure 5-17 shows an overview of a complete 16-bit SPI Frame:



SPI Master (MCU) and SPI Slave (TPS65381) sample received data on the falling SCLK edge and transmit on the rising SCLK edge.

Figure 5-17. 16-Bit SPI Frame

5.5.2 Device SPI Mapped Response

The following tables list the available SPI registers. For each SPI register, the bit names are given along with the default values (values after internal logic reset). These default values apply after each wake-up from IGN or CANWU. The following tables also list an explanation of each bit function.

5.5.2.1 Device Revision and ID

5.5.2.1.1 DEV_REV Register

Read command: ***RD_DEV_REV***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]
0	0	1	1	0	0	0	0

D[7:0] **REV[7:0]**: Device Revision
- REV[3:0]: Device minor revision
- REV[7:4]: Device major revision

5.5.2.1.2 DEV_ID Register

Read command: ***RD_DEV_ID***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]
0	0	0	0	0	0	0	1

5.5.2.2 Device Status

5.5.2.2.1 DEV_STATE Register

Read command: ***RD_DEV_STAT***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	RSV	RSV	CANWU_L	IGN
0	0	0	0	0	0	X	X

D[7:2] RSV

D[1] **CANWU_L**: Latched CAN wake-up event
- The reset value depends on whether a device wake-up event occurred through the CANWU or IGN pin. When a device wake-up occurred through a CANWU, only WR_CAN_STBY command, or any other global Standby condition, this bit can clear to 0

D[0] **IGN**: Deglitched IGN pin (7.5-ms to 22-ms deglitch time)
- The reset value depends on whether a device wake-up event occurred through the CANWU or IGN pin. This bit follows the deglitched IGN signal, and therefore is only cleared to 0 when the deglitched IGN is low or by any other global STANDBY condition

5.5.2.3 Device Configuration

5.5.2.3.1 DEV_CFG1 Register

Read command: ***RD_DEV_CFG1*** *Write command:* ***WR_DEV_CFG1***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
VDD_3_5_SEL	nMASK_VDD1_UV_OV	RSV	RSV	RSV	RSV	RSV	RSV
X	0	0	0	0	0	0	0

D[7] **VDD_3_5_SEL**: Status bit of VDD3/VDD5 selection at power up
- SEL_VDD3/5 input pin is sampled and latched at power up
  - 0: 5-V setting (pin SEL_VDD3/5 to ground)
  - 1: 3.3-V setting (pin SEL_VDD3/5 not connected)
  - Value in RESET state depends on state of SEL_VDD3/5 pin at first power up
- This bit is READ-ONLY

  (NOTE: Same as SAFETY_FUNC_CFG bit D0)

D[6] **nMASK_VDD1_UV_OV**
- Set to 0 per default:
  - Masked VDD1_OV does not impact ENDRV pin state
  - Masked VDD1_UV does not impact NRES state
- The default setting (0, masked) can be used in case VDD1 is not used in an application and external power FET is not populated.

  Note: If VDD1 is used in an application, TI recommends to set this bit to 1 when the device is in the DIAGNOSTIC state after the first start-up or power-up event.

  Note: Even if this bit is set to 1, but the VDD1_SENSE pin is externally floating, the pin will be pulled up. The pull up condition will be detected but the VDD1_OV condition will be masked and ENDRV pin state will not be impacted.

D[5:0] RSV

5.5.2.3.2 DEV_CFG2 Register

Read command: ***RD_DEV_CFG2*** *Write command:* ***WR_DEV_CFG2***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
EN_VDD3/5_OT	EN_VDD5_OT	MASK_VBATP_OV	POST_RUN_RST	RSV	RSV	RSV	RSV
1	1	0	0	0	0	0	0

D[7] **EN_VDD3/5_OT**
- Set to 1 by default.
- When set to 0 and an overtemperature event is detected, VDD3/5 supply is disabled
- When set to 1 and an overtemperature event is detected the device enters STAND-BY state.

D[6] **EN_VDD5_OT**
- Set to 1 by default. Clearing this bit to 0 disables the VDD5 overtemperature shutdown. The VDD5_OT flag is still present in SAFETY_STAT_REG1 bit D1.

D[5] **MASK_VBATP_OV**
- Set to 0 by default. When set 1, VBATP_OV is masked from the RESET condition.

D[4] **POST_RUN_RST**: Set to 0 per default. If this bit is set to 1 when using the IGN_PWRL function, a re-cracking on the IGN pin causes the device to go to the RESET state.

D[3:0] RSV (bits are readable and writable in DIAGNOSTIC state with no impact to device state, ENDRV and NRES output)

5.5.3 Device Safety Status and Control Registers

5.5.3.1 VMON_STAT_1 Register

Read command: ***RD_VMON_STAT_1***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
VBATP_OV	VBATP_UV	VCP17_OV	VCP12_OV	VCP12_UV	AVDD_VMON_ERR	BG_ERR2	BG_ERR1
0	0	0	0	0	0	0	0

D[7] **VBATP_OV**: VBATP overvoltage status bit
- Set to 1 when VBATP overvoltage is detected
- Cleared to 0 if an overvoltage condition is no longer present

D[6] **VBATP_UV**: VBATP undervoltage status bit
- Set to 1 when VBATP undervoltage is detected
- Cleared to 0 if an undervoltage condition is no longer present

D[5] **VCP17_OV**: VCP17 overvoltage status bit
- Set to 1 when VCP17 overvoltage is detected
- Cleared to 0 if an overvoltage condition is no longer present

D[4] **VCP12_OV**: VCP12 overvoltage status bit
- Set to 1 when VCP12 overvoltage is detected
- Cleared to 0 if an overvoltage condition is no longer present

D[3] **VCP12_UV**: VCP12 undervoltage status bit
- Set to 1 when VCP12 undervoltage is detected
- Cleared to 0 if an undervoltage condition is no longer present

D[2] **AVDD_VMON_ERR**: voltage-monitor power-supply power-good status
- Set to 1 when voltage-monitor power supply is not OK.
- Cleared to 0 if an error condition is no longer present

D[1] **BG_ERR2**: Reference bandgap 2 error
- Set to 1 when the voltage monitor is less than the main band gap
- Cleared to 0 if an error condition is no longer present

D[0] **BG_ERR1**: Reference bandgap 1 error
- Set to 1 when the voltage monitor is greater than the main band gap
- Cleared to 0 if an error condition is no longer present

5.5.3.2 VMON_STAT_2 Register

Read command: ***RD_VMON_STAT_2***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
VDD6_OV	VDD6_UV	VDD5_OV	VDD5_UV	VDD3/5_OV	VDD3/5_UV	VDD1_OV	VDD1_UV
0	0	0	0	0	0	0	0

D[7] **VDD6_OV**: VDD6 overvoltage status bit
- Set to 1 when VDD6 overvoltage is detected
- Cleared to 0 if an overvoltage condition is no longer present

D[6] **VDD6_UV**: VDD6 undervoltage status bit
- Set to 1 when VDD6 undervoltage is detected
- Cleared to 0 if an undervoltage condition is no longer present

D[5] **VDD5_OV**: VDD5 overvoltage status bit
- Set to 1 when VDD5 overvoltage is detected
- Cleared to 0 if an overvoltage condition is no longer present

D[4] **VDD5_UV**: VDD5 undervoltage status bit
- Set to 1 when VDD5 undervoltage is detected
- Cleared to 0 if an undervoltage condition is no longer present

D[3] **VDD3/5_OV**: VDD3/5 overvoltage status bit
- Set to 1 when VDD3/5 overvoltage is detected
- Cleared to 0 if an overvoltage condition is no longer present

D[2] **VDD3/5_UV**: VDD3/5 undervoltage status bit
- Set to 1 when VDD3/5 undervoltage is detected
- Cleared to 0 if an undervoltage condition is no longer present

D[1] **VDD1_OV**: VDD1 overvoltage status bit
- Set to 1 when VDD1 overvoltage is detected
- Cleared to 0 if an overvoltage condition is no longer present

D[0] **VDD1_UV**: VDD1 undervoltage status bit
- Set to 1 when VDD1 undervoltage is detected
- Cleared to 0 if an undervoltage condition is no longer present

5.5.3.3 SAFETY_STAT_1 Register

Read command: ***RD_SAFETY_STAT_1***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
VDD5_ILIM	VDD3_5_ILIM	VSOUT1_UV	VSOUT1_OV	VSOUT1_ILIM	VSOUT1_OT	VDD5_OT	VDD_3_5_OT
0	0	0	0	0	0	0	0

D[7] **VDD5_ILIM**: VDD5 current-limit status bit
- Set to 1 when a VDD5 current-limit is exceeded
- Cleared to 0 if a current-limit condition is no longer present

  Note: This status bit is valid only when VDD5_EN bit in SENS_CTRL register is set to 1.

D[6] **VDD3_5_ILIM**: VDD3 current-limit status bit
- Set to 1 when a VDD3 current-limit is exceeded
- Cleared to 0 if a current-limit condition is no longer present

D[5] **VSOUT1_UV**: Sensor-supply undervoltage status bit
- Set to 1 when a VSOUT1 undervoltage is detected
- Cleared to 0 if an undervoltage condition is no longer present

D[4] **VSOUT1_OV**: Sensor-supply overvoltage status bit
- Set to 1 when a VSOUT1 overvoltage is detected
- Cleared to 0 if an overvoltage condition is no longer present

D[3] **VSOUT1_ILIM**: VSOUT1 sensor-supply current-limit status bit
- Set to 1 when a VSOUT current-limit is exceeded
- Cleared to 0 if a current-limit condition is no longer present

D[2] **VSOUT1_OT**: Sensor-supply overtemperature status bit
- Set to 1 when VSOUT overtemperature is exceeded. This bit keeps VSOUT1 regulator disabled as long as this bit is set.
- Cleared to 0 if an overtemperature condition is no longer present

D[1] **VDD5_OT**: VDD5 overtemperature status bit
- Set to 1 when VDD5 overtemperature is exceeded. This bit keeps VDD5 regulator disabled as long as this bit is set by clearing the VDD5_EN control bit in SENS_CTRL register
- Cleared to 0 if an overtemperature condition is no longer present

D[0] **VDD_3_5_OT**: VDD3/5 overtemperature status bit
- Set to 1 when VDD3/5 overtemperature is exceeded. This bit keeps VDD3/5 regulator disabled as long as this bit is set to 1.
- Cleared to 0 if an overtemperature condition is no longer present

5.5.3.4 SAFETY_STAT_2 Register

Read command: ***RD_SAFETY_STAT_2***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	CFG_CRC_ERR	EE_CRC_ERR	RSV	WDT_FAIL_CNT[2]	WDT_FAIL_CNT[1]	WDT_FAIL_CNT[0]
0	0	0	0	0	1	0	1

D[7:6] RSV

D[5] **CFG_CRC_ERR**: CRC Error status bit for safety configuration registers

- Safety configuration registers are protected by CRC8.
- This bit is set to 1 when the calculated CRC8 value for safety configuration registers does not match the expected CRC8 value stored in the SAFETY_CFG register.
- Cleared to 0 when a CRC8 mismatch is no longer present.
- Cleared to 0 when EEPROM CRC performs without error (regardless of CFG_CRC check result)

D[4] **EE_CRC_ERR**: EPROM CRC error status bit

- EEPROM content is protected by CRC8.
- This bit is set to 1 when the calculated CRC8 value does not match the expected CRC8 value stored in the EEPROM DFT register. When this bit is set to 1 and device is in the DIAGNOSTIC state, the device transitions to SAFE state.
- Cleared to 0 when a CRC8 mismatch is no longer present.

D[3] RSV

D[2:0] **WDT_FAIL_CNT[2:0]**: Watchdog failure counter state

- The default value is 5, and is initialized to this value upon entering DIAGNOSTIC and ACTIVE state
- Watchdog failure counter is incremented every time the device watchdog-response failure is detected and decreases each time the correct response is received.
- Watchdog failure counter must decrease below 5 to enable the ENABLE_DRV output pin.
- Watchdog failure is detected on the next bad event
  after the watchdog failure counter reached the count of 7 (that is 7+1) and the WD_FAIL status bit is set to 1 in the SAFETY_ERR_STAT register (setting the WD_FAIL bit to 1 in the SAFETY_ERR_STAT register).

5.5.3.5 SAFETY_STAT_3 Register

Read command: ***RD_SAFETY_STAT_3***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	NRES_ERR	LBIST_ERR	ABIST_UVOV_ERR	ABIST_UVOV_ERR	LBIST_RUN	ABIST_RUN
0	0	0	0	0	0	0	0

D[7:6] RSV

D[5] **NRES_ERR**: Reset error input status
- This bit is set to 1 when a mismatch between NRES output and NRES input feedback is detected.
- Cleared to 0 after SPI Read access if no failure is present anymore.

D[4] **LBIST_ERR**: Logic BIST error-status bit
- This bit is set to 1 when logic BIST fails
- Cleared to 0 after repeated LBIST run completed without failure, followed by SPI read access
- Only valid when the LBIST_RUN bit is 0

D[3] **ABIST_UVOV_ERR**: Analog BIST undervoltage and overvoltage BIST error-status bit
- This bit is set to 1 when analog undervoltage and overvoltage BIST fails. If this bit is set to 1 and device is in DAIGNOSTIC state, device transitions to SAFE state.
- Cleared to 0 after SPI read access
- Only valid when the ABIST_RUN bit is 0

D[2] **ABIST_UVOV_ERR**: Analog BIST undervoltage and overvoltage BIST error-status bit (identical to D3)
- This bit is set to 1 when analog undervoltage and overvoltage BIST fails. If this bit is set to 1 and device is in DAIGNOSTIC state, device transitions to SAFE state.
- Cleared to 0 after SPI read access
- Only valid when the ABIST_RUN bit is 0

D[1] **LBIST_RUN**: Logic BIST run-status bit
- This bit is set to 1 when a logic BIST is running.
- Cleared to 0 after a logic BIST is finished running.

D[0] **ABIST_RUN**: Analog BIST run-status bit
- This bit is set to 1 when an analog BIST is running.
- Cleared to 0 after a analog BIST is finished running.

5.5.3.6 SAFETY_STAT_4 Register

Read command: ***RD_SAFETY_STAT_4***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
SPI_ERR[1]	SPI_ERR[0]	LOCLK	RSV	MCU_ERR	WD_ERR	ENDRV_ERR	TRIM_ERR_VMON
0	0	0	0	0	0	0	0

D[7:6] **SPI_ERR[1:0]**: SPI error-status bits

00: No error

01: Command error

10: Format error (received bit count is not equal to 16)

11: Data output mismatch

– Cleared to 0 after SPI read access.

Note: If a reset to the MCU is asserted during an SPI frame transfer (causing a truncated SPI frame), these SPI error status bits are not cleared, but maintain the status according to the truncated previous SPI frame until SPI read access

D[5] **LOCLK**: Loss of clock-detection status bit

– Set when loss-of-clock failure is detected

– Cleared to 0 after internal NPOR and if clock failure is no longer present.

D[4] RSV

D[3] **MCU_ERR**: MCU error monitor status bit

– This bit is set to 1 when MCU error-signal monitoring module detects MCU_ERROR pin failure on ERROR/WDI pin.

– Cleared to 0 after SPI read access and if bit ERROR_PIN_FAIL in SAFETY_ERR_STAT is cleared

D[2] **WD_ERR**: Watchdog error-status bit

– This bit is set to 1 when on the next bad event
once the watchdog fail counter reaches a count of 7 (that is 7+1) (WD_FAIL_CNT [2:0] in SAFETY_STATUS_2 register) only if bit WD_RST_EN (SAFETY_FUNC_CFG, bit 3) is set to 1

– Cleared to 0 after SPI read access when watchdog fail counter is less than 7

D[1] **ENDRV_ERR**: Enable driver error

– This bit is set to 1 when a mismatch between the EN_DRV output and EN_DRV input feedback is detected.

– Cleared to 0 if failure is no longer present

D[0] **TRIM_ERR_VMON**: VMON trimming error-status bit

– This bit is set to 1 when mismatch voltage-monitor trim error is detected.

– Cleared to 0 after internal NPOR and if failure is not present anymore.

5.5.3.7 SAFETY_STAT_5 Register

Read command: ***RD_SAFETY_STAT_5***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	RSV	FSM[2]	FSM[1]	FSM[0]
0	0	0	0	0	0	1	1

D[2:0] **FSM[2:0]**: Current device state

– Reflects current device state

- STANDBY state: 8'h00
- RESET state: 8'h03
- DIAGNOSTIC state: 8'h07
- ACTIVE state: 8'h05
- SAFE state: 8'h04

5.5.3.8 SAFETY_ERR_CFG Register

Read command: ***RD_SAFETY_ERR_CFG*** *Write command:* ***WR_SAFETY_ERR_CFG***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
SAFE_TO [2]	SAFE_TO [1]	SAFE_TO [0]	SAFE_LOCK_THR [3]	SAFE_LOCK_THR [2]	SAFE_LOCK_THR [1]	SAFE_LOCK_THR [0]	CFG_LOCK
0	0	0	0	0	0	0	0

D[7:5] SAFE_TO[2:0]: SAFE state time-out settings

- Duration of SAFE state is time-limited to protect against potential MCU *locked* state.
- Time-out duration = (2 × SAFE_TO[2:0] + 1) × 22 ms
- Minimum duration is 22 ms
- Maximum duration is 330 ms
- 22-ms time reference has 5% accuracy coming from 4-MHz internal oscillator)

D[4:1] SAFE_LOCK_THR[3:0]

- Sets the corresponding device ERR_CNT threshold at which device remains in SAFE state regardless of time-out event
- When NO_SAFE_TO bit (SAFETY_FUNC_CFG register, bit 7) is set to 1:
  - While ERR_CNT < SAFE_LOCK_THR + 1, time-delay transition from SAFE-to-RESET state is controlled through SAFE_TO[2:0] bit settings. Time-delay duration is calculated (SAFE_TO[2:0] × 2 + 1) × 22 ms
  - Device remains *locked* in SAFE state when ERR_CNT reaches SAFE_LOCK_THR + 1 value.
- When NO_SAFE_TO bit (SAFETY_FUNC_CFG register, bit 7) is set to 0:
  - While ERR_CNT < SAFE_LOCK_THR + 1, time-delay transition from SAFE-to-RESET state is controlled through SAFE_TO[2:0] bit settings. Time-delay duration is calculated (SAFE_TO[2:0] × 2 + 1) × 22 ms
  - When ERR_CNT reaches SAFE_LOCK_THR + 1 value, device transitions to RESET state after 680 ms.
- Intended to support software debug and development and is NOT recommended for normal functional operation.
- The 0000 setting is the default setting, and has same effect as the 1111 setting. Both settings give the minimum threshold.

D[0] CFG_LOCK

- Register lock access control
- When set to 1, the register content cannot be updated by SPI WR access.

5.5.3.9 SAFETY_BIST_CTRL Register

Read command: ***RD_SAFETY_BIST_CTRL*** *Write command:* ***WR_SAFETY_BIST_CTRL***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
BIST_DEG_CNT[1]	BIST_DEG_CNT[0]	AUTO_BIST_DIS	EE_CRC_CHK	RSV	LBIST_EN	ABIST_EN	ABIST_EN
0	0	0	0	0	0	0	0

D[7:6] BIST_DEG_CNT[1:0]: Deglitch filter duration setting during active analog BIST

- This bit controls deglitch filter duration for every safety monitored voltage.
- Resolution is 15 µs (with the minimum setting at 15 µs and the maximum setting at 60 µs): bist_deglitch = (BIST_DEG_CNT[1:0] + 1) × 15 µs)
- 15-µs time reference has 5% accuracy coming from 4-MHz internal oscillator.
- When the ABIST is run in ACTIVE state, TI recommends to set this to the maximum deglitch time

D[5] AUTO_BIST_DIS

- This bit controls automatic BIST start-up in RESET state ONLY when device enters RESET sate from DIAGNOSTIC, ACTIVE, or SAFE state.
- When set to 1, automatic BIST start-up is disabled.

D[4] EE_CRC_CHK: Recalculate EEPROM CRC8

- This bit controls the EEPROM CRC8 check function
- When set to 1, EEPROM content is reloaded and CRC8 re-calculated and compared against expected value stored in EEPROM DFT register.

  Note: With every power-up event, EEPROM content is reloaded and its CRC8 re-calculated.
- The self-test status is checked through bit 4 in SAFETY_STATUS_2 register.

D[3] RSV, readable and writable without effect

D[2] LBIST_EN: Enable digital BIST run

- This bit controls the logic BIST run
- The self-test status is monitored through bits D1 and D4 in the SAFETY_STAT_3 register.
- LBIST_EN clears the DIAG_EXIT_MASK bit to 0. The time-out counter only stops during the running of LBIST. After LBIST completes, the time-out counter continues from last value. To stay in the DIAGNOSTIC state, the DIAG_EXIT_MASK bit must be set to 1 after LBIST completion. For transition from the DIAGNOSTIC state to the ACTIVE state, the DIAG_EXIT bit must be set to 1.

D[1] ABIST_EN: Enable analog BIST run (same as D[0])

- This bit controls the analog UV,OV and LOC BIST run.
- The self-test status is monitored through bits D0, D2, and D3 in the SAFETY_STAT_3 register, and bit D5 in the SAFETY_STAT4 register.

D[0] ABIST _EN: Enable analog BIST run (same as D[1])

- The bit controls the analog UV, OV, and LOC BIST run.
- The self-test status is monitored through bits D0, D2, and D3 in the SAFETY_STAT_3 register, and bit D5in the SAFETY_STAT4 register.

5.5.3.10 SAFETY_CHECK_CTRL Register

Read command: ***RD_SAFETY_CHECK_CTRL*** *Write command:* ***WR_SAFETY_CHECK_CTRL***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
CFG_CRC_EN	RSV	ENABLE_DRV	RSV	RSV	NO_ERROR	DIAG_EXIT_MASK	DIAG_EXIT
0	0	0	1	0	1	0	0

D[7] CFG_CRC_EN

- Controls the enabling of CRC8 protection for the device configuration registers.
- When set to 1, CRC8 is calculated for all device configuration registers and compared with the CRC8 value stored in the SAFETY_CFG_CRC register.
- TI recommends to first to set the desired device configuration, followed by updating the SAFTY_CFG_CRC register before setting this bit to 1.
- The following registers are protected:
  - SAFETY_FUNC_CFG register
  - DEV_REV (device revision) register
  - SAFETY_PWD_THR_CFG register
  - SAFETY_ERR_CFG register
  - WDT_TOKEN_CFG register
  - WDT_WIN1_CFG register
  - WDT_WIN2_CFG register
  - SAFETY_ERR_PWM_L register
  - DEV_CFG2 register
  - DEV_CFG1 register (only bit D6)

D[6] RSV, readable and writeable with no impact to device state, ENDRV, and NRES output

D[5] ENABLE_DRV

- Controls the enabling of the ENDRV output
- In addition to setting this bit to 1, the watchdog failure counter must be decremented below the default count value of 5 to enable the ENDRV output.

D[4:3] RSV, readable and writeable with no impact to device state, ENDRV, and NRES output

D[2] NO_ERROR

- Controls the enabling of the MCU_ERROR pin-monitor function (through the device ERROR/WDI pin) and transition from the ACTIVE state to the SAFE state when an MCU_ERROR pin failure is detected.
  - 1: MCU_ERROR pin failure is not monitored, but a detected failure in the ACTIVE state does not cause a transition to the SAFE state.
  - 0: MCU_ERROR pin failure is monitored, and a detected failure in the ACTIVE state causes a transition to the SAFE state.
- If an MCU_ERROR pin failure is detected, the ERROR_PIN_FAIL status bit in the SAFETY_ERR_STAT register is set, only for setting NO_ERROR = 0.
  - ERROR_PIN_FAIL status bit in SAFETY_ERR_STAT register, and MCU_ERR status bit in SAFETY_STAT_4 are set

D[1] DIAG_EXIT_MASK

- Controls the exit from the DIAGNOSTIC state
- When set to 1, exit from the DIAGNOSTIC state is disabled regardless if a time-out event occurs or if the DIAG_EXIT bit is set.
- This feature is only recommended for software debug and development and must not be activated in functional mode.

D[0] DIAG_EXIT

- Controls exit from the DIAGNOSTIC state.
- When set to 1 and the DIAG_EXIT_MASK bit is 0, the device transitions from the DIAGNOSTIC to the ACTIVE state.

5.5.3.11 SAFETY_FUNC_CFG Register

Read command: ***RD_SAFETY_FUNC_CFG*** *Write command:* ***WR_SAFETY_FUNC_CFG***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
NO_SAFE_TO	ERROR_CFG	WD_CFG	IGN_PWRL	WD_RST_EN	DIS_NRES_MON	RSV	VDD_3_5_SEL
1	0	0	0	0	1	0	X

D[7] NO_SAFE_TO

– Controls the enabling and disabling of the SAFE state time-out function

– When set to 1, the SAFE state time-out is disabled. Device remains *locked* in the SAFE state when ERR_CNT reaches the SAFE_LOCK_THR + 1 value.
– When set to 0, SAFE state time-out is enabled. The device transitions to the RESET state after 680 ms when ERR_CNT reaches the SAFE_LOCK_THR + 1 value.

D[6] **ERROR_CFG**: MCU Error Signal Monitor configuration bit

– When set to 0, PWM monitoring is enabled (can be used as an external clock monitor). Expected ERROR/WDI pin LOW and HIGH durations are controlled by the SAFETY_ERR_PWM_H and SAFETY_ERR_PWM_L registers (see Section 5.5.3.13 and Section 5.5.3.14, respectively).

– When set to 1, the TMS570 ERROR pin mode is enabled. The ERROR pin low-duration threshold is set by the SAFETY_ERR_PWM_L register.

D[5] **WD_CFG**: Watchdog function configuration bit

– When set to 0: WDTI configuration enabled (default) – watchdog trigger input through ERROR/WDTI pin

– When set to 1: Q&A WD configuration enabled – watchdog trigger input through SPI

D[4] **IGN_PWRL**: Ignition-power latch control bit

– Controls the enabling of the ignition-power latch

Note: This bit can only be changed when the device is in DIAGNOSTIC state

– When set to 1, the user can pull the ignition input LOW, but the device remains powered up.

– When cleared to 0 with IGN input pin LOW, device enters STANDBY state. Cleared by a CANWU event

D[3] WD_RST_EN

– 1: Watchdog failure is detected when WD_FAIL_CNT[2:0] reaches the count of 7 (in the SAFETY_STAT_2 register), leading to a transition to the RESET state.

– 0: Watchdog failure events are detected, but device does not transition to RESET state when WD_FAIL_CNT reaches count of 7.

D[2] DIS_NRES_MON

– When set to 1 (default state): NRES monitoring is disabled.

– When set to 0: NRES monitoring is enabled. In this case and device in ACTIVE state, a difference between NRES pin state and NRES driver state (for example: the bit NRES_ERR in SAFETY_STAT_3) will cause a transition to SAFE state

D[1] RSV, readable and writeable in DIAGNOSTIC state with no impact to device state, ENDRV and NRES output

D[0] **VDD_3_5_SEL**: Status bit of VDD3/VDD5 selection at power up

– SEL_VDD3/5 input pin is sampled and latched at power up

- 0: 5-V setting (pin SEL_VDD3/5 not connected)
- 1: 3.3-V setting (pin SEL_VDD3/5 connected to ground)
- Value in RESET state depends on state of SEL_VDD3/5 pin at first power up

– This bit is READ-ONLY

Note: Same as DEV_CFG1 bit D7

5.5.3.12 SAFETY_ERR_STAT Register

Read command: ***RD_SAFETY_ERR_STAT*** *Write command:* ***WR_SAFETY_ERR_STAT***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	ERROR_PIN_FAIL	WD_FAIL	DEV_ERR_CNT[3]	DEV_ERR_CNT[2]	DEV_ERR_CNT[1]	DEV_ERR_CNT[0]
0	0	0	0	0	0	0	0

D[7:6] RSV

D[5] ERROR_PIN_FAIL

– Set to 1 when the MCU Error Signal Monitoring Module detects MCU_ERROR pin failure on ERROR/WDI pin, only if NO_ERROR = 0 (bit D2 in SAFETY_CHECK_CTRL register). Device enters SAFE state when this ERROR_PIN_FAIL bit is set to 1

– Cleared to 0 after SPI WR access or cleared to 0 during reset event

D[4] WD_FAIL

– Set to 1 when the watchdog function failure counter reaches the count of 7 (WD_FAIL_CNT[2:0] in the SAFETY_STATUS_2 register) only if bit WD_RST_EN (SAFETY_FUNC_CFG, bit 3) is set to 1

– Cleared to 0 after SPI WR access when the watchdog fail counter is less than 7 or cleared to 0 during reset event

D[3:0] DEV_ERR_CNT[3:0]

– Tracks the current device error count.

– Overwritten by SPI WR access, but ONLY in the DIAGNOSTIC mode.

5.5.3.13 SAFETY_ERR_PWM_H Register

Read command: ***RD_SAFETY_ERR_PWM_H*** *Write command:* ***WR_SAFETY_PWM_H***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
PWMH[7]	PWMH[6]	PWMH[5]	PWMH[4]	PWMH[3]	PWMH[2]	PWMH[1]	PWMH[0]
1	0	1	0	1	0	0	0

D[7:0] PWMH[7:0]: ERROR pin high-phase duration in PWM mode (15-µs resolution)

– Controls the expected high-phase duration with 15-µs resolution

T_{PWM_HIGH} = (PWMH[7:0] + 1) × 15 µs

(15-µs time reference has 5% accuracy coming from 4-MHz internal oscillator)

5.5.3.14 SAFETY_ERR_PWM_L Register

Read command: ***RD_SAFETY_ERR_PWM_L*** *Write command:* ***WR_SAFETY_PWM_L***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
PWML[7]	PWML[6]	PWML[5]	PWML[4]	PWML[3]	PWML[2]	PWML[1]	PWML[0]
0	0	1	1	1	1	0	1

D[7:0] PWML[7:0]: ERROR pin low-phase duration

– Controls expected low-phase duration

- When the ERR_CFG bit is 0 (in PWM mode): ERR PWM low-phase duration with 15-µs resolution

  T_{PWM_LOW} = (PWML[7:0] + 1) × 15 µs

  (15-µs time reference has 5% accuracy coming from 4-MHz internal oscillator)
- When ERR_CFG bit is 1 (TMS570 mode): ERR low duration with 5-µs resolution

  $T_{TH\_LOW\_TMS570}$ = (PWML[7:0] + 1) × 5 µs

  (5-µs time reference has 5% accuracy coming from 4-MHz internal oscillator)

5.5.3.15 SAFETY_PWD_THR_CFG Register

Read command: ***RD_SAFETY_PWD_THR_CFG*** *Write command:* ***WR_SAFETY_PWD_THR_CFG***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	PWD_THR[3]	PWD_THR[2]	PWD_THR[1]	PWD_THR[0]
0	0	0	0	1	1	1	1

D[7:4] RSV

D[3:0] PWD_THR[3:0]: Device error-count threshold to power down the device

- When DEV_ERR_CNT reaches programmed threshold, the device powers down.
- The device recovers with a new wake-up or ignition event.
- This register can be updated only in DIAGNOSTIC mode.

5.5.3.16 SAFETY_CFG_CRC Register

Read command: ***RD_SAFETY_CFG_CRC*** *Write command:* ***WR_SAFETY_CFG_CRC***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
CFG_CRC[7]	CFG_CRC[6]	CFG_CRC[5]	CFG_CRC[4]	CFG_CRC[3]	CFG_CRC[2]	CFG_CRC[1]	CFG_CRC[0]
0	0	0	1	0	0	0	0

D[7:0] CFG_CRC[7:0]: CRC8 value for safety configuration registers

Note: Can be updated only in the DIAGNOSTIC state

5.5.3.17 Diagnostics

5.5.3.17.1 DIAG_CFG_CTRL Register

Read command: ***RD_DIAG_CFG_CTRL*** *Write command:* ***WR_DIAG_CFG_CTRL***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
MUX_EN	SPI_SDO	MUX_OUT	INT_CON[2]	INT_CON[1]	INT_CON[0]	MUX_CFG[1]	MUX_CFG[0]
0	0	0	0	0	0	0	0

D[7] **MUX_EN**: Enable diagnostic MUX output
- 0: Disabled (tri-stated)
- 1: Enabled

D[6] **SPI_SDO**: To control the SPI_SDO output-buffer state during an interconnect test

To check the SDO diagnostics use the following sequence:
- MUX_CFG configuration must be 0x1 (DIAG_CFG_CTRL register bits [1:0])
  => DIGITAL MUX mode
- SPI NCS must be kept HIGH
- The state of SDO is controlled by bit SPI_SDO

D[5] **MUX_OUT**: Diagnostic MUX output-state control bit

Note: When the MUX_CFG bits are set to 00 and the MUX_EN bit is set to 1

D[4:2] **INT_CON[2:0]**: Device interconnect-test configuration bits
- 000: No active interconnect test
- 001: ERR input state observed on diagnostic MUX output
- 010: SPI_NCS input state observed on diagnostic MUX output
- 011: SPI_SDI input state observed on diagnostic MUX output
- 100: SPI_SCLK input observed on diagnostic MUX output
- 101: Not applicable
- 110: Not applicable
- 111: Not applicable

D[1:0] **MUX_CFG**: Diagnostic MUX configuration
- 00: The MUX output is controlled by MUX_OUT bit (bit 5 in DIAG_CFG_CTRL register)
- 01: Digital MUX mode
- 10: Analog MUX mode
- 11: Device interconnect mode (input-pins interconnect test)

5.5.3.17.2 DIAG_MUX_SEL Register

Read command: ***RD_DIAG_MUX_SEL*** *Write command:* ***WR_DIAG_MUX_SEL***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
MUX_SEL[7]	MUX_SEL[6]	MUX_SEL[5]	MUX_SEL[4]	MUX_SEL[3]	MUX_SEL[2]	MUX_SEL[1]	MUX_SEL[0]
0	0	0	0	0	0	0	0

D[7:0] **MUX_SEL[7:0]**: Diagnostic MUX channel select

Note: The MUX channel table is dependent on the MUX_CFG[1:0] bit settings in the DIAG_CFG_CTRL register (see Section 5.5.3.17.1)

5.5.4 Watchdog Timer

5.5.4.1 WDT_TOKEN_FDBCK Register

Read command: ***RD_WDT_TOKEN_FDBCK*** *Write command:* ***WR_WDT_TOKEN_FDBCK***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
FDBK[3]	FDBK[2]	FDBK[1]	FDBK[0]	TOKEN_SEED[3]	TOKEN_SEED[2]	TOKEN_SEED[1]	TOKEN_SEED[0]
0	0	0	0	0	0	0	0

D[7:4] **FDBK[3:0]**: WDT token FSM feedback-configuration bits

- FDBK [3:0] bits control the sequence of generated questions and respective answers
- There is a set of 16 generated questions, but repetition or sequence ordering can be adjusted by FDBK[3:0] bits

D[3:0] **TOKEN_SEED[3:0]**: WDT token seed value

- The MCU updates the TOKEN seed value to generate a set of new TOKEN values
- New TOKEN seed values can be updated by the MCU only after watchdog function reinitialization:
  - The MCU must set the desired TOKEN seed value
  - After the device transitions through the RESET state the watchdog function is updated with the new seed value
- Only for Q&A WD configuration through SPI

5.5.4.2 WDT_WIN1_CFG Register

Read command: ***RD_WDT_WIN1_CFG*** *Write command:* ***WR_WDT_WIN1_CFG***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]
0	1	1	1	1	1	1	1

D[7] RSV

D[6:0] **RT[6:0]**: WDT open time window duration setting (for Q&A WD configuration through SPI) **or** WDT closed-window duration setting (for WDTI configuration through the ERROR/WDI pin).

- T_{WOW} (Q&A) = T_{WCW} (WDTI) = (RT[6:0]) × 0.55 ms
  (0.55-ms time reference has 5% accuracy coming from 4-MHz internal oscillator)

5.5.4.3 WDT_WIN2_CFG Register

Read command: ***RD_WDT_WIN2_CFG*** *Write command:* ***WR_WDT_WIN2_CFG***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RW[4]	RW[3]	RW[2]	RW[1]	RW[0]
0	0	0	1	1	0	0	0

D[7:5] RSV

D[4:0] **RW[4:0]**

- WDT closed-window duration setting (for QA WD configuration through SPI) or
  WDT open-window duration setting (for WDTI configuration through the ERROR/WDI pin).
- T_{WCW} (QA) = T_{WOW} (WDTI) = (RW[4:0]) × 0.55 ms
  (0.55-ms time reference has 5% accuracy coming from 4-MHz internal oscillator)

5.5.4.4 WDT_TOKEN_VALUE Register

Read command: ***RD_WDT_TOKEN_VALUE***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
WDFAIL_TH	RSV	RSV	RSV	TOKEN[3]	TOKEN[2]	TOKEN[1]	TOKEN[0]
1	0	0	0	0	0	0	0

D[7] **WDFAIL_TH**

- Set to 1 when the watchdog-function failure counter reaches a count of 4 or higher (WD_FAIL_CNT[2:0] in the SAFETY_STATUS_2 register)
- Set to 0 when the watchdog-function failure counter reaches a count of less than 4 (WD_FAIL_CNT[2:0] in the SAFETY_STATUS_2 register)

D[6:4] RSV

D[3:0] **TOKEN[3:0]**: WDT active TOKEN value (or WDT *question* value)

- The MCU must read (or calculate) the current WD token value to generate a correct SPI response (answers).

5.5.4.5 WDT_STATUS Register

Read command: ***RD_WDT_STATUS***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
WDT_ANSW_CNT [1]	WDT_ANSW_CNT [0]	TOKEN_ERR	WD_WRONG_CFG	WD_CFG_CHG	SEQ_ERR	TIME_OUT	TOKEN_ERLY
1	1	0	0	0	0	0	0

D[7:6] **WDT_ANSW_CNT[1:0]**: Current received WD answer count state

- Only for Q&A WD configuration through SPI

D[5] **TOKEN_ERR**: WD token error-status bit

- This bit is set to 1 as soon as one answer byte WD_TOKEN_RESPx is not correct. This flag is cleared if the following answer is correct again. This bit is not cleared on SPI read-out.
- Only for Q&A WD configuration through SPI

D[4] **WD_WRONG_CFG**

- Set to 1 when either WDT_WIN1_CFG or WDT_WIN2_CFG are set to 0x00

D[3] **WD_CFG_CHG**: WD configuration-change status bit

- This bit is set to 1 when switching between the WDTI configuration and Q&A configuration, or when the following occurs.
- Changing OPEN and CLOSE window timer settings

D[2] **SEQ_ERR**: The last token sequence is wrong

- Incorrect timing or the following
- Wrong answer
- Only for Q&A WD configuration through SPI

D[1] **TIME_OUT**: No watchdog trigger received within OPEN or CLOSE window (no-response event)

- In WDTI configuration (default configuration): set to 1 when no trigger event has been received on the ERROR/WDTI pin during an OPEN or CLOSE window
- In Q&A WD configuration: set to 1 when no ANSWERS have been received during an OPEN window
- This flag is used to synchronize the MCU watchdog triggers on the watchdog timer:
  - On transition from the RESET to the DIAGNOSTIC state, the MCU can poll this TIME_OUT flag directly after reboot to detect the completion of an OPEN or CLOSE window. In order to do so, the MCU must not send any trigger event on the ERROR/WDI pin directly after reboot, until this TIME_OUT flag is set.
  - After configuring the watchdog timer, watchdog mode (WDTI or Q&A), or both, the MCU must not send watchdog trigger events until this TIME_OUT flag is set to resynchronize with the OPEN and CLOSE timing.

D[0] **TOKEN_ERLY**: Token sequence completed too early

- Only for Q&A WD configuration through SPI
- Set to 1 if all four ANSWERS are returned during an OPEN window

5.5.4.6 WDT_ANSWER Register

Write command: ***WR_WDT_ANSWER***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
WDT_ANSW[7]	WDT_ANSW[6]	WDT_ANSW[5]	WDT_ANSW[4]	WDT_ANSW[3]	WDT_ANSW[2]	WDT_ANSW[1]	WDT_ANSW[0]
0	0	0	0	0	0	0	0

D[7:0] **WDT_ANSW[7:0]**: MCU watchdog answer response

- Each WDT token (question) requires four 8-bit answers
- Three 8-bit answers (SPI responses) must be returned during OPEN WDT window
- The fourth (last) 8-bit answer must be returned during CLOSE WDT window
- The number of returned answers is tracked with the WDT_ANSW_CNT [1:0] bits in the WDT_STATUS register
- Only for Q&A WD configuration through SPI

5.5.5 Sensor Supply

5.5.5.1 SENS_CTRL Register

Read command: ***RD_SENS_CTRL*** *Write command:* ***WR_SENS_CTRL***

DATA INFORMATION							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	VDD5_EN	RSV	RSV	RSV	VSOUT1_EN
0	0	0	1	0	0	0	0

D[7:5] RSV

D[4] **VDD5_EN**: If cleared to 0, VDD5 then turns off.

- This bit is set to 1 by default, and is cleared in case of VDD5 over-temperature (indicated by the VDD5_OT bit D1 in SAFETY_STAT1).

  Note: When VDD5 is disabled, bit VDD5_ILIM (bit D7 in SAFETY_STAT_1) is set to 1 and remains set to 1 as long as VDD5 is disabled (or VDD5_EN bit is 0).

D[3:1] RSV

D[0] **VSOUT1_EN**: Sensor-supply enable bit (set this bit to 1 to enable the VSOUT1 sensor supply)

- This bit is set to 0 by default, and must be set to 1 by the MCU to enable VSOUT1. In case of VSOUT1 over-temperature (indicated by VSOUT1_OT bit D2 in SAFETY_STAT1), VSOUT1 is disabled; however this bit, VSOUT1_EN, remains set to 1. As soon as the over-temperature in VSOUT1 has disappeared, VSOUT1 is re-enabled.

5.5.6 SPI Command Table

8-BIT HEX COMMAND CODE (WITH PARITY)	7-BIT HEX COMMAND CODE (WITHOUT PARITY)	7-BIT BINARY COMMAND CODE (WITHOUT PARITY)	PARITY	WR SW LOCK PROTECT	REGISTER COMMAND NAME(1)
BD	5E	1011 110	1	N/A	SW_LOCK with data 0xAA (to lock SPI WR access to listed registers)
BB	5D	1011 101	1	N/A	SW_UNLOCK with data 0x55 (to unlock SPI WR access to listed registers)
06	03	0000 011	0	N/A	RD_DEV_ID
0C	06	0000 110	0	N/A	RD_DEV_REV
B7	5B	1011 011	1	YES	WR_DEV_CFG1 (SPI WR update can occur only in DIAGNOSTIC state)
AF	57	1010 111	1	N/A	RD_DEV_CFG1
95	4A	1001 010	1	YES	WR_DEV_CFG2 (SPI WR update can occur only in DIAGNOSTIC state)
48	24	0100 100	0	N/A	RD_DEV_CFG2
7D	3E	0111 110	1	NO	WR_CAN_STBY
24	12	0010 010	0	N/A	RD_SAFETY_STAT_1
C5	62	1100 010	1	N/A	RD_SAFETY_STAT_2
A3	51	1010 001	1	N/A	RD_SAFETY_STAT_3
A5	52	1010 010	1	N/A	RD_SAFETY_STAT_4
C0	60	1100 000	0	N/A	RD_SAFETY_STAT_5
30	18	0011 000	0	N/A	RD_SAFETY_ERR_CFG
DB	6D	1101 101	1	YES	WR_SAFETY_ERR_CFG (SPI WR update can occur only in DIAGNOSTIC state)
A9	54	1010 100	1	YES	WR_SAFETY_ERR_STAT (SPI WR update can occur only in DIAGNOSTIC state)
AA	55	1010 101	0	N/A	RD_SAFETY_ERR_STAT
39	1C	0011 100	1	N/A	RD_SAFETY_PWD_THR_CFG
99	4C	1001 100	1	YES	WR_SAFETY_PWD_THR_CFG (SPI WR update can occur only in DIAGNOSTIC state)
44	22	0100 010	0	N/A	RD_SAFETY_CHECK_CTRL
93	49	1001 001	1	NO	WR_SAFETY_CHECK_CTRL
3C	1E	0011 110	0	N/A	RD_SAFETY_BIST_CTRL
9F	4F	1001 111	1	YES	WR_SAFETY_BIST_CTRL (SPI WR update can occur only in DIAGNOSTIC and ACTIVE states)
2E	17	0010 111	0	N/A	RD_WD_WIN1_CFG
ED	76	1110 110	1	YES	WR_WD_WIN1_CFG (SPI WR update can occur only in DIAGNOSTIC state)
05	02	0000 010	1	N/A	RD_WD _WIN2_CFG
09	04	0000 100	1	YES	WR_WD_WIN2_CFG (SPI WR update can occur only in DIAGNOSTIC state)
36	1B	0011 011	0	N/A	RD_WDT_TOKEN_VALUE
4E	27	0100 111	0	N/A	RD_WDT_STATUS
E1	70	1110 000	1	NO	WR_WDT_ANSWER
11	08	0001 000	1	N/A	RD_DEV_STAT
12	09	0001 001	0	N/A	RD_VMON_STAT_1
A6	53	1010 011	0	N/A	RD_VMON_STAT_2
56	2B	0101 011	0	N/A	RD_SENS_CTRL
7B	3D	0111 101	1	N/A	WR_SENS_CTRL
3A	1D	0011 101	0	N/A	RD_SAFETY_FUNC_CFG

(1) All commands have even parity.

8-BIT HEX COMMAND CODE (WITH PARITY)	7-BIT HEX COMMAND CODE (WITHOUT PARITY)	7-BIT BINARY COMMAND CODE (WITHOUT PARITY)	PARITY	WR SW LOCK PROTECT	REGISTER COMMAND NAME(1)
35	1A	0011 010	1	YES	WR_SAFETY_FUNC_CFG (SPI WR update can occur only in DIAGNOSTIC state)
5A	2D	0101 101	0	N/A	RD_SAFE_CFG_CRC
63	31	0110 001	1	YES	WR_SAFE_CFG_CRC (SPI WR update can occur only in DIAGNOSTIC state)
DD	6E	1101 110	1	N/A	RD_DIAG_CFG_CTRL
CC	66	1100 110	0	NO	WR_DIAG_CFG_CTRL
AC	56	1010 110	0	N/A	RD_DIAG_MUX_SEL
C9	64	1100 100	1	NO	WR_DIAG_MUX_SEL
D7	6B	1101 011	1	N/A	RD_SAFETY_ERR_PWM_H
D8	6C	1101 100	0	YES	WR_SAFETY_ERR_PWM_H (SPI WR update can occur only in DIAGNOSTIC state)
59	2C	0101 100	1	N/A	RD_SAFETY_ERR_PWM_L
7E	3F	0111 111	0	YES	WR_SAFETY_ERR_PWM_L (SPI WR update can occur only in DIAGNOSTIC state)
78	3C	0111 100	0	N/A	RD_WDT_TOKEN_FDBCK
77	3B	0111 011	1	YES	WR_WDT_TOKEN_FDBCK (SPI WR update can occur only in DIAGNOSTIC state)

6 Application and Implementation

NOTE

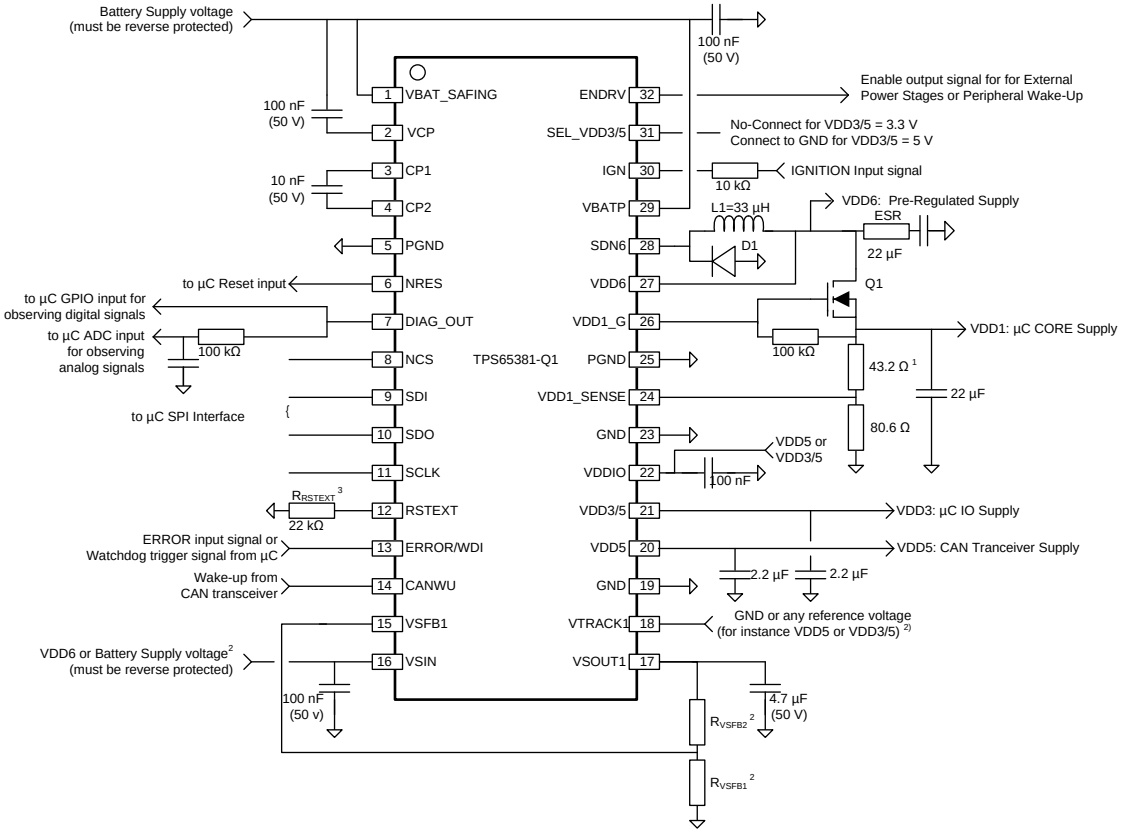
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The TPS65381-Q1 device is a multi-rail power supply including one buck preregulator, one linear controller, one 5-V linear regulator, one programmable 3.3-V or 5-V linear regulator, and one linear tracking regulator with protection against short to battery and ground. The device has many diagnostic and monitoring functions. This device provides a power management basis for many different applications.

6.2 Typical Application

The following design requirements and design procedure are an example of how to select component values for the TPS65381-Q1 device for a typical application. Because many of the regulators are adjustable, the equations should be used to calculate the component values for the specific application. For additional reference, also refer to the design checklist and application notes listed in Section 9.2.1.



Example components:

- Q1: BUK9213-30A
- D1: Vishay SS3H09/10, OnSemi MBRS340T3
- D2: ROHM UDZSTE-176.2B
- L1: EPCOS B82464G4333M000 or COILCRAFT MSS1246T-333ML

NOTE:

1. 43.2 Ω for 1.23-V output voltage (Recommended for TI TMS570 MCU). Change this resistor to obtain different VDD1 output voltage (**Note**: VDD1_SENSE = 800 mV)
2. R_{VSFB1} and R_{VSFB2} configure the VSOUT1 voltage
   - Pin 16 (VSIN) to be connected either to pin 27 (VDD6) for VSOUT1 ≤ 5 V or to pin 29 (VBATP) for 5 V < VSOUT1 < 9.5 V
   - Pin 18 (VTRACK1) to be connected to GND for non-tracking mode, or a reference voltage (for example VDD5 or VDD3/5) for tracking mode.
   - See Section 5.3.5 for details.
3. R_{RSEXT} configures the Reset Extension time. See the *Reset and Enable outputs* section of Section 4.5

Figure 6-1. Typical Application Diagram

6.2.1 Design Requirements

While selecting capacitors for the application consider the following characteristics:

- The effective capacitance at the operating voltage must be used when selecting the proper capacitor. Capacitors derate with operating voltage, sometimes as much as 70%. Therefore the capacitance of the circuit could be outside of the specified value for the capacitor as listed in Section 4.
- The temperature and lifetime of the capacitor may also have an impact on the effective capacitance and should be considered.
- The voltage ratings of the capacitor should be considered, especially on the high-voltage input circuits that may also experience transient voltages.

These impacts must all be considered when selecting a capacitor so that the circuit has the specified capacitance required for this device at the application operating conditions of the capacitor such as temperature, voltage, and lifetime.

VBATP and VBAT_SAFING are the supply inputs to the device. These supplies must be reverse battery protected. The supplies should also be adequately protected against transients and have sufficient noise filtering for the intended application. If the application has noisy and high current output drives that are connected to either VBATP, VBAT_SAFING, or both, additional filtering may be necessary between the output drive and the device.

IGN is a wake-up input to the device. This input provides up to –7 V of protection. Beyond this voltage, IGN must be reverse protected. If the noise occurs longer than the specified deglitch time, IGN should also be adequately protected against transients and have sufficient noise filtering for the intended application.

6.2.2 Detailed Design Procedure

6.2.2.1 VDD6 Preregulator

The inductor, output capacitor, and total effective series resistance of the output capacitance must be considered to achieve balanced operation of the VDD6 preregulator.

The output inductor must be greater than or equal to the minimum 22-µH inductance. The typical specified inductance is 33 µH which was selected for this design.

The effective output capacitance for VDD6 is specified between 22 µF and 47 µF. An effective capacitance of 22 µF at the 6-V DC operating point was selected for this design. This value allows for additional downstream input capacitance on voltage regulator inputs. To filter high frequencies, use 10-nF and 0.1-µF capacitors. If higher effective capacitance is used the voltage ripple is reduced and lowers the required ESR. The effective capacitance of a capacitor should be provided by the capacitor supplier and needs to be de-rated for lifetime, temperature and operating voltage.

Because the VDD6 preregulator is a hysteretic architecture, controlled ESR is required with the output capacitance. The specified ESR range is 100 mΩ to 300 mΩ. Use Equation 5 to calculate the minimum total ESR to achieve balanced operation.

$$R_{ESR} = L / (15 \times C_{Effective}) = 33 / (15 \times 22) = 100\ m\Omega \quad (5)$$

As an example, the data sheet for the capacitor states that the ESR of the capacitor is 4 mΩ and the parasitic extraction of the PCB design is 6 mΩ. An ESR resistor of 100 mΩ can still be used, or the discrete ESR resistor can be sized to 90 mΩ resulting in a total effective ESR at least 100 mΩ. If a larger effective capacitance is used the equation may result in an ESR value below 100 mΩ. In this case, the total ESR should still be brought up to the 100 mΩ total ESR minimum to meet the specification.

A high-voltage surface-mount Schottky rectifier diode, such as SS3H9/10 or MBRS340T3, should be used.

Figure 6-2 shows this configuration.

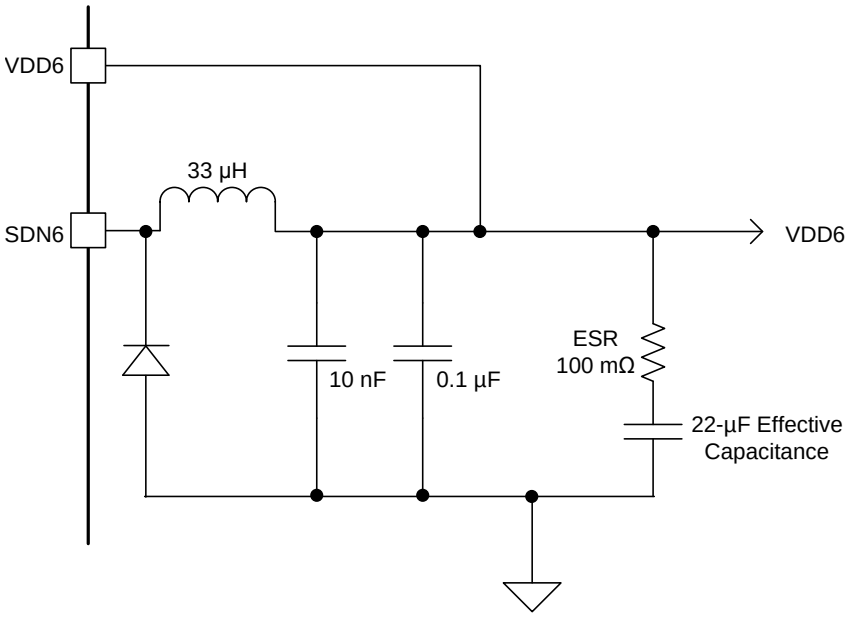


Figure 6-2. VDD6 Design

6.2.2.2 VDD1 Linear Controller

The microprocessor used with the TPS65381-Q1 device requires a core voltage of 1.23 V.

The output voltage of the VDD1 linear controller is set by a resistor divider from the VDD1 output to ground with the divided voltage connected to the VDD1_SENSE pin which must be set to 800 mV. To ensure sufficient bias current through the resistor divider select a value of R1 as 80.6 Ω. Use Equation 6 to calculate the resistance of R2.

$$R2 = ([VDD1 \times R1] / V_{VDD1\_SENSE}) - R1 = ([1.23\ V \times 80.6\ \Omega] / 0.8\ V) - 80.6\ \Omega = 43.3\ \Omega \quad (6)$$

Select the standard value 43.2 Ω.

Select an output FET for the VDD1 linear controller that meets the requirements in the *VDD1 – LDO With External FET* specifications in Section 4.5. An example output FET is BUK9213-30A. The gate of the output FET is connected to VDD1_G. A 100-kΩ resistor is connected between the gate and source of the FET. The drain of the FET is connected to the VDD6 preregulator output which is used as the supply input for the VDD1 linear controller.

A low-ESR ceramic output capacitor with 22-µF effective capacitance at 1.23 V is used to meet the requirements for the output capacitor that are listed in this data sheet. Depending on the application, this output may require a larger output capacitor to ensure the output does not drop below the required regulation specification during load transients. The VDD1 output capacitance is specified up to 40 µF.

Figure 6-3 shows this configuration.

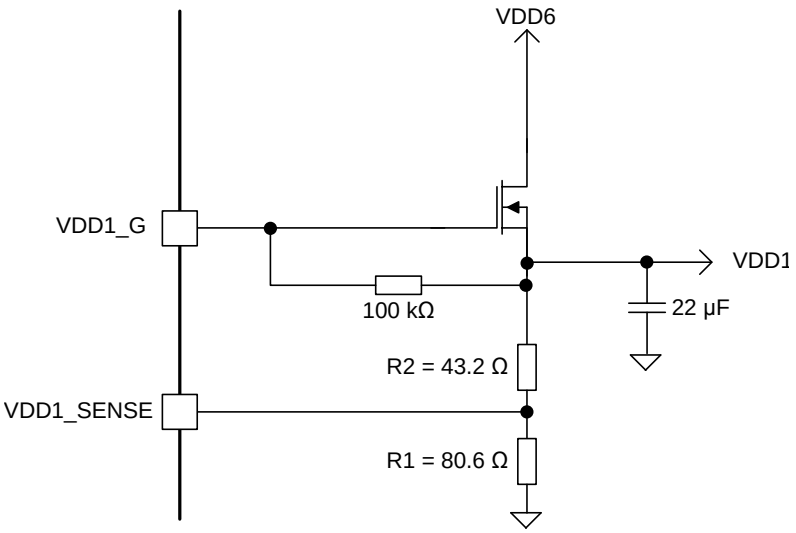


Figure 6-3. VDD1 Design

6.2.2.3 VSOUT1 Tracking Linear Regulator, Configured to Track VDD5

The system has a sensor that requires a 5-V supply that must track the VDD5 supply. The configuration should be set up for higher efficiency.

The VDD5 output is connected to the VTRACK1 pin which configures the regulator for tracking mode. Because the output must track the input, unity gain feedback is used on the VSFB1 pin by connecting it to the VSOUT1 pin.

For efficiency, use the VDD6 preregulator as the supply. Therefore, the VDD6 output is connected to VSIN. A local, low-ESR 100-nF ceramic capacitor is used on the VSIN pin to stabilize the input.

A local, low-ESR 4.7-µF ceramic capacitor is used on the VSOUT1 output for loop stabilization. Depending on the application, this output may require a larger output capacitor to ensure that the output does not drop below the required regulation specification during load transients. The VSOUT1 output capacitance is specified up to 10 µF.

Figure 6-4 shows this configuration.

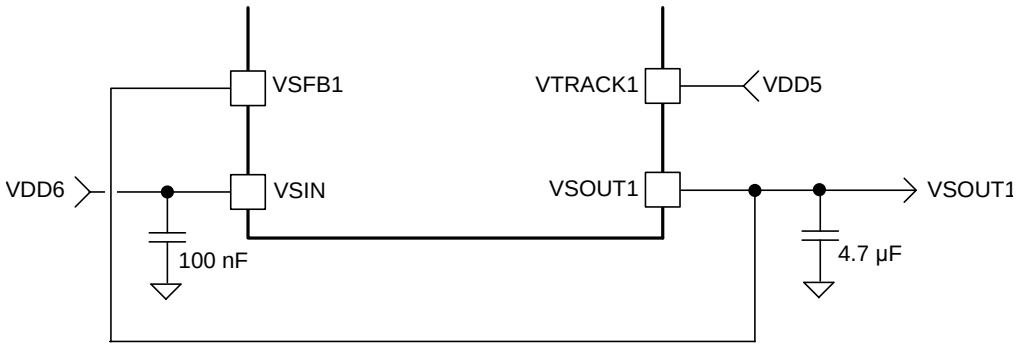


Figure 6-4. VSOUT1 Design—Tracking, No Gain

6.2.2.4 Alternative Use for VSOUT1 Tracking Linear Regulator, Configured for 6-V Output Tracking VDD3/5 In 3.3-V Mode

The system has a sensor that requires a 6-V supply that must track the VDD3/5 supply operating at 3.3 V.

The VDD3/5 supply, operating in 3.3-V mode, is connected to the VTRACK1 pin which configures the regulator for tracking mode. Because the output must have gain to make the 6-V output track a 3.3 V supply, gain feedback is used on the VSFB1 pin. To achieve the required gain, connect a resistor divider the VSOUT1 and VSFB1 pins. Select a value of 3.3 kΩ for the RVSFB1 resistor to balance the current through the resistor divider for reasonable bias current and reasonable losses. Use Equation 7 to calculate the resistance of RVSFB2.

$$RVSFB2 = ([VSOUT1 \times RVSFB1] / VTRACK) - RVSFB1 = ([6\ V \times 3.3\ k\Omega] / 3.3\ V) - 3.3\ k\Omega = 2.7\ k\Omega \quad (7)$$

Select the standard value of 2.7 kΩ.

Because the desired VSOUT1 output is greater than 5 V, the VBATP supply must be used for the tracking supply. Therefore, connect the VBATP supply to the VSIN pin. A local, low-ESR 100-nF ceramic capacitor is used on the VSIN pin to stabilize the input.

A local, low-ESR 4.7-µF ceramic capacitor is used on the VSOUT1 pin for loop stabilization. Depending on the application, this output may require a larger output capacitor to ensure that the output does not drop below the required regulation specification during load transients. The VSOUT1 output capacitance is specified up to 10 µF.

Figure 6-5 shows this configuration.

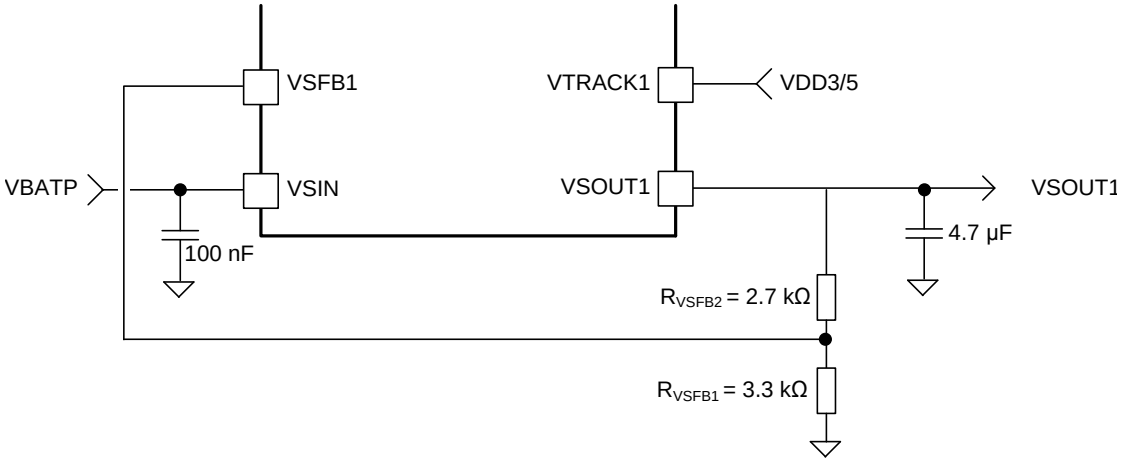


Figure 6-5. VSOUT1 Design—Tracking, With Gain (VDD3/5)

6.2.2.5 Alternative Use for VSOUT1 Tracking Linear Regulator, Configured for 9-V Output Tracking to 5-V Input from VDD5

The system has a sensor that requires a 9-V supply that must track the VDD5 supply operating at 5 V.

The VDD5 supply is connected to VTRACK1 which configures the regulator for tracking mode. Because the output must have gain to make the 9-V output track a 5-V supply, gain feedback is used on the VSFB1 pin. To achieve the required gain, connect a resistor divider between the VSOUT1 and VSFB1 pins. Select a value of 3.3 kΩ for the RVSFB1 resistor to balance the current through the resistor divider for reasonable bias current and reasonable losses. Use Equation 8 to calculate the resistance of RVSFB2.

$$RVSFB2 = ([VSOUT1 \times RVSFB1] / VTRACK) - RVSFB1 = ([9\ V \times 3.3\ k\Omega] / 5\ V) - 3.3\ k\Omega = 2.64\ k\Omega \quad (8)$$

Select the standard value of 2.7 kΩ.

Because the desired VSOUT1 output is greater than 5-V, the VBATP supply must be used as the tracking supply. Therefore, connect the VBATP supply to the VSIN pin. A local, low-ESR 100-nF ceramic capacitor is used on the VSIN pin to stabilize the input.

A local, low-ESR 4.7-µF ceramic capacitor is used on the VSOUT1 pin for loop stabilization. Depending on the application, this output may require a larger output capacitor to ensure that the output does not drop below the required regulation specification during load transients. The VSOUT1 output capacitance is specified up to 10 µF.

Figure 6-6 shows this configuration.

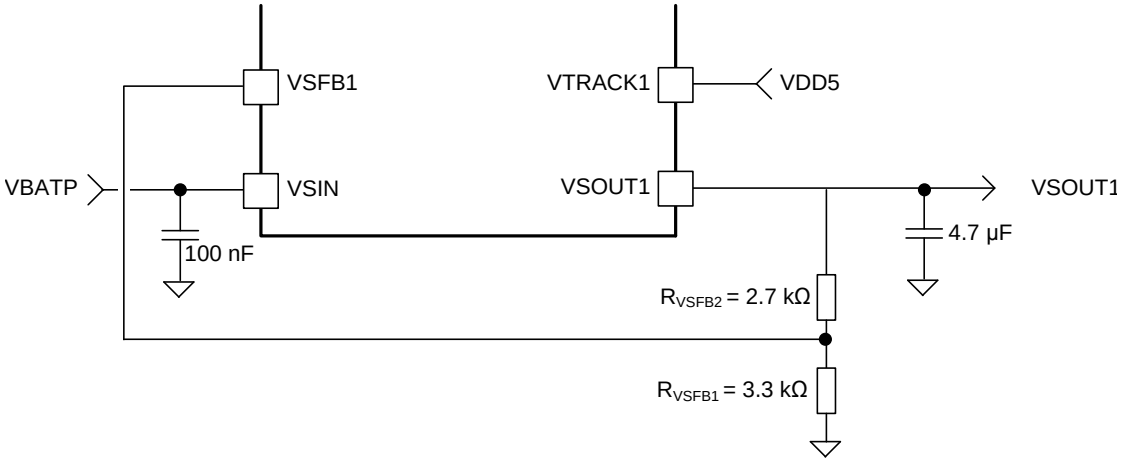


Figure 6-6. VSOUT1 Design—Tracking, With Gain (VDD5)

6.2.2.6 Alternative Use for VSOUT1 Tracking Linear Regulator, Configured in Non-tracking Mode Providing a 4.5-V Output

If the system requires a 4.5-V supply that does not track any other supply.

The VTRACK1 pin is connected to ground (GND) which configures the regulator for non-tracking mode. The output is now proportional to a fixed reference voltage (VREF) of 2.5 V on the VSFB1 pin. Because the output must have gain to result in a 4.5-V output, gain feedback will be used on the VSFB1 pin. To achieve the required gain, connect a resistor divider between the VSOUT1 and VSFB1 pins. Select a value of 3.3 kΩ for the RVSFB1 resistor to balance the current through the resistor divider for reasonable bias current and reasonable losses. Use Equation 9 to calculate the resistance of RVSFB2.

$$RVSFB2 = ([VSOUT1 \times RVSFB1] / VREF) - RVSFB1 = ([4.5\ V \times 3.3\ k\Omega] / 2.5\ V) - 3.3\ k\Omega = 2.64\ k\Omega \quad (9)$$

Select the standard value of 2.7 kΩ.

For efficiency, the VDD6 preregulator is the supply and therefore the VDD6 output is connected to the VSIN pin. A local, low-ESR 100-nF ceramic capacitor is used on the VSIN pin to stabilize the input.

A local, low-ESR 4.7-µF ceramic capacitor is used on the VSOUT1 pin for loop stabilization. Depending on the application, this output may require a larger output capacitor to ensure that the output does not drop below the required regulation specification during load transients. The VSOUT1 output capacitance is specified up to 10 µF.

Figure 6-7 shows this configuration.

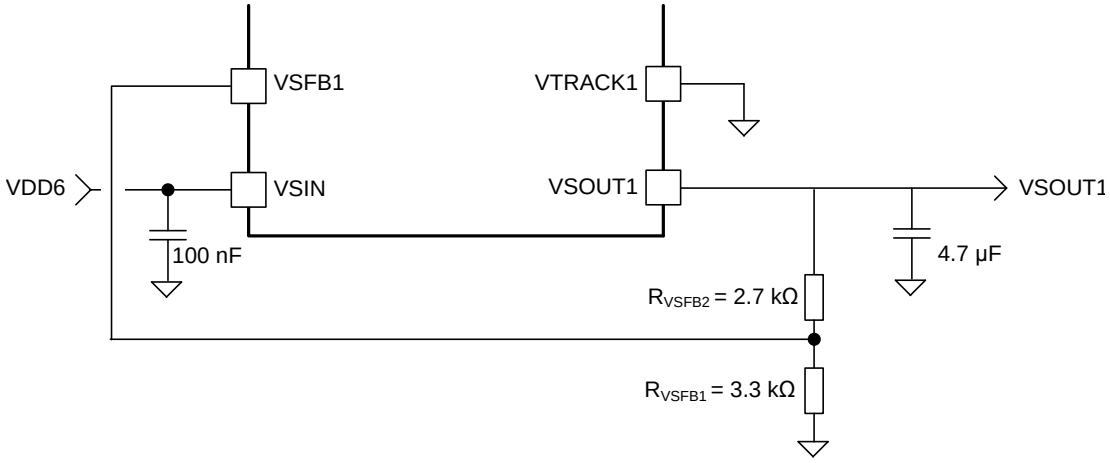


Figure 6-7. VSOUT1 Design—Non-Tracking

6.2.3 Application Curves

For the application curves, see the figures listed in Table 6-1.

Table 6-1. Table of Graphs

FIGURE TITLE	FIGURE NUMBER
SPI SDO Buffer Source/Sink Current	Figure 4-3
VDD6 BUCK Efficiency	Figure 4-4

6.3 System Examples

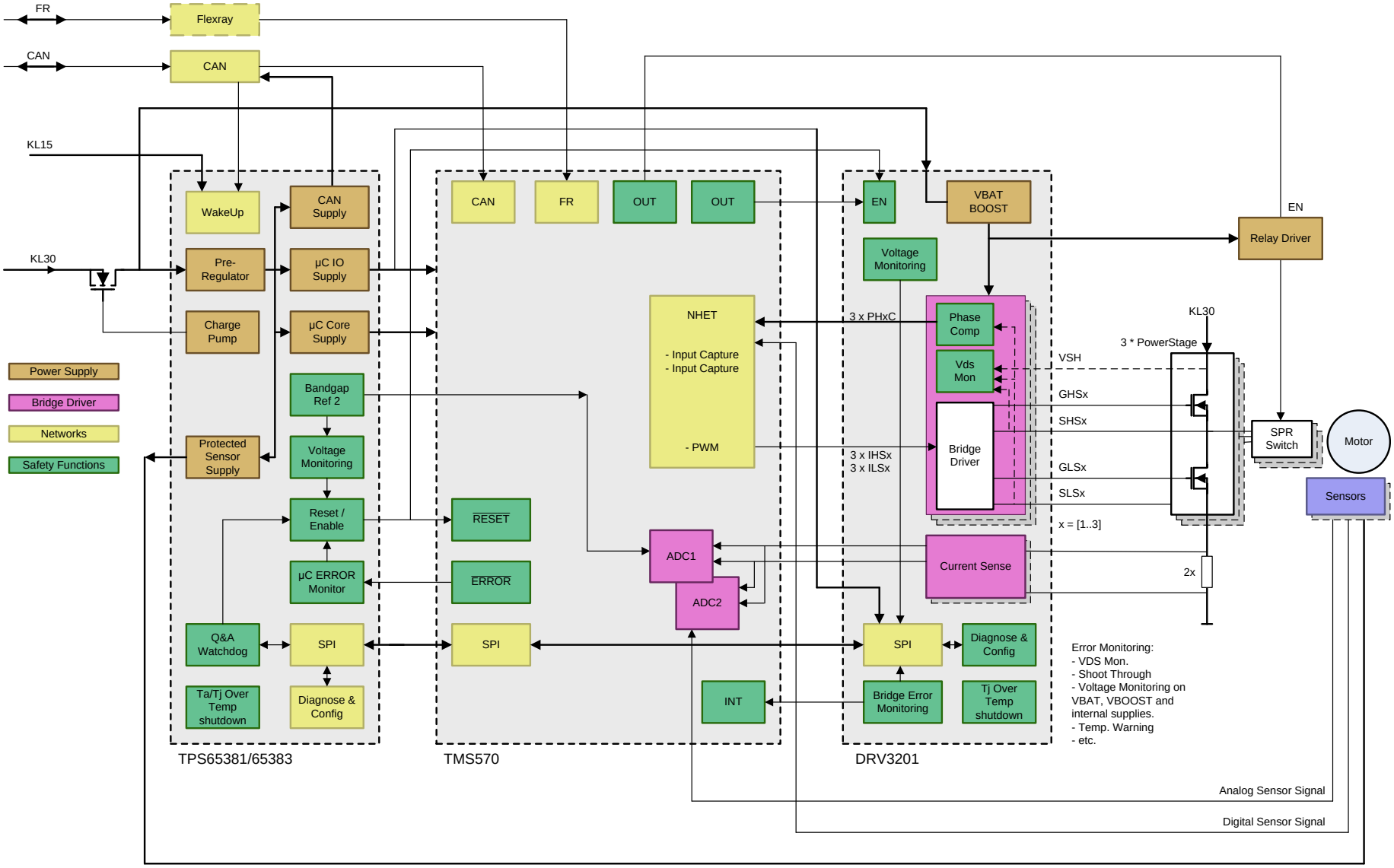


Figure 6-8. Electrical Power-Steering Example

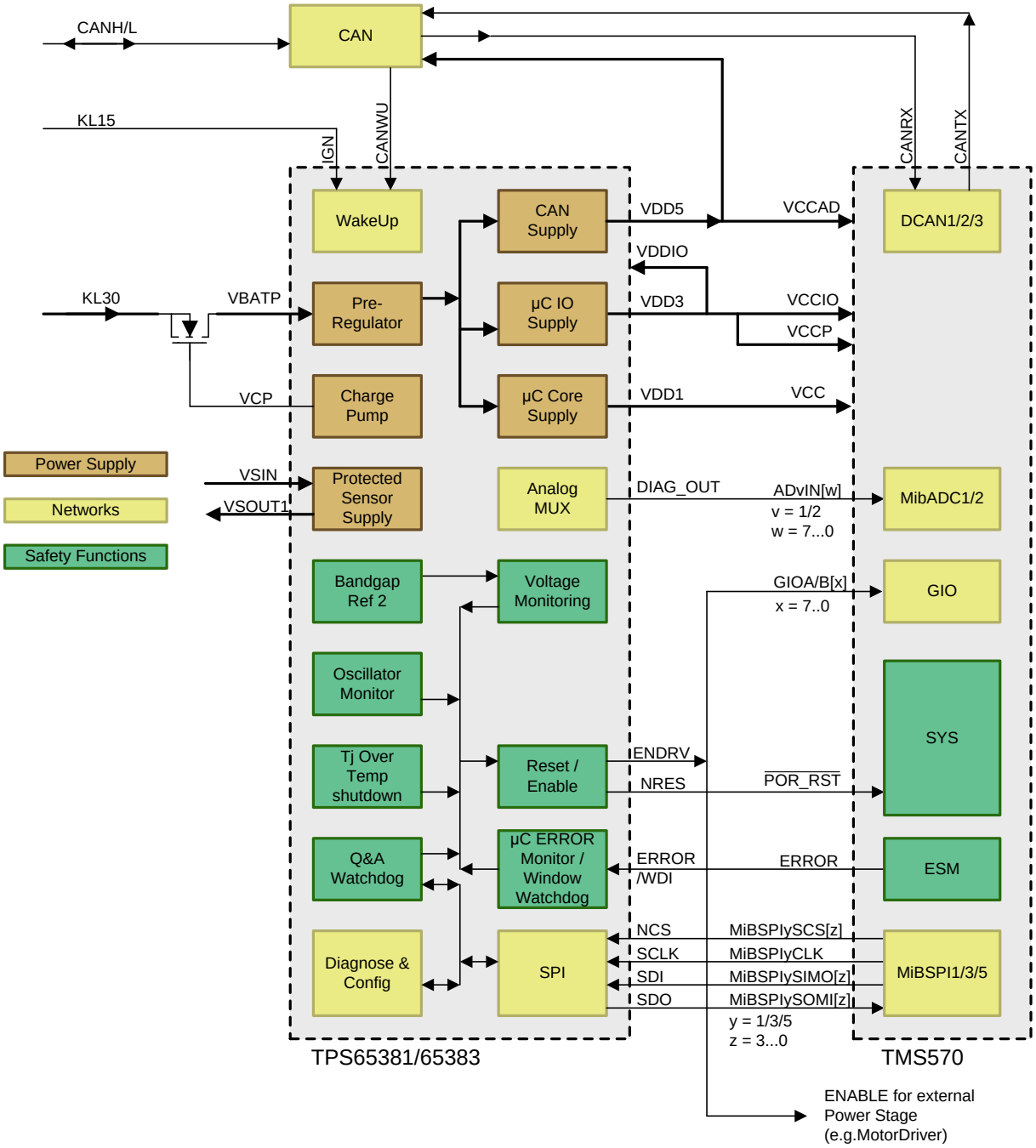
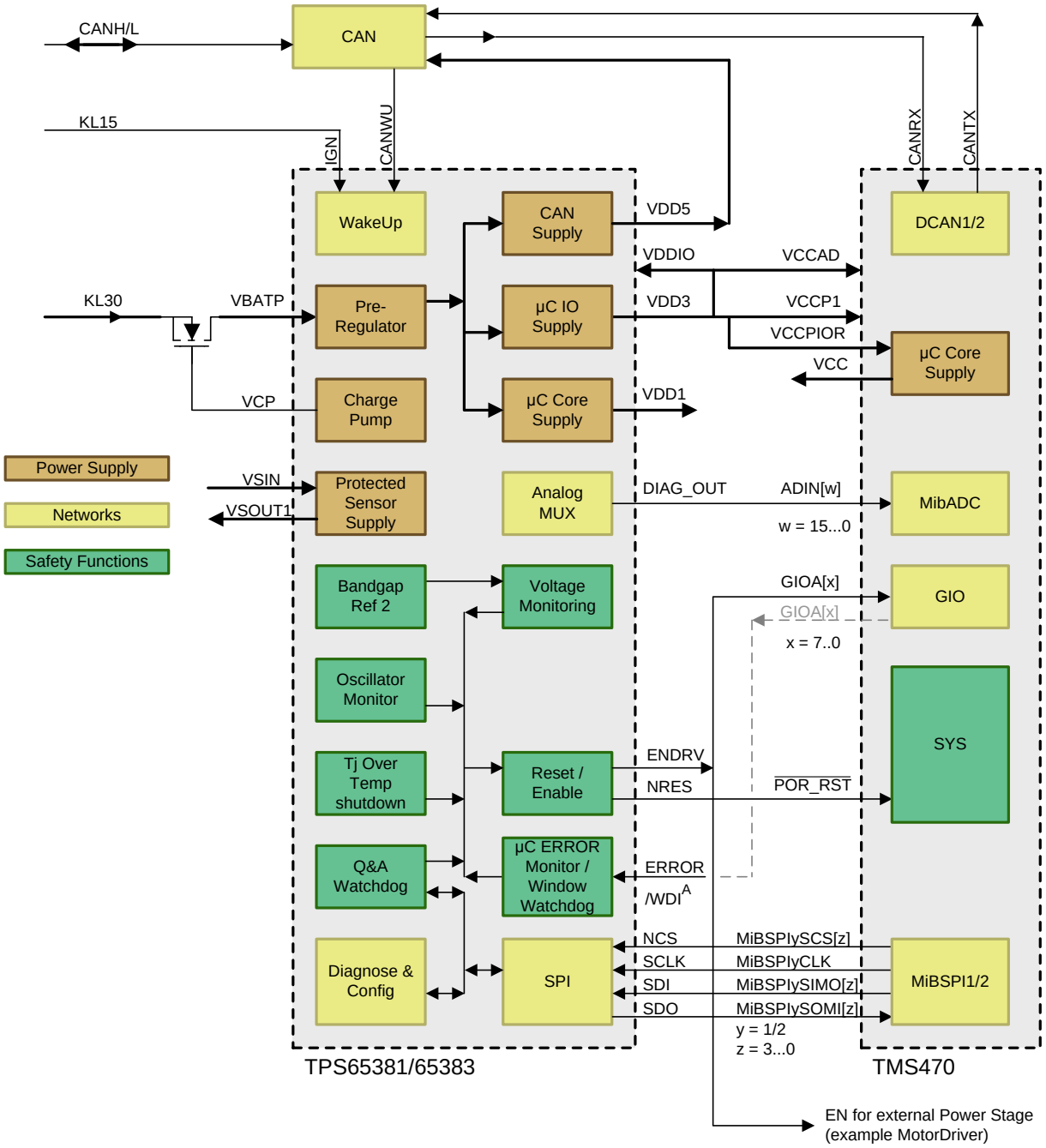


Figure 6-9. Example TPS65381-Q1 With TI's TMS570LS



The ERROR/WDI pin can be configured as an input for the µC ERROR monitor (TMS570 dual core) or as a window watchdog input (TMS470 single core).

Figure 6-10. Example TPS65381-Q1 With TI's TMS470 (Using an Internal MCU Core Supply)

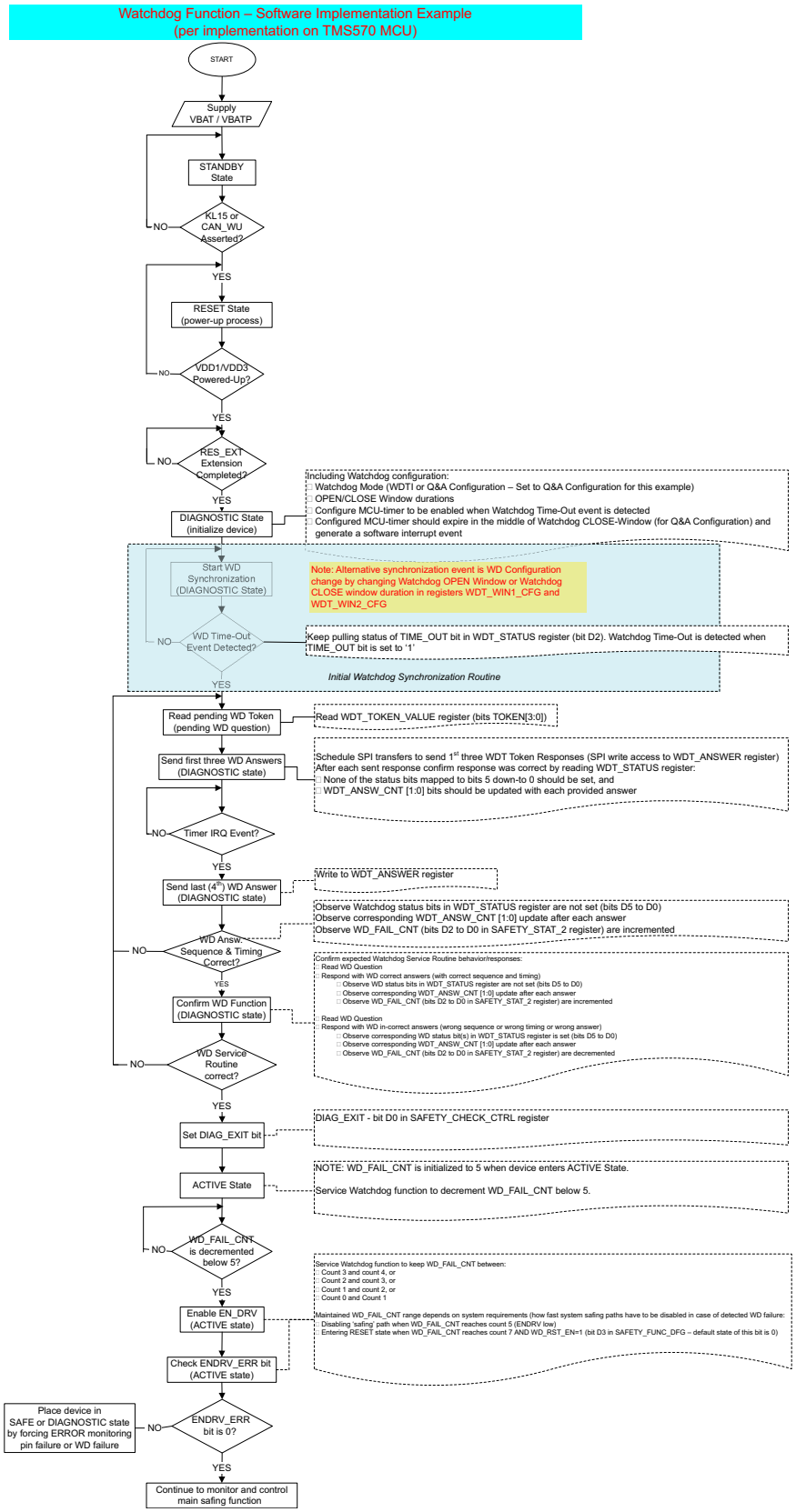


Figure 6-11. Software Flowchart for Synchronizing the MCU With the TPS65381-Q1 Watchdog

7 Power Supply Recommendations

The TPS65381-Q1 device is designed to operate using an input supply voltage range from 5.8 V to 36 V (CAN, I/O, MCU core, and functional sensor-supply regulators) or 4.5 V to 5.8 V (3.3-V I/O and functional MCU-core voltage). For additional power supply recommendations, see the *TPS65381EVM User's Guide*, SLVU847.

8 Layout

8.1 Layout Guidelines

8.1.1 VDD6 Buck Pre-Regulator

- Minimize the loop area for the switching loop of the inductor, ESR resistor and output capacitor and diode.
- Minimize the parasitic trace impedance by using as wide of traces as possible.
- Minimize the parasitic via impedance by using multiple vias, especially on high current and switching nodes.
- Connect the inductor and diode to SDN6 as close as possible to the pin.
- Connect the diode to PGND (ground plane).
- Connect the ESR resistor and output capacitor in series between VDD6 output (inductor output) and PGND.
- Connect the EMC filter capacitor between VDD6 output and PGND.
- Connect the VDD6 output to the VDD6 pin with routing to avoid coupling switching noise. Trace length should be minimized and as wide a trace as possible. This trace is the supply input to the downstream regulators using VDD6 as a pre-regulator, parasitic impedance should be minimized.
- Connect a local decoupling capacitor between the VREG and PGDN1 pin, and between the EXTSUP and PGND1 pin. The length of this trace loop should be short.

Additional consideration: add footprint for a RC snubber circuit if one is necessary for the application. The RC connects in-series between SDN6 and PGND.

8.1.2 VDD1 Linear Regulator Controller

- Connect the drain of the external FET to VDD6 node, the trace should be minimized so that additional downstream buffering capacitors are not needed.
- Connect the output capacitor to the source of the external FET, the length of this trace should be minimized. Connect the output capacitor to the ground plane.
- Connect the gate drive, VDD1_G, to the gate of the FET. Connect the resistor between the gate of the FET and the source of the FET, minimize the trace length.
- The resistor divider for sensing and setting the output voltage connects between the source of the FET (VDD1 output) and GND (IC signal ground). Do not locate these components and their traces near the switching nodes or high-current traces.

8.1.3 VDD5 and VDD3/5 Linear Regulators

Connect the output capacitor as close as possible between the VDDx output and GND.

8.1.4 VSOUT1 Tracking Linear Regulator

- Connect the output capacitor as close as possible between the VSOUT1 output and GND.
- The resistor divider for sensing and setting the output voltage connects between the VSOUT1 and GND (IC signal ground). Do not locate these components and their traces near the switching nodes or high-current traces.
- Connect the local decoupling capacitor between VSIN and PGND. Minimize trace length.
- Route the tracking supply signal, connected to VTRACK1, away from switching nodes or high-current traces.

8.1.5 Charge Pump

- Connect the capacitor as close as possible between the CP1 and CP2.
- Connect the capacitor between VCP and VBATP (reverse protected and filtered) supply.

8.1.6 Other Considerations

- Use ground planes.
- Minimize parasitic impedance on the critical switching and high current paths.
- Short PGNDx and GND to the thermal pad.
- Use a star ground configuration if connecting to a non-ground plane system. Use tie-ins for the, voltage-sense feedback ground, and local biasing bypass capacitor ground networks to this star ground.
- Connect the local decoupling capacitor between VBATP and PGND. Minimize trace length.

8.2 Layout Example

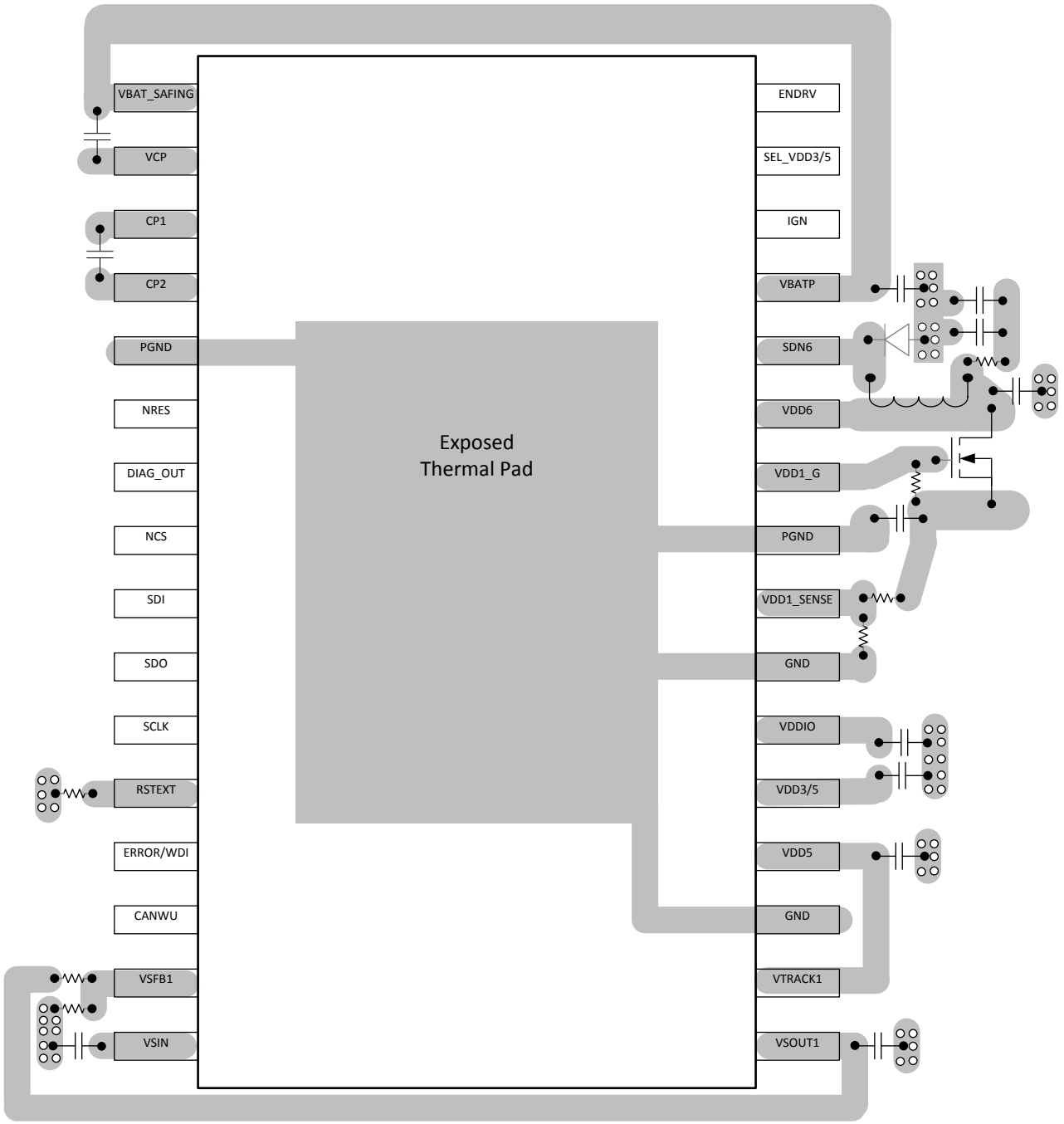


Figure 8-1. TPS65381-Q1 Board Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- *Device Behavior Under Slow VBAT Ramp-Up and Ramp-Down,* SLVA643
- *DPI Evaluation TPS65381-Q1*, SLVA575
- *Efficiency Evaluation TPS65381-Q1*, SLVA606
- *TPS65381EVM User's Guide*, SLVU847
- *TPS65381-Design-Checklist*, SLVA611

9.3 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65381QDAPRQ1	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS65381	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

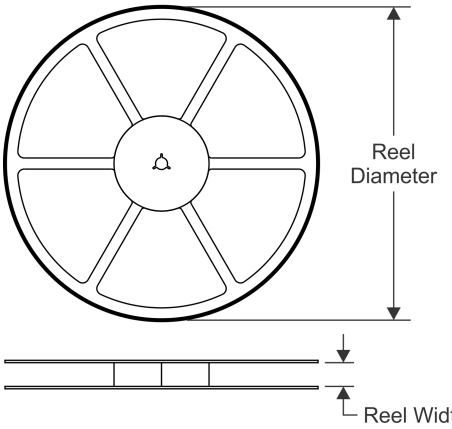
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

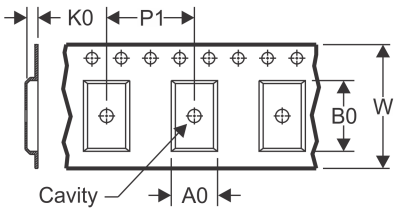
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

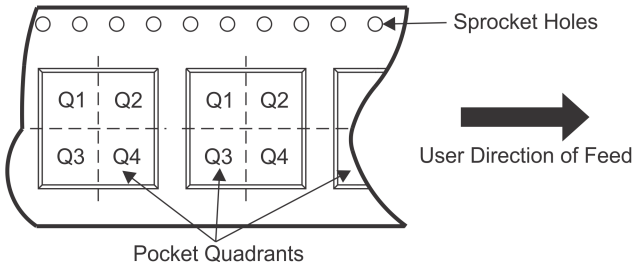


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

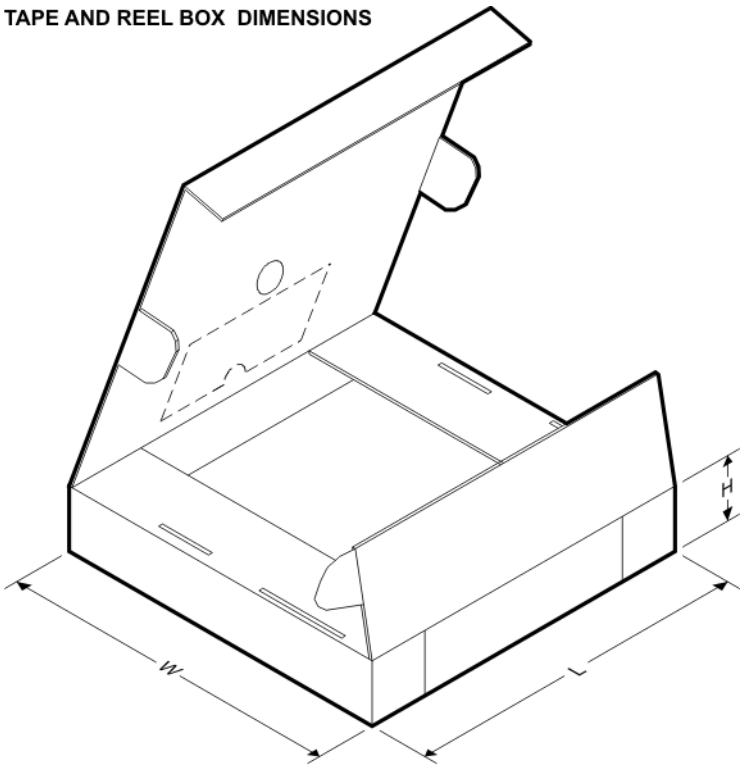
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65381QDAPRQ1	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

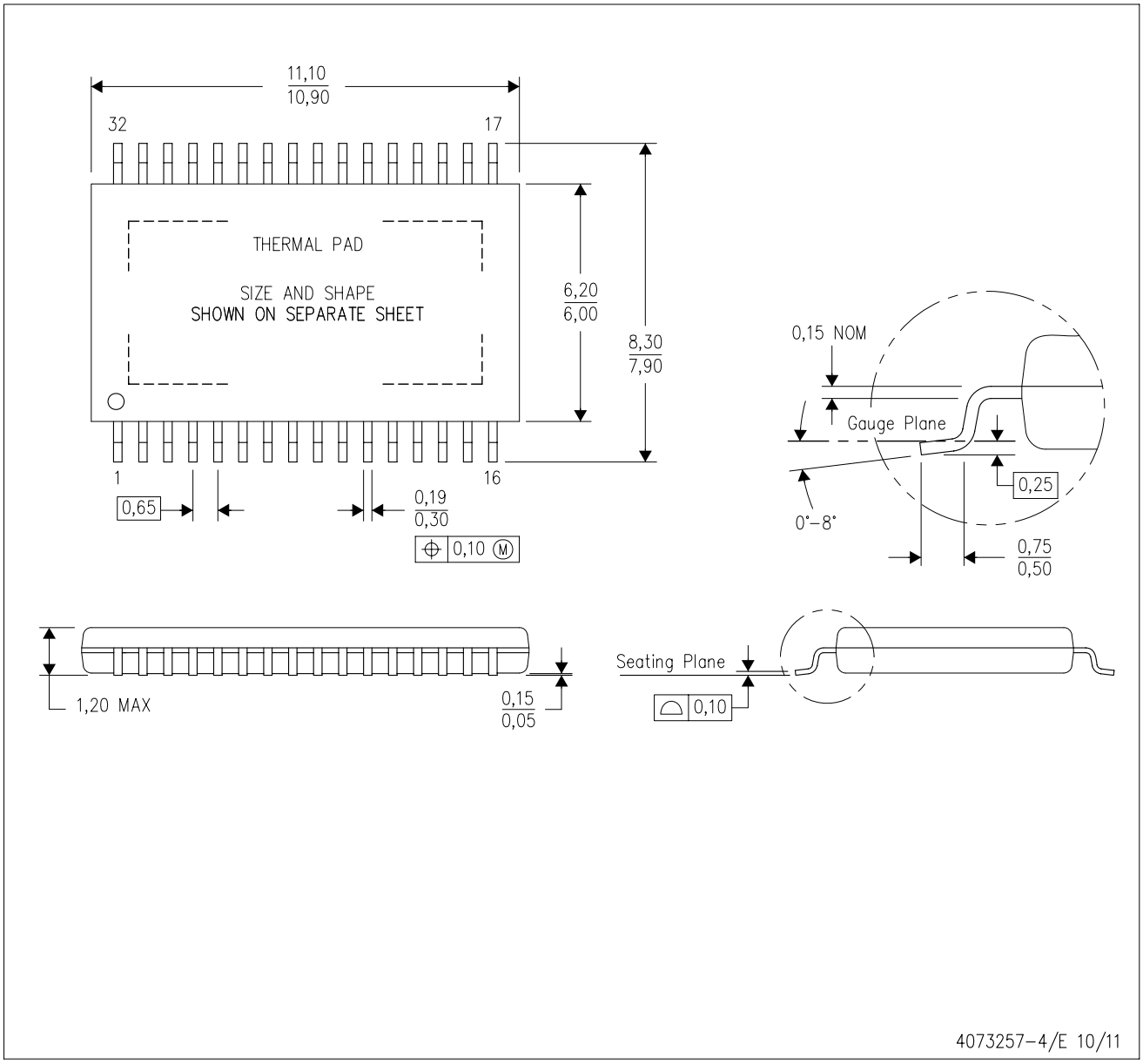
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65381QDAPRQ1	HTSSOP	DAP	32	2000	367.0	367.0	45.0

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

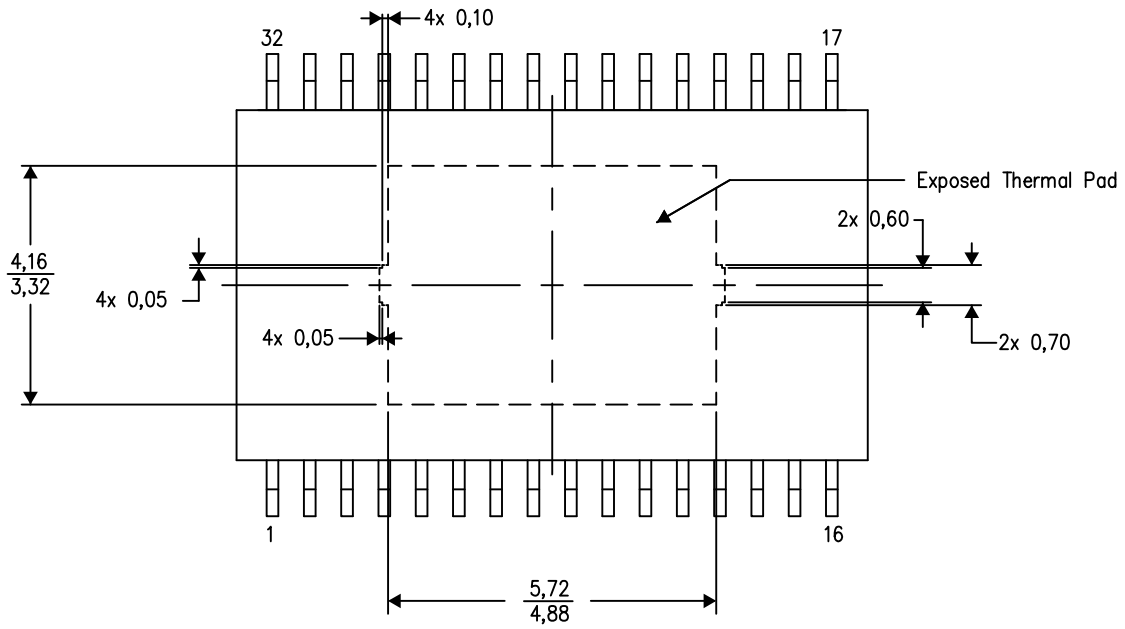
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206319–5/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

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