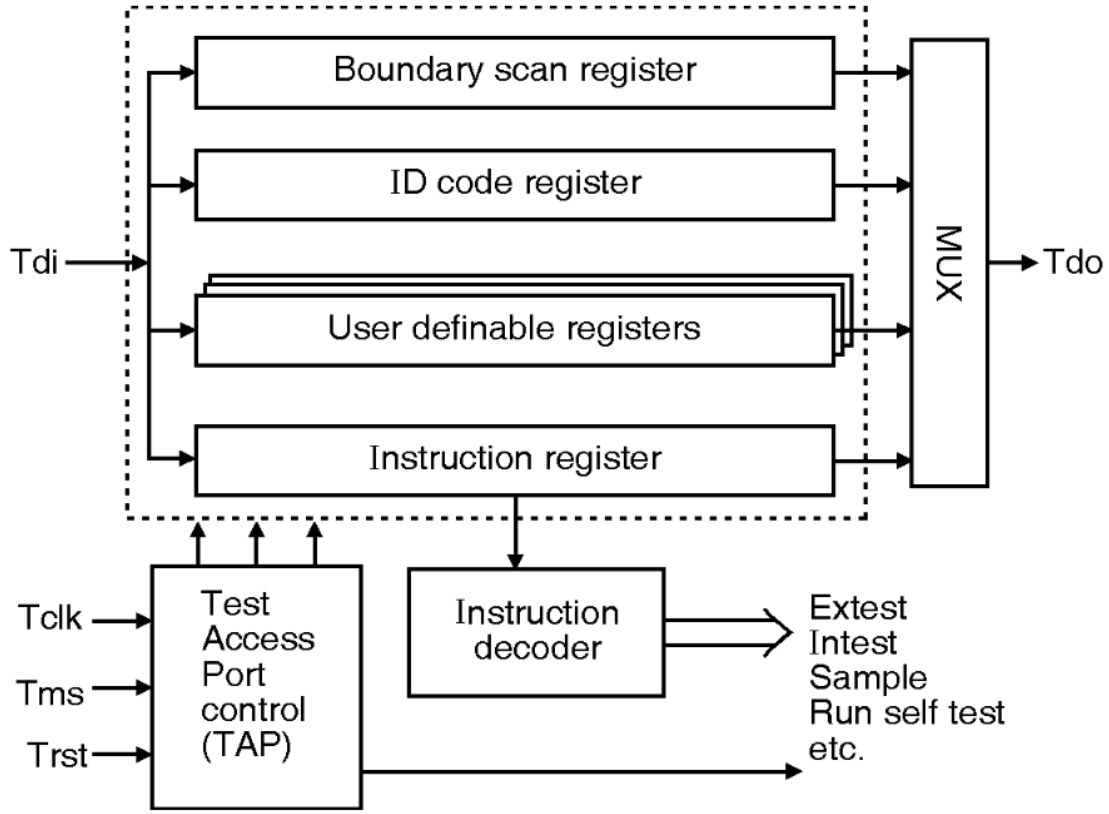
ARCHITECTURE OVERVIEW

Introduction:

JTAG(Joint Test Action Group) 1149.1 is a standard that is aimed at improving the observability and controlling of integrated circuits using defined test instructions.The generic top level schematic of JTAG. The key idea is to decode predefined instructions and connect the TDI and TDO ports with the required register using a multiplexer.



(diagram taken from : electronics-tutorial.net)

I/O ports:

Input ports:

```
input   tms_pad_i;      // JTAG test mode select pad
input   tck_pad_i;      // JTAG test clock pad
input   trst_pad_i;     // JTAG test reset pad
input   tdi_pad_i;      // JTAG test data input pad
input   debug_tdi_i;    // from debug module
input   bs_chain_tdi_i; // from Boundary Scan Chain
input   mbist_tdi_i;    // from Mbist Chain
```

Output ports:

```
output  tdo_pad_o;      // JTAG test data output pad
output  tdo_padoe_o;    // Output enable for JTAG test data output pad
output  shift_dr_o;
output  pause_dr_o;
output  update_dr_o;
output  capture_dr_o;
output  extest_select_o;
output  sample_preload_select_o;
output  mbist_select_o;
output  debug_select_o;
output  tdo_o;
```

Mandatory JTAG ports:

JTAG standard states that the following ports are mandatory for any jtag architecture,

tck_pad_i -- input Test clock input

tms_pad_i -- input Test mode select input

tdi_pad_i -- input Test data input

tdo_pad_o -- output Test data output

Register List:

Name	Width	Access	Description
IR	4	R/W	Instruction Register
IDCODE	32	RO	IDCODE Register

Instruction Register details:

Bit #	Access	Description
3:0	R/W	INSTR – Instruction 0000 = EXTEST 0001 = SAMPLE_PRELOAD 0010 = IDCODE 1000 = DEBUG 1001 = MBIST 1111 = BYPASS

JTAG instruction details:

1.EXTEST:

The EXTEST instruction connects the boundary scan chain, between the primary pins TDI and TDO. In this instruction,the boundary-scan register is selected to drive test data off-chip via the boundary outputs and to receive test data in-chip via the boundary inputs. The bit code of this instruction is defined as all zeroes(0000) by the JTAG standard. This Instruction is capable of capable of checking interconnection between two chips and determine stuck at faults.

2.BYPASS

The BYPASS instruction keeps the IC in a functional mode and selects that the bypass register will be connected between TDI and TDO. It allows data from TDI to be serially transmitted to TDO .The data entered serially will be available in the subsequent clock cycle.Invalid IR instructions result in BYPASS.

3.IDCODE

The IDCODE instruction selects the device identification register (ID register) to be connected between TDI and TDO. The device identification register is a 32-bit read-only register containing information regarding the IC manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the device. The device identification register is available right after the device is powered up.

4.SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction selects the boundary-scan chain to be connected between TDI and TDO. During this instruction, you can access the boundary-scan chain registers via a scan in operation to take a sample of the functional data entering and leaving the IC. The instruction is also used to preload test data into the BS register before loading an EXTEST instruction.

5.MBIST

Connects TDO and TDI to mbist scan input.The IR code required for this instruction is user defined.

6.DEBUG

Connects TDO and TDI to mbist scan input.The IR code required for this instruction is user defined.

TAP controller working:

The TAP controller is a 16 – state FSM that helps in controlling the test infrastructure to validate the device.

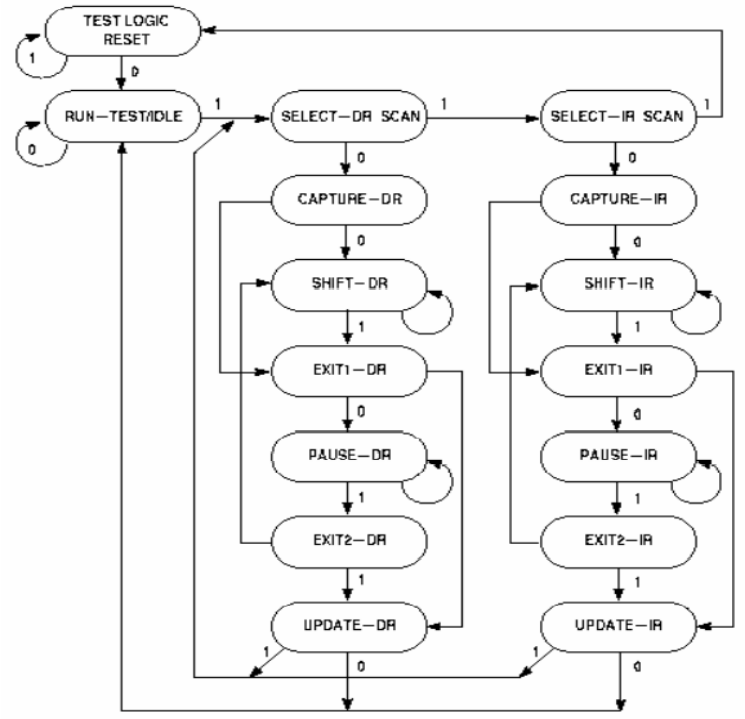


Figure 1: TAP Controller

As shown above tap controller constitutes of seven identical states for IR operation and DR operation. In IR sequence we shift the Test instruction into the Instruction register in shift-IR state and proceed to update. The DR sequence is used to shift data into scan chains to perform other instructions. State transitions are through TMS signal pulsing.

References:

1. **https://opencores.org/projects/jtag**
2. electronics-tutorial.net