Digital Integrated Circuits

Practical 0

Date: 21/01/2022

Aim: To plot the forward and reverse characteristics of PN junction diode and extract the PN junction diode following parameters for the given diode specifications:

η ideality factor (for silicon diode) (N) =2, saturation current (IS)=1E-12 A, parasitic resistance (RS) =10 Ω, zero-bias junction capacitance(CJO) = 5pF, transit time (TT)=10ns, junction potential (VJ)= 1V , reverse brake down voltage (BV) = 10v.

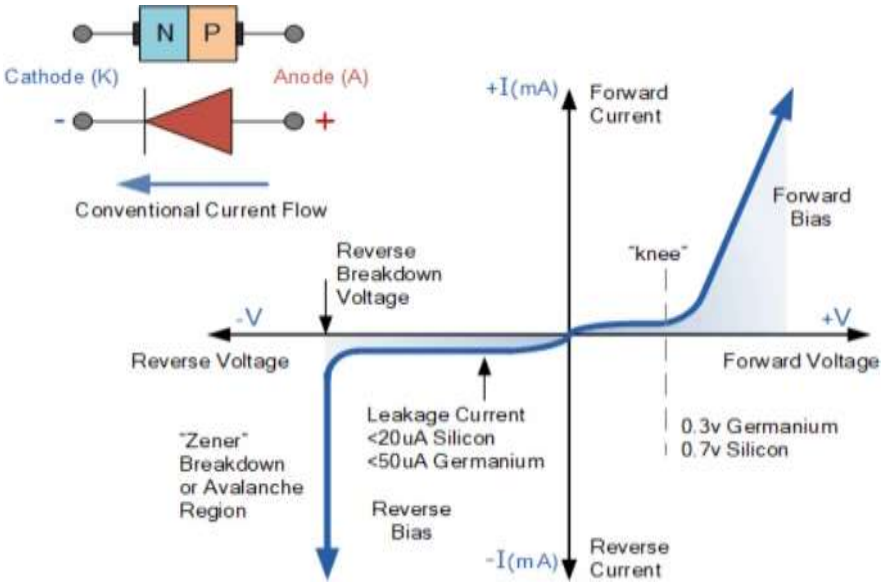
1) Forward resistance and cut in voltage from forward characteristics.
2) Reverse saturation current after break down and Reverse resistance from reverse characteristics.
3) Reverse recovery time of a diode(trr) by applying pulse input.

Software: Win-SPICE

Theory:

A PN Junction Diode is one of the simplest semiconductor devices around, and which has the electrical characteristic of passing current through itself in one direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage. Instead, it has an exponential current-voltage (I-V) relationship and therefore we cannot describe its operation by simply using an equation such as Ohm's law.

If a suitable positive voltage (forward bias) is applied between the two ends of the PN junction, it can supply free electrons and holes with the extra energy they require to cross the junction as the width of the depletion layer around the PN junction is decreased.

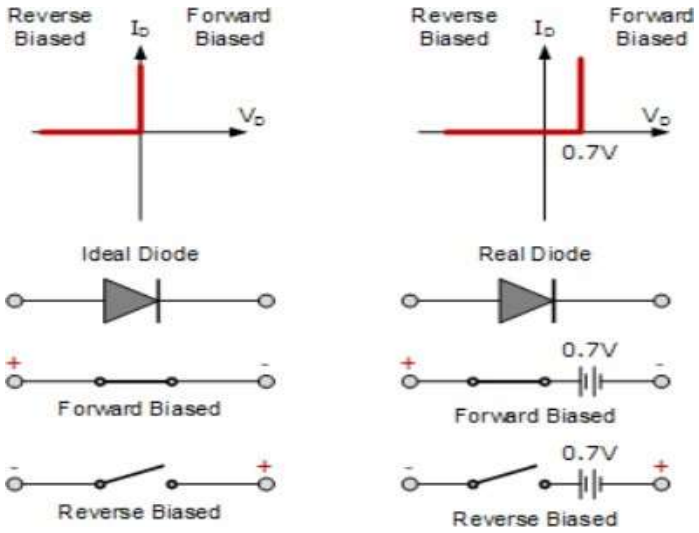


By applying a negative voltage (reverse bias) result in the free charges being pulled away from the junction resulting in the depletion layer width being increased. This has the effect of increasing or decreasing the effective resistance of the junction itself allowing or blocking the flow of current through the diodes pn-junction.

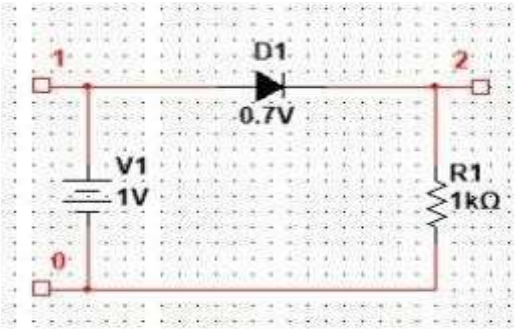
Then the depletion layer widens with an increase in the application of a reverse voltage and narrows with an increase in the application of a forward voltage. This is due to the differences in the electrical properties on the two sides of the PN junction resulting in physical changes taking place. One of the results produces rectification as seen in the PN junction diodes static I-V (current-voltage) characteristics.

There are two operating regions and three possible "biasing" conditions for the standard Junction Diode and these are:

1. Zero Bias – No external voltage potential is applied to the PN junction diode.
2. Reverse Bias – The voltage potential is connected negative, (-ve) to the P-type material and positive, (+ve) to the N-type material across the diode which has the effect of Increasing the PN junction diode's width.
3. Forward Bias – The voltage potential is connected positive, (+ve) to the P-type material and negative, (-ve) to the N-type material across the diode which has the effect of Decreasing the PN junction diodes width.



Circuit Diagram:



Code:

1. Forward Characteristics

```
*Diode Forward characteristics
.Model mod1 D (IS=1E-12 RS=10 CJO=5P TT=10N BV=10)
D1 2 0 mod1

R1 1 2 1k
V1 1 0 dc 1
.dc V1 0 5 0.05
.control
run

* plot v(1)-v(2)
plot -I(V1)
.endc
.end
```

2. Reverse Characteristics

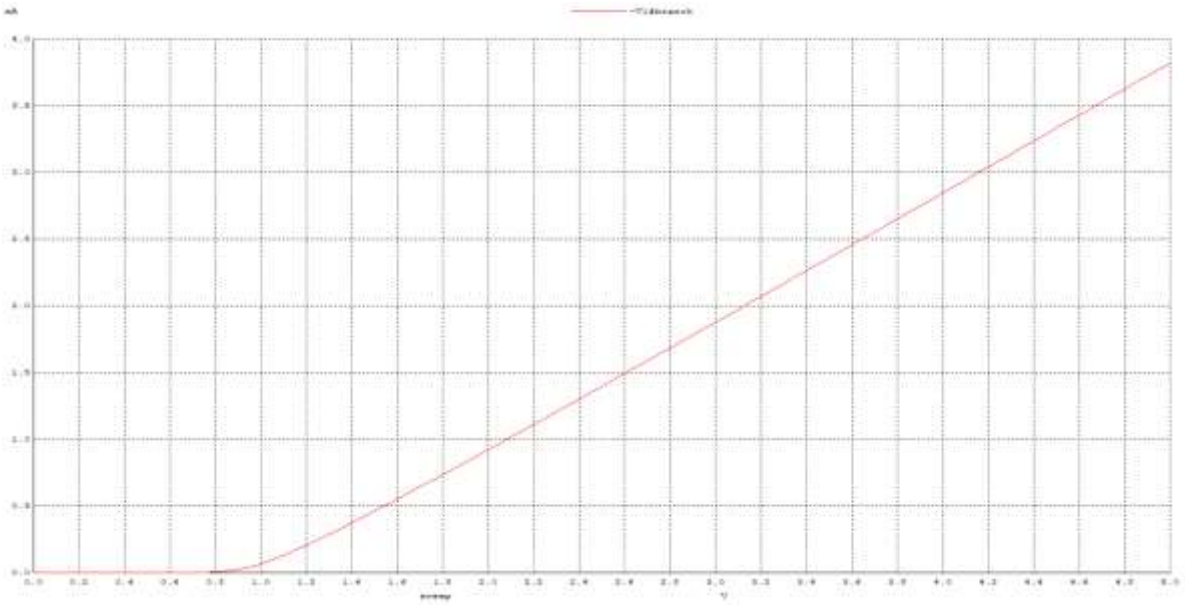
```
* Diode Reverse characteristics

.Model mod1 D (IS=1E-12 RS=10 CJO=5P TT=10N BV=10)
D1 2 0 mod1

R1 1 2 1k
V1 1 0 dc 1
.dc V1 -5 0 0.05
.control
run
plot -I(V1)
.endc
.end
```

3. Reverse Recovery Time

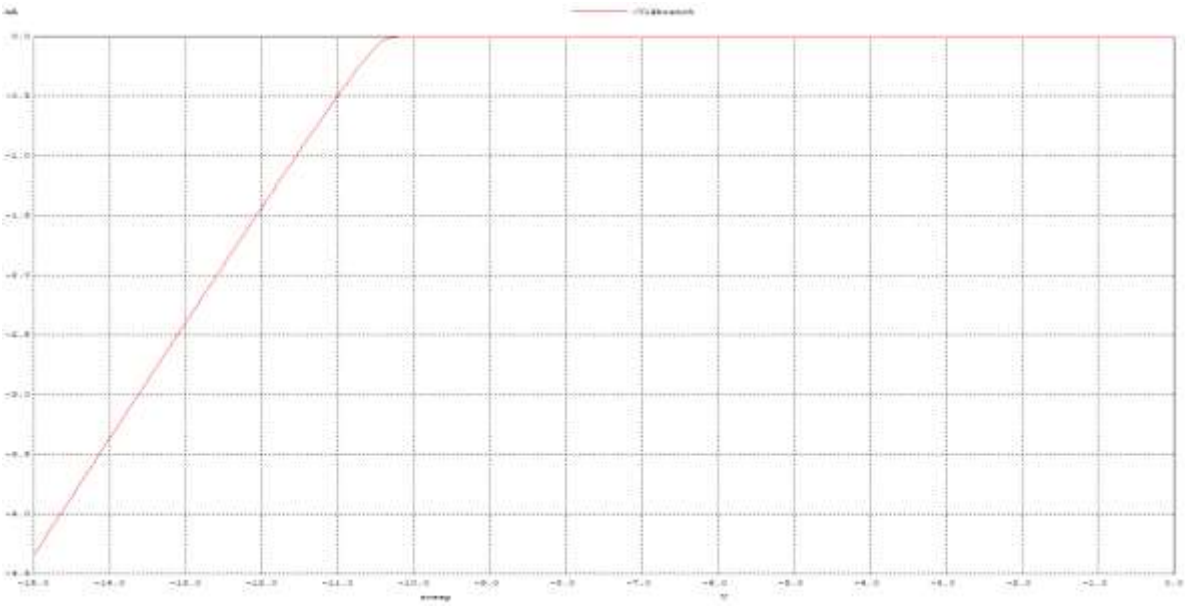
```
* Reverse recovery time of diode
.MODEL SWITCH D (IS=1E-12 RS=10 CJO=5P TT=10N BV=10)
V1 1 0 pulse (5 -3 10N 0.05N 0.05N 30N 50N)
RS 1 2 1K
D1 2 3 Switch
Vo 3 0 0

.TRAN 1N 50N
.control
run
plot v(1) v(2)
plot i(Vo)
.endc
.end
```

Result:

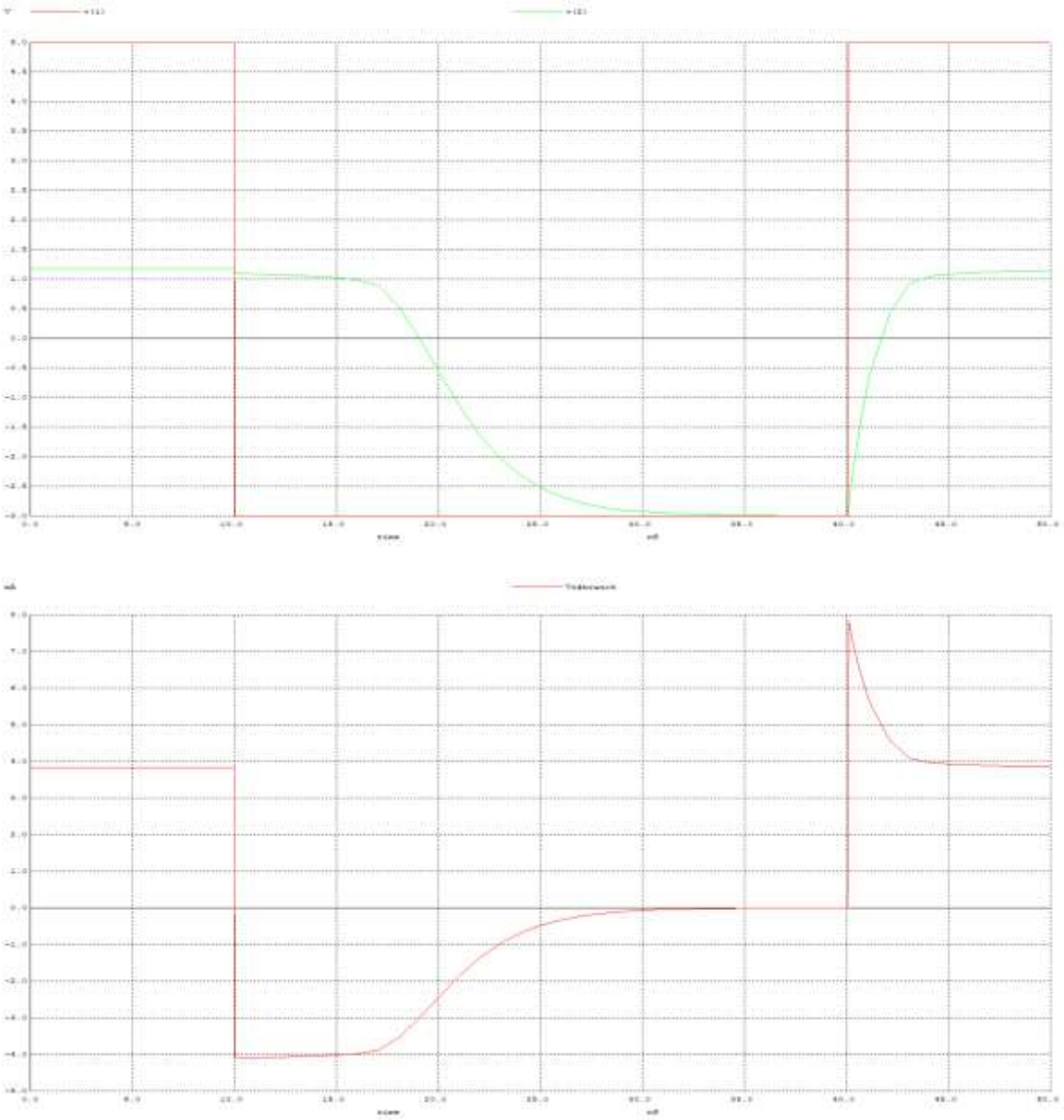
1. Forward Characteristics



2. Reverse Characteristics



3. Reverse Recovery Time



Calculation:

- Forward Resistance (Rf)= ΔVf / ΔIf = (4.62 - 3.45)V /(1.96 – 0.9)mA = 1.043 Kohm Cut in Voltage = 0.7
- Reverse Resistance (Rr)= ΔVr / ΔIr = (4 - 1)V /(5 - 2)mA = 1 Mohm, Breakdown voltage = -10.15 V
- Reverse Recovery Time Of The Diode (Trr) = 24ns

Conclusion:

In this experiment, we implemented the p-n junction diode and plotted forward and reverse characteristics of a p-n junction diode. We also calculated various parameters of diode like forward and reverse resistance, cut-in voltage and Trr.

Digital Integrated Circuits

Practical 1

Date: 28/01/2022

Aim: Implement RTL inverter and TTL inverter using NPN BJT having Bf = 20, Rb = 10k and Rc = 1k.

1. Verify its functionality by performing transient analysis.
2. Plot the VTC & Calculate the Noise margin.
3. Find out theoretical and practical fan-out & compare them.

Software: Win-SPICE

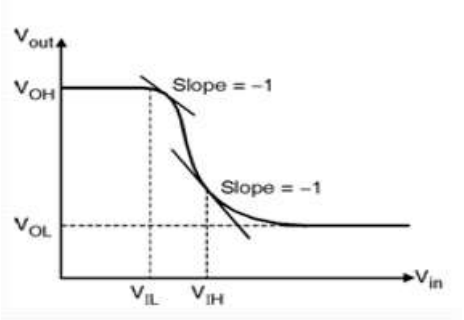
Theory:

RTL Inverter is a circuit used to invert the input signal. It consists of one BJT transistor, Base connected with resistor (Rb), Collector connected with resistor (Rc) and Emitter is grounded. Input Signal is given to Base of transistor through Rb, Vcc is connected to Rc and Output is taken at collector terminal.

Working:

For an input voltage Vi below the cut-in voltage, the transistor is off and the output voltage Vo is close to the supply voltage Vcc. For a sufficiently high input voltage, the BJT is driven to saturation so that the output is nearly at zero voltage. Thus, for the input Increasing from zero voltage to Vcc, the output decreases from about Vcc to Vce(sat), causing the inverter action.

Voltage transfer characteristics (vtc):



To study the noise margins and the fan-out capability of the RTL inverter, we should know the static behaviour of the circuit output Vout when input Vin is increased from 0 to Vcc. When Vin is below the base-emitter cut-in voltage(VIL), collector current is zero and transistor is in the cutoff mode, Vout is almost equal to Vcc (VOH) (assuming no load is connected at output) and VTC will be constant output for 0<Vin<VIL.

As Vin is increased beyond VIL , the transistor enters active mode. The collector current (Ic = βIb) causes a voltage drop in the collector resistor and the collector voltage Vc = Vout = Vcc - IcRc falls. This fall continues until output saturation voltage (Vce=VOL) BJT mode changes to saturation and corresponding input voltage is VIH.

Noise margins:

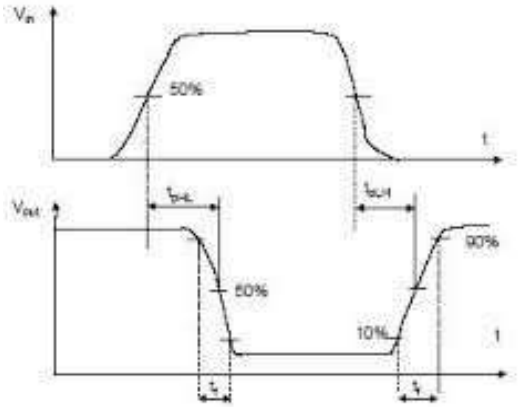
Noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels. In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'.

$NML = VIL - VOL$

$NMH = VOH - VIH$

In practice, noise margins are the amount of noise, that a logic circuit can withstand. Noise margins are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or outright failure.

Transient response:



Transient analysis means analyzing a system in unsteady state. If the variables involved in defining the state of a system does not vary with respect to time, then the system is said to be in steady state.

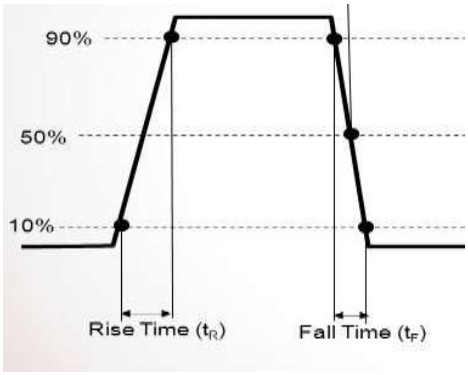
In Transient Analysis, also called time-domain transient analysis, computes the circuit's response a function of time. This analysis divides the time into segments and calculates the voltage and current levels for each interval

Propagation delay:

Propagation delay is a measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

t_{PHL} – the time it takes the output to go from a high to low

t_{PLH} – the time it takes the output to go from a low to high



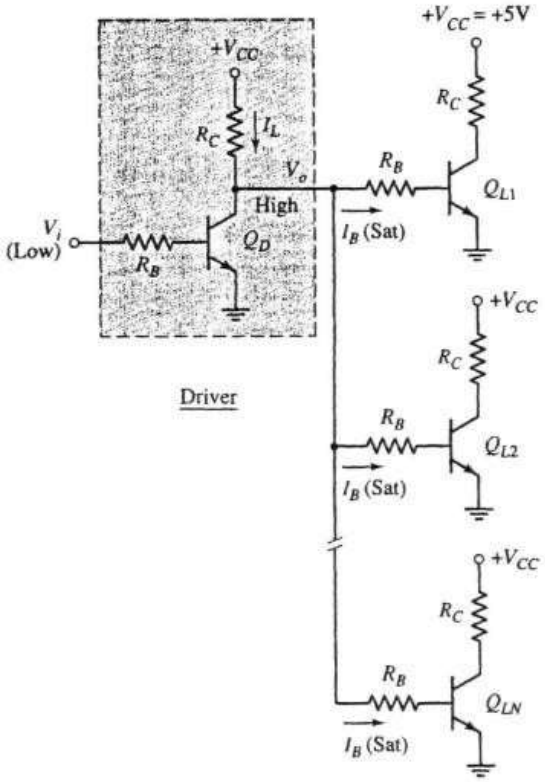
Average Propagation Delay Time $(t_P) = \frac{t_{PHL} + t_{PLH}}{2}$

Rise Time (t_r) = Time from 10% to 90%

Fall Time (t_f) = Time from 90% to 10%

Fan-out:

Fan-out of the inverter is the number of identical circuits that the inverter can drive before Vo enters the transition region. When output of RTL inverter (the driver) is at logic low, it can drive practically any number of identical inverters

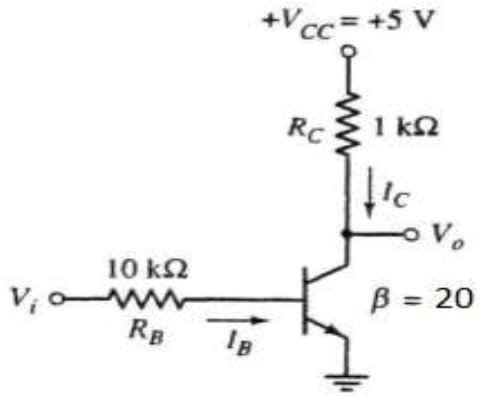


Since, each load transistor is operating in the cutoff mode, no current is drawn via the collector resistor of the driver, and the output voltage remains at logic low.

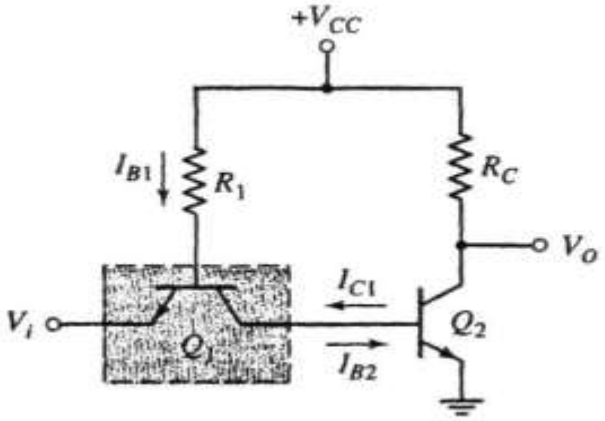
For logic high output of the driver as shown in above figure there are N identical inverters connected to output of driver circuit. Since, the saturation base current of each load inverter is supplied by the driver, output voltage Vo drops from its open circuit voltage of Vcc. The gate fan-out therefore it is limited by the number of load inverters that can be driven into saturation while maintain satisfactory logic high Vo ≥ VIH. The number depends on the current gain β of the driver transistor.

Circuit Diagram:

1. **RTL inverter using NPN BJT**



2. **TTL inverter using NPN BJT**



Code:

1. Voltage Transfer Characteristics (Static Analysis)

```
*RTL inverter DC Analysis
.model switch NPN Bf=20

Q1 2 1 0 switch
Rc 2 3 1k
Rb 4 1 10k
Vcc 3 0 5
Vin 4 0 5

.dc Vin 0 5 0.05

.control
run
plot V(2) V(4)
.endc
.end
```

2. Transient Analysis

```
*RTL inverter Transient Analysis

.model switch NPN Bf=20

Q 2 1 0 switch
Rc 2 3 1k
Rb 4 1 10k
Vcc 3 0 5
Vin 4 0 pulse (0 5 1ns 1ns 1ns 20us 40us)
c 2 0 1p

.tran 1ns 80us

.control
run
plot V(4) V(2)
.endc
.end
```

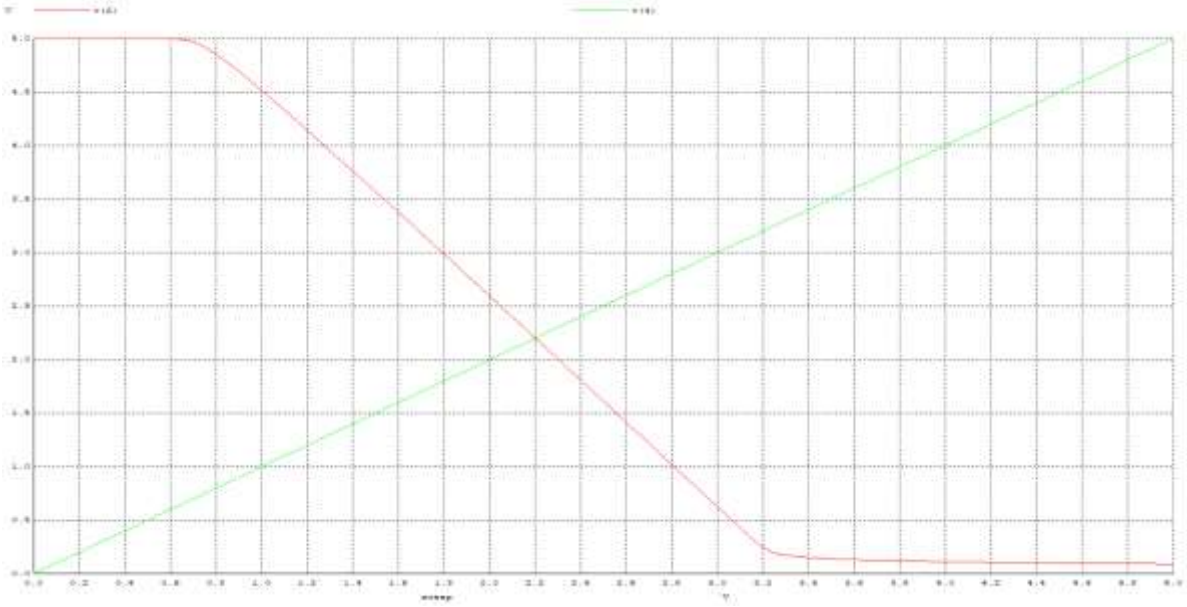
3. Fanout

```
*RTL inverter fanout

.model switch NPN Bf=20

Q 2 1 0 switch
Rc 2 3 1k
Rb 4 1 10k
```

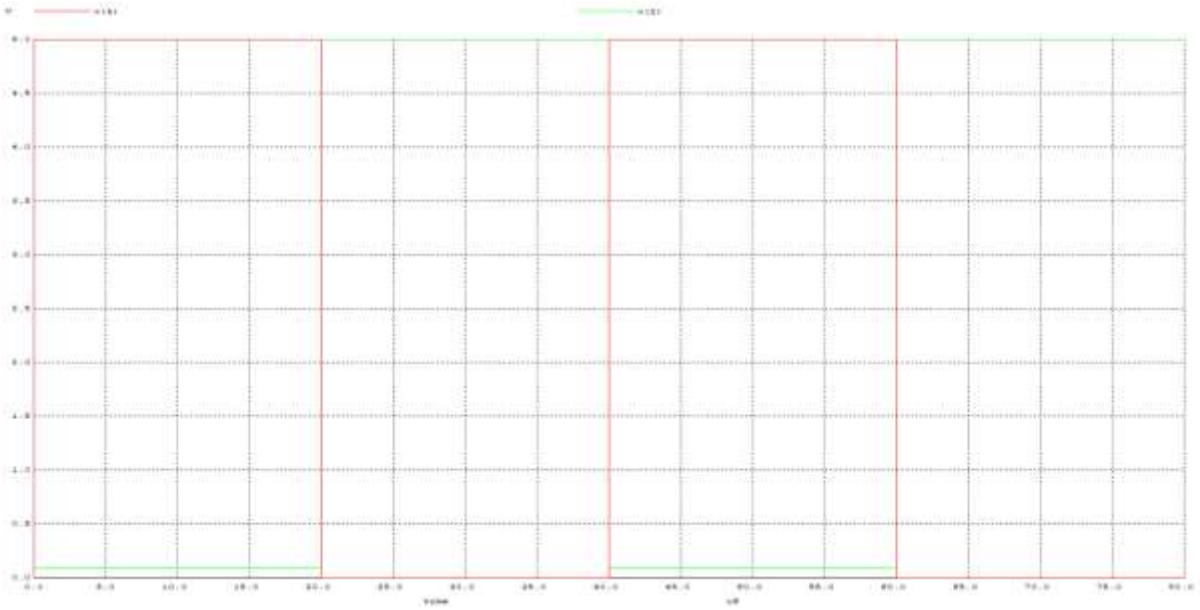
```
Vcc 3 0 5
Vin 4 0 5
.subckt rt1 out in c 0
q2 out y 0 switch
Rb1 in y 10k
Rc1 c out 1k
.ends Rt1

X1 out1 2 3 0 Rt1
X2 out2 2 3 0 Rt1
X3 out3 2 3 0 Rt1
X4 out4 2 3 0 Rt1
X5 out5 2 3 0 Rt1
X6 out6 2 3 0 Rt1
X7 out7 2 3 0 Rt1
X8 out8 2 3 0 Rt1

.dc Vin 0 5 0.05

.control
run
plot V(2) V(4)
*plot V(out1)
.endc
.end
```

Result:

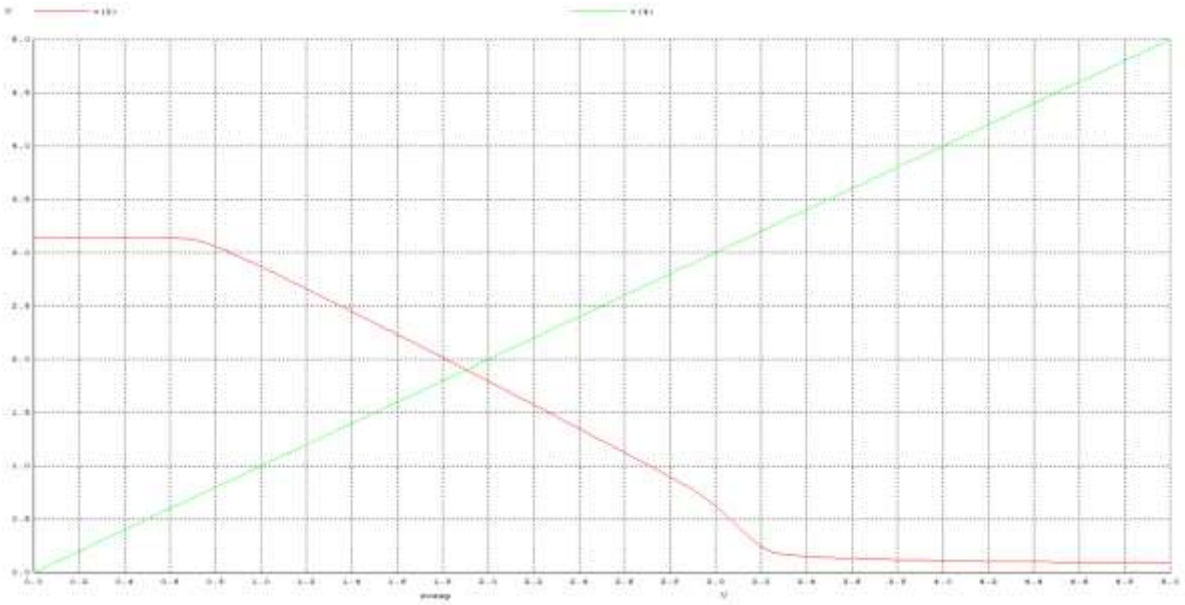
1. Voltage Transfer Characteristics (Static Analysis)



2. **Transient Analysis**



3. **Fanout**



Calculation:

1) **VTH And Noise Margin:**

NML = VIL – VOL = 0.700 – 0.0906 = 0.6094V

NMH = VOH – VIH = 5 – 3.2 = 1.8V

NM = min(NML , NMH) = 0.6094V

VTH = 2.2V

2) Propagation Delay:

a. Low to High

t1 = 60.0025ns, t2 = 60.0033ns

t_lh = t2 – t1 = 0.8 ns

b. High to Low

t1 = 40.00154us, t2 = 40.00232us,

t_hl = t2 -t1 = 0.78ns

t_propogation_delay = avg(0.7, 0.78) = 0.74ps

Trise = 2.3ns

Tfall = 0.96ns

3) Fanout:

After Connecting 8 device Voh>Vih condition violates, therefore Fanout=7

Assignment- TTL inverter using NPN BJT

Code:

1. Voltage Transfer Characteristics and Noise Margin

```
*TTL Inverter static(DC) Analysis
.model switch NPN (Bf=20)
Q1 2 1 4 switch
Q2 3 2 0 switch
R2 5 3 1.6k
R1 5 1 4k
Vcc 5 0 5
Vin 4 0 dc 5

.dc Vin 0 5 0.05
.control
run
plot v(3) v(4)
.endc
.end
```

2. Propagation Delay

```
*TTL Inverter Transient Analysis

.model switch NPN (Bf=20)
Q1 2 1 4 switch
Q2 3 2 0 switch
R2 5 3 1.6k
R1 5 1 4k
Vcc 5 0 5
Vin 4 0 pulse(0 5 1ns 1ns 1ns 20us 40us)
c 3 0 1p
.tran 1ns 80us
.control
run
plot v(3) v(4)
.endc
.end
```

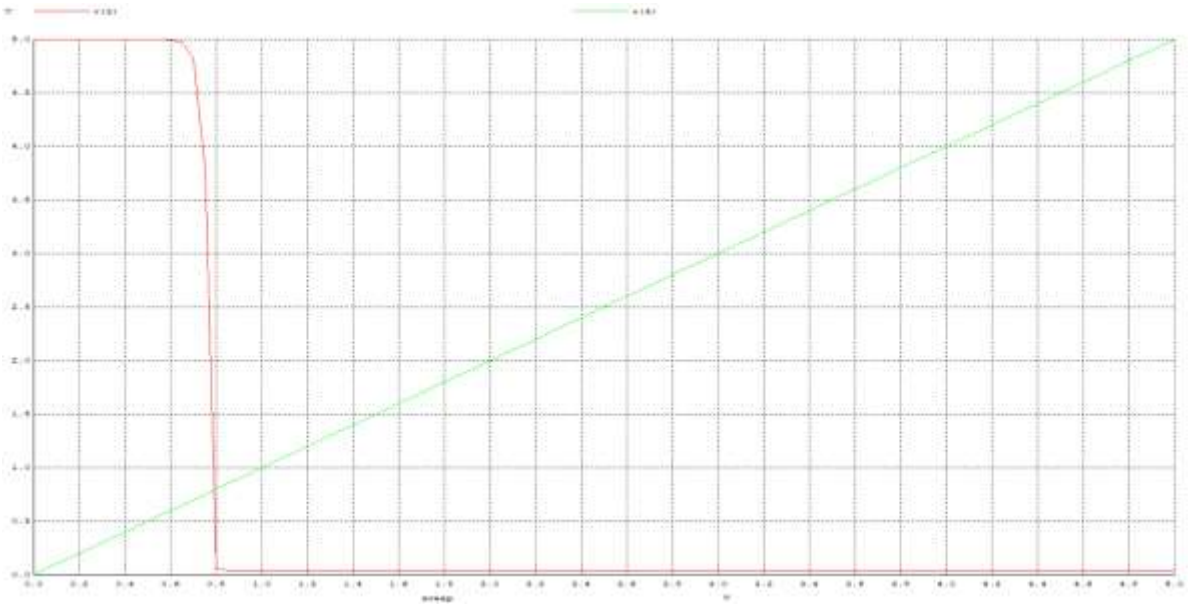
3.Fanout

```
*TTL Inverter fanout
.model switch NPN (Bf=20)

Q1 2 1 4 switch
Q2 3 2 0 switch
R2 5 3 1.6k
R1 5 1 4k
```

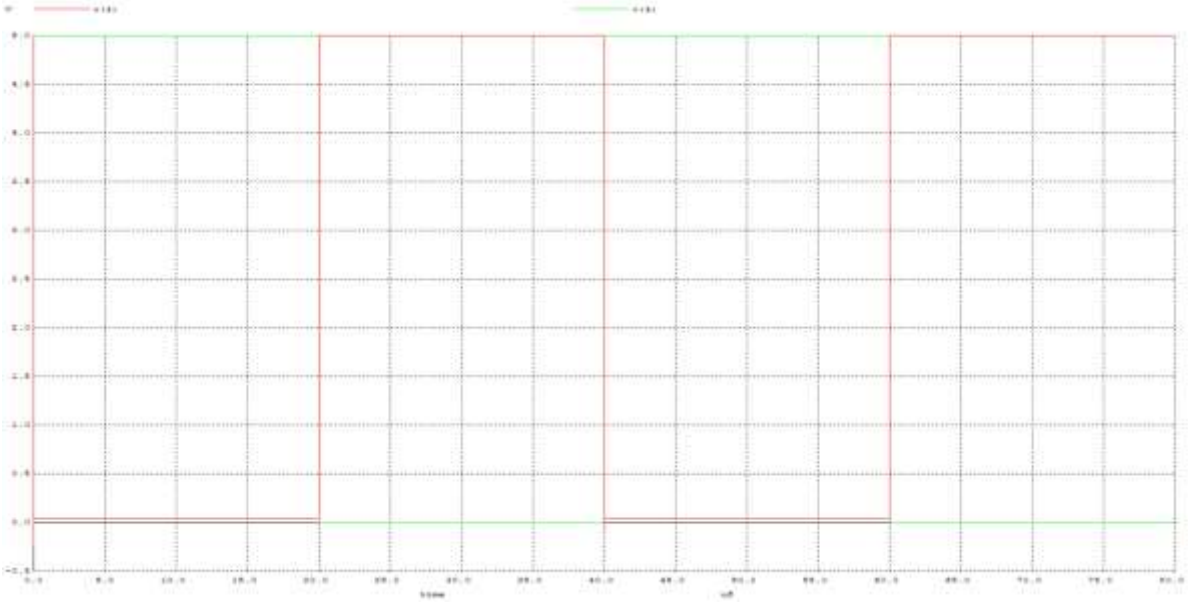
```
Vcc 5 0 5
Vin 4 0 5
.subckt ttl out in c 0
Q3 out y 0 switch
Q4 y z in switch
R3 out c 1.6k
R4 z c 4k
.ends ttl

x1 out1 3 5 0 ttl
x2 out2 3 5 0 ttl
x3 out3 3 5 0 ttl
x4 out4 3 5 0 ttl

.dc Vin 0 5 0.05
.control
run
plot v(3) v(4)
.endc
.end
```

Results:

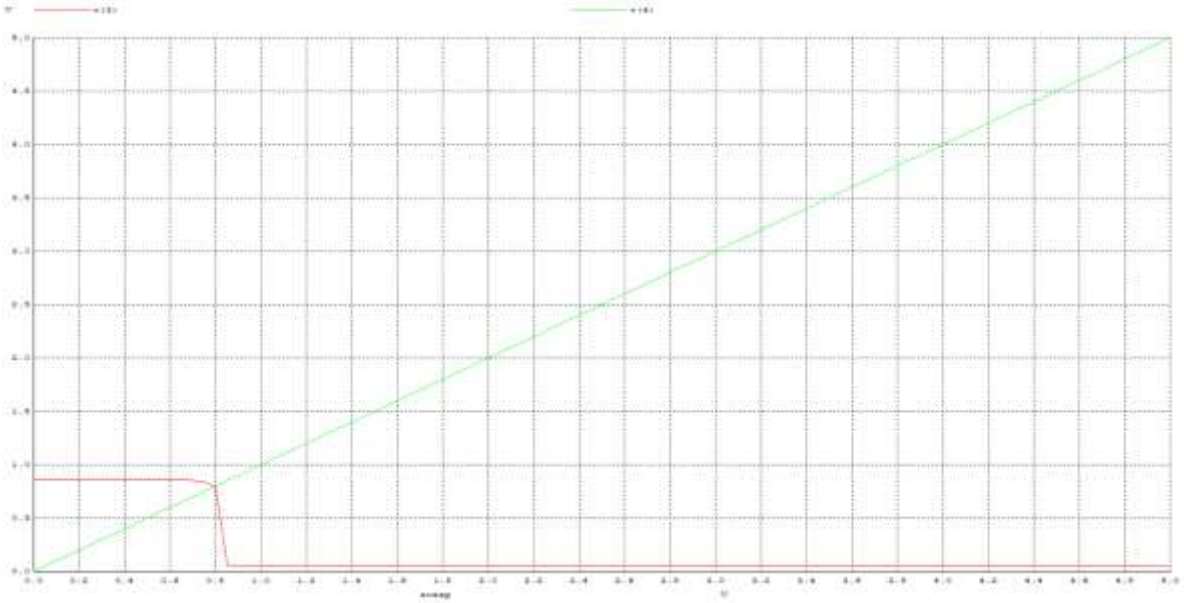
1. VTC and Noise Margin



2. **Propagation Delay**



3. **Plot for Fan Out = 4 (Bf = 20)**



Calculations:

1. **VTL And Noise Margin:**

Vil = 0.7 V, Vih = 0.8 V, Voh =5V, Vol = 0.037 V Vth=0.79V

NM_L = Vil - Vol = 0.7- 0.037V = 0.663 V

NM_H = Voh – Vih = 5 – 0.8 V = 4.2V, NM = min(NM_H, NM_L) = 0.663V

2. **Propagation Delay:**

a) Low to High

t_lh =t2 – t1= 0.25ns

b) High to Low

t_hl = t2 -t1 = 1.5 ns

t_propogation_delay = (1.5+0.25)/2 = 0.875ns

Trise=3.5ns

Tfall=0.2ns

3. **Fanout:**

After Connecting 5 device Voh>Vih condition violates so

Fanout=4

Conclusion:

In this experiment we have implemented the RTL Inverter logic and TTL Inverter logic families and plotted its characteristics and also calculated parameters and fanout of both the circuits.

Digital Integrated Circuits

Practical 2

Date: 04/02/2022

Aim: Implement DTL NAND gate using parameters Bf=50, R1=2k, Rc=4k, R2=20k.
1. Perform the static analysis and calculate the noise margin.
2. Verify its functionality by performing transient analysis.
3. Find out practical Fan-out.

Software: Win-SPICE

Theory:

Introduction

Diode-Transistor Logic, or DTL, refers to the technology for designing and fabricating digital circuits wherein logic gates employ both diodes and transistors. DTL offers better noise margins and greater fan-outs than RTL, but suffers from low speed, especially in comparison to TTL. RTL allows the construction of NOR gates easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.Below figure shows an example of an 2-input DTL NAND gate. It consists of a single transistor Q configured as an inverter, which is driven by a current that depends on the inputs to the three input diodes D1 and D2.

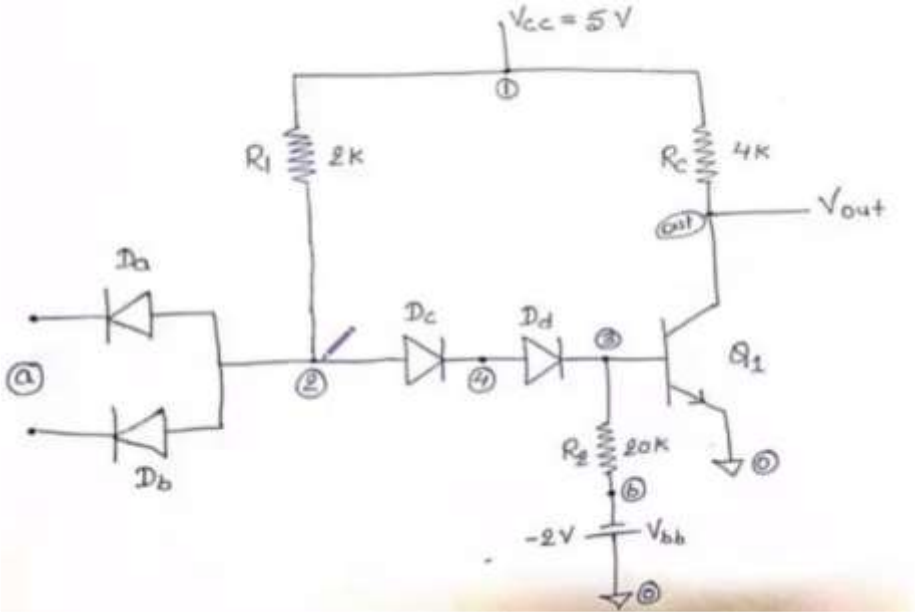
Working principle

In the NAND gate in Figure 1, the current through diodes DA and DB will only be large enough to drive the transistor into saturation and bring the output voltage Vo to logic '0' if all the input diodes D1 qne D3 are 'off', which is true when the inputs to all of them are logic '1'. This is because when D1-D3 are not conducting, all the current from Vcc through R will go through DA and DB and into the base of the transistor, turning it on and pulling Vo to near ground.However, if any of the diodes D1 and D2 gets an input voltage of logic '0', it gets forward-biased and starts conducting. This conducting diode 'shunts' almost all the current away from the reverse-biased DA and DB, limiting the transistor base current. This forces the transistor to turn off, bringing up the output voltage Vo to logic '1'.

Application

One advantage of DTL over RTL is its better noise margin. The noise margin of a logic gate for logic level '0', $\Delta 0$, is defined as the difference between the maximum input voltage that it will recognize as a '0' (Vil) and the maximum voltage that may be applied to it as a '0' (Vol of the driving gate connected to it). For logic level '1', the noise margin $\Delta 1$ is the difference between the minimum input voltage that may be applied to it as a '1' (Voh of the driving gate connected to it) and the minimum input voltage that it will recognize as a '1' (Vih).

Circuit Diagram:



Code:

4. Voltage Transfer Characteristics (Static Analysis)

```
*dtl transfer char*
.model q1 npn bf=50
q11 out 3 0 q1
.model d1 d
da 2 a d1
db 2 a d1
dc 2 4 d1
dd 4 3 d1
r1 1 2 2k
rc 1 out 4k
r2 3 b 20k
vbb b 0 -2
vcc 1 0 5
va a 0 pulse(0 5 0ps 10ps 200ps 1000ps)
.dc va 0 5 0.05
.control
run
plot v(a) v(out)
.endc
.end
```

5. Transient Analysis

```
*dtl NAND transient response*
.model q1 npn bf=50
q11 out 3 0 q1
```

```
.model d1 d
da 2 a d1
db 2 a d1
dc 2 4 d1
dd 4 3 d1
r1 1 2 2k
rc 1 out 4k
r2 3 b 20k
vbb b 0 -2
vcc 1 0 5
va a 0 pulse(0 5 20ps 10ps 10ps 200ps 550ps)

.tran 20ps 1500ps
.control
run
plot v(a) v(out)
.endc
.end
```

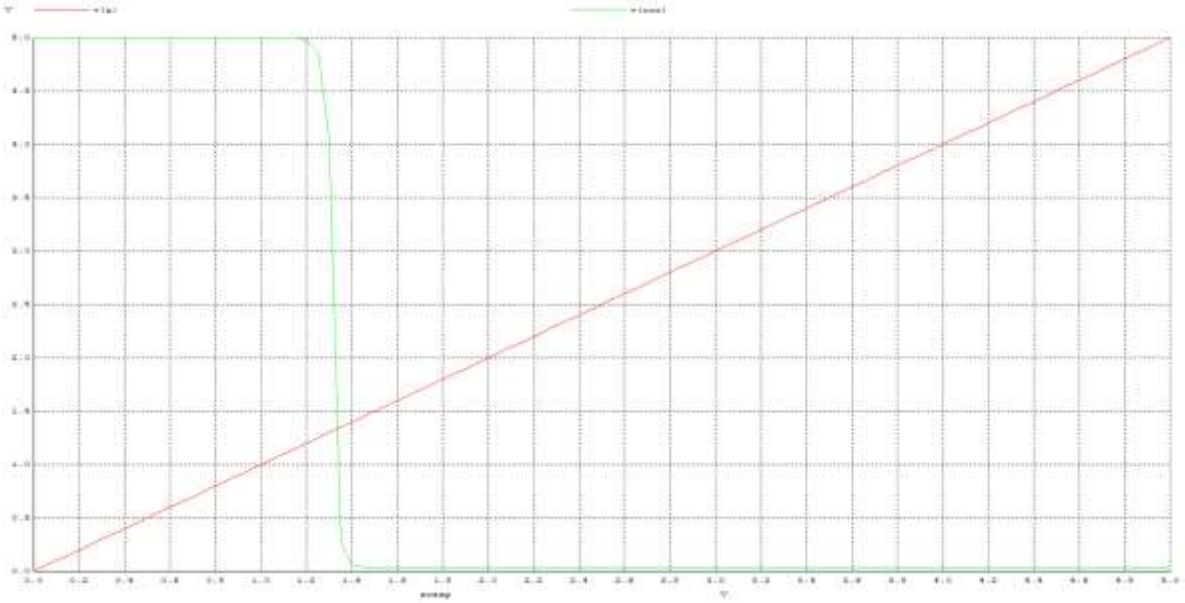
6. Fanout

```
*dtl NAND fanout*
.model q1 npn bf=50
.model d1 d
.subckt dtlckt a b c 1 0 out
q1 out 4 0 q1
da 2 a d1
db 2 a d1
dc 2 3 d1
dd 3 4 d1
r1 2 1 2k
rc 1 out 4k
r2 4 c 20k
.ends dtlckt
*supply
vcc 1 0 5
vbb c 0 -2
va a 0 5
*Driver gate
xd a a c 1 0 out1 dtlckt
*Load gates
XL1 out1 out1 c 1 0 out2 dtlckt
XL2 out1 out1 c 1 0 out3 dtlckt
XL3 out1 out1 c 1 0 out4 dtlckt
XL4 out1 out1 c 1 0 out5 dtlckt
XL5 out1 out1 c 1 0 out6 dtlckt
XL6 out1 out1 c 1 0 out7 dtlckt
XL7 out1 out1 c 1 0 out8 dtlckt
```

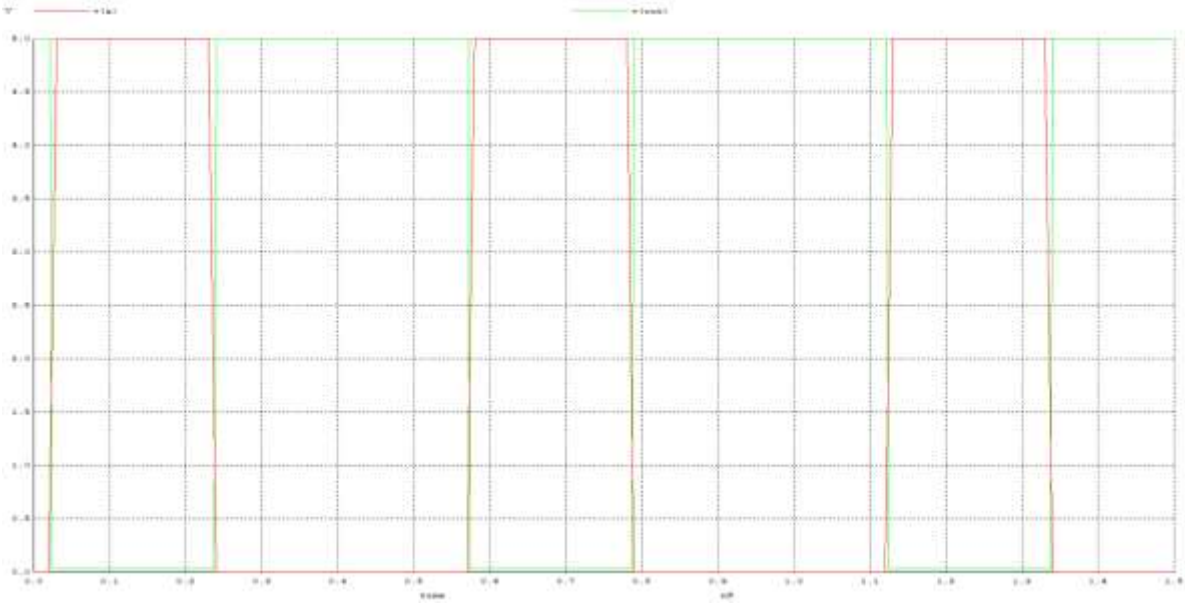
```
XL8 out1 out1 c 1 0 out9 dtlckt
XL9 out1 out1 c 1 0 out10 dtlckt
XL10 out1 out1 c 1 0 out11 dtlckt
XL11 out1 out1 c 1 0 out12 dtlckt
XL12 out1 out1 c 1 0 out13 dtlckt
XL13 out1 out1 c 1 0 out14 dtlckt
XL14 out1 out1 c 1 0 out15 dtlckt
XL15 out1 out1 c 1 0 out16 dtlckt
XL16 out1 out1 c 1 0 out17 dtlckt
XL17 out1 out1 c 1 0 out18 dtlckt
XL18 out1 out1 c 1 0 out19 dtlckt
XL19 out1 out1 c 1 0 out20 dtlckt
XL20 out1 out1 c 1 0 out21 dtlckt
XL21 out1 out1 c 1 0 out22 dtlckt
XL22 out1 out1 c 1 0 out23 dtlckt
XL23 out1 out1 c 1 0 out24 dtlckt
XL24 out1 out1 c 1 0 out25 dtlckt
XL25 out1 out1 c 1 0 out26 dtlckt
XL26 out1 out1 c 1 0 out27 dtlckt
XL27 out1 out1 c 1 0 out28 dtlckt
XL28 out1 out1 c 1 0 out29 dtlckt
XL29 out1 out1 c 1 0 out30 dtlckt
XL30 out1 out1 c 1 0 out31 dtlckt
XL31 out1 out1 c 1 0 out32 dtlckt
XL32 out1 out1 c 1 0 out33 dtlckt
XL33 out1 out1 c 1 0 out34 dtlckt
XL34 out1 out1 c 1 0 out35 dtlckt
XL35 out1 out1 c 1 0 out36 dtlckt
XL36 out1 out1 c 1 0 out37 dtlckt
XL37 out1 out1 c 1 0 out38 dtlckt
XL38 out1 out1 c 1 0 out39 dtlckt
XL39 out1 out1 c 1 0 out40 dtlckt
XL40 out1 out1 c 1 0 out41 dtlckt
XL41 out1 out1 c 1 0 out42 dtlckt
XL42 out1 out1 c 1 0 out43 dtlckt
XL43 out1 out1 c 1 0 out44 dtlckt
*XL44 out1 out1 c 1 0 out45 dtlckt
.dc va 0.5 5 0.05
.control
run
plot v(out1) v(a)
.endc
.end
```

Result:

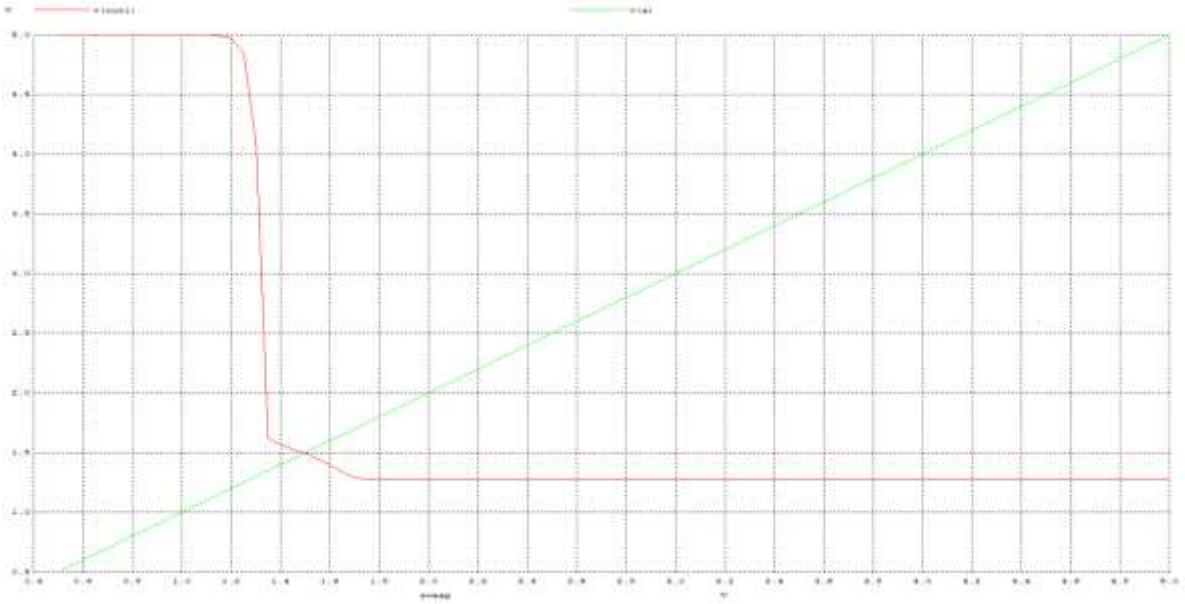
1. Voltage Transfer Characteristics (Static Analysis)



2. Transient Analysis



3. Fanout



Calculation:

1)VTL And Noise Margin:

Vil = 1.2 V, Vih = 1.4 V, Voh =5V, Vol = 0.029 V
NM_H = 1.276 – 0.0535 = 1.2225V
NM_L = 5 – 1.40 = 3.6V, NM = min(NM_H, NM_L) = 1.22V

2)Propagation Delay:

a) Low to High

t1 = 563.26ps, t2 = 566.75ps
t_hl = 3.49ps

b)High to Low

t1 = 572.92ps , t2 = 575ps
t_hl = 2.08ps

t_propogation_delay = avg(2.08, 3.49) = 2.782ps
t_rise = 2.42ps
t_fall = 1.1917ps

3)Fanout:

After Connecting 44 device Vil≥Vol condition violates so Fanout=43. (Bf = 50)

Conclusion:

In this experiment, we implemented DTL NAND gate circuit using NPN BJT in Spice Simulation. We also plotted Voltage Transfer Characteristics of DTL, calculated its noise margin, and verified its functionality by performing transient analysis. We also calculated the fanout for the circuit.

Digital Integrated Circuits

Practical 3

Date: 11/02/2022

Aim:

Implement M-DTL NAND gate using NPN BJT having BF= 20, R1=1.75K R2=2K RC=4K VCC= 5V
(1) Verify the functionality of DTL as NAND
(2) Calculate noise margin from VTC characteristics
(3) Calculate theoretical and practical fanout

Software: Win-SPICE

Theory:

Introduction

Diode-Transistor Logic, or DTL, refers to the technology for designing and fabricating digital circuits wherein logic gates employ both diodes and transistors. DTL offers better noise margins and greater fan-outs than RTL, but suffers from low speed, especially in comparison to TTL. RTL allows the construction of NOR gates easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.Below figure shows an example of an 2-input DTL NAND gate. It consists of a single transistor Q configured as an inverter, which is driven by a current that depends on the inputs to the three input diodes D1 and D2.

Working principle

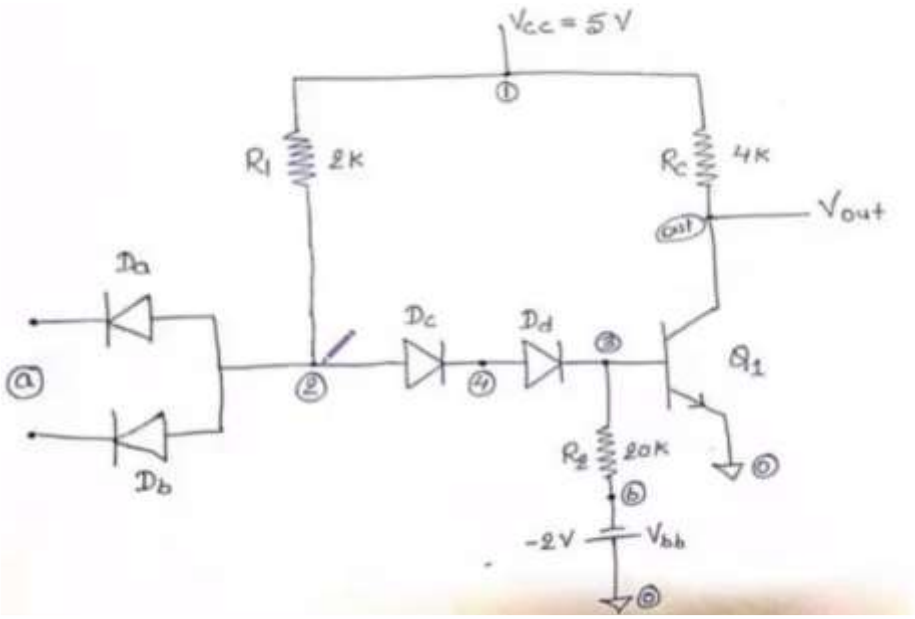
In the NAND gate in Figure 1, the current through diodes DA and DB will only be large enough to drive the transistor into saturation and bring the output voltage Vo to logic '0' if all the input diodes D1 qne D3 are 'off', which is true when the inputs to all of them are logic '1'. This is because when D1-D3 are not conducting, all the current from Vcc through R will go through DA and DB and into the base of the transistor, turning it on and pulling Vo to near ground.However, if any of the diodes D1 and D2 gets an input voltage of logic '0', it gets forward-biased and starts conducting. This conducting diode 'shunts' almost all the current away from the reverse-biased DA and DB, limiting the transistor base current. This forces the transistor to turn off, bringing up the output voltage Vo to logic '1'.

Application

One advantage of DTL over RTL is its better noise margin. The noise margin of a logic gate for logic level '0', $\Delta 0$, is defined as the difference between the maximum input voltage that it will recognize as a '0' (Vil) and the maximum voltage that may be applied to it as a '0' (Vol of the driving gate connected to it). For logic level '1', the noise margin $\Delta 1$ is the difference

between the minimum input voltage that may be applied to it as a '1' (Voh of the driving gate connected to it) and the minimum input voltage that it will recognize as a '1' (Vih).

Circuit Diagram:



Code:

1. **Voltage Transfer Characteristics and Noise Margin-**

```
*MDTL transfer char
.model bjt npn bf=20
.model diode d

.subckt modifiedDTL in1 in2 vccNode gnd out
    rc vccNode out 2k
    q2 out q2base gnd bjt
    r3 q2base gnd 5k
    dd q1emmiter q2base diode
    q1 q1collector q1base q1emmiter bjt
    r2 q1collector q1base 2k
    r1 q1collector vccNode 1.75k
    da q1base in1 diode
    db q1base in2 diode
.ends dtlckt

*supply
vcc vccNode 0 5
Va in 0 5

*driver gate
Xd in in vccNode 0 out1 modifiedDTL
.dc Va 0 5 0.05
.control
run
plot v(in) v(out1)
```

```
.endc
.end
```

2. Propagation Delay

```
*MDTL NAND Transient Response
.Model mybjt NPN bf=20
.Model D1 D
Q1 2 3 5 mybjt
Q2 out 4 0 mybjt
R1 2 1 1.75k
R2 3 2 2k
R3 4 0 5k
Rc 1 out 2k
Da 3 a D1
Db 3 b D1
Dc 5 4 D1
Vcc 1 0 5
Va a 0 pulse(0 5 0ps 10ps 10ps 200ps 550ps)
Vb b 0 pulse(0 5 5ps 10ps 10ps 100ps 550ps)

.tran 20ps 1500ps
.control
run
plot V(a) V(b) V(out)
.endc
.end
```

3. Fanout:

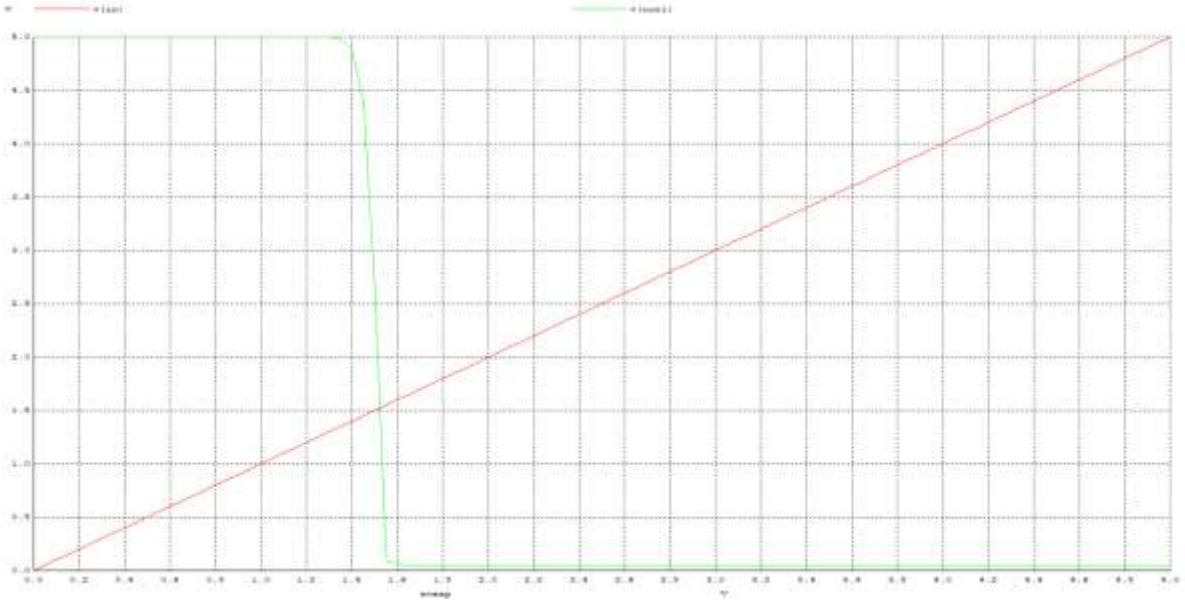
```
*MDTL NAND Fanout

.model q1 npn bf=50
.model d1 d

.subckt dtlckt a 1 0 out
q11 c1 b1 e1 q1
q12 out b2 0 q1
Da b1 a d1
Db b1 a d1
D1 e1 b2 d1
R1 1 c1 1.75k
R2 c1 b1 2k
Rc 1 out 4k
Rb b2 0 5k
.ends dtlckt

*Supply
Vcc 1 0 5
Va a 0 5

*Driver gate
Xd a 1 0 out1 dtlckt
*Load gates
```

```
XL1 out1 1 0 out2 dtlckt
XL2 out1 1 0 out3 dtlckt
XL3 out1 1 0 out4 dtlckt
XL4 out1 1 0 out5 dtlckt
XL5 out1 1 0 out6 dtlckt
XL6 out1 1 0 out7 dtlckt
XL7 out1 1 0 out8 dtlckt
XL8 out1 1 0 out9 dtlckt
XL9 out1 1 0 out10 dtlckt
XL10 out1 1 0 out11 dtlckt
XL11 out1 1 0 out12 dtlckt
XL12 out1 1 0 out13 dtlckt
XL13 out1 1 0 out14 dtlckt
XL14 out1 1 0 out15 dtlckt
XL15 out1 1 0 out16 dtlckt
XL16 out1 1 0 out17 dtlckt
XL17 out1 1 0 out18 dtlckt
XL18 out1 1 0 out19 dtlckt
XL19 out1 1 0 out20 dtlckt
XL20 out1 1 0 out21 dtlckt
XL21 out1 1 0 out22 dtlckt
XL22 out1 1 0 out23 dtlckt
XL23 out1 1 0 out24 dtlckt
XL24 out1 1 0 out25 dtlckt
XL25 out1 1 0 out26 dtlckt
XL26 out1 1 0 out27 dtlckt
XL27 out1 1 0 out28 dtlckt
XL28 out1 1 0 out29 dtlckt
XL29 out1 1 0 out30 dtlckt
XL30 out1 1 0 out31 dtlckt
XL31 out1 1 0 out32 dtlckt
XL32 out1 1 0 out33 dtlckt
XL33 out1 1 0 out34 dtlckt
XL34 out1 1 0 out35 dtlckt
XL35 out1 1 0 out36 dtlckt
XL36 out1 1 0 out37 dtlckt
XL37 out1 1 0 out38 dtlckt
XL38 out1 1 0 out39 dtlckt
XL39 out1 1 0 out40 dtlckt
XL40 out1 1 0 out41 dtlckt
XL41 out1 1 0 out42 dtlckt
XL42 out1 1 0 out43 dtlckt
XL43 out1 1 0 out44 dtlckt
XL44 out1 1 0 out45 dtlckt
XL45 out1 1 0 out46 dtlckt
XL46 out1 1 0 out47 dtlckt
XL47 out1 1 0 out48 dtlckt
XL48 out1 1 0 out49 dtlckt
XL49 out1 1 0 out50 dtlckt
XL50 out1 1 0 out51 dtlckt
XL51 out1 1 0 out52 dtlckt
XL52 out1 1 0 out53 dtlckt
XL53 out1 1 0 out54 dtlckt
XL54 out1 1 0 out55 dtlckt
XL55 out1 1 0 out56 dtlckt
```

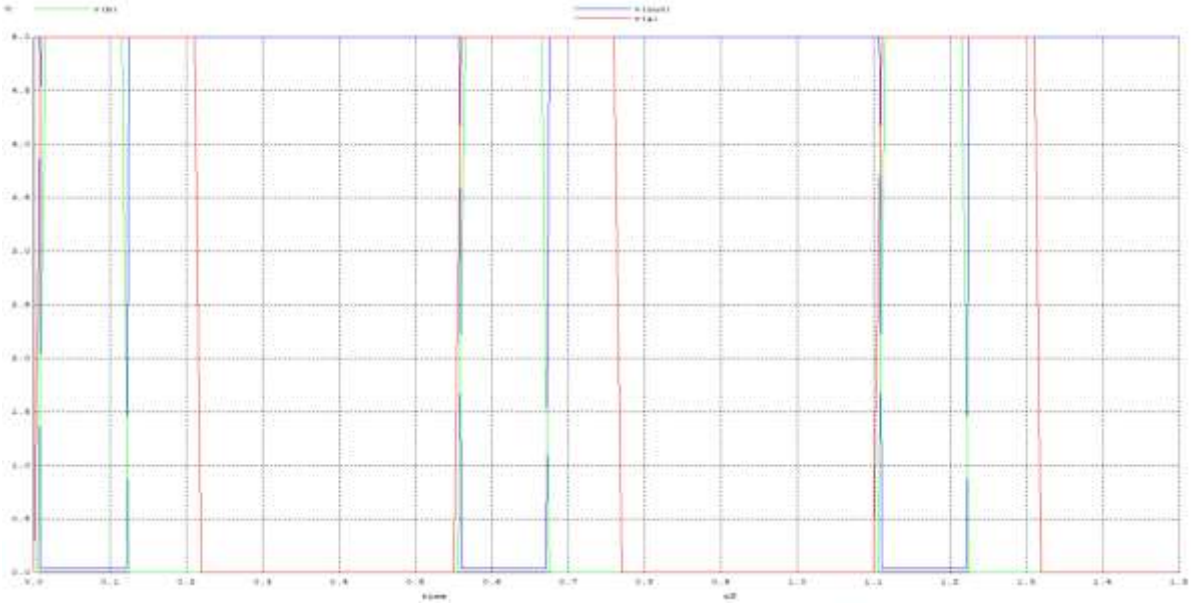
```
XL56 out1 1 0 out57 dtlckt
XL57 out1 1 0 out58 dtlckt
XL58 out1 1 0 out59 dtlckt
XL59 out1 1 0 out60 dtlckt
XL60 out1 1 0 out61 dtlckt
XL61 out1 1 0 out62 dtlckt
XL62 out1 1 0 out63 dtlckt
XL63 out1 1 0 out64 dtlckt
XL64 out1 1 0 out65 dtlckt
XL65 out1 1 0 out66 dtlckt
XL66 out1 1 0 out67 dtlckt
XL67 out1 1 0 out68 dtlckt
XL68 out1 1 0 out69 dtlckt
XL69 out1 1 0 out70 dtlckt
XL70 out1 1 0 out71 dtlckt
XL71 out1 1 0 out72 dtlckt
XL72 out1 1 0 out73 dtlckt
XL73 out1 1 0 out74 dtlckt
XL74 out1 1 0 out75 dtlckt
XL75 out1 1 0 out76 dtlckt
XL76 out1 1 0 out77 dtlckt
XL77 out1 1 0 out78 dtlckt
XL78 out1 1 0 out79 dtlckt
XL79 out1 1 0 out80 dtlckt
XL80 out1 1 0 out81 dtlckt
XL81 out1 1 0 out82 dtlckt
XL82 out1 1 0 out83 dtlckt
XL83 out1 1 0 out84 dtlckt
XL84 out1 1 0 out85 dtlckt
XL85 out1 1 0 out86 dtlckt
XL86 out1 1 0 out87 dtlckt
XL87 out1 1 0 out88 dtlckt
XL88 out1 1 0 out89 dtlckt
XL89 out1 1 0 out90 dtlckt
*XL90 out1 1 0 out91 dtlckt

.dc Va 0 5 0.05
.control
run
plot v(out1) v(a)
.endc
.end
```

Output:

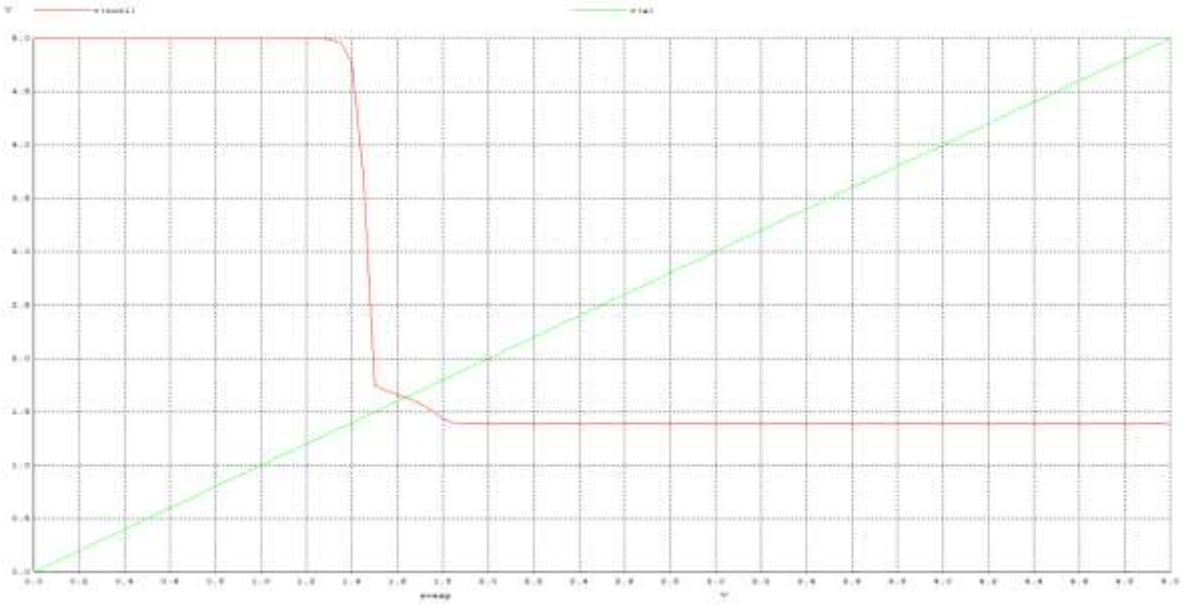
- **Voltage Transfer Characteristics**



- **DTL NAND Transient Response**



- **Fanout**



Calculations:

VTL And Noise Margin:

From graph,

Voh =5V

Vil= 1.43V

Vih= 1.55 V

Vol= 38mV = 0.038V

Vth= 1.52V

NM_L = Vil - Vol = 1.43 – 0.038 V = 1.392V

NM_H = Voh – Vih = 5- 1.55 V = 3.45V,

NM = min(NM_H, NM_L) = 1.392V

Propagation Delay:

a) Low to High

t1 =1.1025ps,

t2 =1.1050ps

t_lh =t2 – t1= 2.5ps

b) High to Low

t1 = 552.4ps,

t2 = 555ps,

t_hl = t2 -t1 = 2.6ps

t_propogation_delay = avg(2.5, 2.6) = 2.55ps

Trise = 3.0ps

Tfall = 0.24ps

Fanout:

After Connecting 34 device for bf =20 Vil≥Vol condition violates, therefore fanout=33

After Connecting 90 device for bf =50 Vil≥Vol condition violates, therefore fanout=89

Beta	Fanout
20	34
50	89

Comparision of DTL and MDTL:

Parameter	DTL	MDTL
Noise Margin	1.15V	1.3V
Propogation delay	2.85us	0.75ns
Fan out	42	88

Conclusion:

In this Experiment we have implemented spice code for Modified diode transistor logic and also calculated its VTC, noise margin and fanout and we observed that the noise margin of MDTL is increased slightly and the propagation delay was reduced by an order of 10^3 and fan out is increased substantially as compared with DTL family.

Digital Integrated Circuits

Practical 4

Date: 18/02/2022

Aim:

To verify the functionality of TTL as inverter and find out propagation delay, noisemargin & fan-out parameters.

1. Verify its functionality by performing transient analysis
2. Plot the VTC & calculate the noise margin
3. Find out practical fan-out.

Theory:

Transistor–transistor logic (TTL) is a logic family built from bipolar junction transistors. Its name signifies that transistors perform both the logic function (the first "transistor") and the amplifying function (the second "transistor"), as opposed to resistor–transistor logic (RTL) or diode–transistor logic (DTL).

This simplified NAND gate circuit consists of an input transistor, TR1 which has two (or more) emitter terminals and a single stage inverting NPN switching transistor circuit of TR2. When either or both of the emitters of TR1 representing inputs “A” and “B” are connected to logic level “0” (LOW), the base current of TR1 passes through its base/emitter junction to ground (0V), TR1 saturates and its collector terminal follows. This action results in the base of TR2 becoming connected to ground (0V), hence TR2 is “OFF” and the output at Q is HIGH.

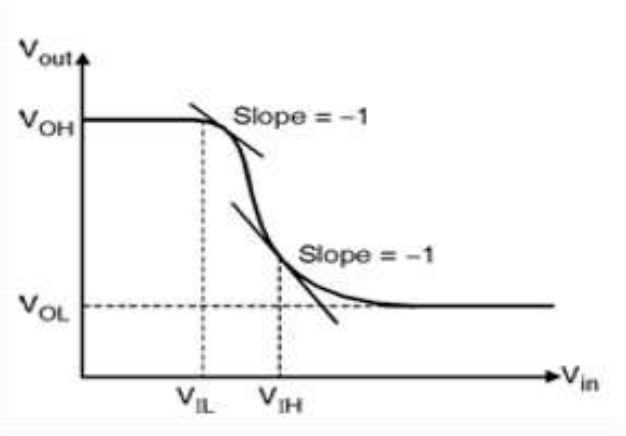
With both inputs “A” and “B” HIGH at logic level “1”, input transistor TR1 turns “OFF”, the base of switching transistor TR2 becomes HIGH and turns it “ON” so the output at Q is LOW due to the switching action of the transistor. The multiple emitters of TR1 are connected as inputs thus producing a NAND gate function.

RTL Inverter is a circuit used to invert the input signal. It consists of one BJT transistor, Base connected with resistor (Rb), Collector connected with resistor (Rc) and Emitter is grounded. Input Signal is given to Base of transistor through Rb, Vcc is connected to Rc and Output is taken at collector terminal.

Voltage Transfer Characteristics (Vtc):

To study the noise margins and the fan-out capability of the RTL inverter, we should know the static behaviour of the circuit output Vout when input Vin is increased from 0 to Vcc. When Vin is below the base-emitter cut-in voltage(VIL), collector current is zero and transistor is in the cutoff mode, Vout is almost equal to Vcc (VOH) (assuming no load is connected at output) and VTC will be constant output for 0<Vin<VIL.

As Vin is increased beyond VIL , the transistor enters active mode. The collector current (Ic = βIb) causes a voltage drop in the collector resistor and the collector voltage Vc = Vout = Vcc - IcRc falls. This fall continues until output saturation voltage (Vce=VOL) BJT mode changes to saturation and corresponding input voltage is VIH.



Noise Margins:

Noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels. In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'.

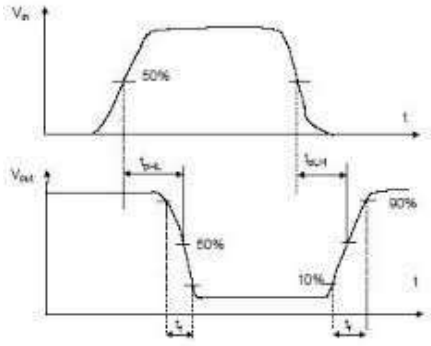
$$NML = VIL - VOL$$

$$NMH = VOH - VIH$$

In practice, noise margins are the amount of noise, that a logic circuit can withstand. Noise margins are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or outright failure.

Transient Response:

Transient analysis means analyzing a system in unsteady state. If the variables involved in defining the state of a system does not vary with respect to time, then the system is said to be in steady state.



In Transient Analysis, also called time-domain transient analysis, computes the circuit's response a function of time. This analysis divides the time into segments and calculates the voltage and current levels for each interval.

Propagation Delay:

Propagation delay is a measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

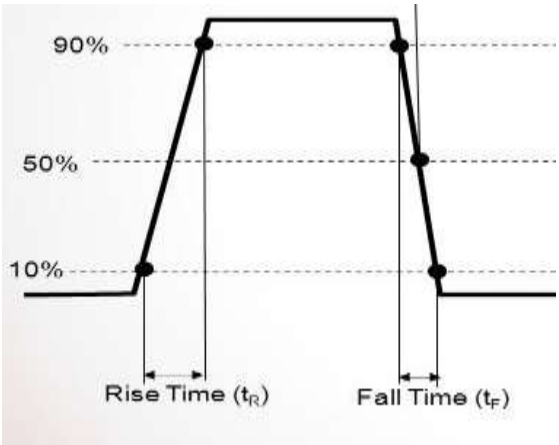
t_{PHL} – the time it takes the output to go from a high to low

t_{PLH} – the time it takes the output to go from a low to high

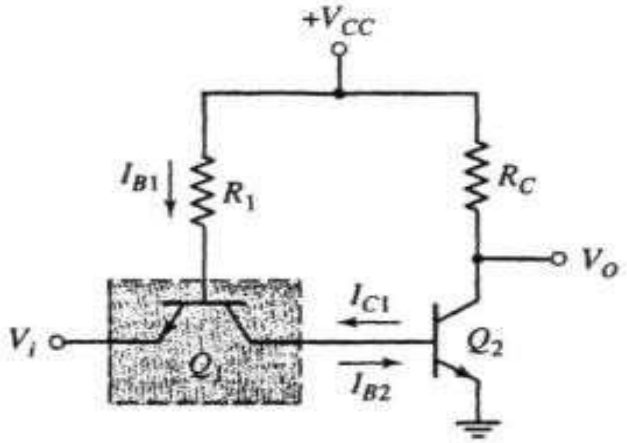
$$\text{Average Propagation Delay Time } (t_P) = \frac{t_{PHL} + t_{PLH}}{2}$$

⇨ Rise Time (t_r) = Time from 10% to 90%

⇨ Fall Time (t_f) = Time from 90% to 10%



Circuit Diagram:



Code:

1. Voltage Transfer Characteristics

```
*TTL inverter static analysis

.model Q1 npn Bf=50
Q11 2 1 0 Q1
Q12 1 5 4 Q1
R2 2 3 1.6K
R1 5 3 4K
Vcc 3 0 5
Vin 4 0 dc 5

.dc Vin 0 5 0.05
.control
run
plot v(2) v(4)
.endc
.end
```

2. Transient Analysis

```
*TTL inverter transient analysis

.model Q1 npn Bf=50
Q11 2 1 0 Q1
Q12 1 5 4 Q1
R2 2 3 1.6K
R1 5 3 4K
Vcc 3 0 5
Vin 4 0 pulse (0 5 1ns 1ns 1ns 20us 40us)
c 2 0 1p

.tran 1ns 80us

.control
run
plot v(2) v(4)
.endc
.end
```

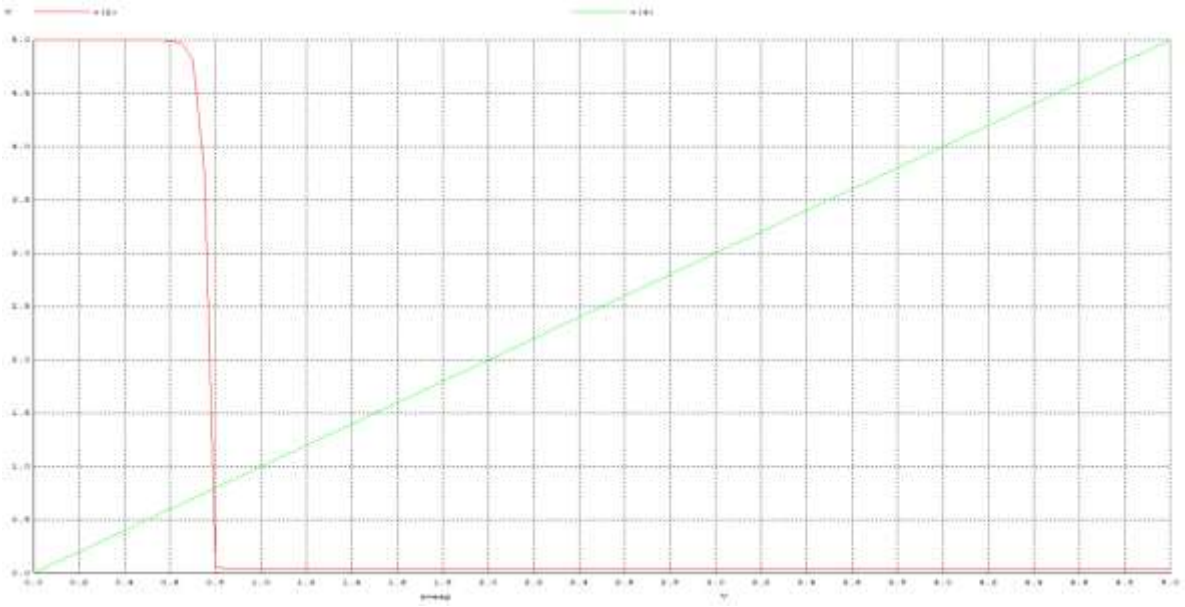
3. Fanout:

```
*TTL fanout calculation

.model Q1 npn Bf=50
Q11 2 1 0 Q1
Q12 1 5 4 Q1
R2 2 3 1.6K
R1 5 3 4K
Vcc 3 0 5
Vin 4 0 5
```

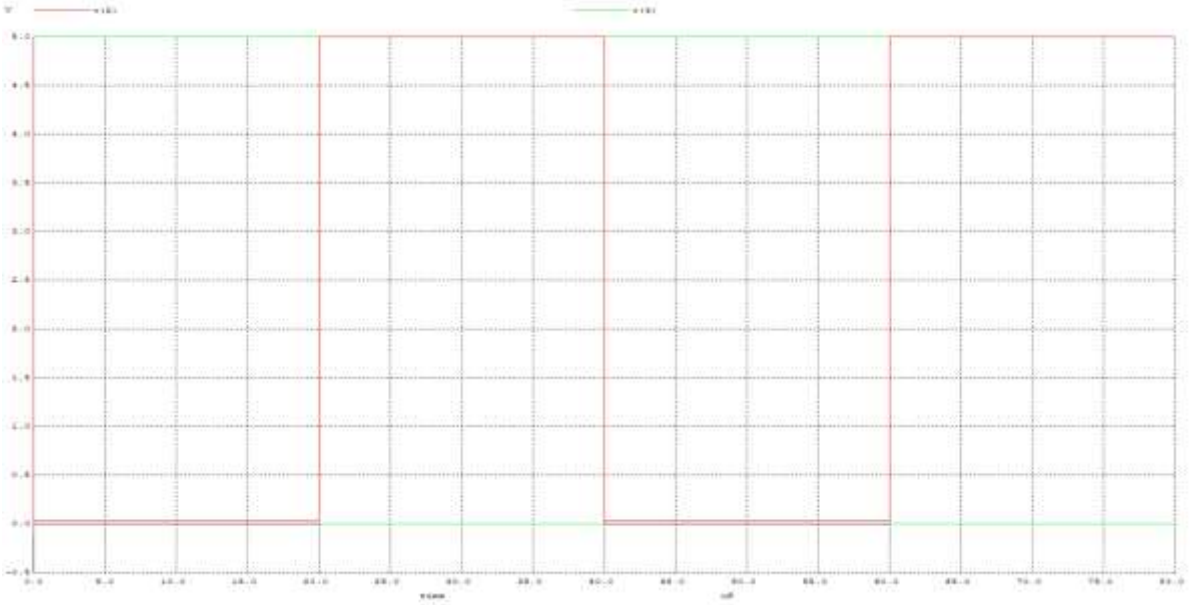
```
.subckt ttl out in c 0
Q21 out y 0 Q1
Q22 y z in Q1
R21 out c 1.6K
R11 z c 4K
.ends ttl

x1 out1 2 3 0 ttl
x2 out2 2 3 0 ttl
x3 out3 2 3 0 ttl
x4 out4 2 3 0 ttl
x5 out5 2 3 0 ttl
x6 out6 2 3 0 ttl
x7 out7 2 3 0 ttl
*x8 out8 2 3 0 ttl          for 830 Vih

.dc Vin 0 5 0.05
.control
run
plot v(2) v(4)
.endc
.end
```

Output:

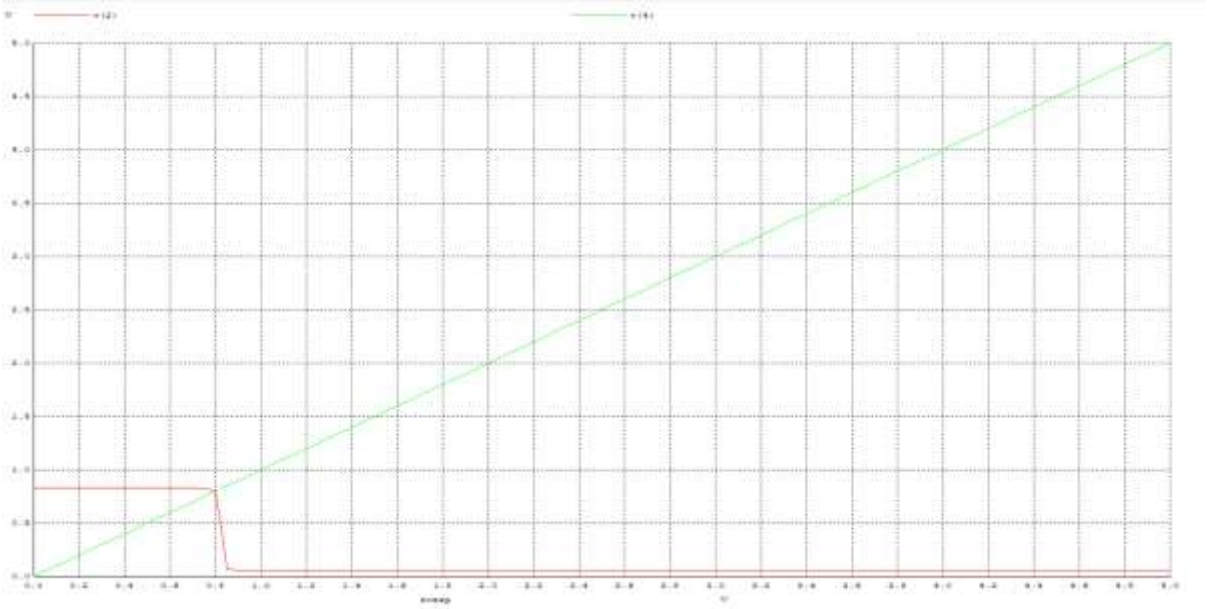
1. **Voltage Transfer Characteristics**



2. DTL NAND Transient Response



3. Fanout



Calculations:

VTL And Noise Margin:

From graph,

V_{OH} =5 V

V_{IL}= 0.7 V

V_{IH}= 0.8 V

V_{OL}= 38mV = 0.038 V

V_{TH}= 0.792 V

$NM_L = V_{IL} - V_{OL}$ = 0.7 – 0.038 V = 0.662 V

$NM_H = V_{OH} – V_{IH}$ = 5- 0.8 V = 4.2 V,

$NM = \min(NM_H, NM_L)$ = 0.662 V

Propagation Delay:

a) Low to High

t_{plh} =t2 – t1= 0.25 ns

b) High to Low

t_{phl} =t2 – t1= 1.5 ns

t_p = avg(1.5, 0.25) = 0.875 ns

Trise = 2.3 ns

Tfall = 0.96s

Fanout:

After Connecting 5 devices Vil≥Vol condition violates, therefore

fanout=4

Comparision of DTL and MDTL:

Parameter	**RTL**	**TTL**
Noise Margin	0.6414 V	0.6628 V
Propogation delay	0.460 ns	0.875 ns
Fan out	7	4

Conclusion:

In this experiment we have implemented the TTL Inverter logic family and plottedits voltage transfer characteristics, transient analysis and fan-out. We have calculated the values of noise margin, propagation delay, rise time, fall time and fan-out and compared the TTL inverter with the RTL inverter.

Digital Integrated Circuits

Practical 5

Date: 04/03/2022

Aim:

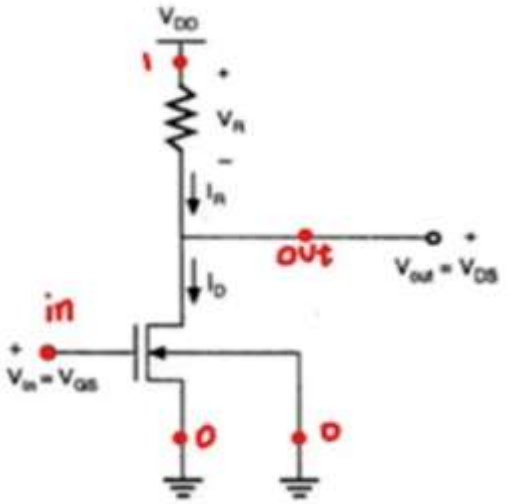
Design and verify the performance of given resistively loaded NMOS inverter circuit to obtain V_{OL} = 0.147 V, for given design parameters:

V_{T0} = 0.8V, V_{DD} = 5V, K_n' = 20µA/V^2, W/L = 2µm/1 µm.

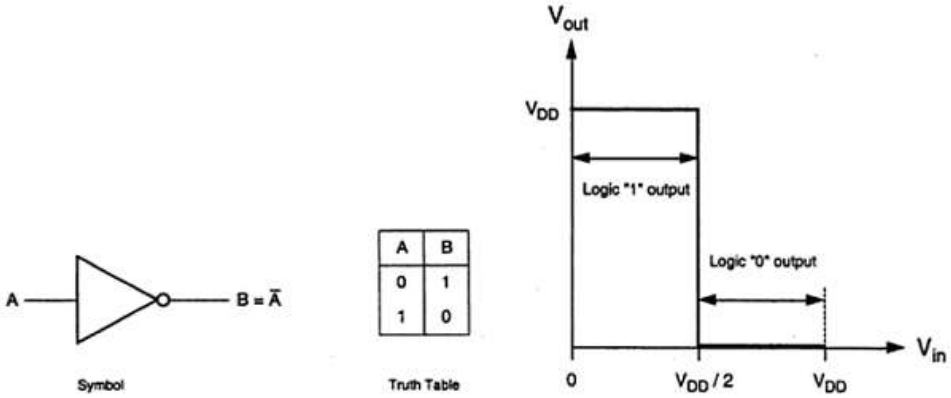
Compare theoretical and practical values of critical voltage on VTC. Find the noise margin of the circuit. Also observe the effect of changes in R_L on noise margin and comment.

Theory:

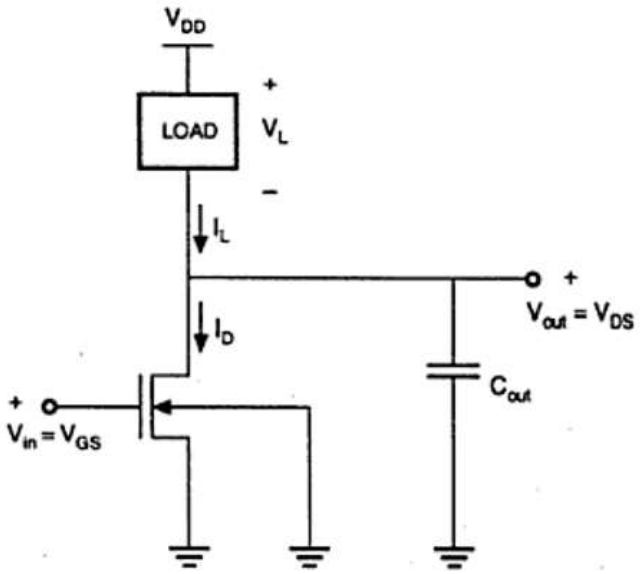
In this enhancement type, nMOS acts as the driver transistor. The load consists of a simple linear resistor R_L. The power supply of the circuit is V_{DD} and the drain current I_D is equal to the load current I_R. When the input of the driver transistor is less than the threshold voltage V_{TH} (V_{IN} < V_{TH}), driver transistor is in cut-off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to V_{DD}. Now, when the input voltage increases further, driver transistor will start conducting the non-zero current and nMOS goes in saturation region.



The logic symbol and truth table of ideal inverter is shown in figure given below. Here A is the input and B is the inverted output represented by their node voltages. Using positive logic, the Boolean value of logic 1 is represented by Vdd and logic 0 is represented by 0. Vth is the inverter threshold voltage, which is Vdd /2, where Vdd is the output voltage. The output is switched from 0 to Vdd when input is less than Vth. So, for 0<Vin<Vth output is equal to logic 0 input and Vth<Vin< Vdd is equal to logic 1 input for inverter.



The characteristics shown in the figure are ideal. The generalized circuit structure of an nMOS inverter is shown in the figure below.

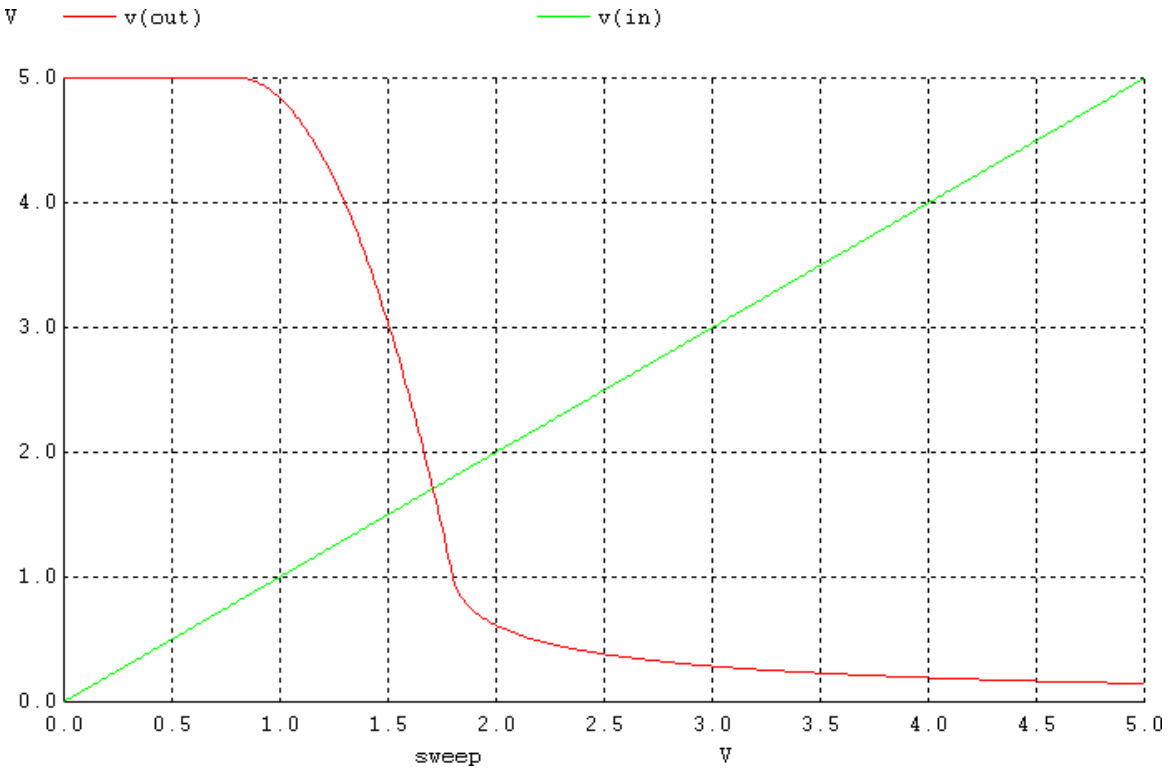


From the given figure, we can see that the input voltage of inverter is equal to the gate to source voltage of nMOS transistor and output voltage of inverter is equal to drain to source voltage of nMOS transistor. The source to substrate voltage of nMOS is also called driver for transistor which is grounded; so VSS = 0. The output node is connected with a lumped capacitance used for VTC.

Calculation & Circuit Design:

Spice Code & Simulation Outputs:

```
*Resistive Loaded NMOS

.model mynmos NMOS(Vt0=0.8 kp=20u)

Vdd 1 0 5V
Vin in 0 5V

RL out 1 200k

M1 out in 0 0 mynmos w=2u l=1u

.dc Vin 0 5 0.01

.control
run
plot V(out) V(in)
.endc
.end
```



Result And Observation Table:

Table 1: With one resistor (200 kΩ)

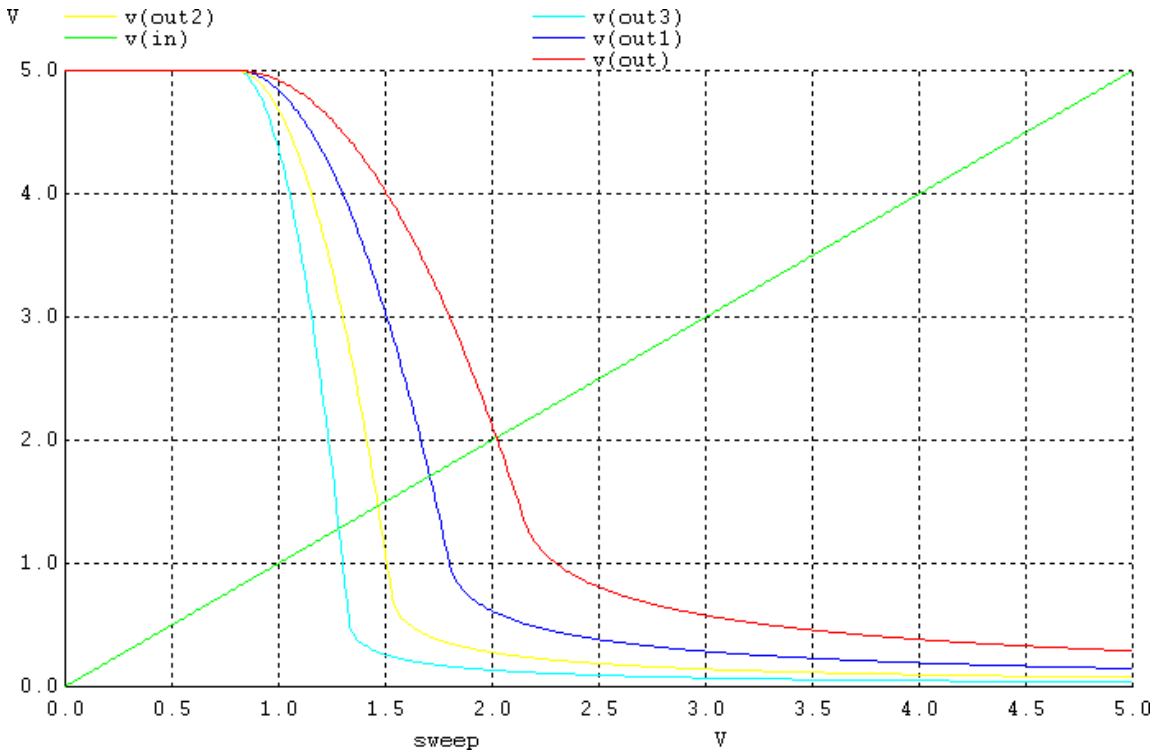
Parameters	Theoretical	Practical
V_{OH}		
V_{OL}		
V_{IH}		
V_{IL}		
V_{TH}		
Noise Margin High		
Noise Margin Low		
Noise Margin		

Table 2: Comparison with variation in load

Parameters	R_L = 100 kΩ	R_L = 200 kΩ	R_L = 400 kΩ	R_L = 800 kΩ
V_{OH}				
V_{OL}				
V_{IH}				
V_{IL}				
V_{TH}				
Noise Margin High				
Noise Margin Low				
Noise Margin				

Variation of R_L

```
*Resistive Loaded NMOS [Variation of RL]

.model mynmos NMOS(Vt0=0.8 kp=20u)

Vdd 1 0 5V
Vin in 0 5V

RL out 1 100k
RL1 out1 1 200k
RL2 out2 1 400k
RL3 out3 1 800k

M out in 0 0 mynmos w=2u l=1u
M1 out1 in 0 0 mynmos w=2u l=1u
M2 out2 in 0 0 mynmos w=2u l=1u
M3 out3 in 0 0 mynmos w=2u l=1u

.dc Vin 0 5 0.01

.control
run
plot V(out) V(in) V(out1) V(out2) V(out3)
.endc
.end
```



Observation Table:

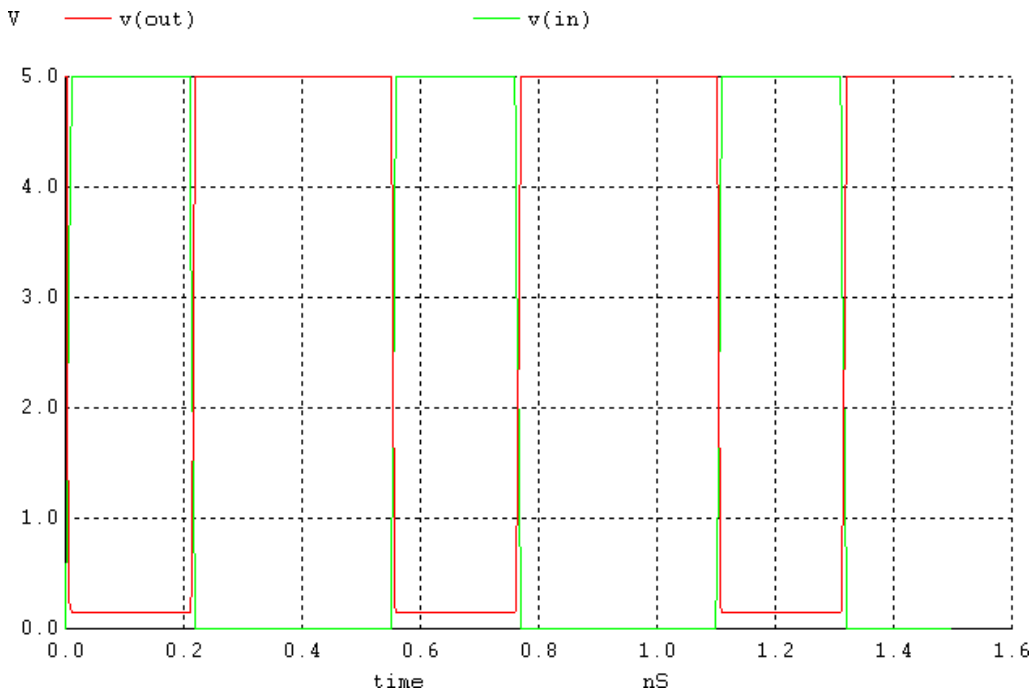
Table 3: Transient Analysis

Parameters	Practical
τ_{PLH}	
τ_{PHL}	
T_{rise}	
T_{fall}	

Calculations:

Transient Analysis

```
* Resistive Loaded NMOS (Transient Analysis)

.model mynmos NMOS(Vt0=0.8 kp=20u)

Vdd 1 0 5V
Vin in 0 pulse(0 5 0ps 10ps 10ps 200ps 550ps)

RL out 1 200k

M1 out in 0 0 mynmos w=2u l=1u

.tran 20ps 1500ps
.control
run
plot V(out) V(in)
.endc
.end
```



Conclusion:

Digital Integrated Circuits

Practical 6

Date:

Aim:

Design and verify the performance of given saturated loaded NMOS inverter circuit to obtain V_{IH} = 2.9 V, for given design parameters:

V_{T0} = 0.8V, V_{DD} = 5V, K_n' = 20µA/V², W/L = 2µm/1 µm.

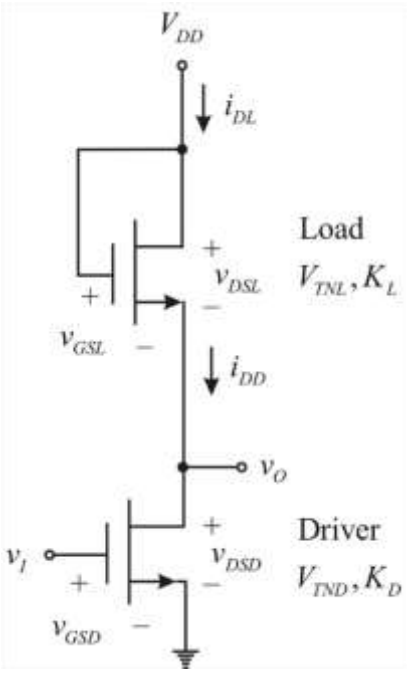
a) Compare theoretical and practical values of critical voltage on VTC and find the noise margin of the circuit.
b) Observe the effect of change in (W/L) loaded on noise margin & comment on it.
c) Also compare the results of noise with resistive loaded NMOS inverter for R_L = 200K.

Theory:

Saturated loaded device:

- An n-channel enhancement-mode MOSFET with the gate connected to the drain can be used as load device in an NMOS inverter.
- Since the gate and drain if the transistor are connected, we have VGS = VDS, when VGS = VDS > VTN, a non-zero drain current is induced in the transistor and thus the transistor operates in saturation only.

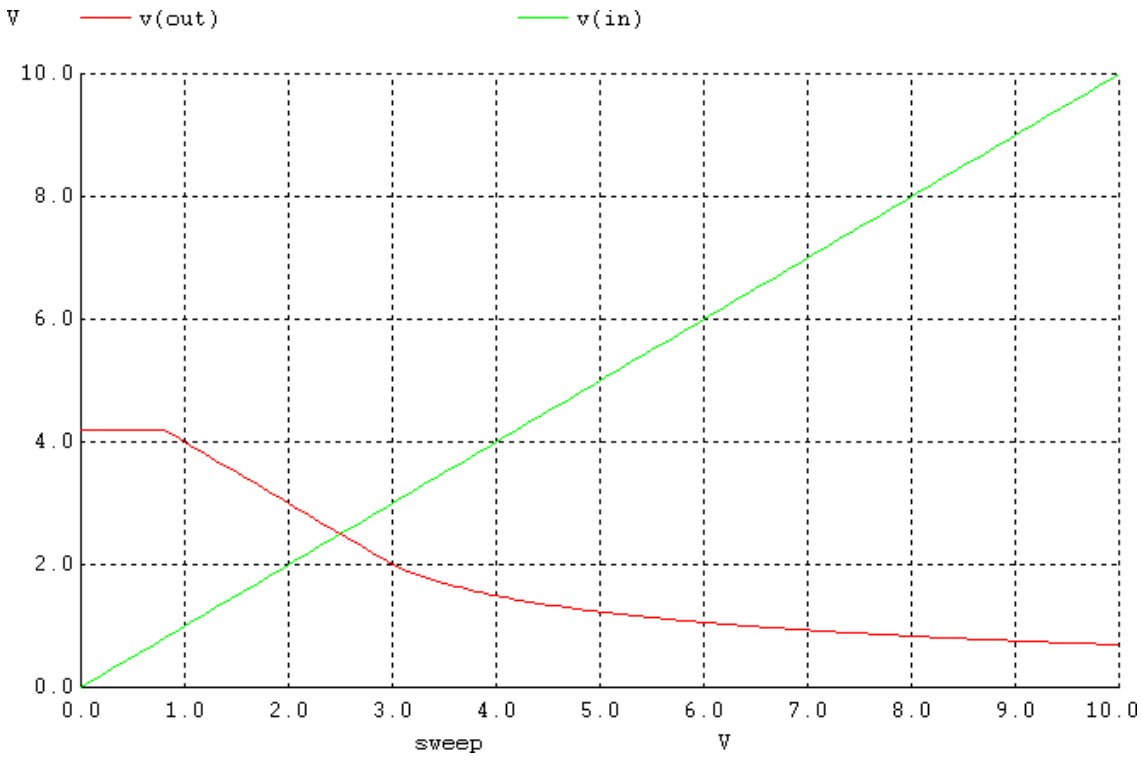
Circuit Diagram:



Calculation & Circuit Design:

Spice Code & Simulation Outputs:

```
*Saturated Loaded NMOS

.model mynmos NMOS(Vt0=0.8 kp=20u)

Vdd 1 0 5V
Vin in 0 5V

M11 1 1 out out mynmos w=2u L=1u
M12 out in 0 0 mynmos w=2u L=1u

.dc Vin 0 10V 0.05

.control
run
plot V(out) V(in)
.endc
.end
```



Result And Observation Table:

Table 1: For W/L = 2 µm

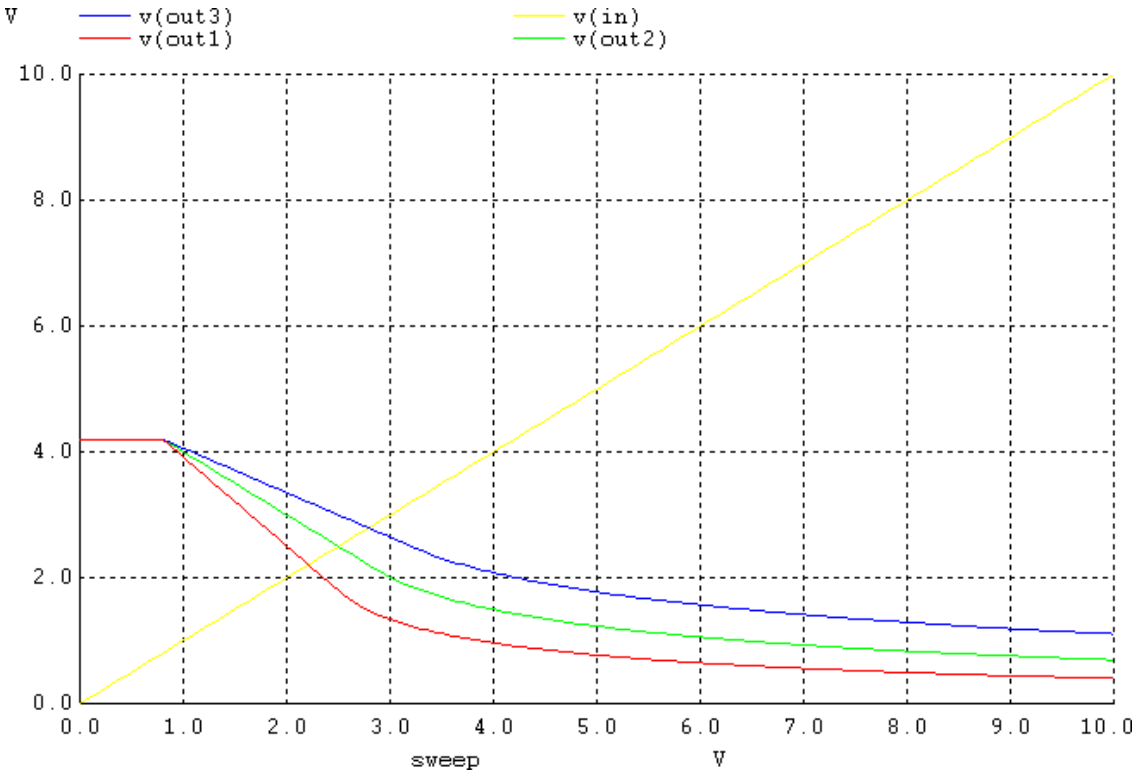
Parameters	Theoretical	Practical
V_{OH}		
V_{OL}		
V_{IH}		
V_{IL}		
V_{TH}		
Noise Margin High		
Noise Margin Low		
Noise Margin		

Table 2: Comparison with variation in W/L

Parameters	W/L = 1µm/1µm	W/L = 2µm/1µm	W/L = 4 µm/1µm
V_{OH}			
V_{OL}			
V_{IH}			
V_{IL}			
V_{TH}			
Noise Margin High			
Noise Margin Low			
Noise Margin			

Variation of W/L

```
*Saturated Loaded NMOS [Variation of W/L]

.model mynmos NMOS(Vt0=0.8 kp=20u)

Vdd 1 0 5V
Vin in 0 5V

M11 1 1 out1 out mynmos w=1u L=1u
M12 out1 in 0 0 mynmos w=2u L=1u

M21 1 1 out2 out mynmos w=2u L=1u
M22 out2 in 0 0 mynmos w=2u L=1u

M31 1 1 out3 out mynmos w=4u L=1u
M32 out3 in 0 0 mynmos w=2u L=1u

.dc Vin 0 10V 0.05

.control
run
plot V(out1) V(out2) V(out3) V(in)
.endc
.end
```



Observation Table:

Table 3: Transient Analysis

Parameters	Practical
τ_{PLH}	
τ_{PHL}	
τ_{P}	
T_{rise}	
T_{fall}	
Frequency	

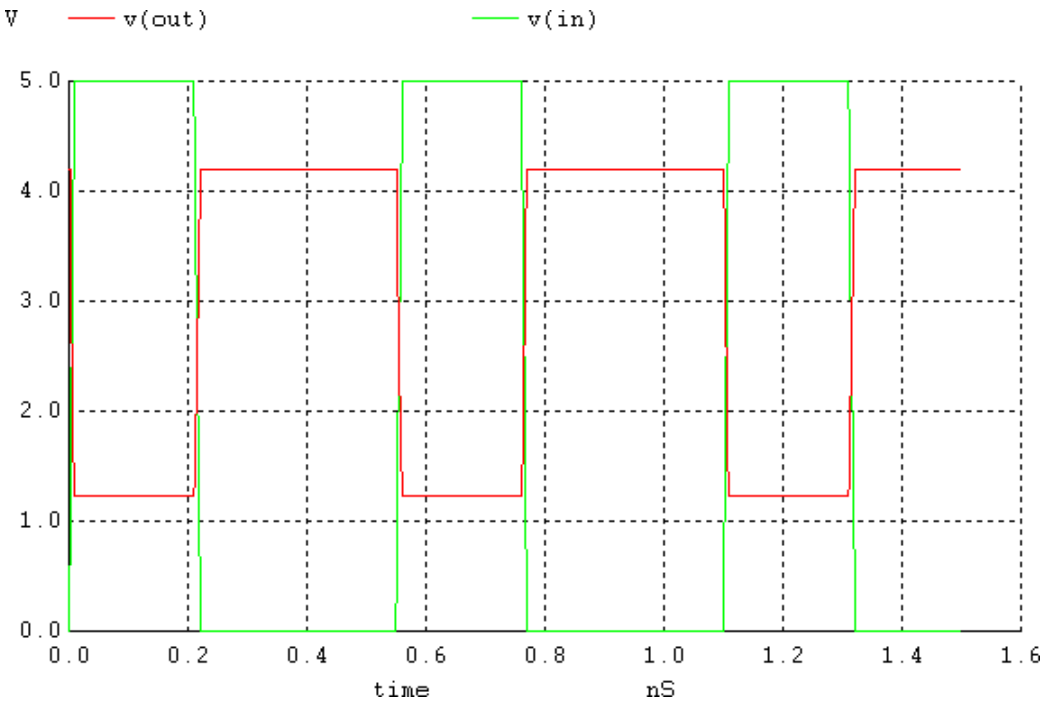
Calculations:

Table 4: Comparison of Resistive Load NMOS with Saturated Load NMOS

Parameters	Resistive Load NMOS inverter	Saturated Load NMOS inverter
Noise Margin Low		
Noise Margin High		
Propagation Delay		
Frequency		

Transient Analysis

```
* Saturated Loaded NMOS (Transient Analysis)

.model mynmos NMOS(Vt0=0.8 kp=20u)

Vdd 1 0 5V
Vin in 0 pulse(0 5 0ps 10ps 10ps 200ps 550ps)

RL out 1 200k

M1 out in 0 0 mynmos w=2u l=1u

.tran 20ps 1500ps
.control
run
plot V(out) V(in)
.endc
.end
```



Conclusion:

Digital Integrated Circuits

Practical 7

Date:

Aim:

Design and verify the performance of given CMOS inverter circuit to obtain switching threshold voltage of 2.2V. Given specifications for the CMOS inverter are:

V_{TN} = 0.8V, V_{TP} = -1V, V_{DD} = 5V, K_n' = 20µA/V^2, K_p' = 50µA/V^2, $L_n = L_p$ = 1µm.

Compare the theoretical and practical values of critical voltages on VTC and find the noise margin of the circuit. Observe the following parameters and comment on it.

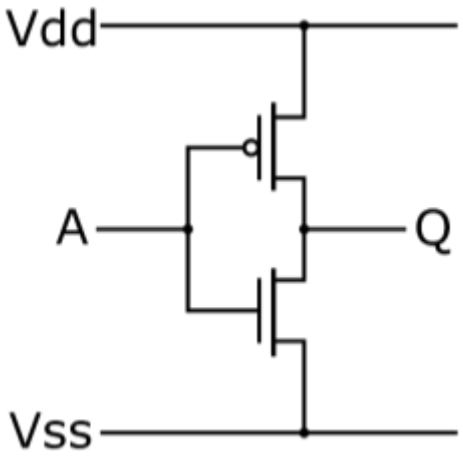
1. Variation of VDD from 5V to 3.3V on the switching threshold voltage of CMOS inverter.
2. Variation of Kr at 0.25, 1 and 4 on the switching characteristics.

Theory:

The term CMOS stands for "Complementary Metal Oxide Semiconductor". CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs and mobile phones make use of this technology due to several key advantages. This technology make use of both p-channel (PMOS) and n-channel (NMOS) semiconductor devices.

The main advantage of CMOS over NMOS and bipolar technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. VTC Characteristics are more symmetrical in CMOS than NMOS and noise margin offered is much higher. This allows integrating more CMOS gates on an IC than in MOS or bipolar technology, resulting in much better performance.

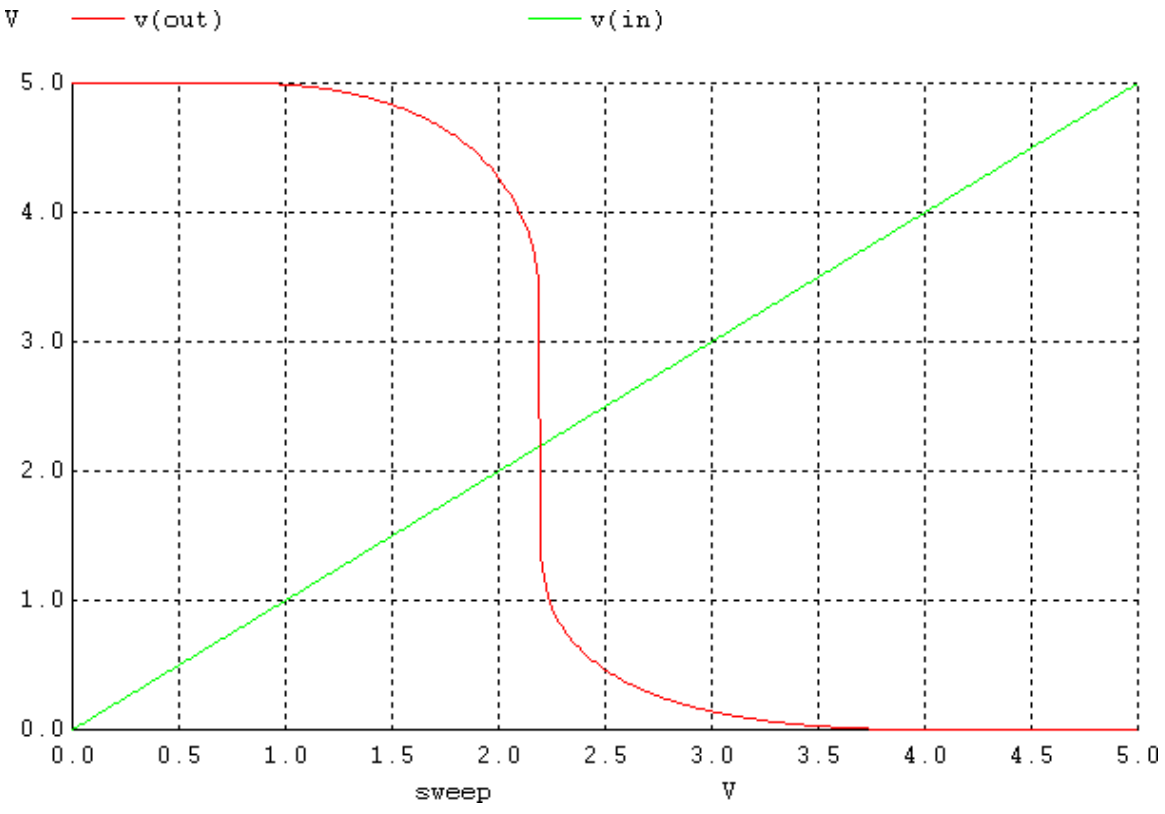
Circuit Diagram:



Calculation & Circuit Design:

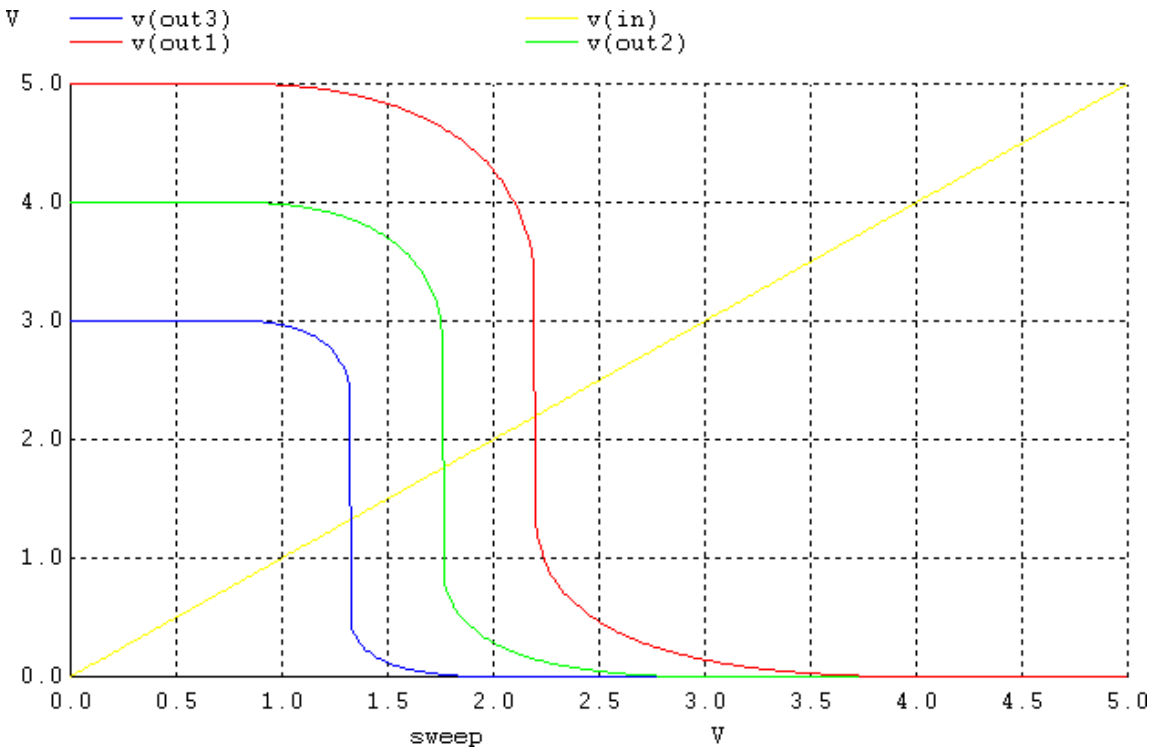
Spice Code & Simulation Outputs:

```
*CMOS Inverter

.model mynmos NMOS(Vt0=0.8 kp=50u)
.model mypmos PMOS(Vt0=-1 kp=20u)

Vdd 1 0 5V
Vin in 0 5V

M11 out in 0 0 mynmos w=1u L=1u
M12 out in 1 1 mypmos w=1.51u L=1u

.dc Vin 0 5V 0.01

.control
run
plot V(out) V(in)
.endc
.end
```



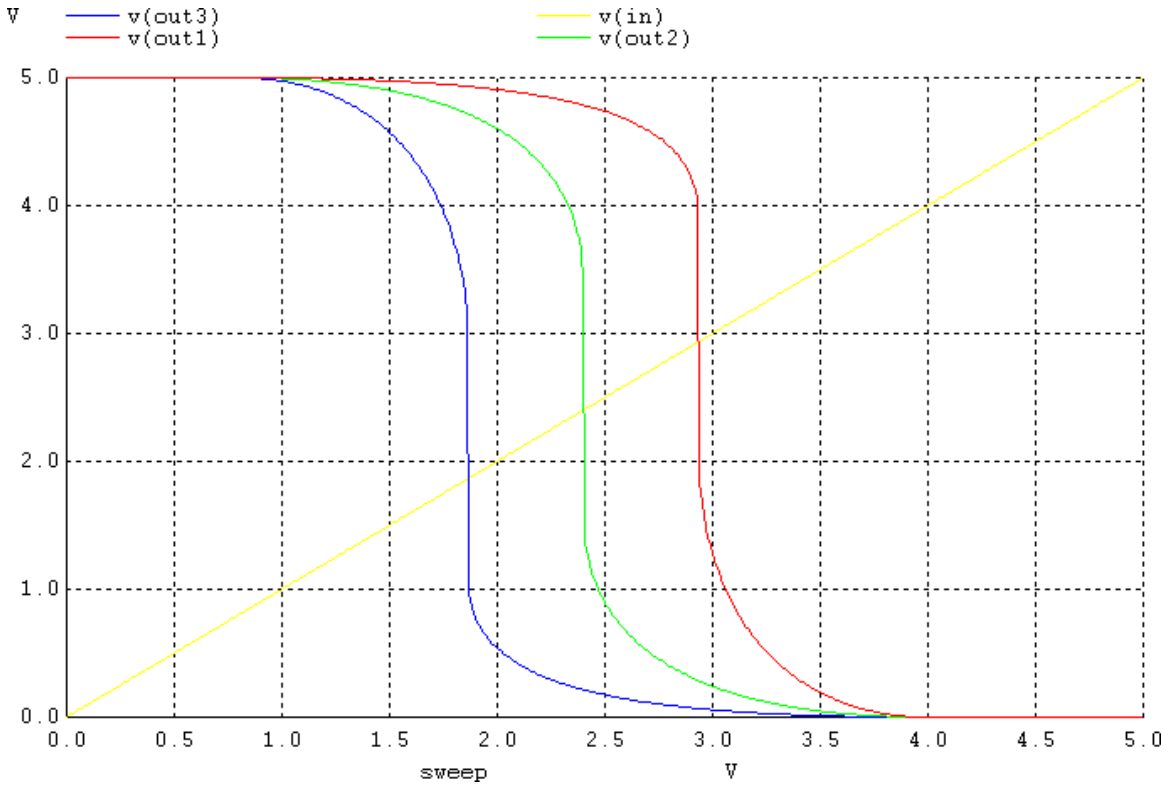
Part (A) Variation Of Vdd

```
*CMOS Inverter (Variation of Vdd)

.model mynmos NMOS(Vt0=0.8 kp=50u)
.model mypmos PMOS(Vt0=-1 kp=20u)

Vdd1 1 0 5V
Vdd2 2 0 4V
Vdd3 3 0 3V
Vin in 0 5V

M11 out1 in 0 0 mynmos w=1u L=1u
M12 out1 in 1 1 mypmos w=1.51u L=1u

M21 out2 in 0 0 mynmos w=1u L=1u
M22 out2 in 2 2 mypmos w=1.51u L=1u

M31 out3 in 0 0 mynmos w=1u L=1u
M32 out3 in 3 3 mypmos w=1.51u L=1u

.dc Vin 0 5V 0.01
.control
run
plot V(out1) V(out2) V(out3) V(in)
.endc
.end
```



Part (b) Variation of Kr

```
*CMOS Inverter (Variation of kr)

.model mynmos NMOS(Vt0=0.8 kp=50u)
.model mypmos PMOS(Vt0=-1 kp=20u)

Vdd 1 0 5V
Vin in 0 5V

M11 out1 in 0 0 mynmos w=1u L=1u
M12 out1 in 1 1 mypmos w=10u L=1u

M21 out2 in 0 0 mynmos w=1u L=1u
M22 out2 in 1 1 mypmos w=2.5u L=1u

M31 out3 in 0 0 mynmos w=1u L=1u
M32 out3 in 1 1 mypmos w=0.625u L=1u

.dc Vin 0 5V 0.01
.control
run
plot V(out1) V(out2) V(out3) V(in)
.endc
.end
```



Result And Observation Table:

Table 1: Noise Margin

Parameters	Theoretical	Practical
V_{OH}		
V_{OL}		
V_{IH}		
V_{IL}		
V_{TH}		
Noise Margin High		
Noise Margin Low		
Noise Margin		

Table 2: Effect of V_{DD} variation on V_{TH}

V_{DD} (V)	V_{TH} (V)
5	
4	
3	

Table 3: Effect of k_r variation on V_{TH}

k_r	V_{TH} (V)
0.25	
1	
4	

Conclusion:

Digital Integrated Circuits

Practical 8

Assignment 1

Date: 08/04/2022

Aim:

Write a winspice code to verify the functionality of given bicmos inverter circuit using default model parameters for the transistor.

Software Used: WinSpice Software

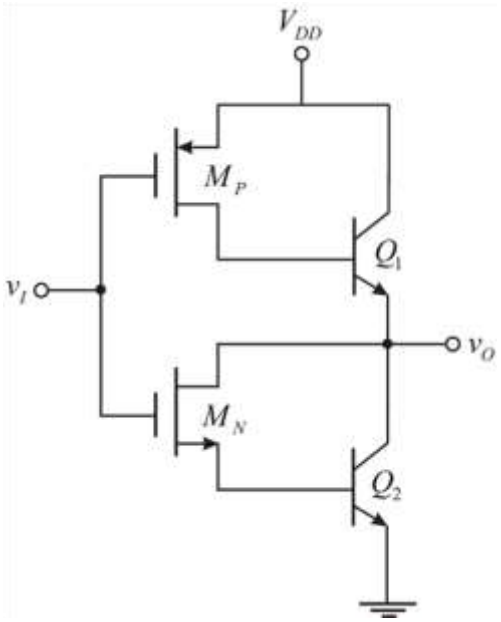
Theory:

In BiCMOS technology, both the MOS and bipolar device are fabricated on the same chip.The objective of the BiCMOS is to combing bipolar and CMOS so as to exploit the advantages of both the technologies.Today BiCMOS has become one of the dominant technologies used for high speed, low power and highly functional VLSI circuits.

Advantages of bipolar and CMOS circuits can be retained in BiCMOS chips.

- BiCMOS technology enables high performance integrated circuits IC's but increases process complexity..
- CMOS technology offers less power dissipation, smaller noise margins, and high packing density.
- Bipolar technology, on the other hand, ensure high switching and I/O speed and good noise performance. Now we are in 3rd Generation BiCMOS Technology.
- BiCMOS technology accomplishes both improved speed over CMOS and lower power dissipation than bipolar technology.
- The main drawback of BiCMOS technology is the higher costs due to the added process complexity.
- This greater process complexity in BiCMOS results in a cost increase compared to conventional CMOS technology.

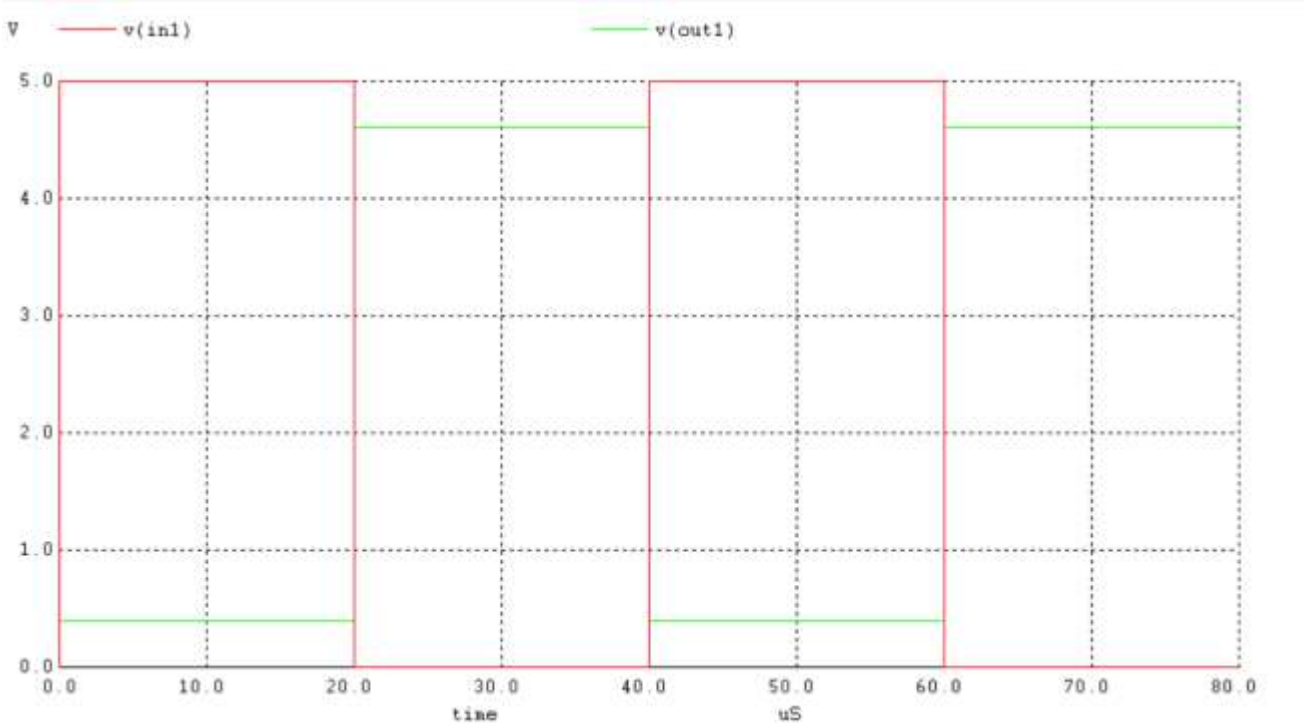
Circuit Diagram:



Winspice Codes:

```
*BICMOS transient char*

.model q1 npn bf=50
.model mynmos nmos Vto=0.8 Kp=50
.model mypmos pmos Vto=-1 Kp=20

.subckt BI in vdd_node out1 out2 src
M1 out1 in src src mynmos w=1u l=1u
M2 out2 in vdd_node vdd_node mypmos w=1.51u l=1u
.ends BI

q11 vdd_node out2 out1 q1
q12 out1 src 0 q1
xd1 in1 vdd_node out1 out2 src BI
Vdd vdd_node 0 5

Vin in1 0 pulse(0 5 1ns 1ns 1ns 20us 40us)

.tran 1ns 80us
.control
run
plot v(in1) v(out1)
.endc
.end
```

Output:



Transient Analysis

Conclusion:

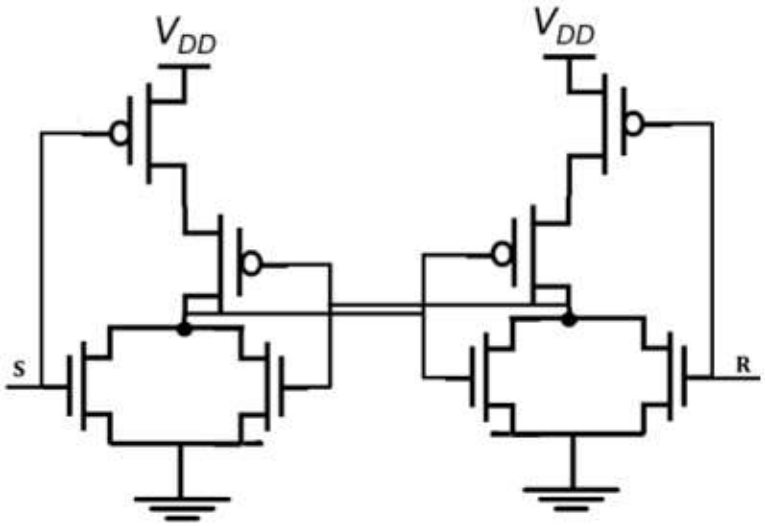
From the above experiment we implemented a Bi-CMOS circuit using WinSpice and verified its functionality using transient analysis as an invertor circuit.

Assignment 2

Aim:

Write WinSpice code to verify the functionality of NOR based SR Latch circuit.

Circuit Diagram:

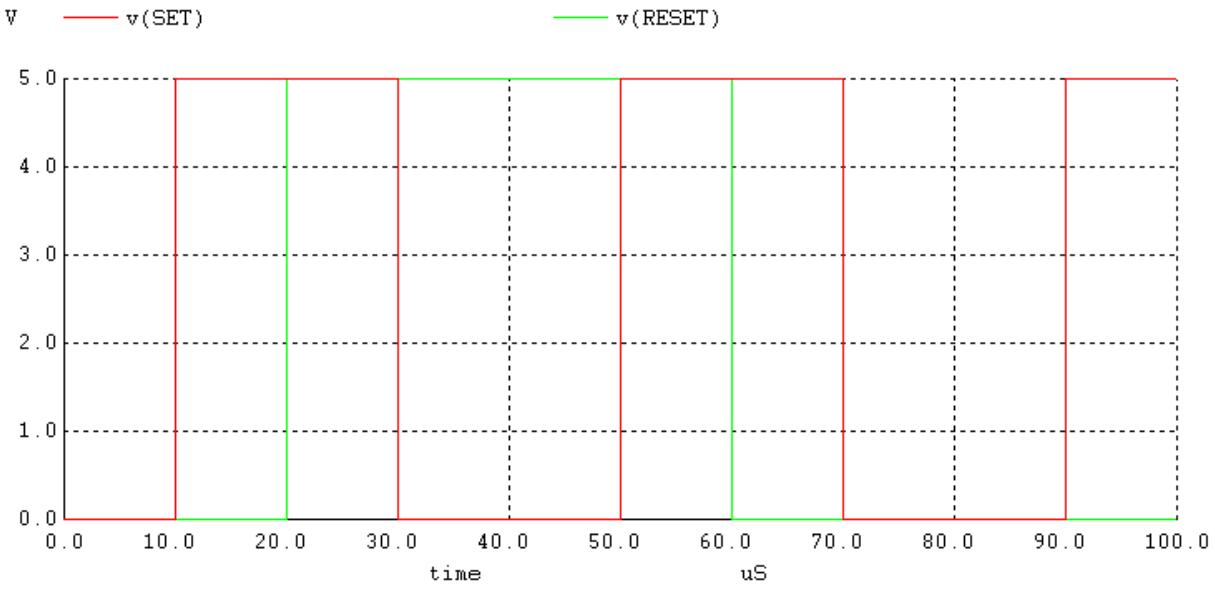


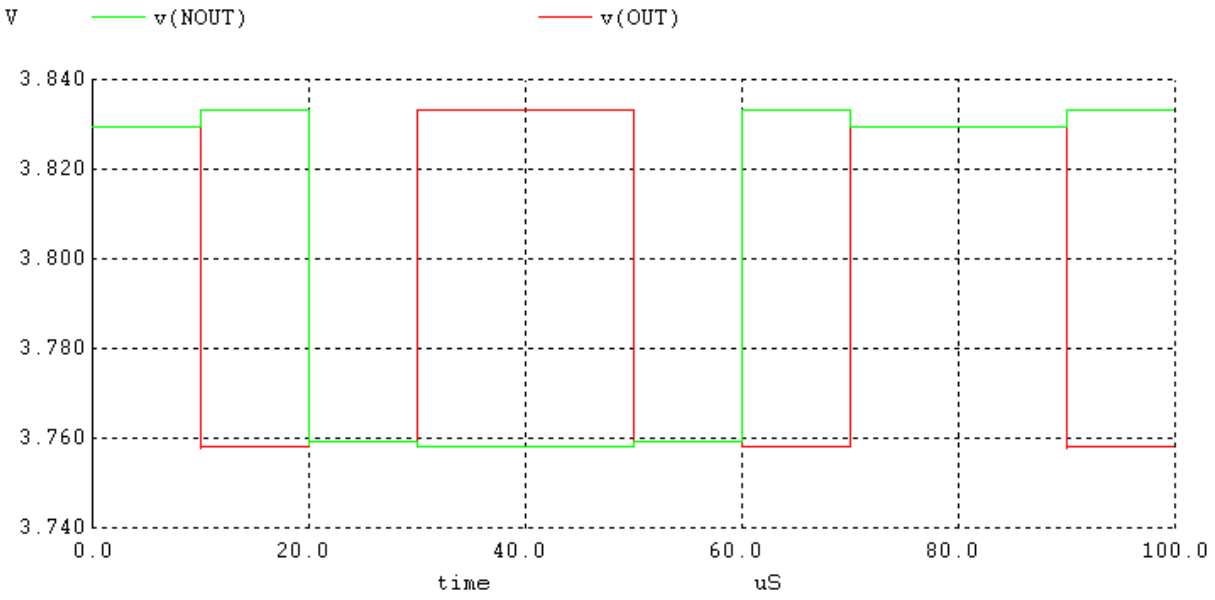
Spice Simulation Code:

```
* NOR based SR Latch

* MODEL *
   .MODEL NMOS120 NMOS (VTO=0.8 KP=20u)
   .MODEL PMOS120 PMOS (VTO= -1 KP=20u)

* NETLIST *
   MP1     3     SET    1     1     PMOS120 (W=1u L=1u)
   MP2     1     NOUT   OUT   OUT   PMOS120 (W=1u L=1u)
   MP3     3     RESET  2     2     PMOS120 (W=1u L=1u)
   MP4     2     OUT    NOUT  NOUT  PMOS120 (W=1u L=1u)
   MN1     OUT   SET    0     0     NMOS120 (W=1u L=1u)
   MN2     OUT   NOUT   0     0     NMOS120 (W=1u L=1u)
   MN3     NOUT  RESET  0     0     NMOS120 (W=1u L=1u)
   MN4     NOUT  OUT    0     0     NMOS120 (W=1u L=1u)
   VDD     3     0                  5V
   Vset    SET   0                  PULSE (0 5 10u 1n 1n 20u 40u)
   Vreset  RESET  0                 PULSE (0 5 20u 1n 1n 40u 80u)

* STIMULUS *
   .TRAN 1n 100u

* CONTROL BLOCK *
   .CONTROL
   RUN
```

```
PLOT V(SET)
PLOT V(RESET)
PLOT V(OUT) V(NOUT)
.ENDC
.END
```

Spice Simulation Results





Conclusion:

From the above experiment we implemented a NOR based SR Latch using WinSpice and verified its functionality using transient analysis.