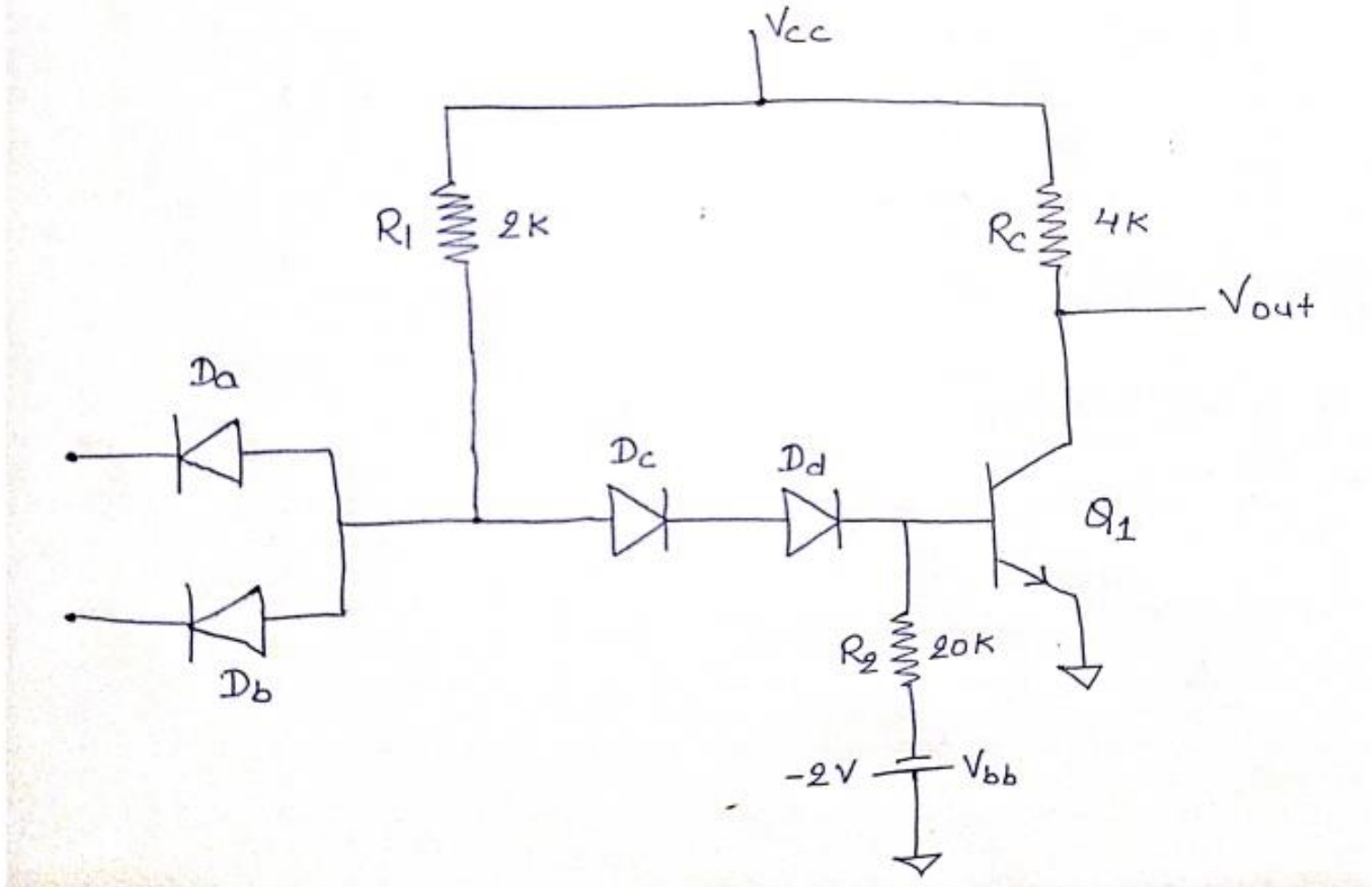
Experiment 3

Implement DTL NAND gate using parameters Bf=50, R1=2k, Rc=4k, R2=20k.

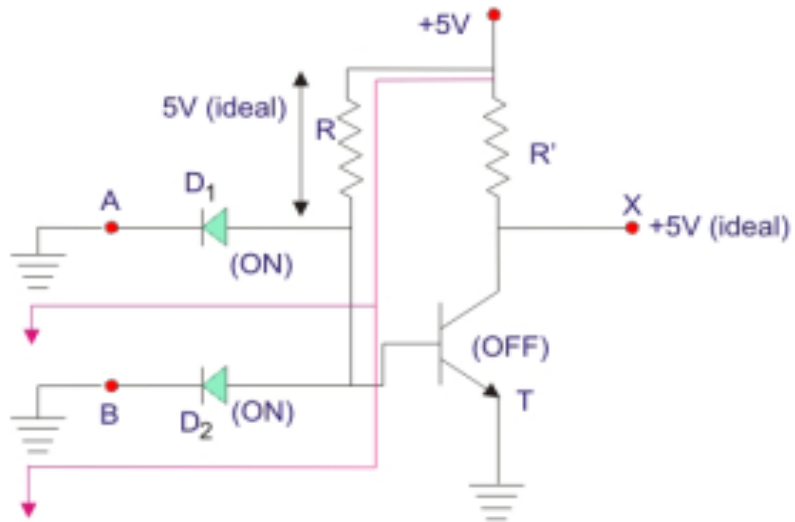
1. **Perform the static analysis and calculate the noise margin.**
2. **Verify its functionality by performing transient analysis.**
3. **Find out practical Fan-out.**

DTL NAND Gate

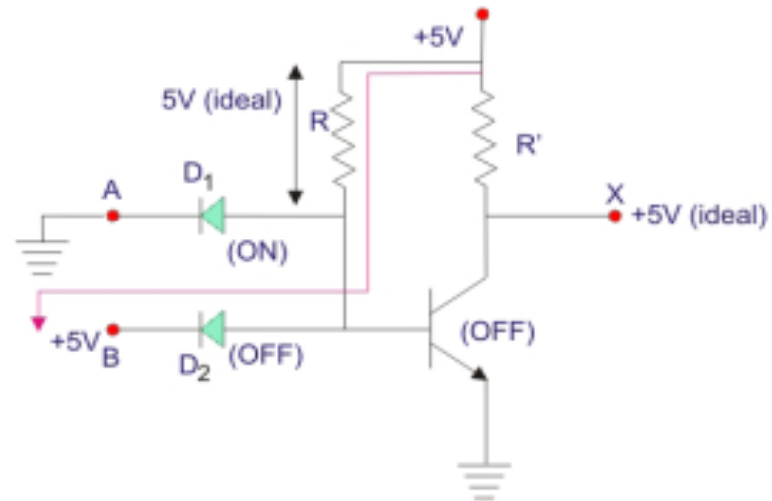


DTL NAND Gate Operation

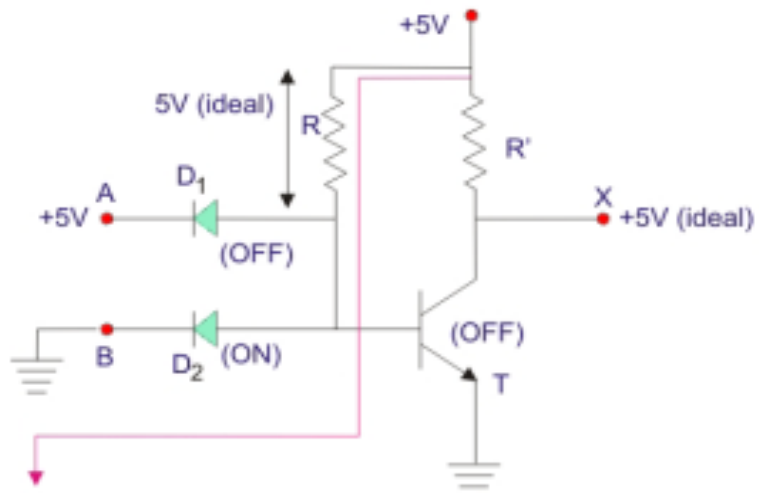
When A=B=0



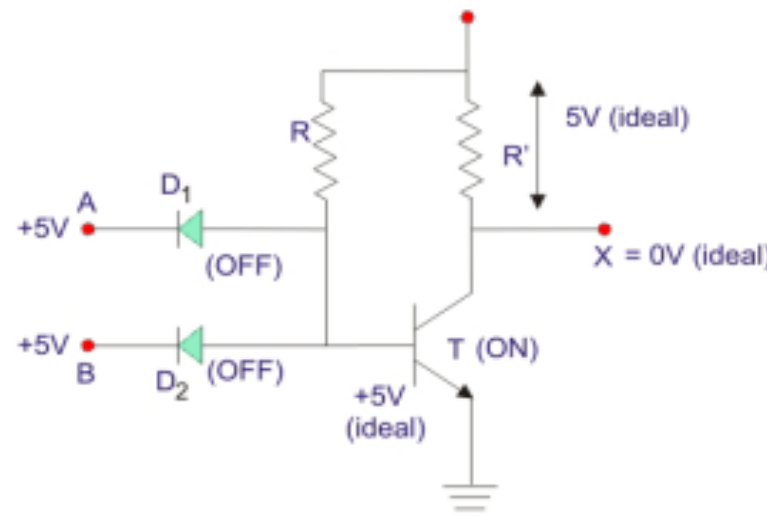
When A=0 and B=1



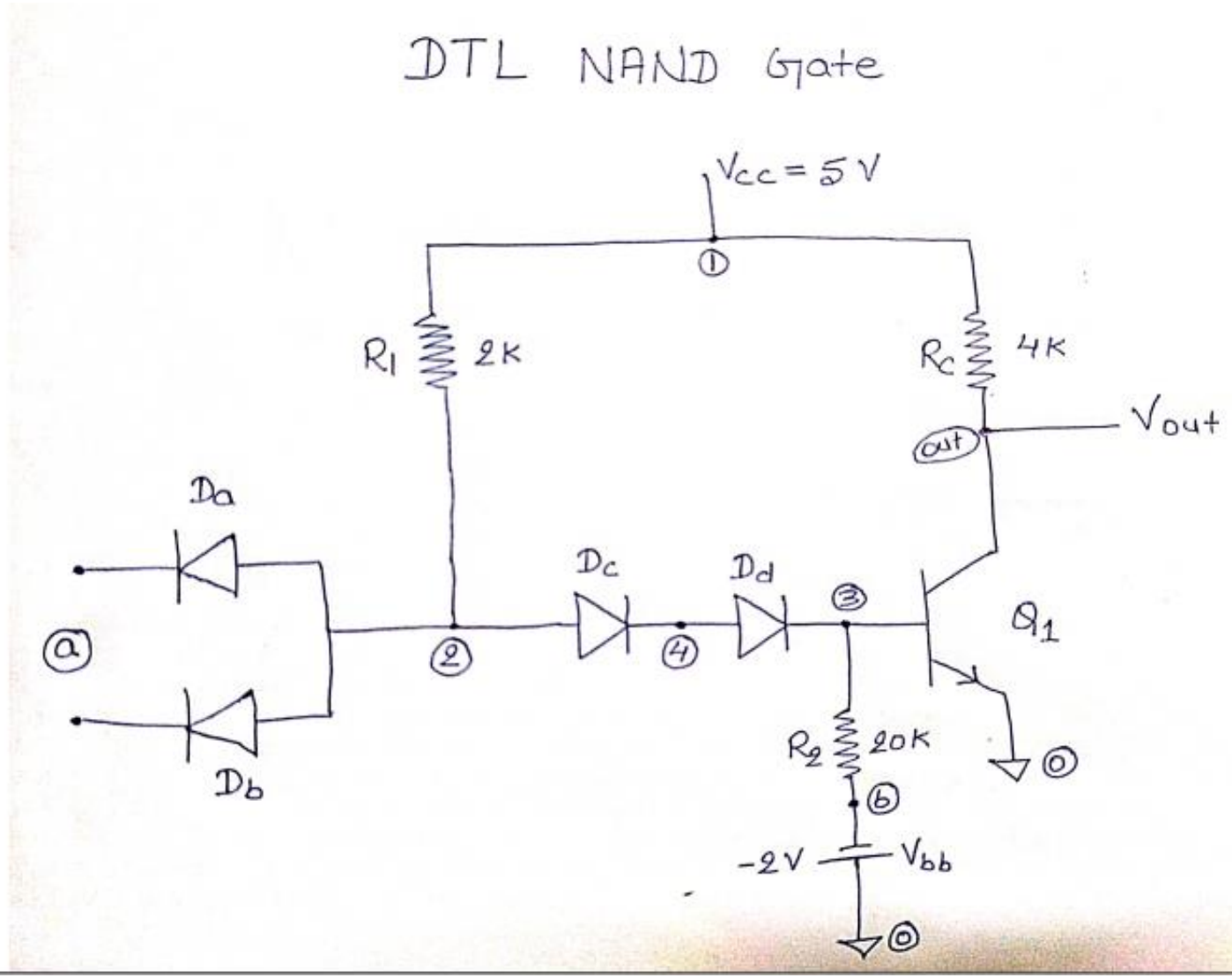
When A=1 and B=0



When A=B=1

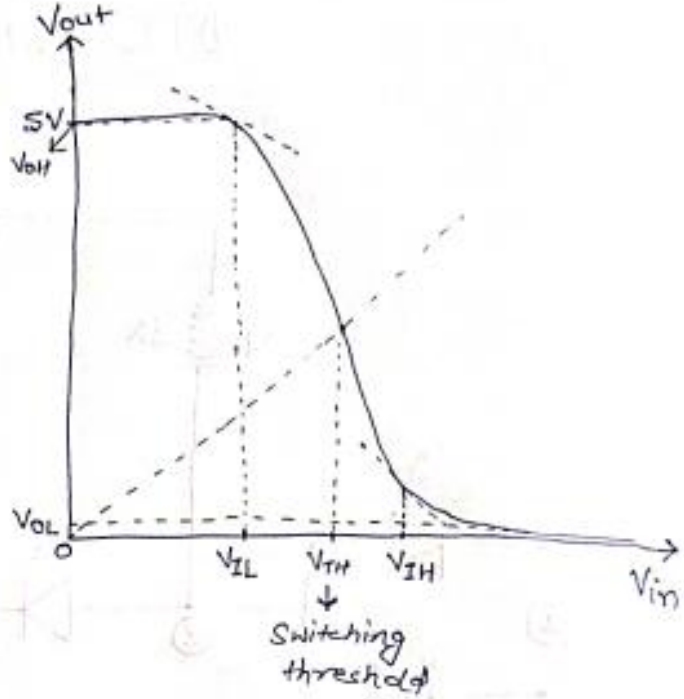


DTL NAND Gate



① DTL NAND Gate Static Analysis :-

```
*dtl transfer char*
.model q1 npn bf=50
q11 out 3 0 q1
.model d1 d
da 2 a d1
db 2 a d1
dc 2 4 d1
dd 4 3 d1
r1 1 2 2k
rc 1 out 4k
r2 3 b 20k
Vbb b 0 -2
Vcc 1 0 5
Va a 0 pulse(0 5 0ps 10ps 10ps 200ps 1000ps)
.dc Va 0.5 5 0.05
.control
run
Plot V(a) V(out)
.endc
.end
```



Calculation of Noise Margin :

$NM_L = V_{IL} - V_{OL}$

$NM_H = V_{OH} - V_{IH}$

→ Observation from static Analysis :-

$V_{OH} = 5\,V$
$V_{OL} = 0.03\,V$
$V_{IL} = 1.12\,V$
$V_{IH} = 1.35\,V$

$\Rightarrow$

$NM_L = 1.12 - 0.03 = 1.09\,V$
$NM_H = 5 - 1.35 = 3.65\,V$

② DTL NAND Gate Transient Analysis :-

```
*dtl NAND transient response*
.model Q1 npn bf=50
Q11 out 3 0 Q1
.model d1 d
da 2 a d1
db 2 a d1
dc 2 4 d1
dd 4 3 d1
R1 1 2 2K
Rc 1 out 4K
R2 3 b 20K
Vbb b 0 -2
Vcc 1 0 5
Va a 0 pulse(0 5 20ps 10ps 10ps 200ps 550ps)

.tran 20ps 1500ps
.control
run
Plot V(a) V(out)
.endc
.end
```

Calculation of Delay :- from transient analysis

$t_1 = 238ps$, $t_2 = 235ps$

$\therefore t_{PLH} = t_1 - t_2 = 3ps$

$t_1' = 1.125ns$, $t_2' = 1.123ns$

$\therefore t_{PHL} = 2ps$

$\because t_p = \frac{t_{PLH} + t_{PHL}}{2} = \frac{2+3}{2} = 2.5ps$

③ DTL NAND Gate Fan-out :—

```
*DTL NAND FANOUT*
.model q1 npn bf=50
.model d1 d
.subckt dtlckt a b c 1 0 out
q1 out 4 0 q1
da 2 a d1
db 2 b d1
dc 2 3 d1
dd 3 4 d1
r1 2 1 2K
rc 1 out 4K
r2 4 c 20K
.ends dtlckt
*supply*
Vcc 1 0 5
Vbb c 0 -2
Va a 0 5
* driver gate
Xd a a c 1 0 out1 dtlckt
* Load gates
XL1 out1 out1 c 1 0 out2 dtlckt
XL2 out1 out1 c 1 0 out3 dtlckt
XL3 out1 out1 c 1 0 out4 dtlckt
.
.
.
XL42 out1 out1 c 1 0 out43 dtlckt
.dc Va 0.5 5 0.05
.control
run
Plot V(out1) V(a)
.endc
.end
```

$V_{OH} > V_{IH}$

$V_{OL} < V_{IL}$