Starting Vivado:

echo source/tools/Xilinx/Vivado/2019.2/settings64.sh >myenv.sh

source myenv.sh

Board #: xc7a35tcpg236-1

```
set_msg_config -new_severity "ERROR" -id "Synth 8-87"
set_msg_config -new_severity "ERROR" -id "Synth 8-327"
set_msg_config -new_severity "ERROR" -id "Synth 8-3352"
set_msg_config -new_severity "ERROR" -id "Synth 8-5559"
set_msg_config -new_severity "ERROR" -id "Synth 8-6090"
set_msg_config -new_severity "ERROR" -id "Synth 8-6858"
set_msg_config -new_severity "ERROR" -id "Synth 8-6859"
set_msg_config -new_severity "ERROR" -id "Timing 38-282"
set_msg_config -new_severity "ERROR" -id "VRFC 10-3091"
set_msg_config -new_severity "WARNING" -id "Timing 38-313"
set_msg_config -suppress -id "Constraints 18-5210"
set_property INCREMENTAL false [get_filesets sim_1]
set_property -name {xsim.simulate.runtime} -value 0ns -objects [get_filesets sim_1]
```

Vivado Basics:

New file set: create_fileset -simset sim_2
add_files -fileset sim_2 tb_alu.sv

Global Parameters: localparam[3:0] ALUOP_AND = 4'b0000;

Concatenate: accumulator_ext = {{16{accumulator[15]}}, accumulator};

Instantiate module: alu
ALU(.op1(accumulator_ext), .op2(sw_ext), .alu_op(alu_op), .zero(isZero), .result(alu_out));

Include header file(put inside module): `include "riscv_alu_constants.sv"
Header Guards:

```
`ifndef RISCV_ALU_CONSTANTS
`define RISCV_ALU_CONSTANTS

// Add all your constants here


`endif // RISCV_ALU_CONSTANTS
```

/

TCL FILES:

Hex Forces: add_force op1 ffe123b3 -radix hex

Reset tcl file:

```
restart
run 20 ns
add_force clk {0} {1 5} -repeat_every 10
run 20 ns
```

Ecen 323:

```
##################################################################################################
#Filename: alu_sim.tcl
#
#Author: Caleb Price
#Class: Ecen 323, Section 2
#Date: 1/23/23
#Semester: winter 2023
#
#Description: This .tcl FIle is built to test the calc module it resets the inputs and runs
#a few basic tests.
#
##################################################################################################


////////////////////////////////////////////////////////////////////////////////
//Filename: calc.sv
//
//Author: Caleb Price
//Class: Ecen 323, Section 2
//Date: 1/23/23
//Semester: winter 2023
//Modules: calc, Oneshot, alu
//
//Description: This is a higher level design that implents the alu and our oneshot module
//The switches are now connected to op2, op1 is still the result of the previous
//calculation. The result is shown through the leds.
//
////////////////////////////////////////////////////////////////////////////////
```