wassolldas – An audio player using an Arty A7-35t FPGA Development Board

# Introduction

This project “wassolldas” aims to implement the WSOLA algorithm for Time-Scale Modulation on an arbitrary sound file. In simpler terms, a given sound file shall be played back either slowed down or sped up without a change in pitch. An Arty A7-35t FPGA development board should run this algorithm over a sound file which is sourced from internal ROM storage. Having slowed down or sped up the sound file, it should play back the sound file using a Pmod module called “Pmod I2S2”. This module contains two audio jacks, a line in and a line out connection. Needless to say, “wassolldas” exclusively uses the line out connection.

As the implementation of WSOLA proved to be incredibly complex, I attempted to implement OLA instead.

# Material

* Arty A7-35t FPGA Development Board
* PmodSD 1.2
* Pmod I2S2
* Pieye Edushield for debug purposes

# Resources

## Basics

* [(66) ESP32 Sound - Working with I2S - YouTube](https://www.youtube.com/watch?v=m-MPBjScNRk&t=1527s)
* [GitHub - schreibfaul1/ESP32-audioI2S: Play mp3 files from SD via I2S](https://github.com/schreibfaul1/ESP32-audioI2S)
* https://youtu.be/ZNunxg7o8l0
* <https://www.fpga4fun.com/VHDLTips.html>
* [Taming Multiple Drivers (xilinx.com)](https://support.xilinx.com/s/article/1034745?language=en_US)

## Component specific

* [Pmod I2S2 Reference Manual - Digilent Reference](https://digilent.com/reference/pmod/pmodi2s2/reference-manual)
* [Getting Started with Digilent Pmod IPs - Digilent Reference](https://digilent.com/reference/learn/programmable-logic/tutorials/pmod-ips/start)
* [Pmod MicroSD - Digilent Reference](https://digilent.com/reference/pmod/pmodmicrosd/start?redirect=1)
* [GitHub - Digilent/vivado-library](https://github.com/Digilent/vivado-library)
* [Vivado Library - Digilent Reference](https://digilent.com/reference/vivado:library)
* [vivado-library/ip/Pmods at master · Digilent/vivado-library · GitHub](https://github.com/Digilent/vivado-library/tree/master/ip/Pmods)
* [vivado-library/ip/Pmods/PmodSD\_v1\_0 at master · Digilent/vivado-library · GitHub](https://github.com/Digilent/vivado-library/tree/master/ip/Pmods/PmodSD_v1_0)
* [AXI Basics 1 - Introduction to AXI (xilinx.com)](https://support.xilinx.com/s/article/1053914?language=en_US)
* <https://www.xilinx.com/support/documentation-navigation/design-hubs/dh0012-vivado-high-level-synthesis-hub.html>
* <https://github.com/riccardonicolaidis/PmodSD_Arty_A7_Project>
* <https://docs.xilinx.com/v/u/en-US/pg058-blk-mem-gen>

## Previous implementations

* [Playing audio with an FPGA - Hackster.io](https://www.hackster.io/Kampino/playing-audio-with-an-fpga-d2bc85) goat
* [Play wav-files from an SD card with the ZYBO - Hackster.io](https://www.hackster.io/Kampino/play-wav-files-from-an-sd-card-with-the-zybo-ba4469)
* <https://justanotherelectronicsblog.com/?p=402>
* [Playing an Audio File - Programming FPGAs Getting Started with Verilog - FPGAkey](https://www.fpgakey.com/tutorial/section570)
* [Project FPGA-Audio – FPGA based MP3/WAV Player - FPGA SOLUTIONS (google.com)](https://sites.google.com/site/tgptechnologies/fpga-project/fpga-audio-fpga-based-mp3-wav-player)
* [Playing MP3s From An FPGA | Hackaday](https://hackaday.com/2012/03/13/playing-mp3s-from-an-fpga/)
* [GitHub - ultraembedded/FPGAmp: 720p FPGA Media Player (RISC-V + Motion JPEG + SD + HDMI on an Artix 7)](https://github.com/ultraembedded/FPGAmp)

## Time stretching

* [Audio time stretching and pitch scaling - Wikipedia](https://en.wikipedia.org/wiki/Audio_time_stretching_and_pitch_scaling)
* <https://www.jstage.jst.go.jp/article/elex/11/14/11_11.20140387/_article>
* <https://github.com/k2kobayashi/Shifter/blob/master/shifter/shifter.py>
* <https://www.audiolabs-erlangen.de/content/05-fau/professor/00-mueller/01-students/2011_DriedgerJonathan_TSM_MasterThesis.pdf>

## Python

* <https://www.pythontutorial.net/python-basics/python-write-text-file/>

# Development Process

The audio was largely inspired by [Daniel Kampert’s tutorial on how to play audio with an FPGA](https://www.hackster.io/Kampino/playing-audio-with-an-fpga-d2bc85). Although the author wrote their tutorial with the Zybo Z7 in mind, i. e. a different development board, I was able to quickly adapt their code to run on the Arty A7.

## TODO:

Familiarize myself with FPGA development

Output sound

~~Read SD Card data~~

Modulate speed

# Implementation

## Naïve resampling

## OLA

## WSOLA

Look at timing graph of block memory

ROMReader takes two cycles from increment to update.

AXI?

<https://stackoverflow.com/questions/66413266/vhdl-fsm-output-delayed-of-1-clock-cycle>